ASIX AX88140A

100BASE-TX/FX PCI Bus Fast Ethernet MAC Controller Data Sheet(11/03/'97)

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FIGURES

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1.0 Introduction

1.1 General Description:

l The AX88140A Fast Ethernet Controller is a high performance and highly integrated PCI Bus Ethernet Controller chip.

l The AX88140A is cost effective, high performance solution for PCI add-in adapters, PC motherboards, or bridge/hub applications.

l It implements both 10Mbps and 100Mbps Ethernet function based on IEEE802.3 LAN standard.

l The AX88140A contains a high speed 32 bit PCI Bus master interface to host CPU. Two large independent transmit and receive FIFO allow the AX88140A to buffer the Ethernet packet efficiently.

l The 10/100Mbps ports can be programmed to support 10Mbps, 100Mbps media-independent interface (MII), or 100BASE-TX physical coding sub-layer (PCS)mode, For 10Mbps operation AX88140A provides a standard serial Interface to the external 10Mbps ENDEC chip.

1.2 Features

- Single chip PCI bus Fast Ethernet Controller.
- Direct interface to PCI bus.
- Support both 10Mbps and 100Mbps data rate.
- Full or Half duplex operation supported for both10Mbps and 100Mbps operation.
- Provides a MII port for both 10/100Mbps operation.
- On chip PCS support for 100BASE-TX symbol mode operation.
- On chip external 10Mbps ENDEC Interface.
- Support 21MHz to 33MHz no wait state PCI Bus Interface.
- Two large Independent FIFO for transmit and receive. no additional On board buffer memory required.
- Interface to serial ROM for Ethernet ID address and jumper-less board design.
- 256KB boot ROM support.
- On chip general purpose, programmable register and I/O pins.
- Unlimited PCI burst.
- external and internal loop-back capability.
- Support early interrupts on transmit.
- Powerful on chip buffer management DMA. And PCI Bus master operation reduce CPU utilization.
- Big and little endian byte ordering supported.
- IEEE 802.3u 100BASE-T, TX, and T4 Compatible.
- 160 pin or 144 pin PQFP package.
- 5V CMOS process.

1.3 Block Diagram:

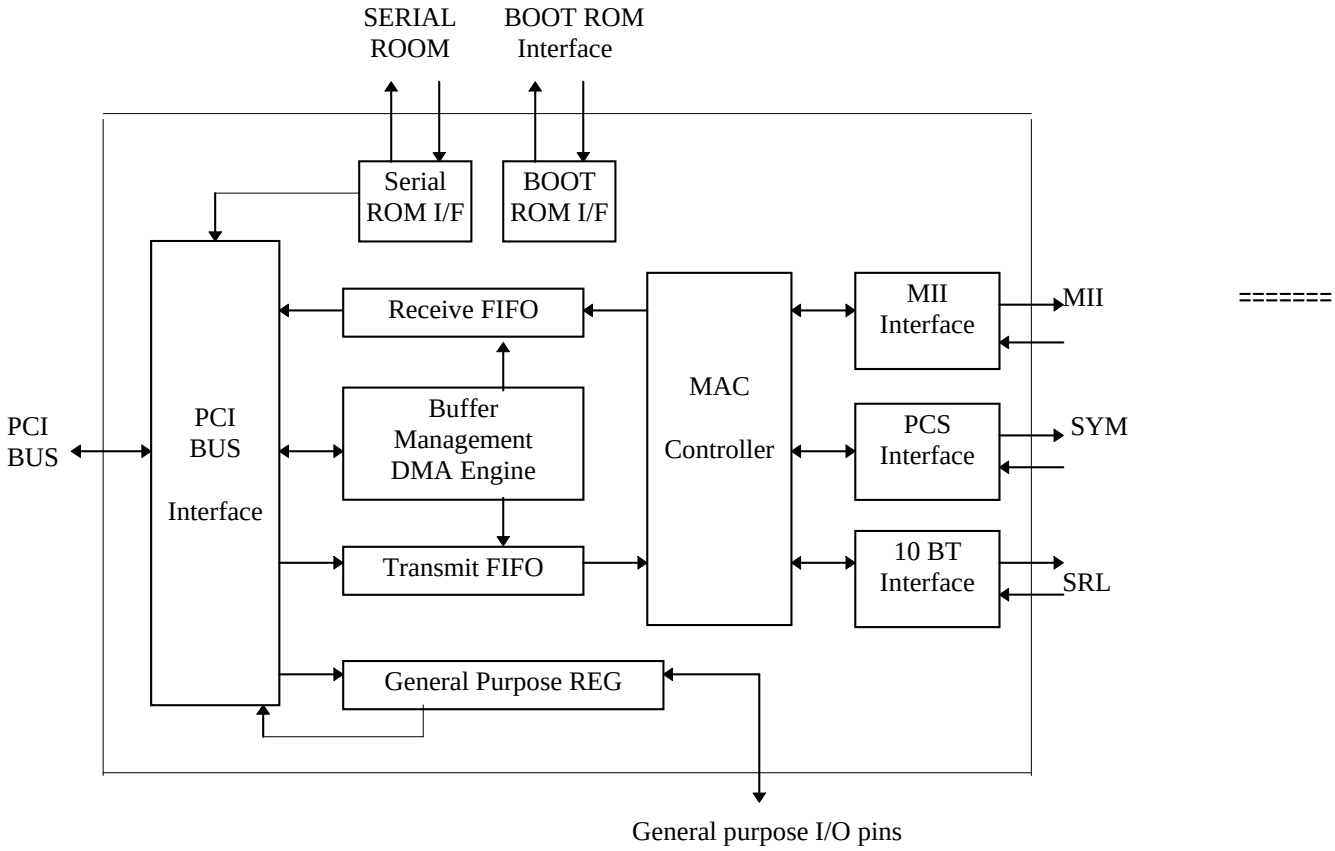


Fig - 1 AX88140A Block Diagram

1.4 AX88140AQ Pin Connection Diagram for 160-pin

The AX88140A is housed in the 160-pin plastic quad flat pack. Fig - 2 shows the AX88140A pin connection diagram.

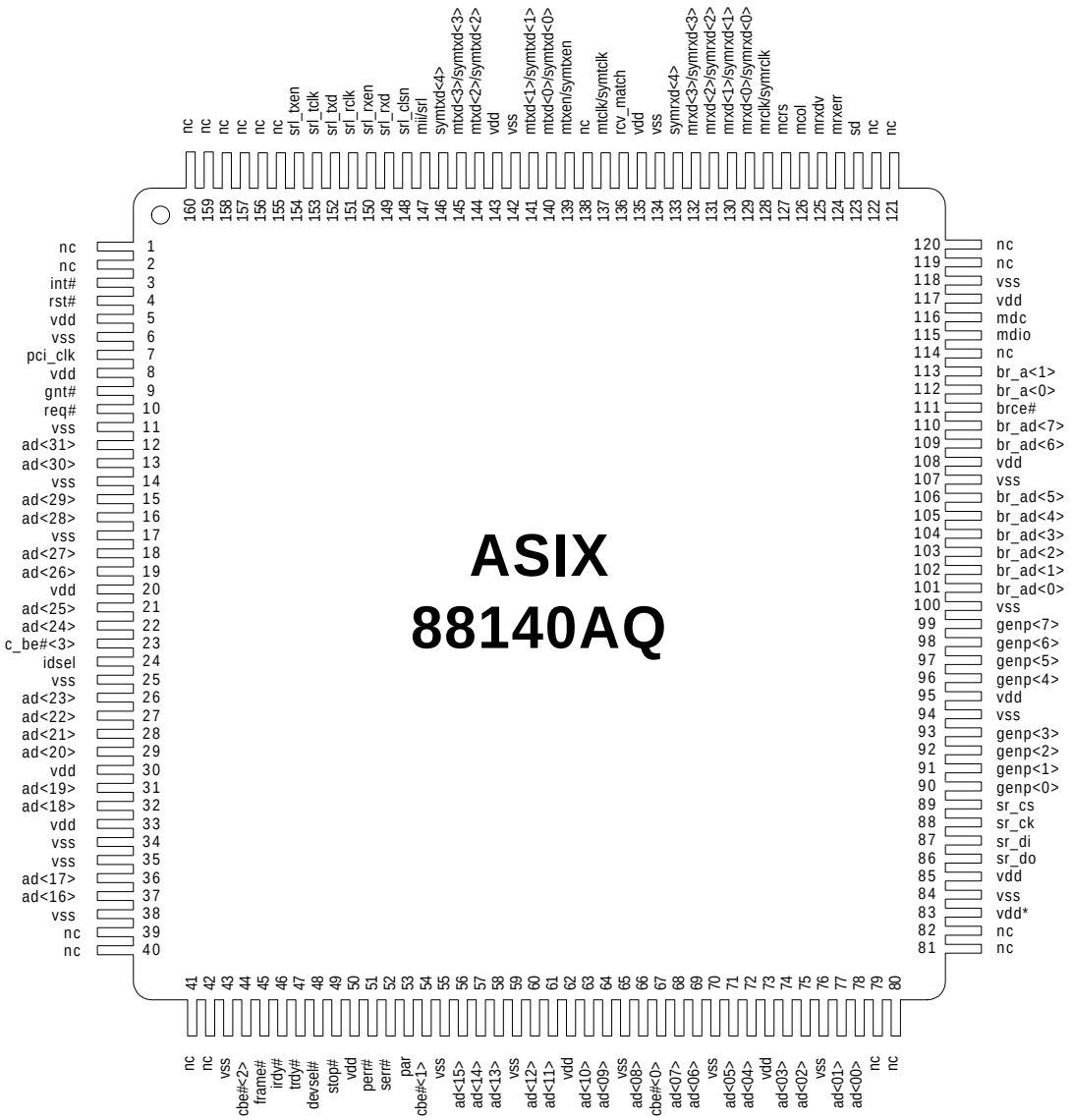


Fig - 2 AX88140AQ Pin connection diagram for 160-pin

1.5 AX88140AP Pin Connection Diagram for 144-pin

The AX88140A is housed in the 144-pin plastic quad flat pack. *Fig - 3* shows the AX88140A pin connection diagram.

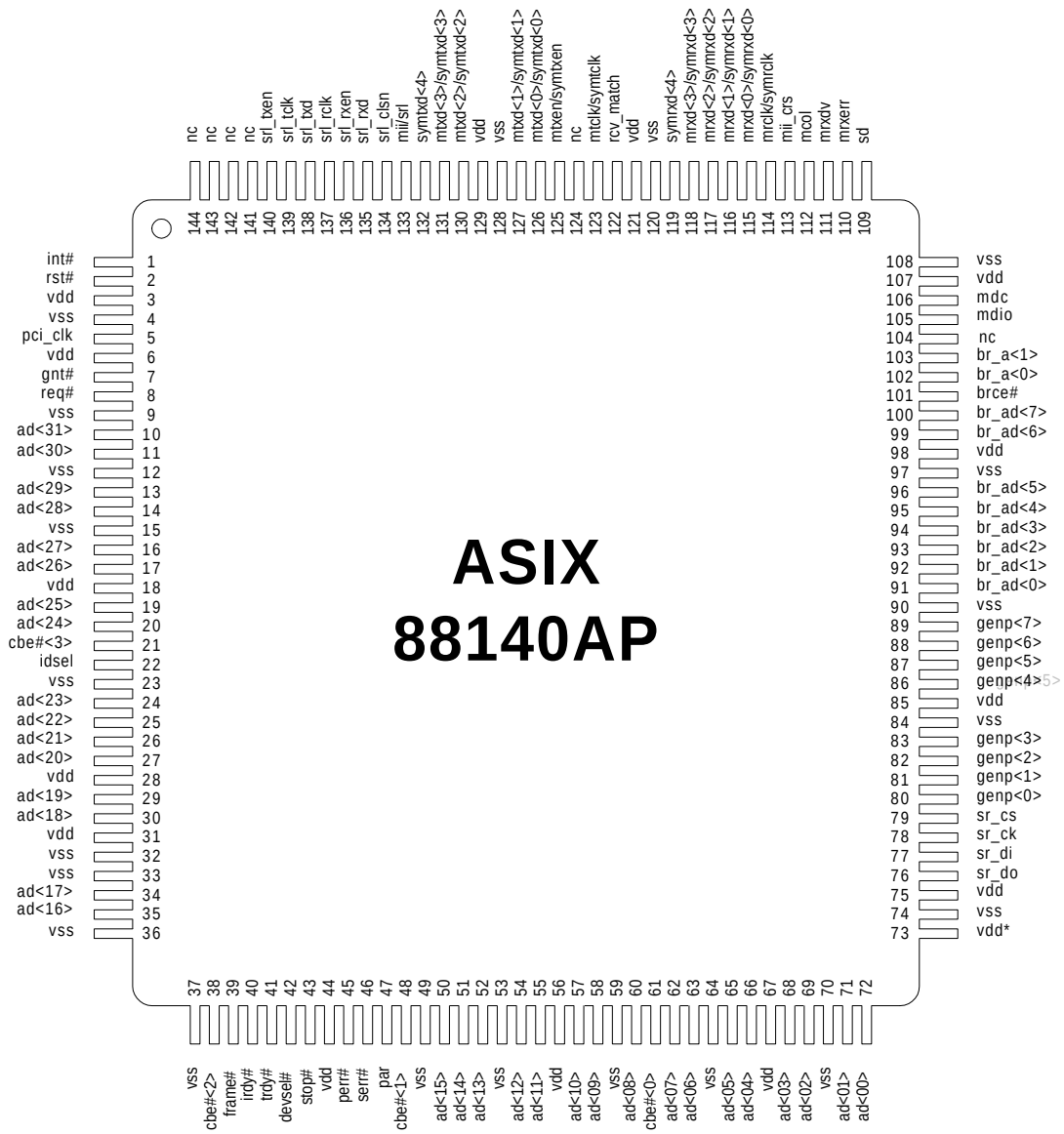


Fig - 3 AX88140AP Pin connection diagram for 144-pin

2.0 Signal Description

2.1 Signal Descriptions for 160-pin and 144-pin

The following terms describe the AX88140A pin-out:

l Address phase

Address and appropriate bus commands are driven during this cycle.

l Data phase

Data and the appropriate byte enable codes are driven during this cycle.

l #

All pin names with the # suffix are asserted low.

The following abbreviations are used in Tab - 1 PCI interface group Tab - 2 Boot ROM , Serial ROM , General-purpose signals group ,*Tab* - 3 MII/SYM/SRL interface signals group ,*Tab* - 4 Extended , NC, Power pins group..

I	**Input**
O	**Output**
I/O	**Input /Output**
O/D	**Open Drain**

2.2 PCI interface group

SIGNAL	TYPE	PIN NUMBER FOR 160 PIN	PIN NUMBER FOR 144 PIN	DESCRIPTION
AD<31> AD<30> AD<29> AD<28> AD<27> AD<26> AD<25> AD<24> AD<23> AD<22> AD<21> AD<20> AD<19> AD<18> AD<17> AD<16> AD<15> AD<14> AD<13> AD<12> AD<11> AD<10> AD<9> AD<8> AD<7> AD<6> AD<5> AD<4> AD<3> AD<2> AD<1> AD<0>	I/O	12, 13, 15, 16, 18, 19, 21, 22, 26, 27, 28, 29, 31, 32, 36, 37, 56, 57, 58, 60, 61, 63, 64, 66, 68, 69, 71, 72, 74, 75, 77, 78	10, 11, 13, 14, 16, 17, 19, 20, 24, 25, 26, 27, 29, 30, 34, 35, 50, 51, 52, 54, 55, 57, 58, 60, 62, 63, 65, 66, 68, 69, 71, 72	Address and data bits are multiplexed on the same pins. During the address phase, the AD<31:0> contain a physical address (32 bits). During, data phases, AD<31:0> contain 32 bits of data. The AX88140A supports both read and write bursts (in master operation only). Little and big endian byte ordering can be used.
CBE#<3> CBE#<2> CBE#<1> CBE#<0>	I/O	23, 44, 54, 67	21, 38, 48, 61	BUS COMMAND and BYTE ENABLE Are multiplexed on the same PCI pins. During the address phase of the transaction, CBE#<3:0> Provide the BUS COMMAND. During the data phase, CBE#<3:0> Provide the BYTE ENABLE. The BYTE ENABLE determines which byte lines carry valid data., CBE#<0> Applies to byte 0, and CBE#<3> Applies to byte 3.
DEVSEL#	I/O	48	42	Device select Is asserted by the target of the current bus access. When the AX88140A is the master of the current bus access, the target assert DEVSEL# confirming the access. It is driven by AX88140A When AX88140A is selected as a slave.
FRAME#	I/O	45	39	The FRAME# Signal is driven by the AX88140A To indicate the beginning and duration of an access. FRAME# Asserts to indicate the beginning of a bus transaction. While FRAME# is asserted, data transfers continue. When FRAME# deasserts the next data phase is the final data phase transaction.
GNT#	I	9	7	BUS GRANT Indicates to the AX88140A That access to the bus is granted.
IDSEL	I	24	22	Initialization devise select asserts To indicate that the host is issuing a configuration cycle to the AX88140A.
INT#	O/D	3	1	Interrupt request asserts When one of the appropriate bits of reg5 sets and causes an interrupt, provided that the corresponding mask bit in reg7 is not asserted. interrupt request deasserts by writing a 1 into the appropriate crs5 bit. This pin must be pulled up by an external resistor.
IRDY#	I/O	46	40	Initiator ready Indicates the bus master ability to complete the current data phase of the transaction. A data phase is completed on any rising edge of the clock When both IRDY# and target ready TRDY# are asserted. Wait cycles are inserted until both IRDY# and TRDY# are asserted together. When the AX88140A is the bus master, IRDY# is asserted during write operations to indicate that valid data is present on the AD<31:0>. During read operations, the AX88140A asserts

				IRDY# to indicate that it is ready to accept data.
PAR	I/O	53	47	Parity is an even parity bit for the AD<31:0> AD and CBE#<3:0>. During address and data phases, parity is calculated on all the AD<31:0> AND CBE#<3:0>lines whether or not any of these lines carry meaningful information.
PCI_CLK	I	7	5	The clock provides the timing for the AX88140A related PCI bus transactions. All the bus signals are sampled on the rising edge of PCI_CLK. The clock frequency range is between 21MHZ and 33MHZ.
PERR#	I/O	51	45	Parity error asserts when a data parity error is detected. When the AX88140A is the bus master it monitor PERR# to see if the target report a data parity error., when the AX88140A is the bus target and a parity error is detected, the AX88140A asserts PERR#. This pin must be pulled up by an external resistor.
REQ#	O	10	8	Bus request is asserted by the AX88140A to indicate to the bus arbiter that it wants to use the bus.
RST#	I	4	2	Resets the AX88140A to its initial state. This signal must be asserted for at least 10 active PCI clock cycles. When is the reset state, all PCI output pins are put into tri-state and all PCI o/d signals are floated.
SERR#	I/O	52	46	System Error is used by AX88140A to report address parity Error. This pin must be pulled up by an external resistor.
STOP#	I/O	49	43	Stop indicator indicates that the current target is requesting the bus master to stop the current transaction. The AX88140A responds to the assertion of STOP# when it is the bus master, and stop the current transaction.
TRDY#	I/O	47	41	Target ready indicates the target ability to complete the current data phase of the transaction. A data phase is completed on any clock when both TRDY# and IRDY# are asserted. Wait cycles are inserted until both IRDY# and TRDY# are asserted together. When the AX88140A is the bus master, target ready is asserted by the bus slave on the read operation, indicating that valid data is present on the ad lines. During a write cycle, it indicates that the target is prepared to accept data.

Tab - 1 PCI interface group

2.3 Boot ROM , Serial ROM , General-purpose signals group

SIGNAL	TYPE	PIN NUMBER FOR 160 PIN	PIN NUMBER FOR 144 PIN	DESCRIPTION
BR_A<0>	0	112	102	Boot ROM address line bit 0.
BR_A<1>	0	113	103	Boot ROM address line bit 1. This pin also latches the boot ROM address and control lines by the two external latches.
BR_AD<7> BR_AD<6> BR_AD<5> BR_AD<4> BR_AD<3> BR_AD<2> BR_AD<1> BR_AD<0>	I/O	110, 109, 106, 105, 104, 103, 102, 101	100, 99, 96, 95, 94, 93, 92, 91	Boot ROM address and data multiplexed lines bits 7 through 0. In the first of two consecutive address cycles, these lines contain the boot ROM address bits 9 through 2; followed by boot ROM address bits 17 through 10 in the second cycle. During the data cycle, bits 7 through 0 contain data.
BR_CE#	O	111	101	Boot ROM chip enable.
SR_CK	O	88	78	Serial ROM clock signal.
SR_CS	O	89	79	Serial ROM chip-select signal.
SR_DI	O	87	77	Serial ROM data-in signal.
SR_DO	I	86	76	Serial ROM data-out signal.
GENP<7> GENP<6> GENP<5> GENP<4> GENP<3> GENP<2> GENP<1> GENP<0>	I/O	99, 98, 97, 96, 93, 92, 91, 90	89, 88, 87, 86, 83, 82, 81, 80	General-purpose pins can be used by software as either status pins or control pins. These pins can be configured by software to perform either input or output functions.

Tab - 2 Boot ROM , Serial ROM , General-purpose signals group

2.4 MII/SYM/SRL interface signals group

SIGNAL	TYPE	PIN NUMBER FOR 160 PIN	PIN NUMBER FOR 144 PIN	DESCRIPTION
MCOL	I	126	112	Collision detected is asserted when detected by an external physical layer protocol(PHY) device.
MCRS	I	127	113	Carrier sense is asserted by the PHY when the media is active.
MRXDV	I	125	111	Data valid is asserted by an external PHY when receive data is present on the MRXD/SYRXD lines and is deasserted at the end of the packet. This signal should be synchronized with the MRCLK/SYMRCLK signal.
MRXERR	I	124	110	Receive error asserts when a data decoding error is detected by an external PHY device. This signal is synchronized to MRCLK/SYMRCLK and can be asserted for a minimum of one receive clock. When asserted during a packet reception, it sets the cyclic redundancy check(CRC) error bit in the receive descriptor (RDESO).
MDC	O	116	106	MII management data clock is sourced by the AX88140A to the PHY devices as a timing reference for the transfer of information on the MII_MDIO signal.
MDIO	I/O	115	105	MII management data input/output transfers control information and status between the PHY and the AX88140A.
MII/SRL	O	147	133	Indicates the selected port: SRL or MII/SYM. When asserted, the MII/SYM port is active. When deasserted, the SRL port is active.

MRCLK/SYMRCLK	I	128	114	Supports either the 25-MHZ or 2.5-MHZ receive clock. This clock is recovered by the PHY.
MRXD<3>/SYMRXD<3> MRXD<2>/SYMRXD<2> MRXD<1>/SYMRXD<1> MRXD<0>/SYMRXD<0>	I	132, 131, 130, 129	118, 117, 116, 115	Four parallel receive data lines When MII mode is selected. This data is driven by an external PHY that attached the media and should be synchronized with the MRCLK/SYMRCLK signal.
MTCLK/SYMTCLK	I	137	123	Supports the 25-MHZ or 2.5-MHZ transmit clock supplied by the external physical layer medium dependent (PMD) device. This clock should always be active.
MTXD<3>/SYMTXD<3> MTXD<2>/SYMTXD<2> MTXD<1>/SYMTXD<1> MTXD<0>/SYMTXD<0>	O	145, 144, 141, 140	131, 130, 127, 126	Four parallel transmit data lines. This data is synchronized to the assertion of the MTCLK/SYMTCLK signal and is latched by the external PHY on the rising edge of the MTCLK/SYMTCLK signal.
MTXEN/SYMTXEN	O	139	125	Transmit enable signals that the transmit is active to an external PHY device. In PCS mode (REG6<23>), This signal reflects the transmit activity of the MAC sub-layer.
RCV_MATCH	O	136	122	Receive match indication is asserted when a received packet has passed address recognition. Receive match indication is asserted when a received packet has passed address recognition.
SD	I	123	109	Signal detect indication supplied by an external physical layer medium dependent (PMD) device.
SRL_CLSN	I	148	134	Collision detect signals a collision occurrence on the Ethernet cable to the AX88140A. It may be asserted and deasserted asynchronously by the external ENDEC to the receive clock.
SRL_RCLK	I	151	137	Receive clock carries the recovered receive clock supplied by an external ENDEC. during idle periods, SRL_RCLK may be inactive.
SRL_RXD	I	149	135	Receive data carries the input receive data from the external ENDEC. The incoming data should be synchronous with the SRL_RCLK signal.
SRL_RXEN	I	150	136	Receive enable signals activity on the Ethernet cable to the AX88140A. It is asserted when receive data is present on the Ethernet cable and is deasserted at the end of a frame. It may be asserted and deasserted asynchronously to the receive clock (SRL_RCLK) by the external ENDEC.
SRL_TCLK	I	153	139	Transmit clock carries the transmit clock supplied by an external ENDEC. This clock must always be active (even during reset).
SRL_TXD	O	152	138	Transmit data carries the serial output data from the AX88140A. This data is synchronized to the SRL_TCLK signal.
SRL_TXEN	O	154	140	Transmit enable signals an external ENDEC That the AX88140A transmit is in progress.
SYMRXD <4>	I	133	119	Receive data, together with the four receive lines MII/SYM_RXD<3:0>, Provide five parallel lines of data in symbol from for use in PCS mode (100BASE-T, REG6<23). This data is synchronized on the rising edge of the MTCLK/SYMTCLK signal.
SYMTXD<4>	O	146	132	Transmit data, together with the our transmit lines MII/SYM_TXD<3:0>,provide five parallel lines of data in symbol form for use in PCS mode (100BASE-T, REG6<23>). This data is synchronized on the rising edge of the MII/SYM_TCLK signal.

Tab - 3 MII/SYM/SRL interface signals group

2.5 Extended , NC, Power pins group

SIGNAL	TYPE	PIN NUMBER FOR 160 PIN	PIN NUMBER FOR 144 PIN	DESCRIPTION
EC<15:0>	O	160,159,122, 121,120,119, 82,81,80,79,42,41 ,40,39,2,1	NONE	Expended pins. do not connect.
NC	O	114,138,155,156, 157,158	104,124,141,142, 143,144	No connection.
VDD	P	5,8,20,30,33, 50,62,73,85, 95,108,117, 135,143	3,6,18,28,31, 44,56,67,75, 85,98,107, 121,129	5-V supply input voltage.
VDD*	P	83	73	5.0-V reference for 5.0-V signaling environments
VSS	P	6,11,14,17,25, 34,35,38,43, 55,59,65,70, 76,84,94,100, 107,118,134, 142	4,9,12,15,23, 32,33,36,37, 49,53,59,64, 70,74,84,90,97,10 8,120,128	Ground pins.

Tab - 4 Extended , NC, Power pins group

3.0 Configuration Operation

1. Software reset (REG0<0>) has no effect on the configuration registers.

2. Hardware reset puts the configuration registers in default values.

3. The configuration registers could be accessed in byte, word , and long-word.

3.1 Configuration Space Mapping

CONFIGURATION REGISTER	IDENTIFIER	I/O ADDRESS OFFSET
DEVICE/VENDOR ID	CSID	00H
COMMAND AND STATUS	CSCS	04H
REVISION	CSRV	08H
LATENCY TIMER	CSLT	0CH
BASE I/O ADDRESS	CBIO	10H
BASE MEMORY ADDRESS	CBMA	14H
RESERVED	-	18H-28H
SUBSYSTEM ID	-	2CH
EXPANSION ROM BASE ADDRESS	CBER	30H
RESERVED	-	34H - 38H
INTERRUPT	CSIT	3CH
Special Use	SUD	40H

Tab - 5 Configuration Space Mapping

3.2 Configuration Space

3.2.1 Configuration ID Register (CSID)

FIELD	R/W	DESCRIPTION
31:16	R	Device ID : Provides the unique AX88140A ID number (1400H)
15:0	R	Vender ID : Provides the manufacturer of the AX88140A (125BH)

Tab - 6 CSID Configuration ID Register Description

3.2.2 Command and Status Configuration Register (CSCS)

FIELD	R/W	TYPE	DESCRIPTION
31	R	STATUS	Detected Parity Error : active high
30	R	STATUS	Signal System Error : active high
29	R	STATUS	Received Master Abort : active high
28	R	STATUS	Received Target Abort : active high
26:25	R	STATUS	Device Select Timing : fixed at 01 which indicates a medium assertion of DEVSEL#
24	R	STATUS	Data Parity Report : active high
23	R	STATUS	Fast Back-to-Back : always set
22:9	-	RESERVED	
8	R/W	COMMAND	System Error Enable : active high
6	R/W	COMMAND	Parity Error Response : active high
2	R/W	COMMAND	Master Operation : active high
1	R/W	COMMAND	Memory Space Access : active high
0	R/W	COMMAND	I/O Space Access : Active high

Tab - 7 CSCS Command and Status Configuration Register

3.2.3 Configuration Revision Register (CSRV)

FIELD	R/W	DESCRIPTION
31:24	R	Base Class : Always equal to 2H that indicates the network controller
23:16	R	Subclass : Always equal to 0H that indicates the fast Ethernet controller
7:4	R	Revision Number : Indicates the AX88140A revision number and is equal to 0H
3:0	R	Step Number : Indicates the AX88140A step number and is referred to current silicon step.

Tab - 8 CSRV Configuration Revision Register Description

3.2.4 Configuration Latency Timer Register (CSLT)

FIELD	R/W	DESCRIPTION
31:16	R/W	Reserved
15:8	R/W	Configuration Latency Timer. The value after hardware reset equal to 0h.
7:0	R/W	Reserved

Tab - 9 CSLT Configuration ID Register Description

3.2.5 Configuration Base I/O Address Register (CBIO)

FIELD	R/W	DESCRIPTION
31:7	R/W	Configuration Base I/O Address : Defines the address assignment mapping of AX88140A's regs.
6:1	R	This field value is 0 when read
0	R	I/O Space Indicator : Determines that the register maps into the I/O space. The value in this field is 1.

Tab - 10 CBIO Configuration Base I/O Address Register Description

3.2.6 Configuration Base Memory Address Register (CBMA)

FIELD	R/W	DESCRIPTION
31:7	R/W	Configuration Base Memory Address : Defines the address assignment mapping of AX88140A's regs.
6:1	R	This field value is 0 when read
0	R	Memory Space Indicator : Determines that the register maps into the memory space. The value in this field is 0.

Tab - 11 CBMA Configuration Base Memory Address Register Description

3.2.7 Expansion ROM Base Address Register (CBER)

FIELD	R/W	DESCRIPTION
31:10	R/W	Expansion ROM Base Address
9:1	R	This field value is 0 when read
0	R/W	Expansion ROM Enable Bit : Active high

Tab - 12 CBER Expansion ROM Base Address Register Description

3.2.8 Configuration Interrupt Register (CSIT)

FIELD	R/W	DESCRIPTION
31:24	R	MAX_LAT : time unit is equal to 0.25 microsecond.(28H)
23:16	R	MIN_GNT : Time unit is equal to 0.25 microsecond.(14H)
15:8	R	Interrupt Pin : The AX88140A uses INTA# and the read value is (01H).
7:0	R/W	Interrupt Line : The BIOS writes the routing information into this field.

Tab - 13 CSIT Configuration Interrupt Register Description

4.0 Registers Operation

1. The REGs are quad-word aligned, 32-bits long, and must be accessed using long-word instruction with quad-word aligned addresses only.

2. Reserved bits should be written with 0.; Reserved bits are UNPREDICTABLE on read access.

3. Retries on second data transactions occur in response to burst accesses.

4.1 Registers Mapping

REGISTER	MEANING	OFFSET FROM REG BASE ADDRESS (CBIO,CBMA)
REG0	BUS MODE	00H
REG1	TRANSMIT POLL DEMAND	08H
REG2	RECEIVE POLL DEMAND	10H
REG3	RECEIVE LIST BASE ADDRESS	18H
REG4	TRANSMIT LIST BASE ADDRESS	20H
REG5	STATUS	28H
REG6	OPERATION MODE	30H
REG7	INTERRUPT ENABLE	38H
REG8	MISSED FRAME AND OVERFLOW COUNTER	40H
REG9	SERIAL ROM, AND MII MANAGEMENT	48H
REG10	-	50H
REG11	GENERAL-PURPOSE TIMER	58H
REG12	GENERAL-PURPOSE PORT	60H
REG13	FILTERING BUFFER INDEX	68H
REG14	FILTERING BUFFER DATA	70H

Tab - 14 Command and Status Register Mapping

4.2 Host REGs

4.2.1 Bus Mode Register (REG0)

FIELD	R/W/C	DESCRIPTION
31:22	-	RESERVED
21	R/W	RML - Read Multiple When set, the AX88140A supports the memory-read-multiple command on the PCI bus. This bus command is used in memory read bursts with more than one longword. When reset, the AX88140A uses memory-read command in all its memory read accesses on the PCI bus.
20	R/W	DBO - Descriptor Byte Ordering Mode When set, the AX88140A operates in big edian ordering mode for descriptors only. When reset, the AX88140A operates in little endian mode.
19:14	-	Reserved.--Written as “0” for future compatibility concern.
13:8	R/W	PBL - Programmable Burst Length Indicates the maximum number of longwords to be transfered in one DMA transaction. If reset, the ax88140a burst is limited only by the amount of data stored in the receive FIFO (at least 16 longword), or by the amount of free space in the transmit FIFO (at least 16 longword) before issuing a bus request. The PBL can be programmed with permissible values 0,1,2,4,8,16, or 32. After reset, the PBL default value is 0.
7	R/W	BLE - Big/Little Endian When set, the AX88140A operates in big endian byte ordering mode. When reset, the AX88140A operates in little endian byte ordering mode. Big endian is applicable only for data buffer
6:2	-	RESERVED
1	R/W	BAR - Bus Arbitration Selects the internal bus arbitration between the receive and transmit processes. When set, a round robin arbitration scheme is applied resulting in equal sharing between processes. When reset, the receive process has priority over the transmit process, unless the ax88140a is currently transmitting.
0	R/W	SWR - Software Reset When set, the AX88140A resets all internal hardware with the exception of the configuration area and also, it does not change the port select setting (REG6<18>). Software reset does not affect the configuration area.

Tab - 15 REG0 Bus Mode Register Description

4.2.2 Transmit Poll Demand (REG1)

FIELD	R/W	DESCRIPTION
31:0	W	TPD - Transmit Poll Demand When written with any value, the AX88140A checks for frames to be transmitted. If no descriptor is available, the transmit process returns to the suspended states and REG5<2> is asserted. If the descriptor is available the transmit process resumes.

Tab - 16 REG1 Transmit Poll Demand Register Description

4.2.3 Receive Poll Demand (REG2)

FIELD	R/W/C	DESCRIPTION
31:0	W	RPD - Receive Poll Demand When written with any value, the AX88140A checks for receive descriptors to be required. If no descriptor is available, the receive process returns to the suspended states and REG5<7> is not asserted. If the descriptor is available the receive process resumes.

Tab - 17 REG2 Receive Poll Demand Register Description

4.2.4 Receive List Base Address (REG3)

1. The register is used to point the AX88140A to the start of receive descriptors list.

2. The descriptor list resides in physical memory space and must be longword aligned. The AX88140A behaves UNPREDICTABLY when the list are not longword aligned.

3. Writing to REG3 is permitted only when receive process is in the stopped state. That is, the REG3 must be written before the receive START command is given .

REG3 Receive List Base Address Register Description

FIELD	R/W/C	DESCRIPTION
31:2	R/W	Start of receive list
1:0	R/W	Must be 00 for longword alignment

Tab - 18 REG3 Receive List Base Address Register Description

4.2.5 Transmit List Base Address (REG4)

1. The register is used to point the AX88140A to the start of transmit descriptors list.

2. The descriptor list resides in physical memory space and must be long-word aligned. The AX88140A behaves UNPREDICTABLY when the list are not long-word aligned.

3. Writing to REG4 is permitted only when transmit process is in the stopped state. That is, the REG4 must be written before the transmit START command is given .

FIELD	R/W/C	DESCRIPTION
31:2	R/W	Start of transmit list
1:0	R/W	Must be 00 for long-word alignment

Tab - 19 REG4 Transmit List Base Address Register Description

4.2.6 Status Register (REG5)

1. The status register contains all the status bits that the AX88140A reports to the host.
2. Most of the fields in this register cause the host to be interrupted.
3. REG5 bits are not cleared when read.
4. Writing 1 to these bits clears them; writing 0 has no effect. Each field can be masked.

Field	R/W/C	Description
31:26	-	Reserved
25:23	R	EB - Error Bits (Not generate interrupt) Indicates the type of error that caused system error. Valid only when fatal bus error REG5<13> is set.

25	24	23	Description
0	0	0	Parity error
0	0	1	Master abort
0	1	0	Target abort
0	1	1	Reserved
1	x	x	Reserved

22:20	-	Reserved.--Written as “0” for future compatibility concern.
19:17	-	Reserved.--Written as “0” for future compatibility concern.
16	R	NIS - Normal Interrupt Summary Only the unmasked bits affect normal interrupt summary REG5<16> bit Normal interrupt summary bit. Its value is the logical OR of :

CSR5<0>	transmit interrupt
CSR5<2>	transmit buffer unavailable
CSR5<6>	receive interrupt
CSR5<10>	Early transmit interrupt
CSR5<11>	General-purpose timer expired

15	R	AIS - Abnormal Interrupt Summary Only unmasked bits affect only the abnormal interrupt summary REG5<15> bit. Abnormal interrupt summary bits. Its value is the logical OR of :

CSR5<1>	transmit process stopped
CSR5<3>	transmit jabber time out
CSR5<5>	transmit under-flow
CSR5<7>	receive buffer unavailable
CSR5<8>	receive process stopped
CSR5<9>	receive watchdog time out
CSR5<13>	fatal bus error

13	R	FBE - Fatal Bus Error Indicates that a system error occurred. If a system error occurs, all bus accesses are disabled
11	R/W/C	GTE - General Purpose Timer Expired Indicates that the general-purpose timer (REG11) counter has expired. This timer is mainly used by the software driver.
10	R/W/C	ETI - Early Transmit Interrupt Indicates that the packet to be transmitted was fully transferred into the chip‘s internal transmit FIFOs. Transmit interrupt (REG5<0>) automatically clears this bit.
9	R/W/C	RWT - Receive watchdog Time out Indicates that the receive watchdog timer expired and another node is still active on the network. In case of overflow, the long packets may not be received.
8	R/W/C	RPS - Receive Process Stopped Asserts when the receive process enters stopped state.
7	R/W/C	RU - Receive Buffer Unavailable Indicates the next descriptor in the receive list is owned by the host and cannot be acquired by the AX88140A.The reception process is suspended.
6	R/W/C	RI - Receive Interrupt Indicates the completion of a frame reception. Specific frame status information has been posted in the descriptor. The reception process remains in the running state.
5	R/W/C	UNF - Transmit Under-flow Indicates that the transmit FIFO had an under-flow condition during the packet transmission. The transmit process is placed in the suspended state and under-flow error TDES0<1> is set.
4	-	Reserved.--Written as “0” for future compatibility concern.

3	R/W/C	TJT - Transmit Jabber Time-out Indicates that the transmit jabber timer expired, meaning that the AX88140A transmitter had been excessively active. The transmission process is aborted and placed in the stopped state. This event causes the transmit jabber time-out TDES0<14> is set.
2	R/W/C	TU - Transmit Buffer Unavailable Indicates that the next descriptor on the transmit list is owned by the host and cannot be acquired by the AX88140A.The transmission process is suspended. To resume processing transmit descriptors, the host should change the ownership bit of the descriptor and then issue a transmit poll demand command.
1	R/W/C	TPS - Transmit Process Stopped Asserts when the transmit process enters the stopped state.
0	R/W/C	TI - Transmit Interrupt Indicates that a frame transmission was completed, while TDES1<31> is asserted in the first descriptor of the frame.

Tab - 20 REG5 Status Register Description

4.2.7 Operation Mode Register (REG6)

1. REG6 establishes the receive and transmit operating modes and commands.
2. REG6 should be the last REG to be written as part of initialization.

Field	R/W/C	Description		
31	-	Reserved		
30	R/W	RA - Receive All	1	All incoming packets will be received
			0	Filtering mode
29:25	-	Reserved.--Written as “0” for future compatibility concern.		
24	R/W	SCR - Scrambler Mode	1	Enable Scrambler
			0	Disable Scrambler
23	R/W	PCS - PCS Mode	1	PCS functions are active
			0	MII/SYM port is not selected
22	R/W	TTM - Transmit Threshold Mode	1	Threshold is 10Mb/s
			0	Threshold is 100Mb/s
21	R/W	SF - Store and Forward	1	Enable Store and Forward
			0	Disable Store and Forward
20	-	Reserved.--Written as “0” for future compatibility concern.		
19	R/W	HBD - Heartbeat Disable	1	Heartbeat Disable
			0	Heartbeat Enable
18	R/W	PS - Port Select	1	MII/SYM port is selected.
			0	SRL port is selected
17:16	-	Reserved.--Written as “0” for future compatibility concern.		
15:14	R/W	TR - Threshold Control Bits The threshold value has a direct impact on the AX88140A bus arbitration scheme . Transmission starts when the frame size within the transmit FIFO is larger than the threshold. In addition, full frames with a length less than the threshold are also transmitted. The transmit process must be in the stopped state to change these bits. Controls the selected threshold level for the AX88140A transmit FIFO. Four threshold levels are allowed.		

		REG6<18>=0	REG6<18>=1	REG6<18>=1
REG6<21>	REG6<15:14>	REG6<22>=X	REG6<22>=1	REG6<22>=0
0	00	72	72	128
0	01	96	96	256
0	10	128	128	512
0	11	160	160	1024
1	XX	Store & Forward	Store & Forward	Store & Forward

13	R/W	ST - Start/Stop Transmission	1	Start Transmission
			0	Stop Transmission
12	R/W	FC - Force Collision Mode	1	Enable force collision
			0	Disable force collision
11:10	R/W	OM - Operating Mode	00	Normal
			01	Internal Loop-back
			10	External Loop-back
9	R/W	FD - Full-Duplex Mode	1	Full-Duplex

			0	Half-Duplex
8	R/W	RB - Receive broadcast packet	1	Accept broadcast packet
			0	Reject broadcast packet
7	R/W	PM - Pass All Multicast	1	Enable Pass All Multicast
			0	Disable Pass All Multicast
6	R/W	PR - Promiscuous Mode	1	Indicates that any incoming valid frame is received, regardless of its destination address.
			0	Disable Promiscuous Mode.
5:4	-	Reserved.--Written as “0” for future compatibility concern.		
3	R/W	PB - Pass Bad Frames	1	All incoming frames that passed the address filtering are received, including runt frames, collided fragments, or truncated frames caused by FIFO over-flow. If any received bad frames are required, promiscuous mode (REG6<6>) should be set to 1.
			0	Disable pass bad frame.
2	-	Reserved.--Written as “0” for future compatibility concern.		
1	R/W	SR - Start/Stop Receive	1	Start Receive
			0	Stop Receive
0	R	PLS - PCS_SYM Link Status : Active high.		

Tab - 21 REG6 Operation Mode Register Description

Port and Data Rate Selection

REG6 <18>	REG6 <22>	REG6 <23>	REG6 <24>	ACTIVE PORT	DATA RATE	FUNCTION
0	0	X	X	SRL	10MB/S	Conventional 10MB/S ENDEC interface
1	1	0	0	MII/SYM	10MB/S	MII with transmit FIFO thresholds appropriate for 10MB/S
1	0	0	0	MII/SYM	100MB/S	MII with transmit FIFO thresholds appropriate for 100MB/S
1	0	1	0	MII/SYM	100MB/S	PCS function for 100BASE-FX
1	0	1	1	MII/SYM	100Mb/s	PCS and scrambler functions for 100BASE-T

Tab - 22 Port and Data Rate Selection

4.2.8 Interrupt Enable Register (REG7)

1. The interrupt enable register (REG7) enables the interrupts reported by REG5.
2. Setting bit to 1 enables a corresponding interrupt. After a hardware or software reset, all interrupts are disabled.

Field	R/W/C	Description	
31:17	-	Reserved	
16	R/W	NI - Normal Interrupt Summary Enable When set, normal interrupt is enabled. When reset, no normal interrupt is enabled. This bit (REG7<16>) enables the following bits :	
		CSR5<0>	Transmit interrupt
		CSR5<2>	Transmit buffer unavailable
		CSR5<6>	Receive interrupt
		CSR5<10>	Early transmit interrupt
		CSR5<11>	General-purpose timer expired
15	R/W	AI - Abnormal Interrupt Summary Enable When set, abnormal interrupt is enabled. When reset, no abnormal interrupt is enabled. This bit (REG7<15>) enables the following bits :	
		CSR5<1>	transmit process stopped
		CSR5<3>	transmit jabber time-out
		CSR5<5>	transmit under-flow
		CSR5<7>	receive buffer unavailable
		CSR5<8>	receive process stopped
		CSR5<9>	receive watchdog time-out
		CSR5<11>	fatal bus error
13	R/W	FBE - Fatal Bus Error interrupt enable. Active high.	
11	R/W	GPT - General purpose Timer interrupt Enable. Active high.	
10	R/W	ETE - Early Transmit Interrupt Enable. Active high.	
9	R/W	RW - Receive Watchdog Time out interrupt Enable. Active high	
8	R/W	RS - Receive Stopped interrupt Enable. Active high.	
7	R/W	RU - Receive Buffer Unavailable interrupt Enable. Active high.	
6	R/W	RI - Receive Interrupt Enable. Active high.	
5	R/W	UN - under-flow interrupt Enable. Active high.	
4	-	Reserved.--Written as “0” for future compatibility concern.	
3	R/W	TJ - Transmit Jabber Time out interrupt Enable. Active high.	
2	R/W	TU - Transmit Buffer Unavailable interrupt Enable. Active high.	
1	R/W	TS - Transmission Stopped interrupt Enable. Active high.	
0	R/W	TI - Transmit Interrupt Enable. Active high.	

Tab - 23 REG7 Interrupt Enable Register Description

4.2.9 Missed Frame and Overflow Counter (REG8)

Field	R/W	Description
31:29	-	Reserved
28	R/C	Overflow counter overflow Sets When the overflow counter overflows, Resets When REG8 is read.
27:17	R/C	Overflow counter Indicates the number of frames discarded because of overflow. The counter clears when read.
16	R/C	Missed frame overflow Sets When the missed frame counter overflows; Resets When reg8 is read.
15:0	R/C	Missed Frame Counter Indicates the number of frames discarded because no host receive descriptors were available. The counter clears when read.

Tab - 24 REG8 Missed Frame and Overflow Counter Description

4.2.10 Serial ROM and MII Management Register (REG9)

1. The register provides an interface to the Microwire serial ROM and to the physical layer protocol (PHY). It selects the device and contains both the commands and data to be read from and stored in the serial ROM.
2. The MII management selects and operation mode for reading and writing the MII.

FIELD	R/W/C	DESCRIPTION
31:20	-	Reserved.--Written as “0” for future compatibility concern.
19	R	MDI - MII management data_in Used by the AX88140A to read data from the PHY
18	R/W	MII - MII management operation mode Defines the operation mode (read or write) of the PHY.
17	R/W	MDO - MII Management write data Specifies the value of the data that AX88140A writes to the PHY
16	R/W	MDC - MII Management clock MII management data clock (MII_MDC) is an output signal to the PHY. it is used as a timing reference.
14	R/W	RD - Read operation Read control bit. When set together with REG9<12>, The AX88140A performs read cycles from the BOOT ROM, and the serial ROM.
13:12	-	Reserved.--Written as “0” for future compatibility concern.
11	R/W	SR - SERIAL ROM select When set together with either SERIAL ROM read operation (REG9<14>) or SERIAL ROM Write operation (REG9<13>), The AX88140A selects the SERIAL ROM.
10:4	-	Reserved.--Written as “0” for future compatibility concern.
3	R/W	SDO - SERIAL ROM data_out SERIAL ROM data output(SR_DO) From the SERIAL ROM device to the AX88140A.
2	R	SDI - SERIAL ROM data_in SERIAL ROM Data input(SR_DI) To the SERIAL ROM device from the AX88140A.
1	R/W	SCLK - SERIAL ROM serial clock Serial clock (SR_CK) Output to the SERIAL ROM.
0	R/W	SCS - Serial ROM Chip Select Chip select (sr_cs) output to the serial ROM.

Tab - 25 REG9 Serial ROM, and MII Management Register Description

4.2.11 General -Purpose Timer (REG11)

1. This register contains a 16 bit general-purpose timer. It is used mainly by the software driver for timing functions not supplied by the operating system. After the timer is loaded, it starts counting down . The expiration of the timer causes an interrupt in REG5<11>.
2. If the timer expires with the CON bit on, the counter will load itself automatically with the last value. The timer is not active in snooze mode.

Field	R/W/C	Description		
31:17	-	Reserved.--Written as “0” for future compatibility concern.		
16	R/W	CON - Continuous Mode	1	Continuous operating mode.
			0	One-shot operating mode.
15:0	R/W	Timer value Contains the general-purpose timer value within a N microsecond cycle.		
		SRL_10M : 204.8us		
		MII_10M : 819.2us		
		MII_100M : 81.92us		

Tab - 26 REG11 General -Purpose Timer Register Description

4.2.12 General -Purpose Port Register (REG12)

Field	R/W/C	Description		
31:9	-	Reserved.--Written as “0” for future compatibility concern.		
8	R/W	GPC - General Purpose Control . When a hardware reset is initiated, all gep pins become input pins.	1	Indicate next write REG12<7:0> is use for define General purpose port in/out direction.
			0	Indicate next write REG12<7:0> is use for read/write general purpose port data.
7:0	R/W	MD - General Purpose Mode and Data		

Tab - 27 REG12 General -Purpose Port Register Description

4.2.13 Filtering Index (REG13)

FIELD	R/W/C	DESCRIPTION
31:6	-	Reserved.--Written as “0” for future compatibility concern.
5:0	R/W	FI - Filtering Index When writing data to filtering buffer, uses filtering index register REG13 to point the position (buffer number) in filtering buffer. The valid value is between 0 and 3.

Tab - 28 REG13 Filtering Index Register Description

4.2.14 Filtering data (REG14)

FIELD	R/W/C	DESCRIPTION
31:0	R/W	FD - Filtering Data By indexed by filtering index register REG13, write the filtering data register REG14 to put filtering address/hash table into filtering buffer..

Tab - 29 REG14 Filtering Data Register Description

Filtering Buffer

The AX88140A stores one Ethernet address for local physical address and filters the packets with multicast addresses by 64 bits array. For any incoming frame with a multicast destination address, the AX88140A applies the standard Ethernet cyclic redundancy check function to the destination address, then uses the most significant 6 bits of the result as a bit index into the table. If the indexed bit is set, the frame is accepted. If the bit is reset, the frame is rejected.

Description of Filtering Buffer

BUFFER NUMBER	DESCRIPTION
0	BYTE 0 - 3 OF LOCAL PHYSICAL ADDRESS
1	BYTE 4 - 5 OF LOCAL PHYSICAL ADDRESS IN THE LEAST SIGNIFICANT WORD
2	BIT 0 - 31 OF MULTICAST ADDRESS FILTERING TABLE
3	Bit 32 - 63 of multicast address filtering table

Tab - 30 Description of Filtering Buffer

Layout of Filtering Buffer

BUFFER NUMBER	BYTE 3	BYTE 2	BYTE 1	BYTE 0
0	PHYSICAL ADDRESS BYTE 3	PHYSICAL ADDRESS BYTE 2	PHYSICAL ADDRESS BYTE 1	PHYSICAL ADDRESS BYTE 0

1	RESERVED	RESERVED	PHYSICAL ADDRESS BYTE 5	PHYSICAL ADDRESS BYTE 4
2	MULTICAST ADDRESS FILTERING TABLE BIT 24 - 31	MULTICAST ADDRESS FILTERING TABLE BIT 16 - 23	MULTICAST ADDRESS FILTERING TABLE BIT 8 - 15	MULTICAST ADDRESS FILTERING TABLE BIT 0 - 7
3	multicast address filtering table bit 56 - 63	multicast address filtering table bit 48 - 55	multicast address filtering table bit 40 - 47	multicast address filtering table bit 32 - 39

Tab - 31 Layout of Filtering Buffer

5.0 Host Communication

Descriptor lists and data buffers, collectively called the host communication, reside in the host memory and manage the actions and status related to buffer management.

5.1 Descriptor Lists and Data Buffers

The AX88140A transfers data frames to the receive buffers and from the transmit buffers in host memory. Descriptors that reside in the host memory act as pointers to these buffers.

There are two descriptor lists, one for receive and one for transmit. The base address of each list is written into REG3 and REG4, respectively. A descriptor list is forward-linked (explicitly). The last descriptor may point back to the first entry to create a ring structure. Explicit chaining of descriptors is accomplished by setting the address pointer chained in both the receive and transmit descriptors (RDES3 and TDES3). The descriptor lists reside in the host physical memory address space.
A data buffer consists of either an entire frame or part of a frame, but it cannot exceed a single frame. Buffers contain only data; buffer status is maintained in the descriptor. Data chaining refers to frames that span multiple data buffers.

Descriptor Structure Example

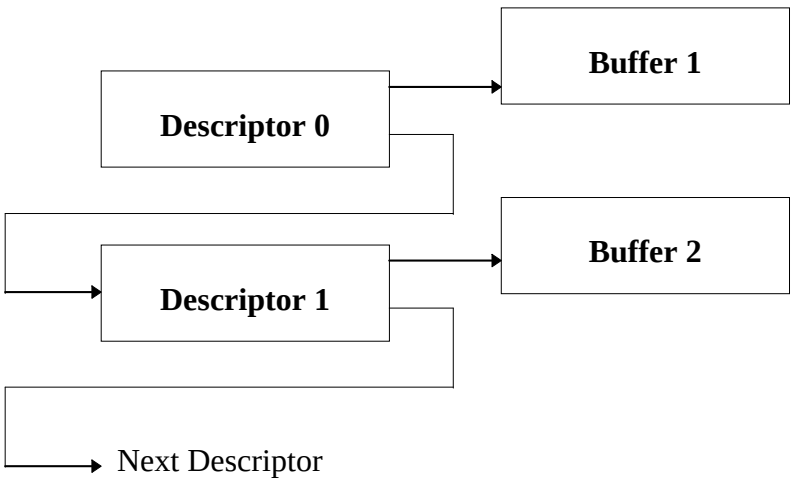


Fig - 4 Descriptor Structure Example

5.2 Receive Descriptors

The receive descriptor provides one buffer, one byte-count buffer, and one address pointer in each descriptor. Descriptors and receive buffers addresses must be long-word aligned.

Receive Descriptor Format

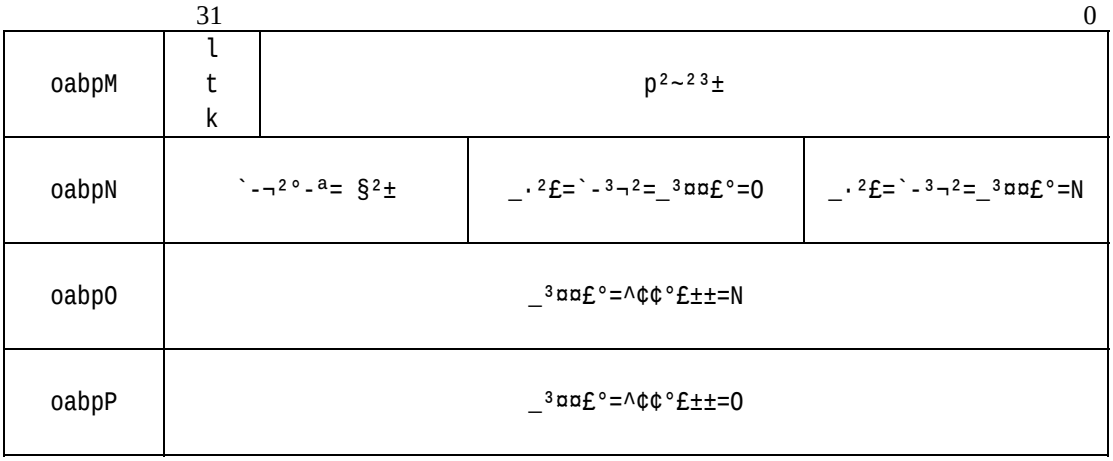


Fig - 5 Receive Descriptor Format

5.2.1 Receive Descriptor 0 (RDES0)

RDES0 contains the received frame status, the frame length, and the descriptor ownership information.

Field	Description		
31	OWN - Own Bit The AX88140A clears this bit either when it completes the frame reception or when the buffers that are associated with this descriptor are full.	1	Indicates that the descriptor is owned by the AX88140A
		0	Indicates that the descriptor is owned by the host
30	FF - Filtering Fail This bit can be set only when receive all (REG6<30>) is set.	1	Indicates that the frame failed the address recognition filtering
		0	Indicates that the frame passed the address recognition filtering
29:16	FL - Frame Length Indicates the length in bytes of the received frame including the cyclic redundancy check (CRC). This field is valid only when last descriptor (RDES0<8>) is set and descriptor error (RDES0<14>) is reset.		
15	ES - Error Summary Indicates the logical OR of the following RDES0 bits : This field is valid only when last descriptor (RDES0<8>) is set.		
	RDES0<1>	CRC error	
	RDES0<6>	collision seen	
	RDES0<7>	frame too long	
	RDES0<11>	runt frame	
	RDES0<14>	descriptor error	
14	DE - Descriptor Error. The frame is truncated. Active high. This field is valid only when last descriptor (RDES0<8>) is set.		
13:12	Reserved.--Written as “0” for future compatibility concern.		
11	RF - Runt Frame. Indicates that this frame is a runt frame. Active high. This field is valid only when last descriptor (RDES0<8>) is set .		

10	MF - Multicast Frame Indicates that this frame is a multicast address. This field is valid only when last descriptor (RDES0<8>) is set.		
9	FS - First Descriptor	1	Indicates that this descriptor contains the first buffer of a frame.
		0	Indicates that this descriptor is the middle or last buffer of a frame.
8	LS - Last Descriptor	1	Indicates that the buffers pointed to by this descriptor, are the last buffers
		0	Indicates that this descriptor is the middle or first buffer of a frame.
7	TL - Frame Too Long. Frame length grater then 1518 bytes. Active high. This field is valid only when last descriptor (RDES0<8>) is set.		
6	CS - Collision Seen. This is a late collision. This field is valid only when last descriptor (RDES0<8>) is set.		
5	Reserved.--Written as “0” for future compatibility concern.		
4	RW - Receive Watchdog time expire. Active high. This field is valid only when last descriptor (RDES0<8>) is set.		
3	RE - Report on MII Error. Active high.		
2	DB - Dribbling Bit Active high. If set, and CRC error (RDES0<1>) is reset, then the packet is valid.		
1	CE - CRC Error. Active high. This field is valid only when last descriptor (RDES0<8>) is set.		
0	FIFO Overrun. Active high.		

Tab - 32 Receive Descriptor 0

5.2.2 Receive Descriptor 1 (RDES1)

FIELD	DESCRIPTION
31:11	Reserved.--Written as “0” for future compatibility concern.
10:0	RBS - Receive Data Buffer Size Indicates the size in bytes of the data buffer. If this field is 0, the AX88140A ignores this buffer. The buffer size must be a multiple of 4.

Tab - 33 Receive Descriptor 1

5.2.3 Receive Descriptor 2 (RDES2)

FIELD	DESCRIPTION
31:0	Data Buffer Pointer Indicates the physical address of data buffer. The buffer must be long-word-aligned (RDES2<1:0>=00).

Tab - 34 Receive Descriptor 2

5.2.4 Receive Descriptor 3 (RDES3)

FIELD	DESCRIPTION
31:0	Address Pointer Indicates the physical address of next descriptor. The address must be long-word aligned (RDES3<1:0>=00).

Tab - 35 Receive Descriptor 3

5.3 Transmit Descriptors

Providing one buffer, one byte-count buffer, and two address pointers in each descriptor .

Transmit Descriptor Format

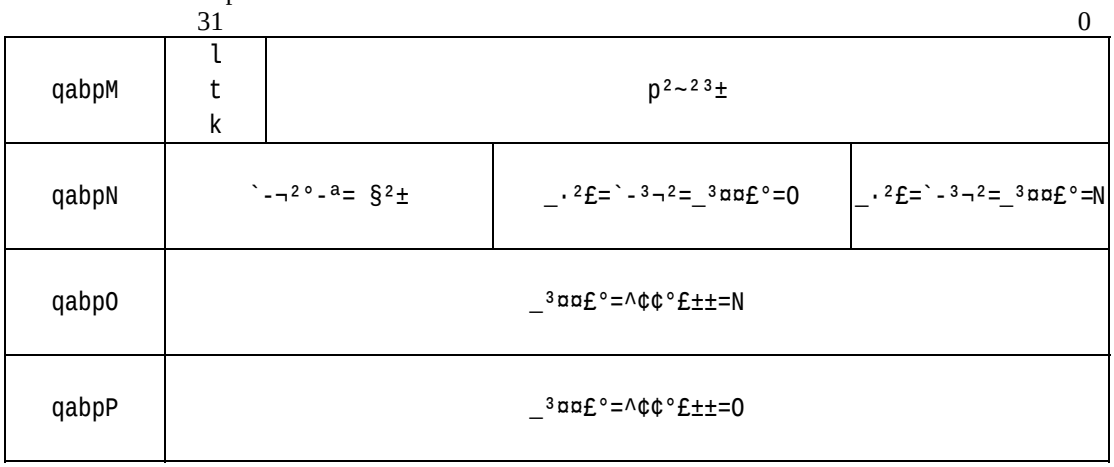


Fig - 6 Transmit Descriptor Format

5.3.1 Transmit Descriptor 0 (TDES0)

TDES0 contains transmitted frame status and descriptor ownership information.

Field	Description		
31	OWN - Own Bit	1	Indicates that the descriptor is owned by the AX88140A.
		0	Indicates that the descriptor is owned by the host.
30:16	Reserved.--Written as “0” for future compatibility concern.		
15	ES - Error Summary Indicates the logical OR of the following bits :		
	TDES0<1>	under-flow error	
	TDES0<8>	successive collisions	
	TDES0<9>	late collision	
	TDES0<10>	no carrier	
	TDES0<11>	loss of carrier	
	TDES0<14>	transmit jabber time-out	
14	TO - Transmit Jabber Time-out : Active high. The transmission process is aborted and placed in the STOPPED state. When TDES0<14> is set any heartbeat fail indication (TDES0<7>) is not valid.		
13:12	Reserved.--Written as “0” for future compatibility concern.		
11	LO - Loss of Carrier during transmission. Active high. (The status is no meaning except 10BASE SRL mode) Not valid in internal loop-back mode (REG6<11:10>=01).		
10	NC - No Carrier. Indicates that the carrier signal from the transceiver was not present during transmission. Active high. Not valid in internal loop-back mode (REG6<11:10>=01).		
9	LC - Late Collision. When set, indicates that the frame transmission was aborted due to collision occurring after the collision window of 64 bytes. Not valid if under-flow error (TDES0<1>) is set.		
8	EC - Excessive Collision When set, indicates that the transmission was aborted after 16 successive collisions while attempting to transmit the current frame.		
7	HF - Heartbeat Fail This bit is effective only in 10Mb/s operation mode. When set, indicates a heartbeat collision check failure This bit is not valid if under-flow error (TDES0<1>) is set. On the second transmission attempt, after the first transmission was aborted due to collision, the AX88140A does not check heartbeat fail and (TDES0<7>) is reset.		
6:3	CC - Collision Count This 4-bit counter indicates the number of collisions that occurred before the frame was transmitted. Not valid when the excessive collisions bit (TDES0<8>) is also set.		
2	Reserved.--Written as “0” for future compatibility concern.		

1	UF - Under-flow Error When set, indicates that the transmitter aborted the message because data arrived late from memory. Under-flow error indicates that the AX88140A encountered an empty transmit FIFO while transmitting a frame. The transmission process enters the suspended state and sets both transmit under-flow (REG5<0>) and transmit interrupt (REG5<0>).
0	DE - Deferred When set, indicates that the AX88140A had to defer while ready to transmit a frame because the carrier was asserted.

Tab - 36 Transmit Descriptor 0

5.3.2 Transmit Descriptor 1 (TDES1)

Field	Description		
31	IC - Interrupt on Completion When set, the AX88140A sets transmit interrupt (REG5<0>) after the present frames has been transmitted. It is valid only when first segment (TDES1<30>) is set.		
30	LS - Last Segment	1	Indicates that the buffer contains the last segment of a frame.
		0	Indicates that the buffer contains the first or middle segment of a frame.
29	FS - First Segment	1	Indicates that the buffer contains the first segment of a frame.
		0	Indicates that the buffer contains the middle or last segment of a frame.
28:27	Reserved.--Written as “0” for future compatibility concern.		
26	AC - Add CRC Disable When set, the AX88140A does not append the CRC to the end of the transmitted frame. This field is valid only when first segment (TDES1<29>) is set.		
25:24	Reserved.--Written as “0” for future compatibility concern.		
23	DPD - Disabled Padding The CRC field is added despite the state of the add CRC disable (TDES1<26>) flag.	1	the AX88140A does not automatically add a padding field, so a packet shorter than 64 bytes.
		0	The AX88140A automatically adds a padding field and also a CRC field to a packet shorter than 64 bytes.
22:11	Reserved.--Written as “0” for future compatibility concern.		
10:0	Data Buffer Size Indicates the size, in bytes, of the data buffer. If this field is 0, the AX88140A ignores this buffer.		

Tab - 37 Transmit Descriptor 1

5.3.3 Transmit Descriptor 2 (TDES2)

Field	Description
31:0	Data Buffer Pointer Physical address of data buffer. There are no limitations on the buffer address alignment.

Tab - 38 Transmit Descriptor 2

5.3.4 Transmit Descriptor 3 (TDES3)

Field	Description
31:0	Address Pointer Physical address of next descriptor address. There are no limitation on the buffer address alignment.

Tab - 39 Transmit Descriptor 3

6.0 Electrical Specification and Timings

6.1 Absolute Maximum Ratings

Description	SYM	Min	Max	Units
Operating Temperature	Ta	0	+70	°C
Storage Temperature	Ts	-55	+150	°C
Supply Voltage	Vcc	-0.5	+7	V
Input Voltage	Vin	Vss-0.5	Vdd+0.5	V
Output Voltage	Vout	Vss-0.5	Vdd+0.5	V
Lead Temperature (soldering 10 seconds maximum)	Tl	-55	+250	°C

Note : Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to Absolute Maximum Ratings conditions for extended period, adversely affect device life and reliability

6.2 General Operation Conditions

Description	SYM	Min	Max	Units
Operating Temperature	Ta	0	+70	°C
Supply Voltage	Vdd	+4.75	+5.25	V

6.3 DC Characteristics

(Vdd=4.75V to 5.25V, Vss=0V, Ta=0°C to 70°C)

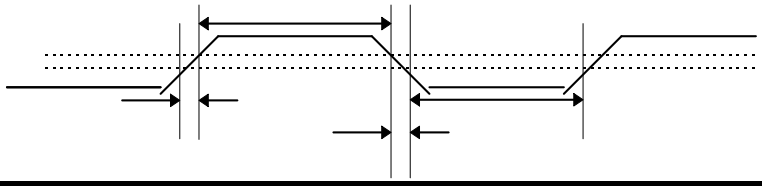
Description	SYM	Min	Max	Units
Low Input Voltage	Vil	Vss-0.5	0.8	V
High Input Voltage	Vih	2	Vdd+0.5	V
Low Output Voltage	Vol	-	0.4	V
High Output Voltage	Voh	2.4	-	V
Input Leakage Current 1 (Note 1)	Iil1	-	10	uA
Input Leakage Current 2 (Note 2)	Iil1	-	500	uA
Output Leakage Current	Iol	-	10	uA

Note :

1. All the input pins without pull low or pull high.
2. Those pins had been pull low or pull high.

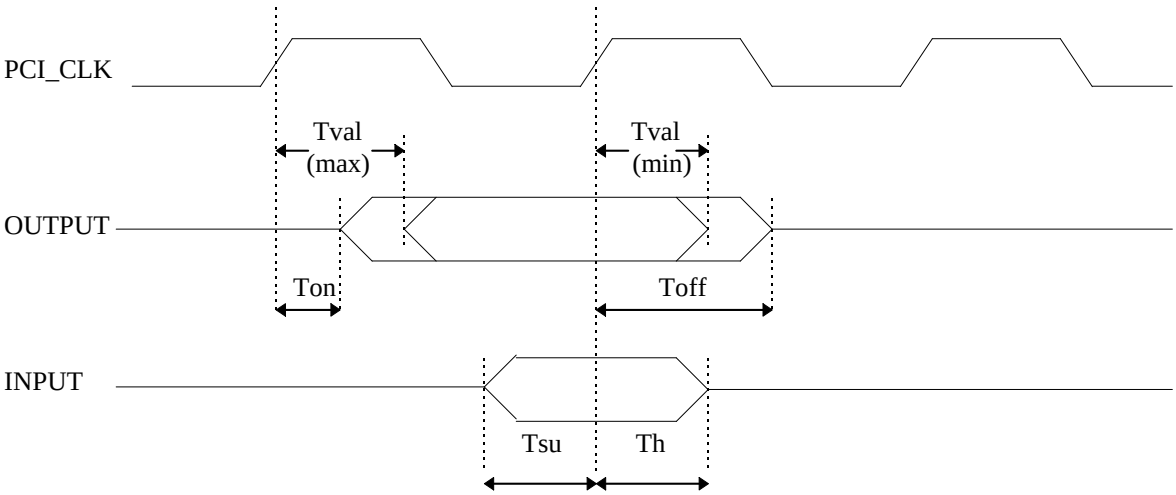
6.4 A.C. Timing Characteristics

6.4.1 PCI CLOCK



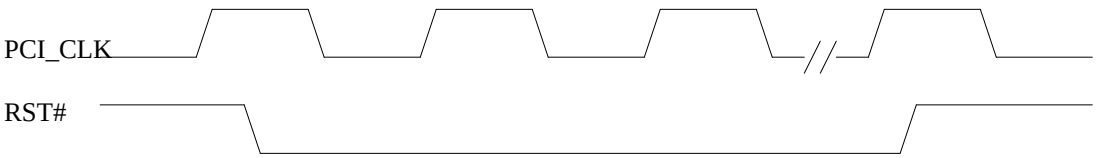
Symbol	Description	Min	Typ.	Max	Units
Tcyc	CYCLE TIME	30	-	45	ns
Thigh	PCI_CLK HIGH TIME	11	-	-	ns
Tlow	PCI_CLK LOW TIME	11	-	-	ns
Tr/Tf	PCI_CLK SLEW RATE	1	-	4	ns

6.4.2 PCI Timings



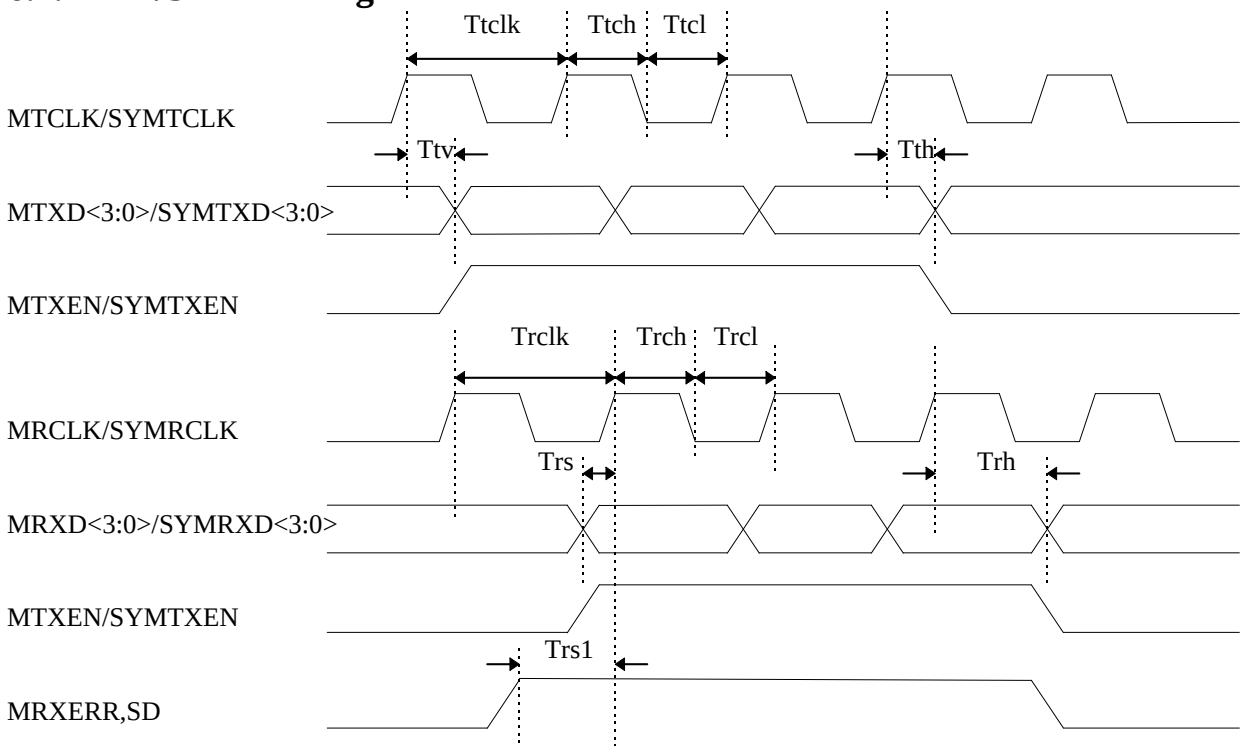
Symbol	Description	Min	Typ.	Max	Units
Tval	CLK TO SIGNAL VALID DELAY	2	-	11	ns
Ton	FLOAT TO ACTIVE DELAY	2	-	-	ns
Toff	ACTIVE TO FLOAT DELAY	-	-	28	ns
Tsu	INPUT SETUP TIME TO CLK	7	-	-	ns
Th	INPUT HOLD TIME FROM CLK	0	-	-	ns

6.4.3 Reset Timing



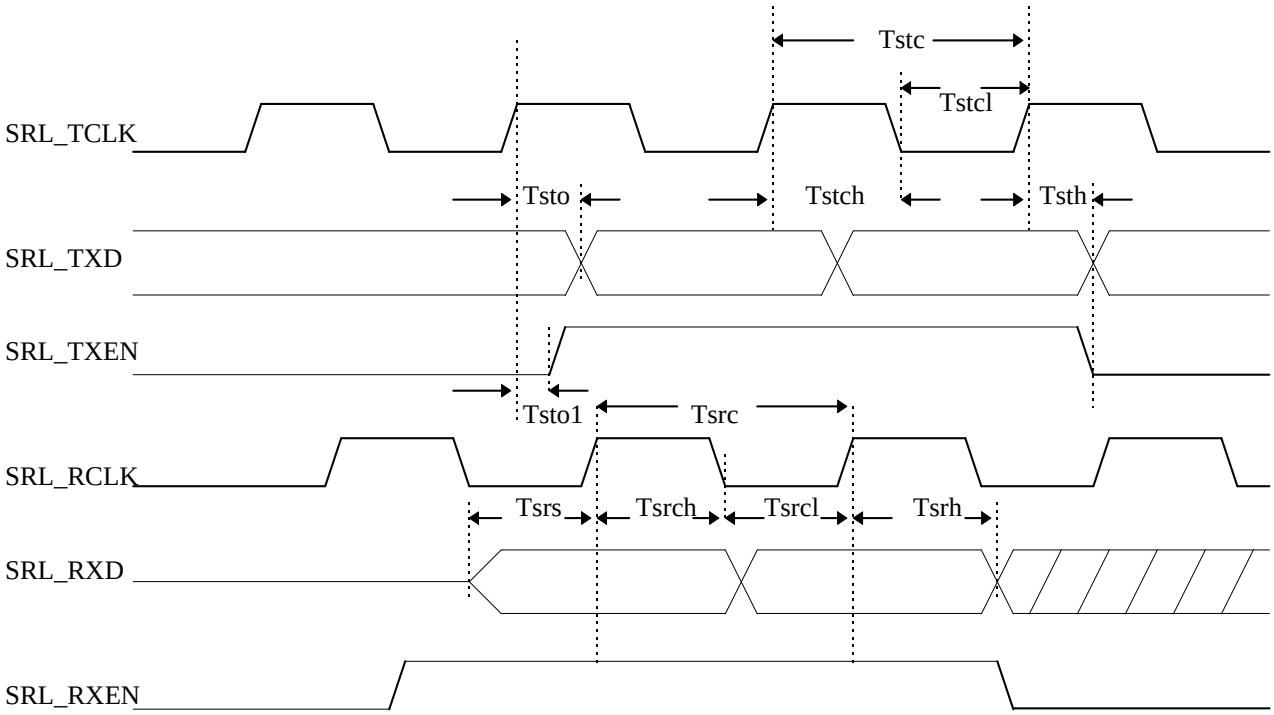
Symbol	Description	Min	Typ.	Max	Units
Trst	Reset pulse width	10	-	-	PCI Clk

6.4.4 MII/SYM Timing



Symbol	Description	Min	Typ.	Max	Units
Ttclk	Cycle time(100Mbps)	-	40	-	ns
Ttclk	Cycle time(10Mbps)	-	400	-	ns
Ttch	high time(100Mbps)	14	-	26	ns
Ttch	high time(10Mbps)	140	-	260	ns
Trch	low time(100Mbps)	14	-	26	ns
Trch	low time(10Mbps)	140	-	260	ns
Ttv	Clock to data valid	-	-	20	ns
Tth	Data output hold time	5	-	-	ns
Trclk	Cycle time(100Mbps)	-	40	-	ns
Trclk	Cycle time(10Mbps)	-	400	-	ns
Trch	high time(100Mbps)	14	-	26	ns
Trch	high time(10Mbps)	140	-	260	ns
Trcl	low time(100Mbps)	14	-	26	ns
Trcl	low time(10Mbps)	140	-	260	ns
Trs	data setup time	6	-	-	ns
Trh	data hold time	10	-	-	ns
Trs1	SD, MRXERR data setup time	10	-	-	ns

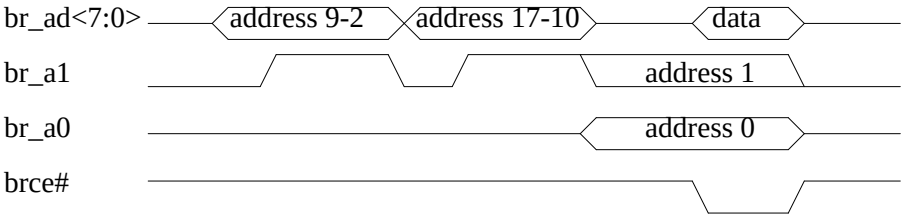
6.4.5 10Mbps serial timing



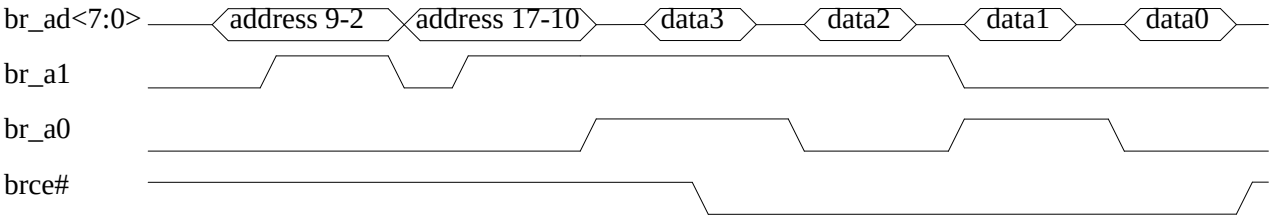
Symbol	Description	Min	Typ.	Max	Units
Tstc	SRL_TCLK Cycle time	85	-	118	ns
Tstch	Clock high time	45	-	55	ns
Tstcl	Clock low time	45	-	55	ns
Tsto	Data output delay	-	-	26	ns
Tsto1	SRL_TXEN data output delay	-	-	26	ns
Tsth	Data output hold time	5	-	-	ns
Tsrc	SRL_RCLK Cycle time	85	-	118	ns
Tsrch	Clock high time	45	-	55	ns
Tsrcl	Clock low time	45	-	55	ns
Tsrs	Data input Setup time	10	-	-	ns
Tsrh	Data input hold time	5	-	-	ns

6.4.6 Boot ROM Read Cycles

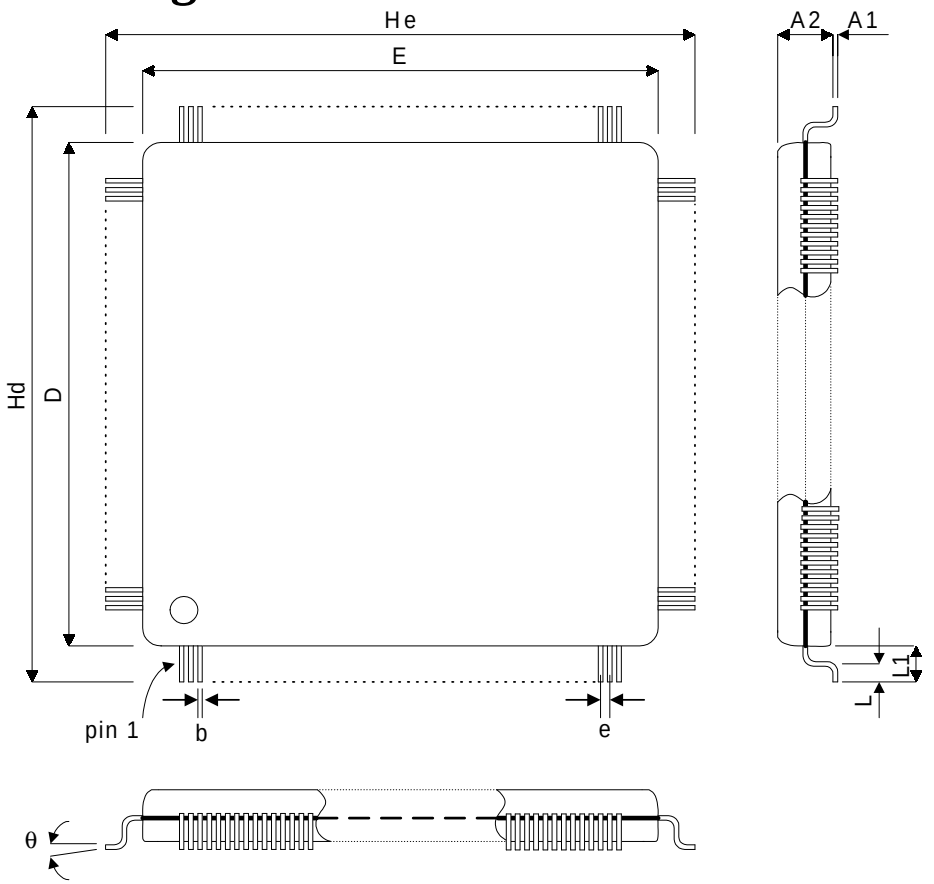
Boot ROM Byte Read Cycle



Boot ROM Dword Read Cycle



7.0 Package Information

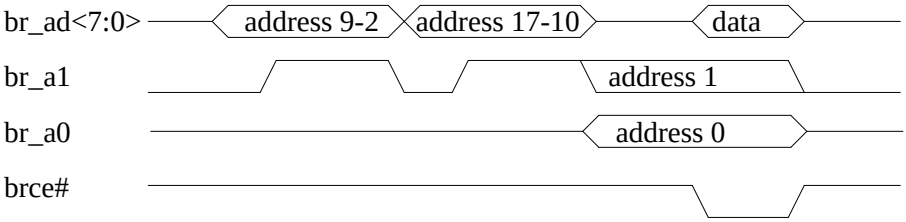


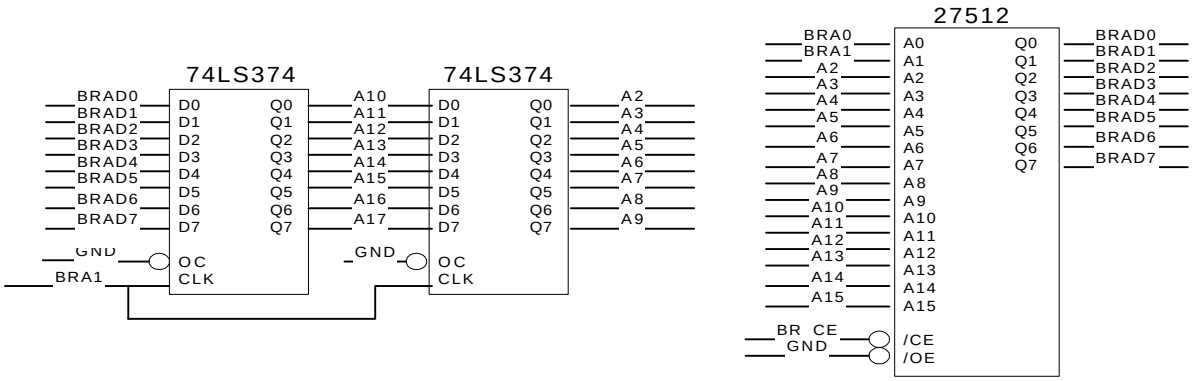
SYMBOL	MILIMETER		
	MIN.	NOM	MAX
A1	0.05	0.25	0.5
A2	3.17	3.32	3.47
b	0.20	0.30	0.40
D	27.90	28.00	28.10
E	27.90	28.00	28.10
e		0.65	
Hd	30.95	31.20	31.45
He	30.95	31.20	31.45
L	0.65	0.80	0.95
L1		1.60	
θ	0		10

APPENDIX A H/W NOTE

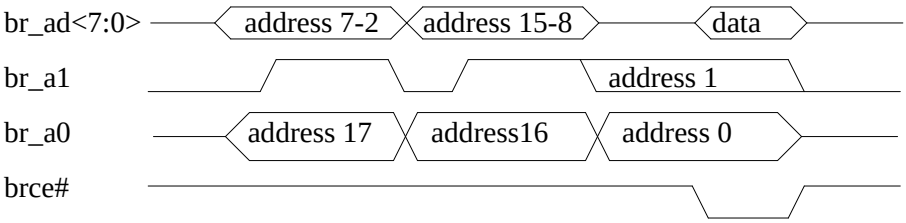
A.1 Boot ROM read cycle

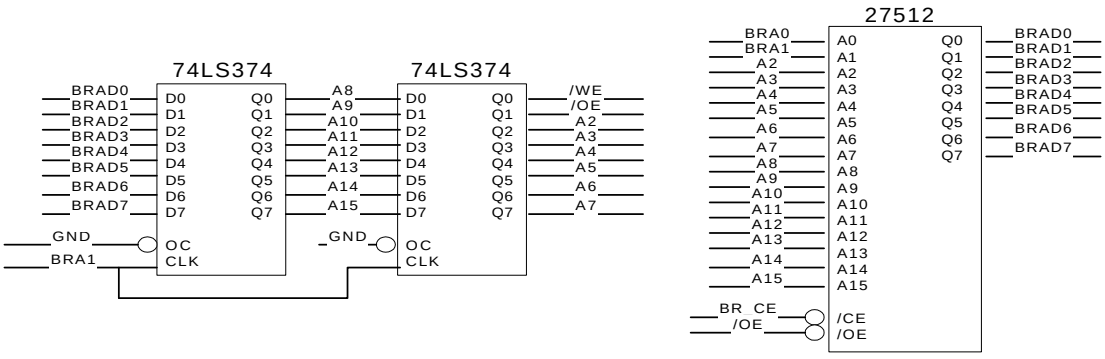
ASIX 88140 Boot ROM Byte Read Cycle





DEC 21140 Boot ROM Byte Read Cycle:





A.2 Power Supply

AX88140A power supply is +5V DC
DEC 21140 power supply is +3.3V DC

A.3 Boundary Scan Test Pins

AX88140A do not support boundary scan test pins
DEC 21140 supports boundary scan test pins

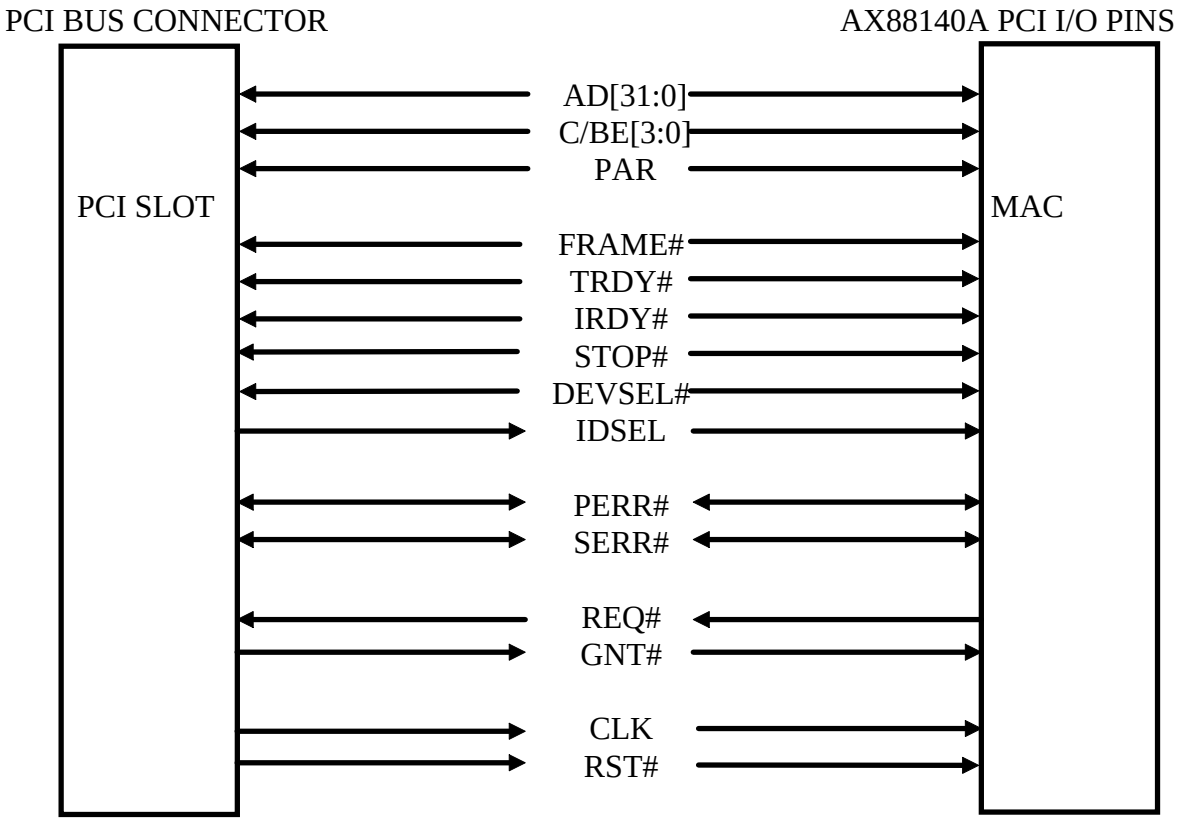
APPENDIX B Function Application

B.1 Application for PCI Interface

Features :

- l Direct interface to PCI Bus.
- l Support 33 MHz no wait state PCI Bus Interface.
- l Powerful on chip buffer management DMA. And PCI Bus master operation reduce CPU utilization.
- l 5 Volt CMOS process.

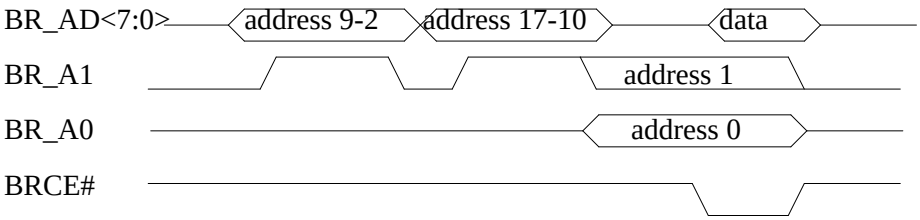
PCI Interface Schematic:

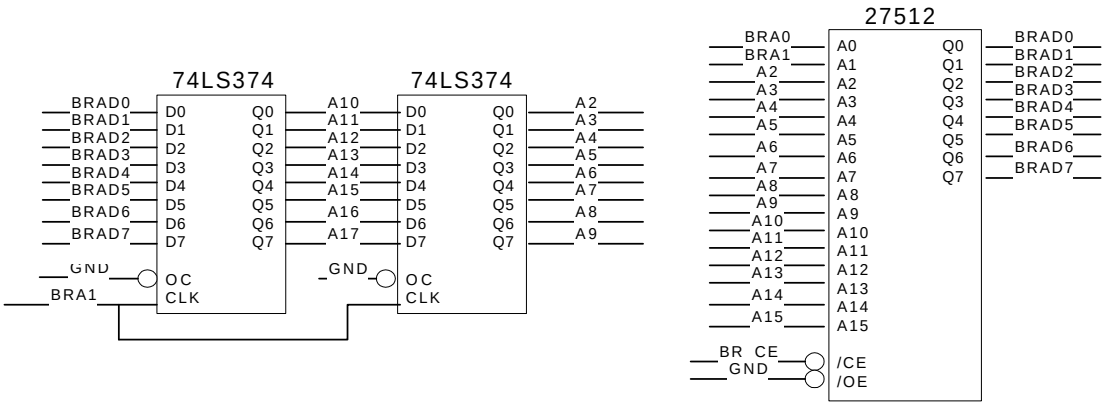


The pull high resisters are required for pin REQ#, GNT#, PERR#, and SERR# on MAC for more detail please to check the schematic.

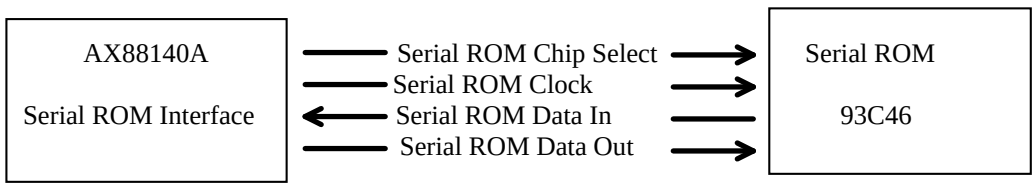
B.2 Application for Boot ROM Interface

AX88140A
Boot ROM Byte Read Cycle





B.3 Application for Serial ROM Interface



B.4 Application for PHY Interface

B.4.1 AX88140A, QSI6611, & MTD213 Application

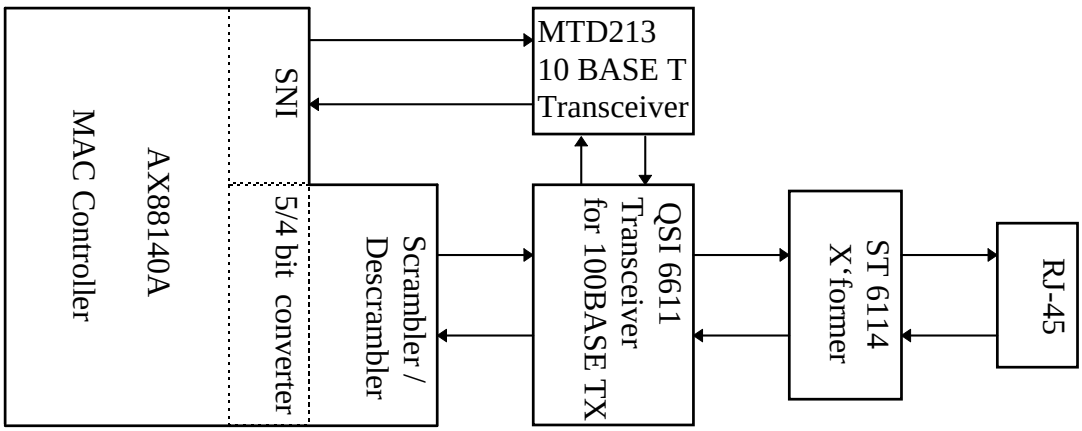


Fig - 7 Application for PCS / Serial Mode

B.4.2 Application for MII Mode : LEVEL ONE LXT970

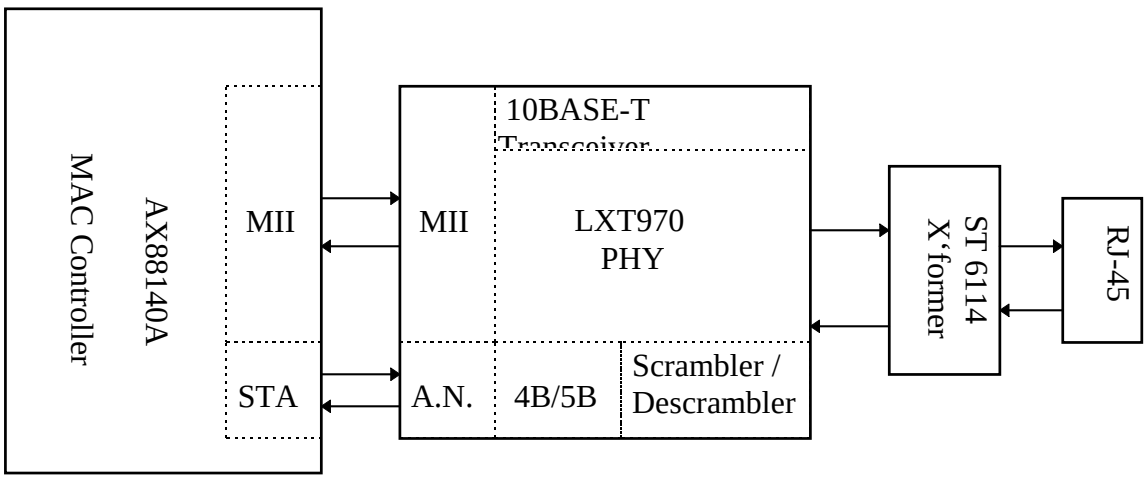


Fig - 8 Application for MII Mode with LXT970

B.4.3 Application for MII Mode : MYSON MTD972 + MTD971

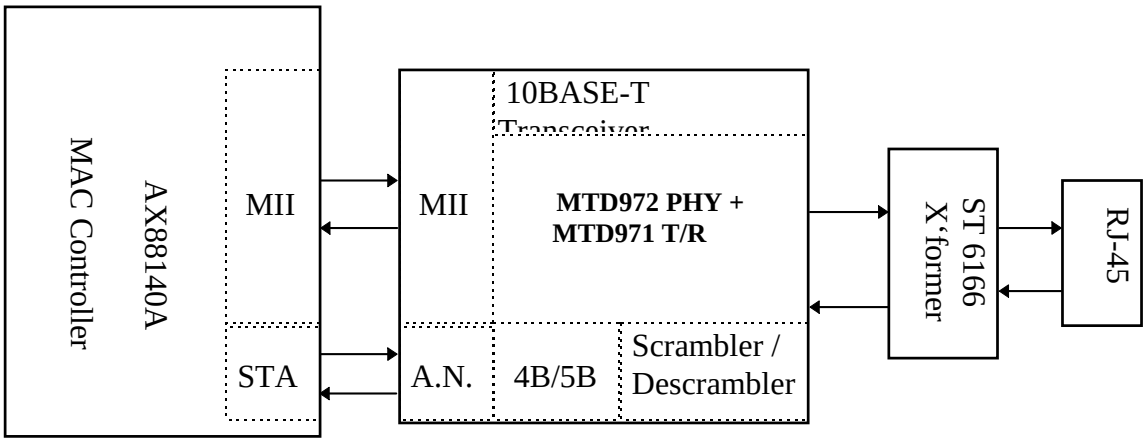


Fig - 9 Application for MII Mode with MTD972 +MTD971

B.4.4 Application for MII Mode : DAVICOM DM9101

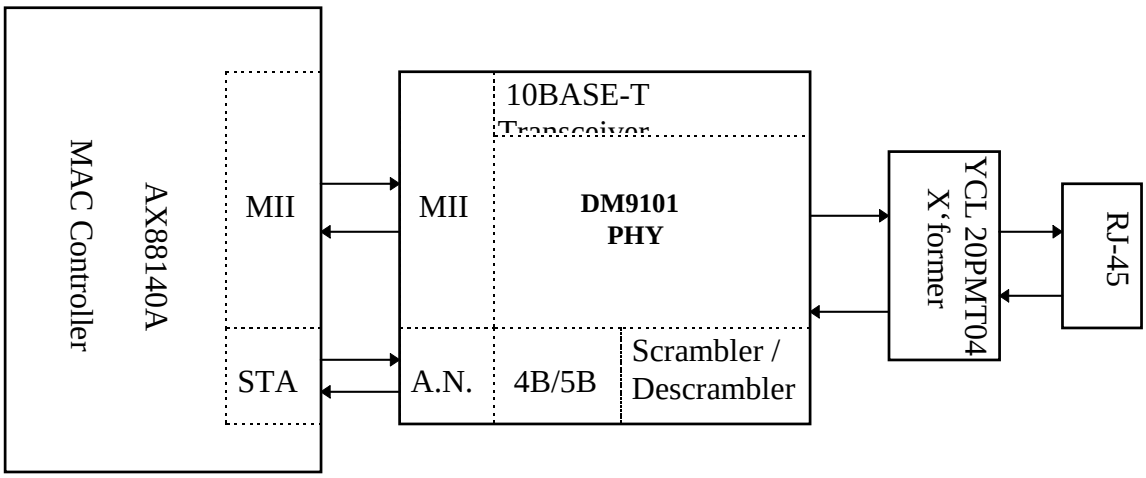


Fig - 10 Application for MII Mode with DM9101