

High Performance Current Mode PWM Controllers

PL384XBQ8

Description

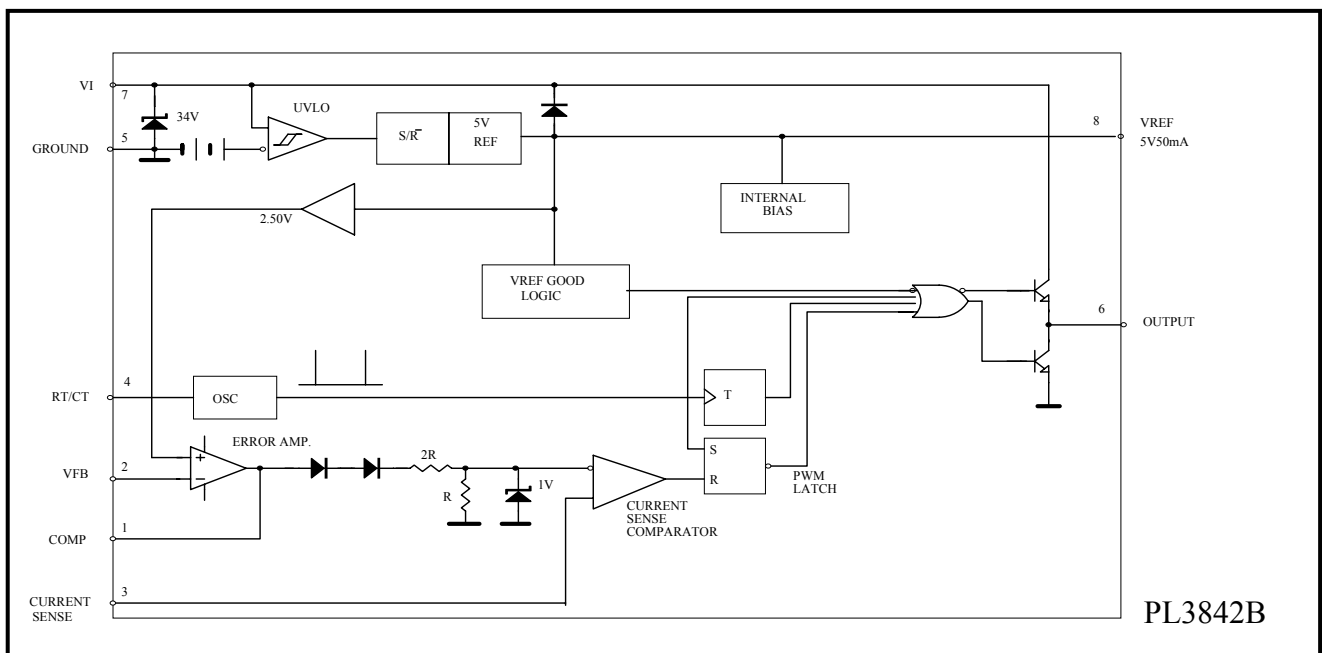
The PL384XBQ8 family of control ICs provides the necessary features to implement off-line or DC to DC fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include a trimmed oscillator for precise duty cycle control, under voltage lockout featuring start-up current less than 0.5mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N-channel MOSFETs, is low in the off-state.

Differences between members of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The PL3842B and PL3844B have UVLO thresholds of 16V (on) and 10V (off), ideally suited off-line applications. The corresponding thresholds for the PL3843B and PL3845B are 8.5V and 7.9V. The PL3842B and PL3843B can operate to duty cycles approaching 100%. A range of the zero to <50% is obtained by the PL3844B and PL3845B by the addition of an internal toggle flip flop which blanks the output off every other clock cycle.

Features

- Trimmed oscillator for precise frequency control
- Oscillator frequency guaranteed at 250 kHz
- Current mode operation to 500kHz
- Automatic feed forward compensation
- Latching PWM for cycle-by-cycle current limiting
- Internally trimmed reference with undervoltage lockout
- High current totem pole output
- Undervoltage lockout with hysteresis
- Low start-up and operating current

Block Diagram(toggle flip flop used only in PL3844B and PL3845B)

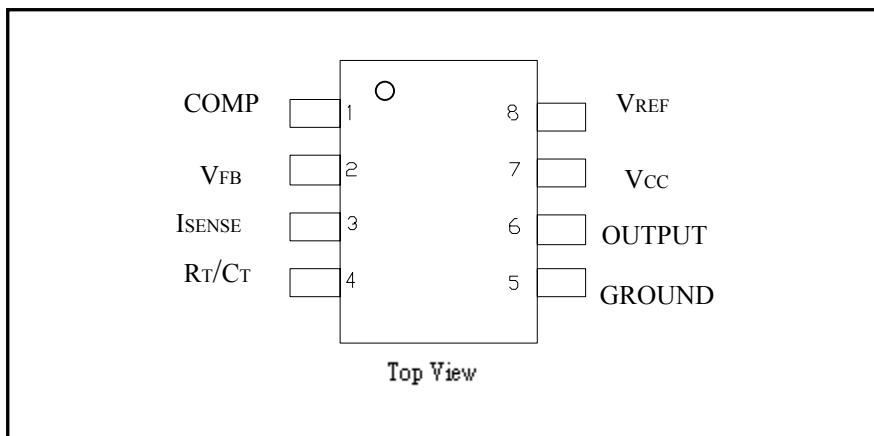


Absolute Maximum Ratings

| Symbol | Parameter | Value | Unit |
|-----------|--|---------------|------------------|
| V_I | Supply Voltage (low impedance source) | 30 | V |
| V_I | Supply Voltage ($I_i < 30\text{mA}$) | Self Limiting | |
| I_o | Output Current | ± 1 | A |
| E_o | Output Energy (capacitive load) | 5 | μJ |
| | Analog Inputs (pins 2, 3) | -0.3 to 5.5 | V |
| | Error Amplifier Output Sink Current | 10 | mA |
| P_{tot} | Power Dissipation at $T_{amb} \leq 25^\circ\text{C}$ | 800 | mW |
| T_{stg} | Storage Temperature Range | -65 to +150 | $^\circ\text{C}$ |
| T_J | Junction Operating Temperature | -40 to +150 | $^\circ\text{C}$ |
| T_L | Lead Temperature (soldering 10s) | 300 | $^\circ\text{C}$ |

Note : All voltages are with respect to pin 5, all currents are positive into the specified terminal.

Pin Connection (top view)



Pin Functions

| No | Function | Description |
|----|-------------|---|
| 1 | COMP | This pin is the Error Amplifier output and is made available for loop compensation. |
| 2 | V_{FB} | This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider. |
| 3 | I_{SENSE} | A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction. |
| 4 | R_T/C_T | The oscillator frequency and maximum output duty cycle are programmed by connecting resistor R_T to V_{REF} and capacitor C_T to ground. Operation to 500kHz is possible. |
| 5 | GROUND | This pin is the combined control circuitry and power ground. |
| 6 | OUTPUT | This output directly drives the gate of a power MOSFET. Peak currents up to 1A are sourced and sunk by this pin. |
| 7 | V_{CC} | This pin is the positive supply of the control IC. |
| 8 | V_{REF} | This is the reference output. It provides charging current for capacitor C_T through resistor R_T . |

Thermal Data

| Symbol | Description | Value | Unit |
|-----------------|---|-------|---------------------------|
| $R_{th, j-amb}$ | Thermal Resistance, junction to ambient | 150 | $^\circ\text{C}/\text{W}$ |



Electrical Characteristics ([note 1] Unless otherwise stated, these specifications apply for $0 \leq T_{amb} \leq 70^\circ C, V_i = 15V$ (note 5), $R_T = 10k, C_T = 3.3nF$)

| Parameter | Test Conditions | Symbol | Min. | Typ. | Max. | Unit |
|--------------------------------------|---|-----------------------------|------|------|------|----------------|
| <i>Reference Section</i> | | | | | | |
| Output Voltage | $T_j = 25^\circ C, I_o = 1mA$ | V_{REF} | 4.9 | 5.0 | 5.1 | V |
| Line Regulation | $12V \leq V_i \leq 25V$ | ΔV_{REF} | - | 2 | 20 | mV |
| Load Regulation | $1mA \leq I_o \leq 20mA$ | ΔV_{REF} | - | 3 | 25 | mV |
| Temperature Stability | (Note 2) | $\Delta V_{REF} / \Delta T$ | - | 0.2 | - | mV/ $^\circ C$ |
| Total Output Variation | Line, Load, Temperature | | 4.82 | - | 5.18 | V |
| Output Noise Voltage | $10Hz \leq f \leq 10kHz, T_j = 25^\circ C$ (note 2) | e_N | - | 50 | - | μV |
| Long Term Stability | $T_{amb} = 125^\circ C, 1000$ Hrs (note 2) | | - | 5 | 25 | mV |
| Output Short Circuit | | I_{SC} | -30 | -100 | -180 | mA |
| <i>Oscillator Section</i> | | | | | | |
| Frequency | $T_j = 25^\circ C$ | f_{osc} | 49 | 52 | 55 | kHz |
| | $T_A = 0$ to $70^\circ C$ | | 48 | - | 56 | kHz |
| | $T_j = 25^\circ C$ ($R_T = 6.2k, C_T = 1nF$) | | 225- | 250 | 275 | kHz |
| Frequency Change with Volt | $V_{CC} = 12V$ to $25V$ | $\Delta f_{osc} / \Delta V$ | - | 0.2 | 1.0 | % |
| Frequency Change with Temp | $T_A = 0$ to $70^\circ C$ | $\Delta f_{osc} / \Delta T$ | - | 0.5 | 1.0 | % |
| Oscillator Voltage Swing | Peak to peak | V_{osc} | - | 1.6 | - | V |
| Discharge Current ($V_{osc} = 2V$) | $T_j = 25^\circ C$ | I_{dischg} | 7.8 | 8.3 | 8.8 | mA |
| | $T_A = 0$ to $70^\circ C$ | | 7.6 | - | 8.8 | mA |
| <i>Error Amp Section</i> | | | | | | |
| Input Voltage | $V_{PIN1} = 2.5V$ | V_2 | 2.42 | 2.50 | 2.58 | V |
| Input Bias Current | $V_{FB} = 5V$ | I_b | - | -0.1 | -2 | μA |
| A_{VOL} | $2V \leq V_o \leq 4V$ | | 65 | 90 | - | dB |
| Unity Gain Bandwidth | $T_j = 25^\circ C$ | BW | 0.7 | 1 | - | MHz |
| Power Supply Rejec. Ratio | $V_i = 12V$ to $25V$ | PSRR | 60 | 70 | - | dB |
| Output Sink Current | $V_{PIN2} = 2.7V, V_{PIN1} = 1.1V$ | I_o | 2 | 12 | - | mA |
| Output Source Current | $V_{PIN2} = 2.3V, V_{PIN1} = 5V$ | I_o | -0.5 | -1 | - | mA |
| V_{OUT} High | $V_{PIN2} = 2.3V, R_L = 15k\Omega$ to ground | | 5 | 6.2 | - | V |
| V_{OUT} Low | $V_{PIN2} = 2.7V, R_L = 15k\Omega$ to Pin 8 | | - | 0.8 | 1.1 | V |
| <i>Current Sense Section</i> | | | | | | |
| Gain | (note 3 & 4) | G_v | 2.85 | 3 | 3.15 | V/V |
| Maximum Input Signal | $V_{PIN1} = 5V$ (note 3) | V_3 | 0.9 | 1 | 1.1 | V |
| Supply Voltage Rejection | $12V \leq V_i \leq 25V$ | SVR | - | 70 | - | dB |
| Input Bias Current | | I_b | - | -2 | -10 | μA |
| Delay to Output | | | - | 150 | 300 | ns |
| <i>Output Section</i> | | | | | | |
| Output Low Level | $I_{SINK} = 20mA$ | V_{OL} | - | 0.1 | 0.4 | V |
| | $I_{SINK} = 200mA$ | | - | 1.6 | 2.2 | V |
| Output High Level | $I_{SOURCE} = 20mA$ | V_{OH} | 13 | 13.5 | - | V |
| | $I_{SOURCE} = 200mA$ | | 12 | 13.5 | - | V |
| UVLO Saturation | $V_{CC} = 6V, I_{SINK} = 1mA$ | V_{OLS} | - | 0.1 | 1.1 | V |
| Rise Time | $T_j = 25^\circ C, C_L = 1nF$ (note 2) | t_r | - | 50 | 150 | ns |
| Fall Time | $T_j = 25^\circ C, C_L = 1nF$ (note 2) | t_f | - | 50 | 150 | ns |

**Electrical Characteristics** (continued)

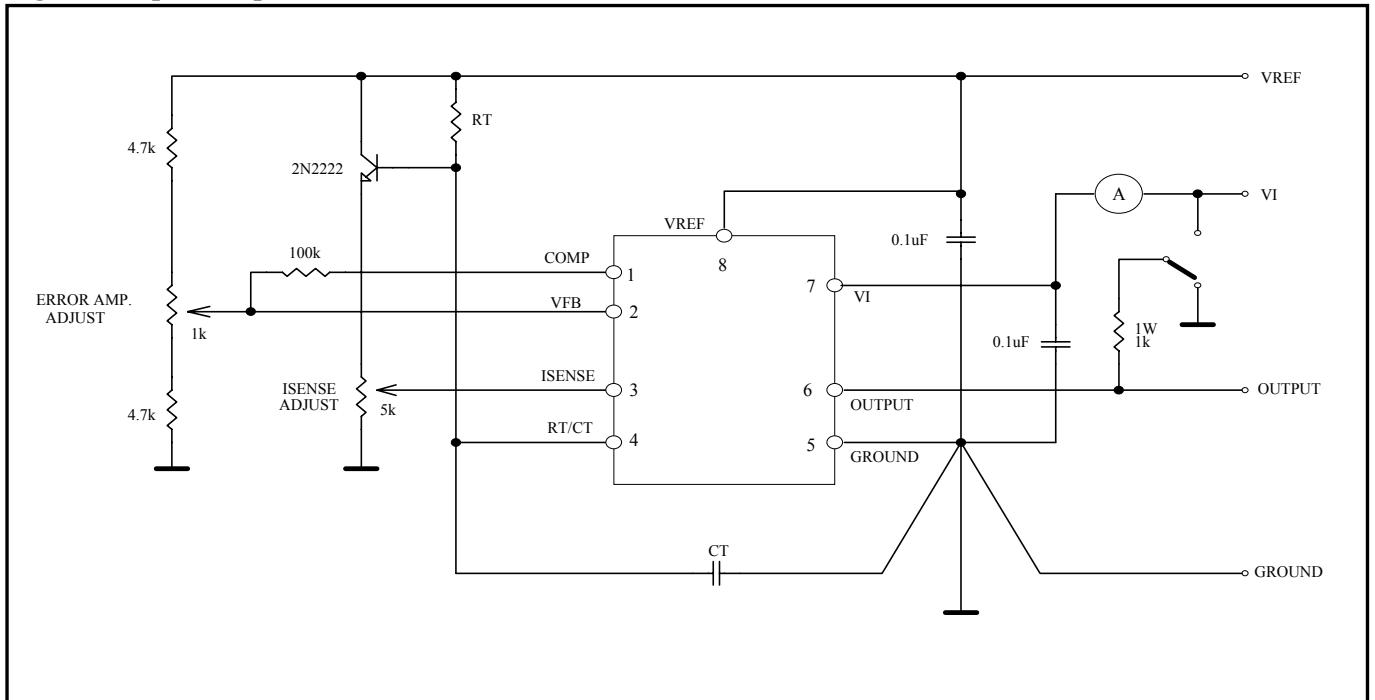
| Parameter | Test Conditions | Symbol | Min. | Typ. | Max. | Unit |
|--|--|-----------------|------|------|------|------|
| <i>Undervoltage Lockout Section</i> | | | | | | |
| Start Threshold | PL3842B/PL3844B | | 14.5 | 16 | 17.5 | V |
| | PL3843B/PL3845B | | 7.8 | 8.4 | 9.0 | V |
| Min Operating Voltage After Turn-on | PL3842B/PL3844B | | 8.5 | 10 | 11.5 | V |
| | PL3843B/PL3845B | | 7.0 | 7.6 | 8.2 | |
| <i>PWM Section</i> | | | | | | |
| Maximum Duty Cycle | PL3842B/PL3843B | | 94 | 96 | 100 | % |
| | PL3844B/PL3845B | | 47 | 48 | 50 | % |
| Minimum Duty Cycle | | | - | - | 0 | % |
| <i>Total Standby Current</i> | | | | | | |
| Start-up Current | V _I =6.5V for PL3843B/45B | I _{st} | - | 0.3 | 0.5 | mA |
| | V _I =14V for PL3842B/44B | | - | 0.3 | 0.5 | mA |
| Operating Supply Current | V _{PIN 2} = V _{PIN 3} = 0V | I _I | - | 12 | 17 | mA |
| Zener Voltage | I _I = 25 mA | V _{Iz} | 30 | 36 | - | V |

- Notes: 1. Max. package power dissipation limits must be respected; low duty cycle pulse techniques are used during test maintain T_j as close to T_{amb} as possible.
2. These parameters, although guaranteed, are not 100% tested in production.
3. Parameter measured at trip point of latch with V_{PIN 2} = 0 .
4. Gain defined as:

$$A = \frac{\Delta V_{PIN 1}}{\Delta V_{PIN 3}}, \quad 0 \leq V_{PIN 3} \leq 0.8V$$

5. Adjust V_I above the start threshold before setting at 15V.

Figure 1: Open Loop Test Circuit



High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground. The transistor and 5kΩ potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

Figure 2: Timing Resistor vs Oscillator Frequency

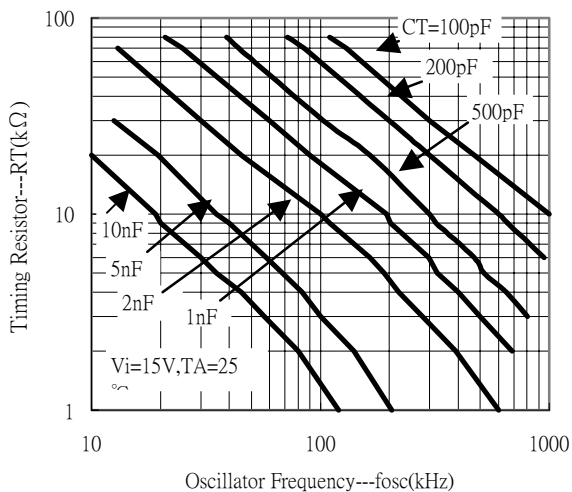


Figure 3: Output Dead-Time vs Oscillator Frequency

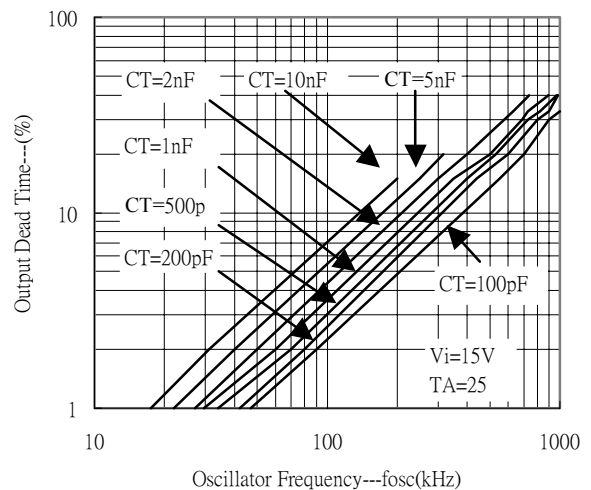


Figure 4: Oscillator Discharge Current vs Temperature

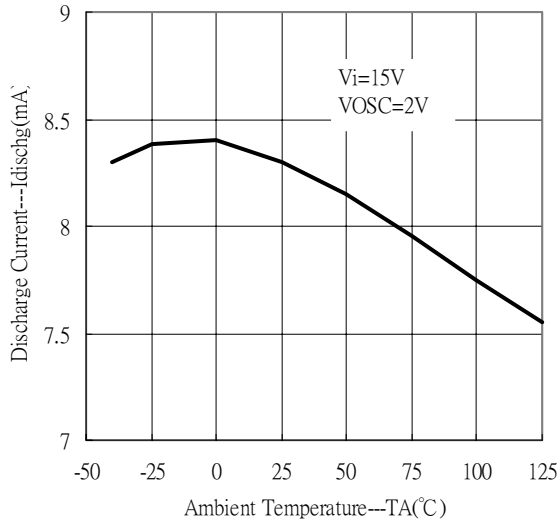


Figure 5: Maximum Output Duty Cycle vs Timing Resistor

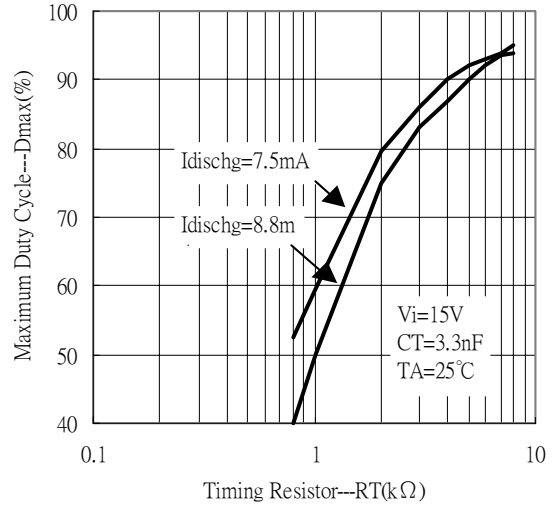


Figure 6: Error Amp Open-Loop Gain vs Frequency

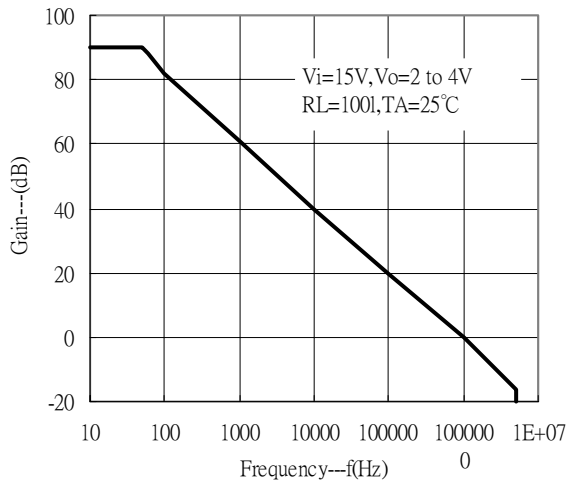


Figure 7: Error Amp Phase vs Frequency

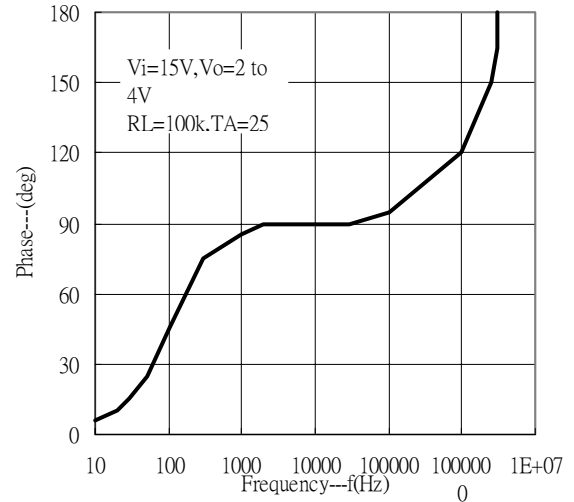


Figure 8: Current Sense Input Threshold vs Error Amp Output Voltage

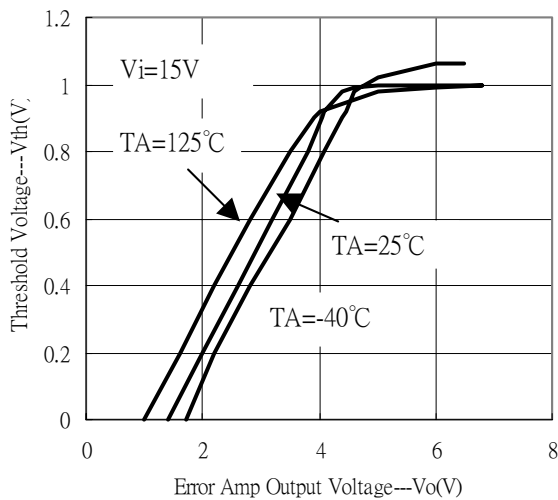


Figure 9: Reference Short Circuit Current vs Temperature

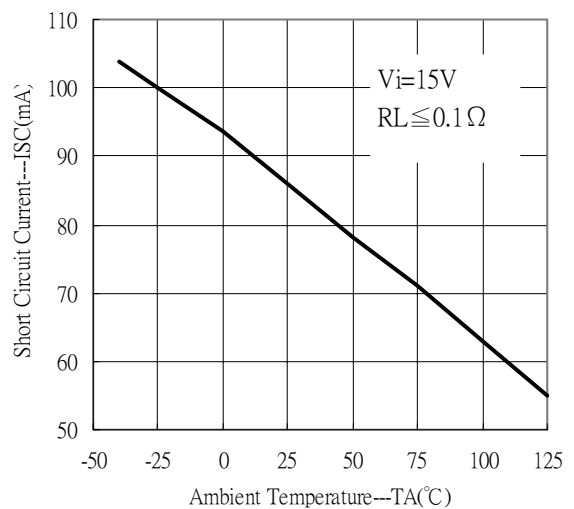


Figure 10. Oscillator and Output Waveforms

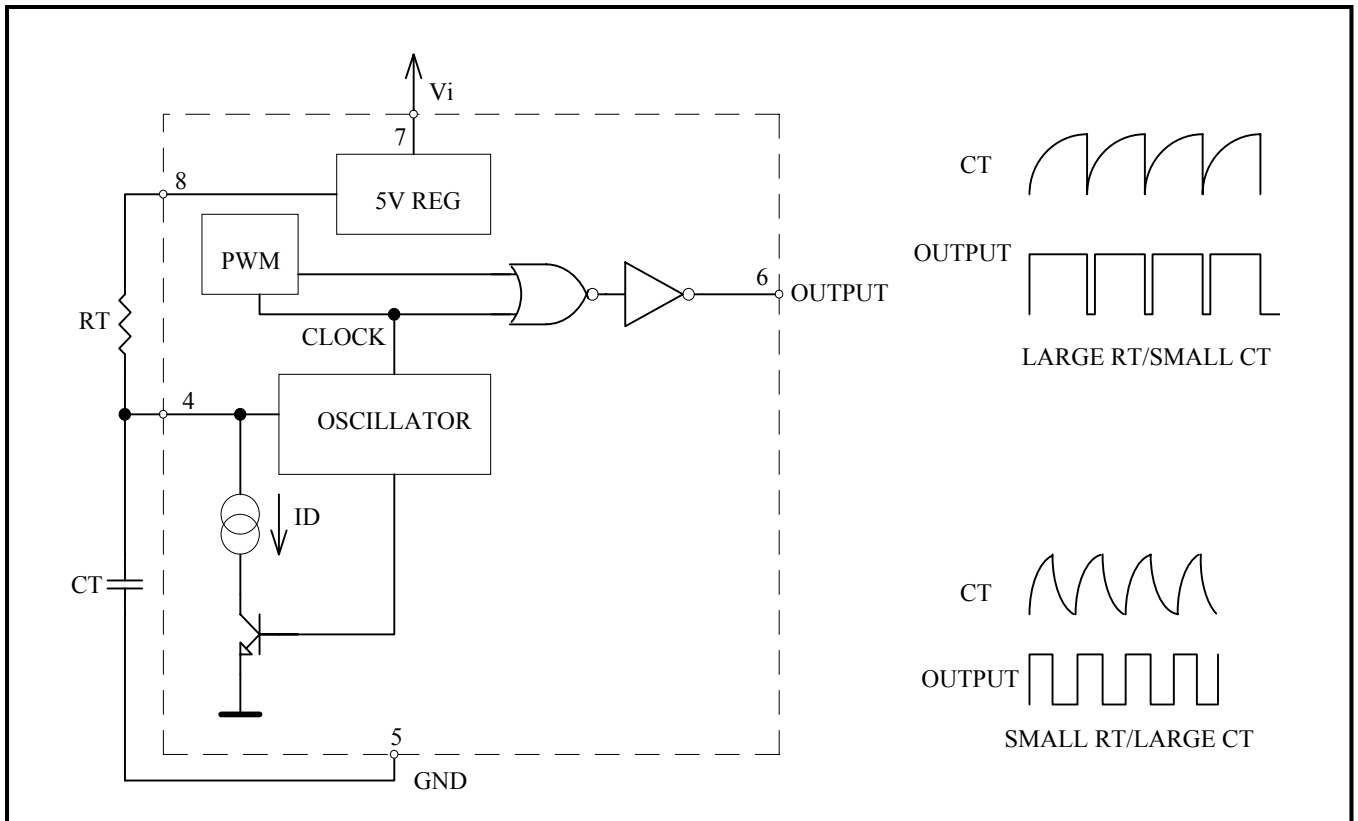


Figure 11: Error Amp Configuration

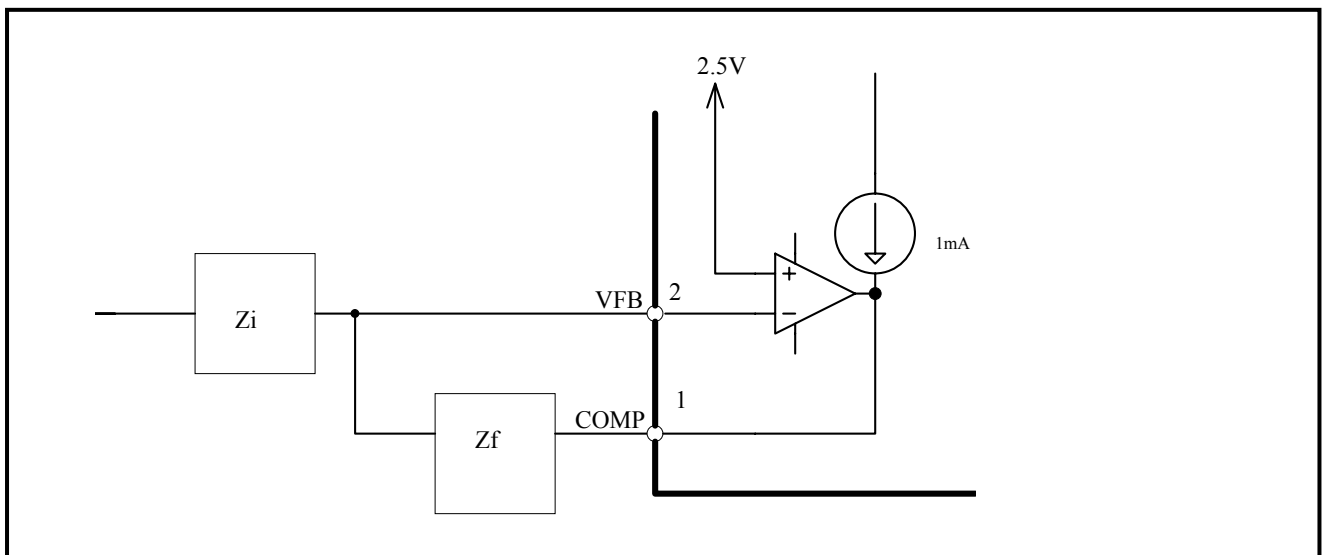


Figure 12: Under Voltage Lockout

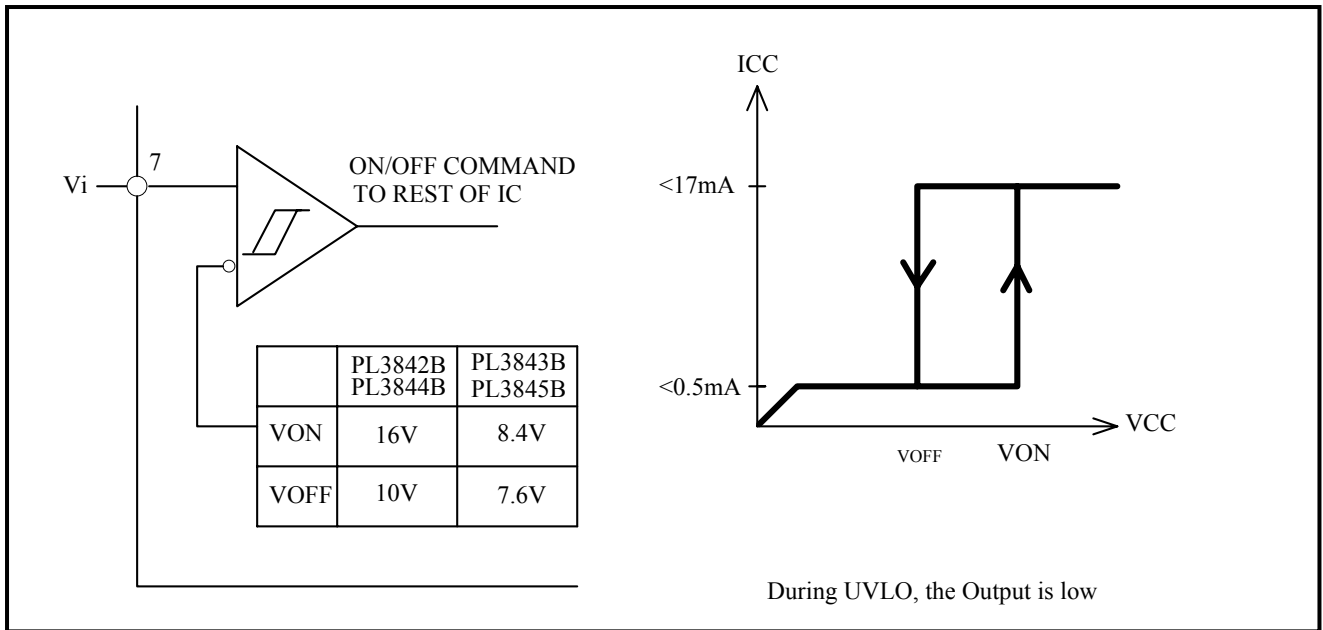


Figure 13: Current Sense Circuit

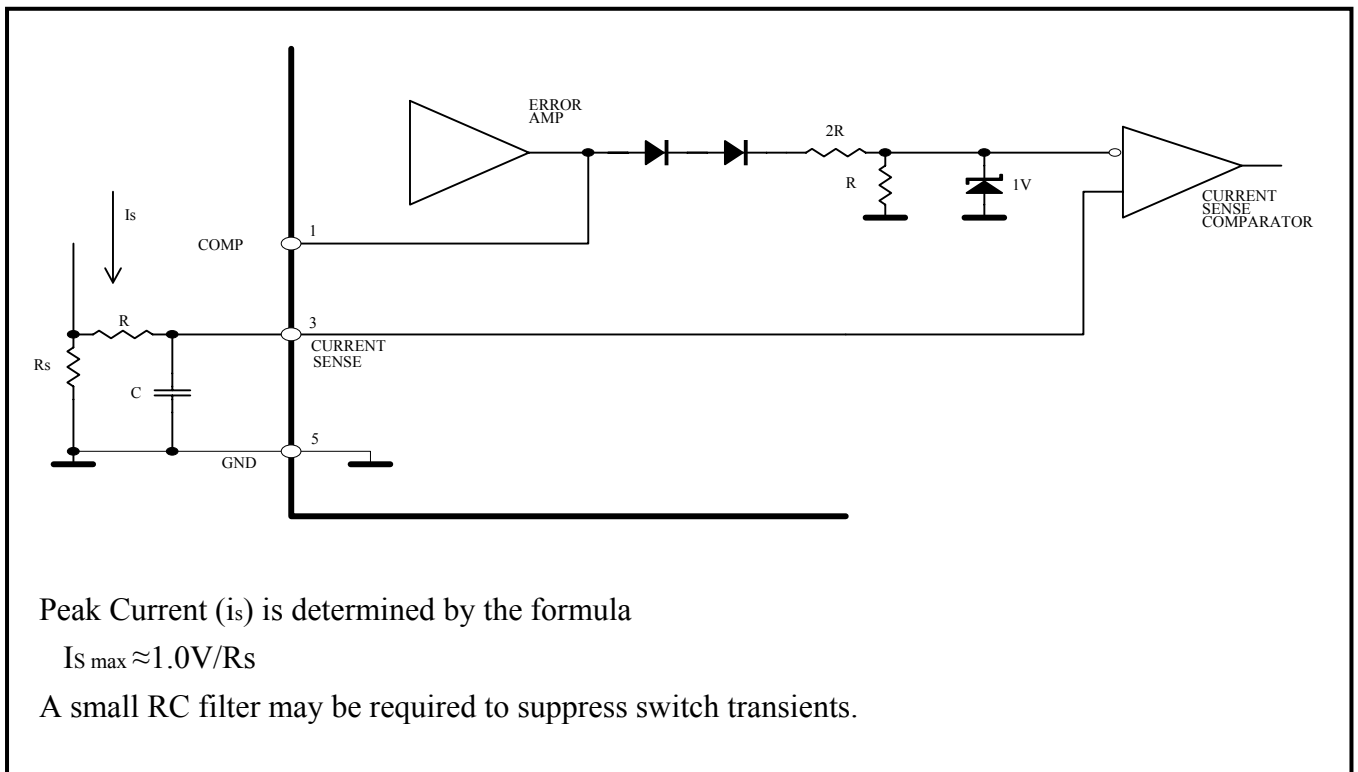


Figure 14: Slope Compensation Techniques.

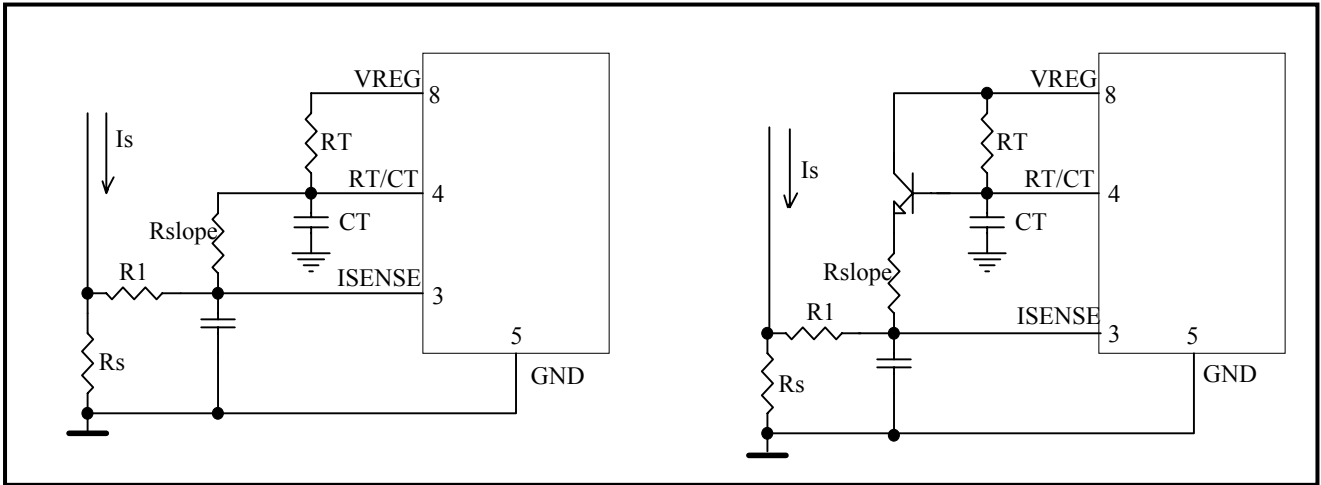


Figure 15: Isolated MOSFET Drive and Current Transformer Sensing

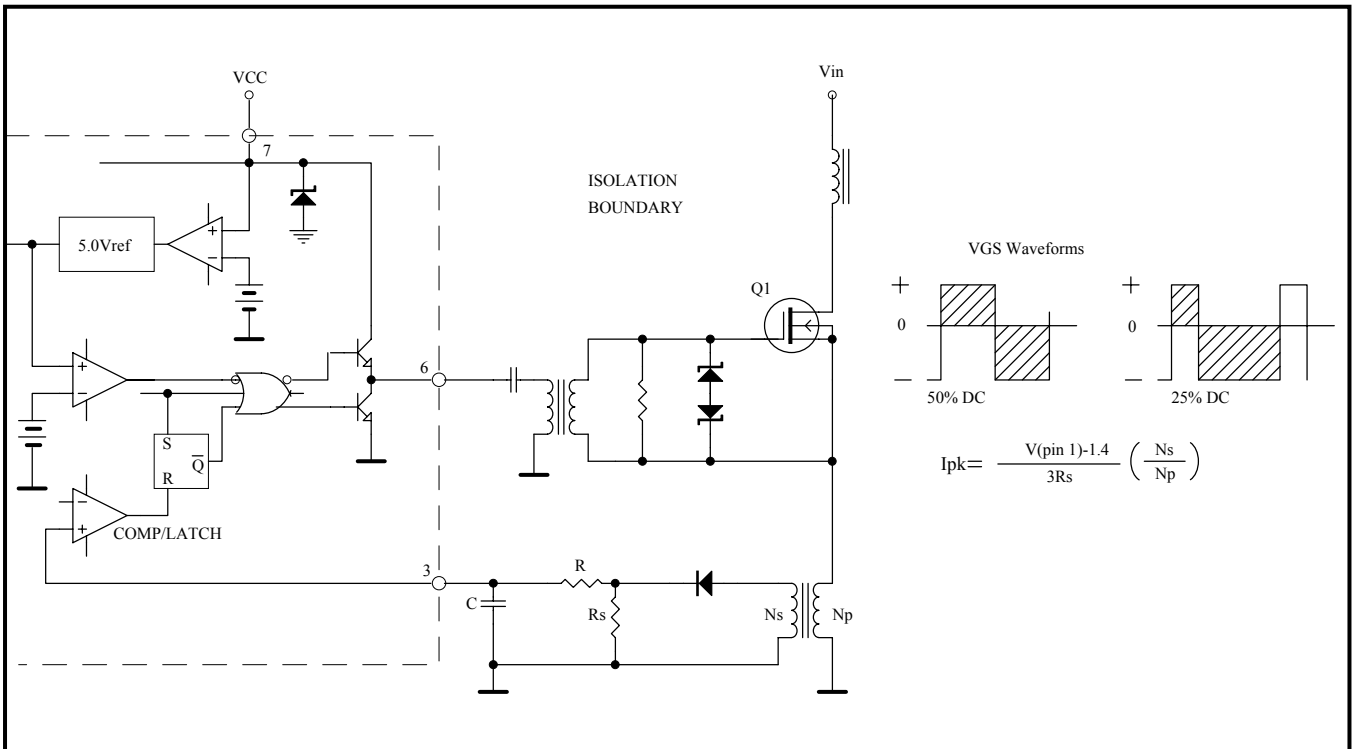


Figure 16:Latched Shutdown

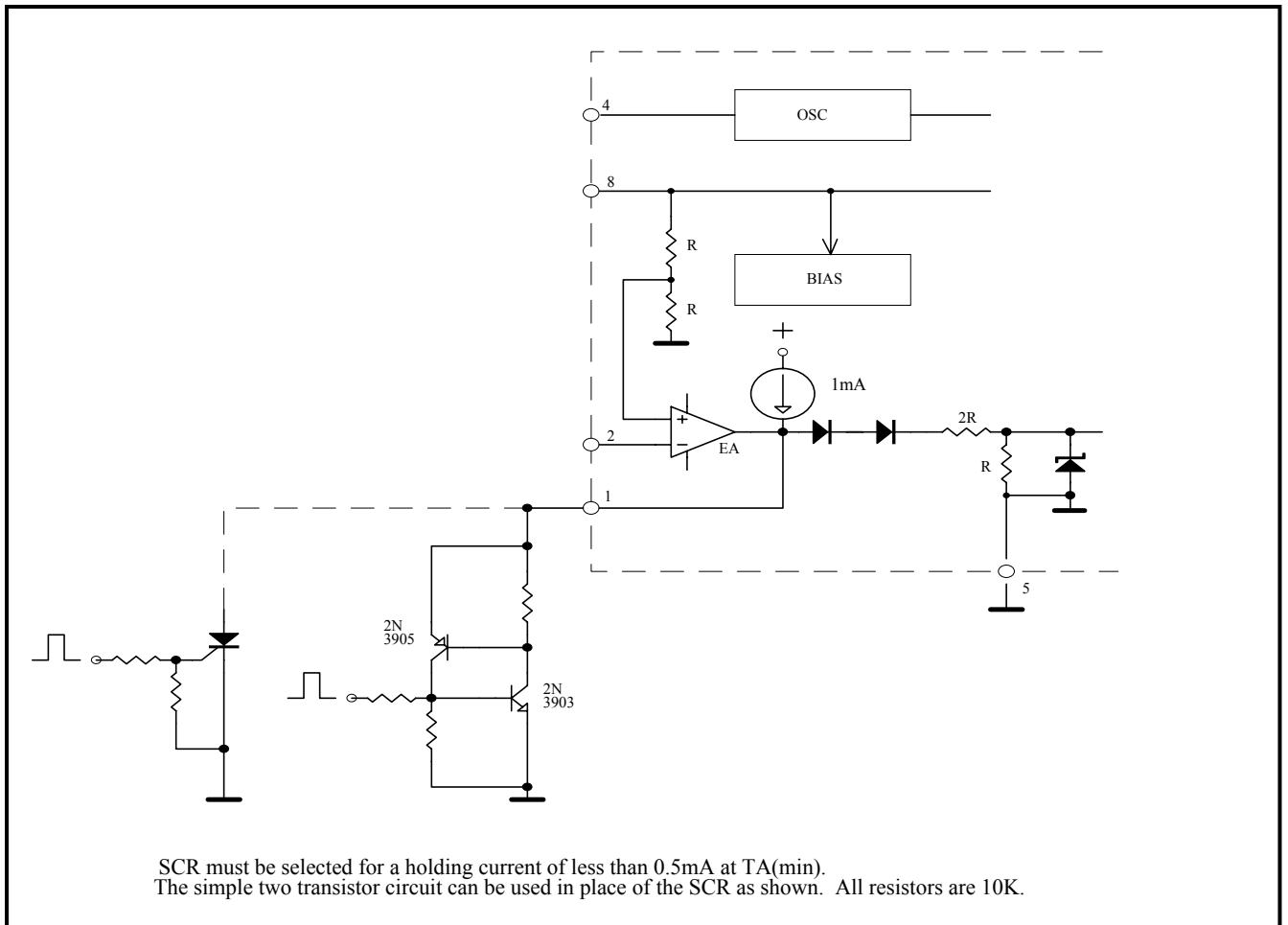


Figure 17:External Clock Synchronization

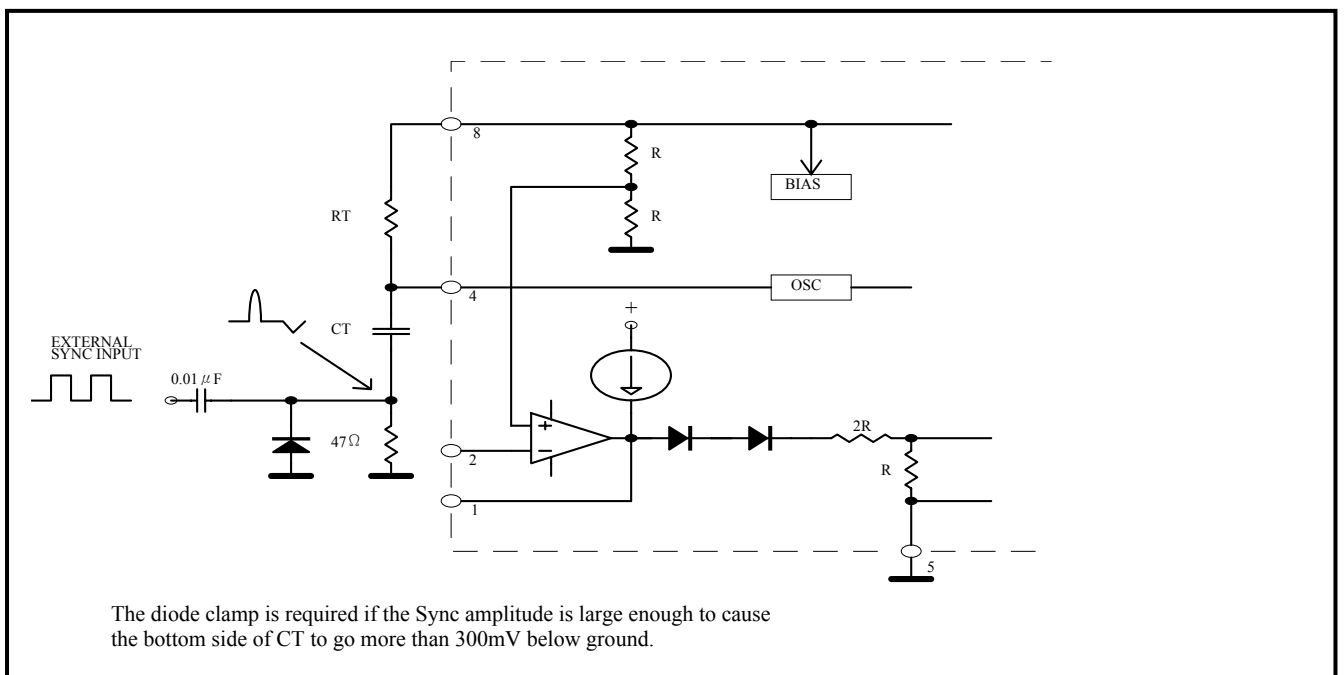
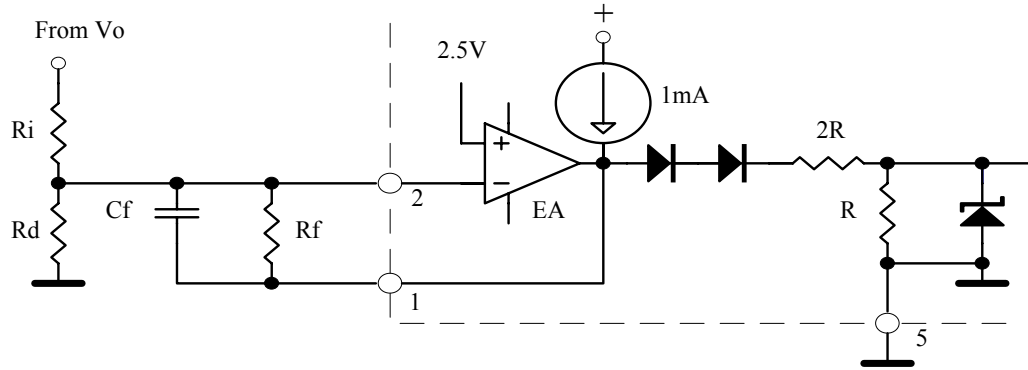
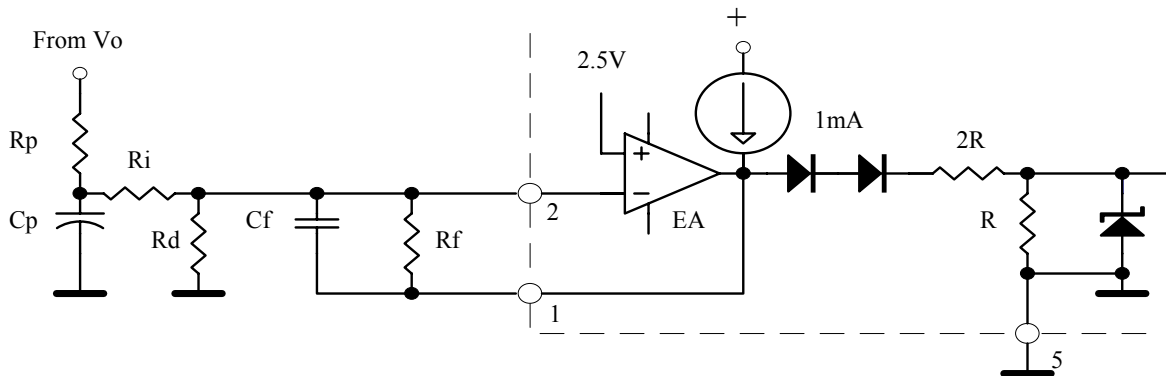


Figure 18: Error Amplifier Compensation



Error Amp compensation circuit for stabilizing any current -mode topology except for boost and flyback converters operating with continuous inductor current.



Error Amp compensation circuit for stabilizing current--mode boost and flyback

Figure 19: External Duty Cycle Clamp and Multi Unit Synchronization

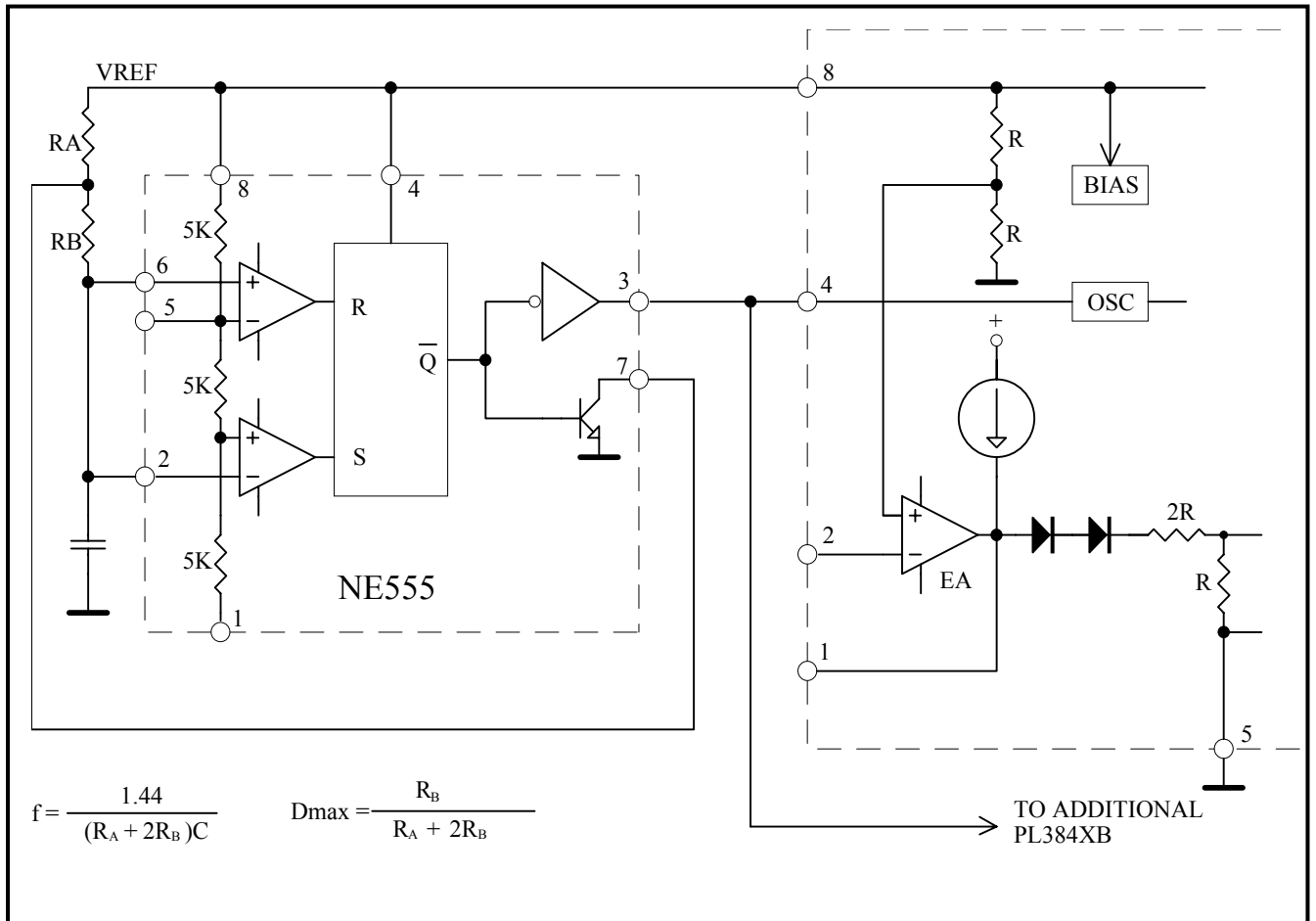


Figure 20:Soft-Start Circuit

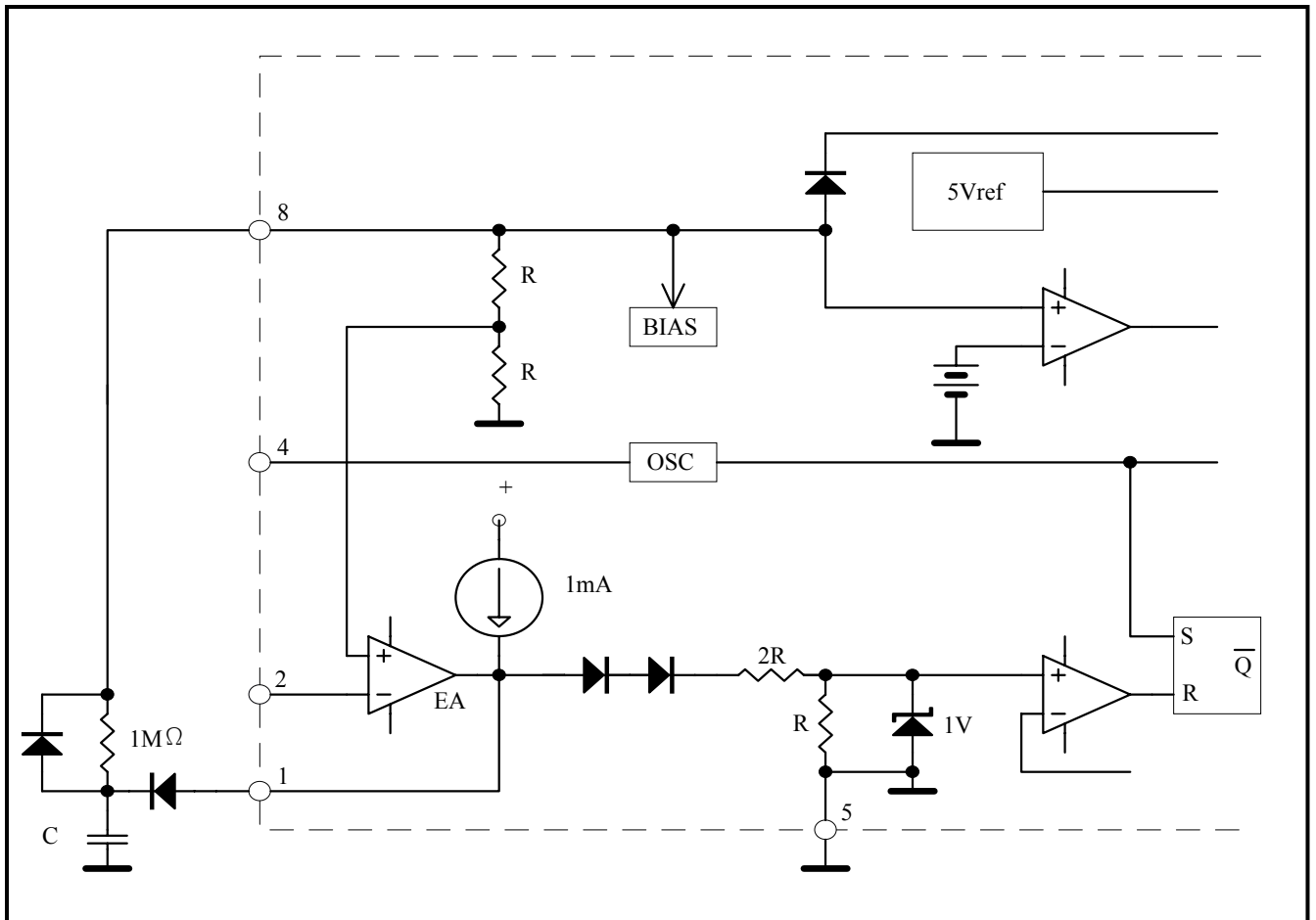
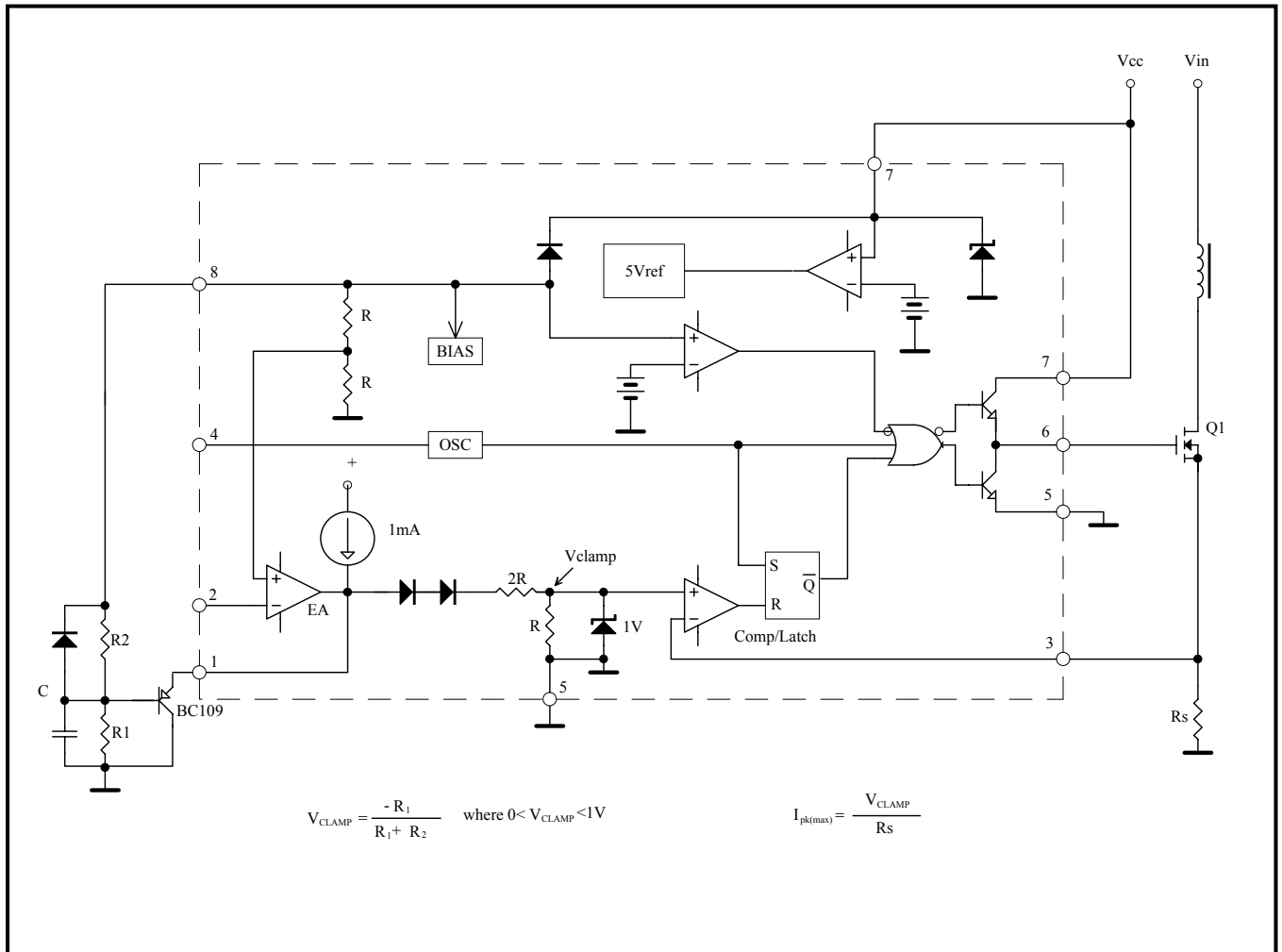
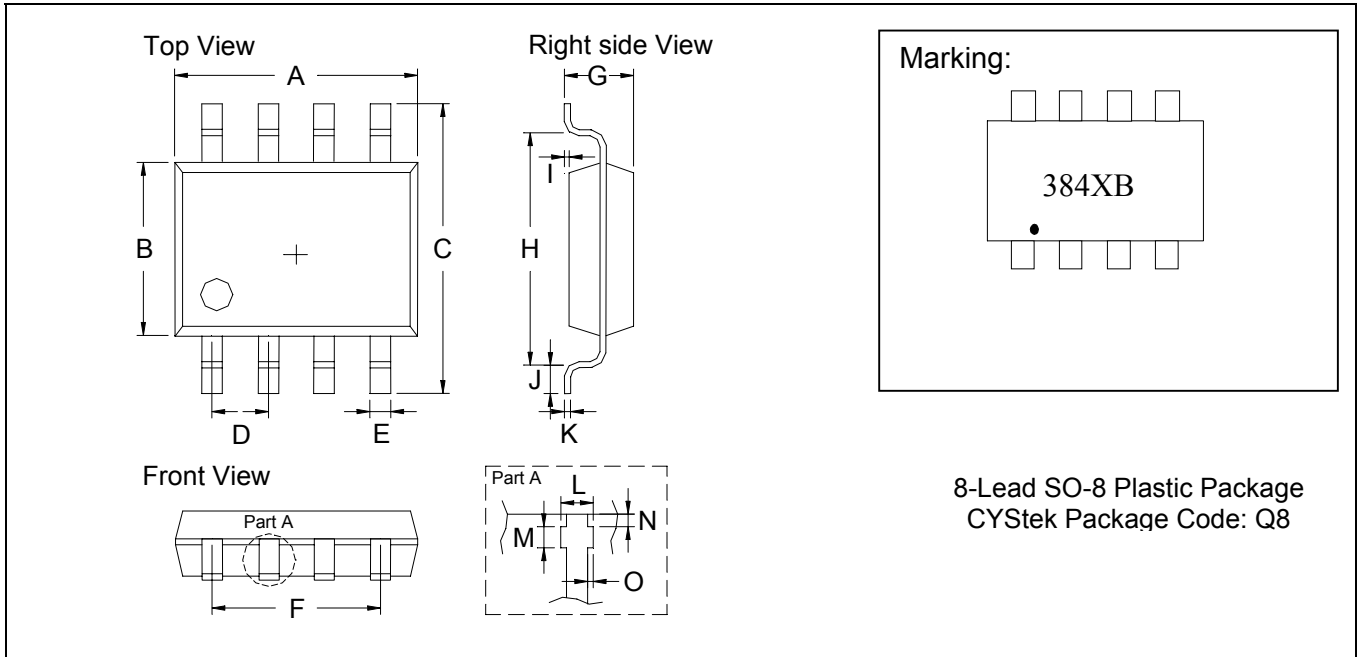


Figure 21: Soft-Start and Error Amplifier Output Duty Cycle Clamp.



SO-8 Dimension



*: Typical

| DIM | Inches | | Millimeters | | DIM | Inches | | Millimeters | |
|-----|--------|--------|-------------|------|-----|--------|--------|-------------|------|
| | Min. | Max. | Min. | Max. | | Min. | Max. | Min. | Max. |
| A | 0.1909 | 0.2007 | 4.85 | 5.10 | I | 0.0019 | 0.0078 | 0.05 | 0.20 |
| B | 0.1515 | 0.1555 | 3.85 | 3.95 | J | 0.0118 | 0.0275 | 0.30 | 0.70 |
| C | 0.2283 | 0.2441 | 5.80 | 6.20 | K | 0.0074 | 0.0098 | 0.19 | 0.25 |
| D | 0.0480 | 0.0519 | 1.22 | 1.32 | L | 0.0145 | 0.0204 | 0.37 | 0.52 |
| E | 0.0145 | 0.0185 | 0.37 | 0.47 | M | 0.0118 | 0.0197 | 0.30 | 0.50 |
| F | 0.1472 | 0.1527 | 3.74 | 3.88 | N | 0.0031 | 0.0051 | 0.08 | 0.13 |
| G | 0.0570 | 0.0649 | 1.45 | 1.65 | O | 0.0000 | 0.0059 | 0.00 | 0.15 |
| H | 0.1889 | 0.2007 | 4.80 | 5.10 | | | | | |

Notes: 1. Controlling dimension: millimeters.
 2. Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3. If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: 42 Alloy; solder plating
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.