

Addendum

HC908JB8AD/D
Rev. 0, 4/2002

Addendum to
MC68HC908JB8
Technical Data



This addendum provides additional information to the
MC68HC908JB8 Technical Data, Rev. 2
(Motorola document number MC68HC908JB8/D),

MC68HC08JB8A

The MC68HC08JB8A is the ROM part equivalent to the MC68HC908JB8. The entire MC68HC908JB8 data book apply to this ROM device, with exceptions outlined in this addendum.

Table 1. Summary of MC68HC08JB8A and MC68HC908JB8 Differences

| | MC68HC08JB8A | MC68HC908JB8 |
|--|--|---|
| Memory (\$DC00–\$FBFF) | 8,192 bytes ROM | 8,192 bytes FLASH |
| User vectors (\$FFF0–\$FFFF) | 16 bytes ROM | 16 bytes FLASH |
| Registers at \$FE08 and \$FF09 | Not used; locations are reserved. | FLASH related registers. \$FE08 — FLCR \$FF09 — FLBPR |
| Monitor ROM (\$FC00–\$FDFF and \$FE10–\$FFDF) | \$FC00–\$FDFF: Not used. \$FE10–\$FFDF: Used for testing purposes only. | Used for testing and FLASH programming/erasing. |
| OSC1 and OSC2 pins | V _{DD} level (5V logic) | V _{REG} level (3.3V logic) |

MCU Block Diagram **Figure 1** shows the block diagram of the MC68HC08JB8A.

Memory Map The MC68HC08JB8A has 8,192 bytes of user ROM from \$DC00 to \$FBFF, and 16 bytes of user ROM vectors from \$FFF0 to \$FFFF. On the MC68HC908JB8, these memory locations are FLASH memory.

Figure 2 shows the memory map of the MC68HC08JB8A.

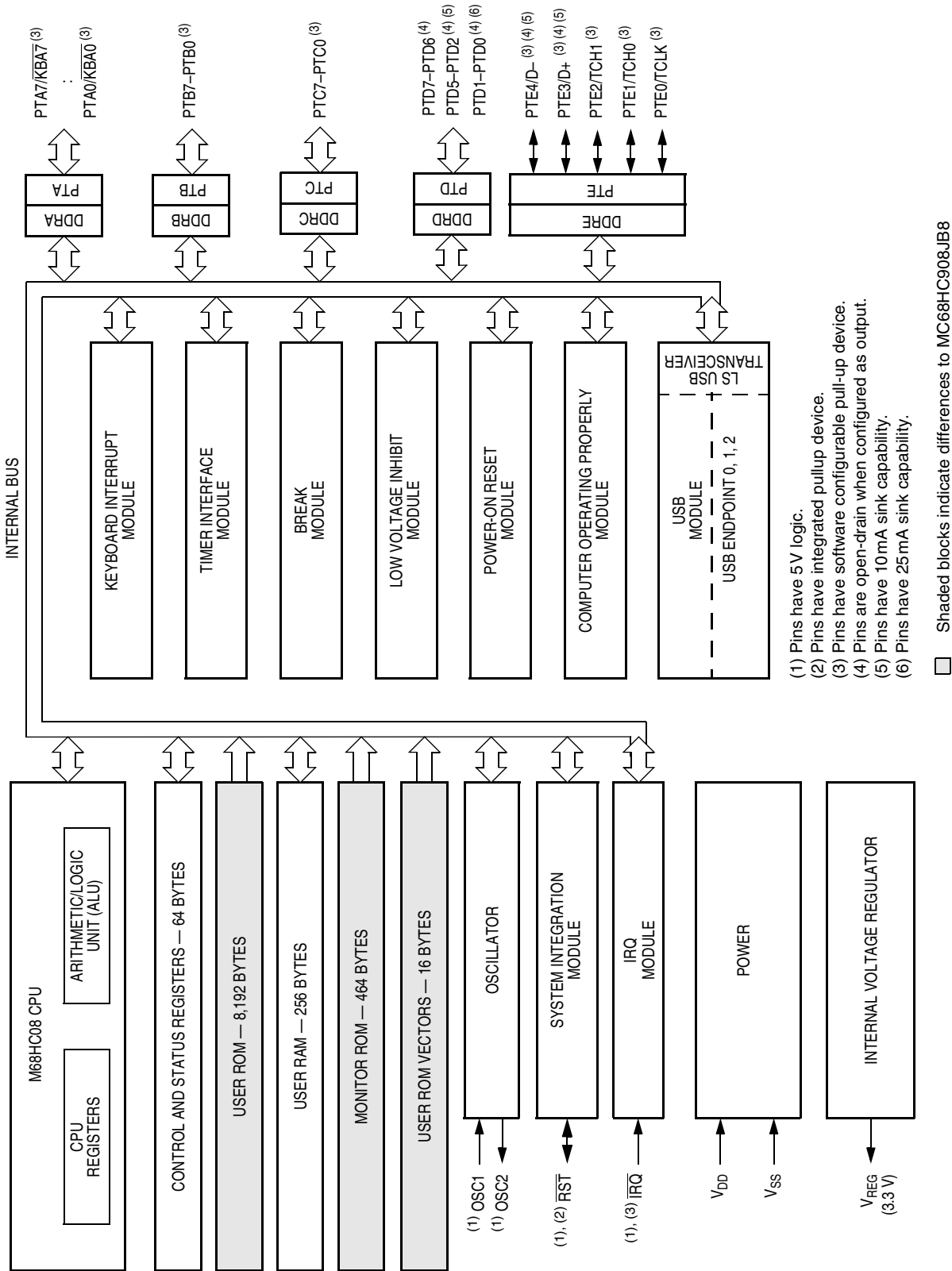


Figure 1. MC68HC08JB8A Block Diagram

| | |
|-----------------------|--|
| \$0000 ↓ \$003F | I/O Registers 64 Bytes |
| \$0040 ↓ \$013F | RAM 256 Bytes |
| \$0140 ↓ \$DBFF | Unimplemented 56,000 Bytes |
| \$DC00 ↓ \$FBFF | ROM 8,192 Bytes |
| \$FC00 ↓ \$FDFF | Unimplemented 512 Bytes |
| \$FE00 | Break Status Register (BSR) |
| \$FE01 | Reset Status Register (RSR) |
| \$FE02 | Reserved |
| \$FE03 | Break Flag Control Register (BFCR) |
| \$FE04 | Interrupt Status Register 1 (INT1) |
| \$FE05 | Reserved |
| \$FE06 | Reserved |
| \$FE07 | Reserved |
| \$FE08 | Reserved |
| \$FE09 | Reserved |
| \$FE0A | Reserved |
| \$FE0B | Reserved |
| \$FE0C | Break Address High Register (BRKH) |
| \$FE0D | Break Address Low Register (BRKL) |
| \$FE0E | Break Status and Control Register (BRKSCR) |
| \$FE0F | Reserved |
| \$FE10 ↓ \$FFDF | Monitor ROM 464 Bytes |
| \$FFE0 ↓ \$FFEF | Reserved 16 Bytes |
| \$FFF0 ↓ \$FFFF | ROM Vectors 16 Bytes |

Figure 2. MC68HC08JB8A Memory Map

Reserved Registers The two registers at \$FE08 and \$FE09 are reserved locations on the MC68HC08JB8A.

On the MC68HC908JB8, these two locations are the FLASH control register and the FLASH block protect register respectively.

Monitor ROM The monitor program (monitor ROM: \$FE10–\$FFDF) on the MC68HC08JB8A is for device testing only. \$FC00–\$FDFF are unused.

Electrical Specifications Electrical specifications for the MC68HC908JB8 apply to the MC68HC08JB8A, except for the parameters indicated below.

DC Electrical Characteristics

Table 2. DC Electrical Characteristics

| Characteristic ⁽¹⁾ | Symbol | Min | Typ ⁽²⁾ | Max | Unit |
|--|-----------|---|--------------------|---|------|
| Regulator output voltage | V_{REG} | 3.0 | 3.3 | 3.6 | V |
| Output high voltage ($I_{Load} = -2.0$ mA) PTA0–PTA7, PTB0–PTB7, PTC0–PTC7, PTE0–PTE2 | V_{OH} | $V_{REG} - 0.8$ | — | — | V |
| Output low voltage ($I_{Load} = 1.6$ mA) All I/O pins ($I_{Load} = 25$ mA) PTD0–PTD1 in ILDD mode ($I_{Load} = 10$ mA) PTE3–PTE4 with USB disabled | V_{OL} | — — — | — — — | 0.4 0.5 0.4 | V |
| Input high voltage All ports, OSC1 \overline{IRQ} , \overline{RST} | V_{IH} | $0.7 \times V_{REG}$ $0.7 \times V_{DD}$ | — — | V_{REG} V_{DD} | V |
| Input low voltage All ports, OSC1 \overline{IRQ} , \overline{RST} | V_{IL} | V_{SS} V_{SS} | — — | $0.3 \times V_{REG}$ $0.3 \times V_{DD}$ | V |
| Output low current ($V_{OL} = 2.0$ V) PTD2–PTD5 in LDD mode | I_{OL} | 12 (17) | 17 (22) | 22 (27) | mA |
| V_{DD} supply current, $V_{DD} = 5.25$ V, $f_{OP} = 3$ MHz | | | | | |
| Run, with low speed USB ⁽³⁾ | I_{DD} | — | 6.0 (5.0) | 7.5 | mA |
| Run, with USB suspended ⁽³⁾ | | — | 5.5 (4.5) | 6.5 | mA |
| Wait, with low speed USB ⁽⁴⁾ | | — | 4.0 (3.0) | 5.0 | mA |
| Wait, with USB suspended ⁽⁴⁾ | | — | 3.0 (2.5) | 4.0 | mA |
| Stop ⁽⁵⁾ 0 °C to 70°C | | — | 30 | 100 | μA |

Table 2. DC Electrical Characteristics

| Characteristic ⁽¹⁾ | Symbol | Min | Typ ⁽²⁾ | Max | Unit |
|--|-----------------------|---------------------|--------------------|--------------------------|------------|
| I/O ports Hi-Z leakage current | I_{IL} | — | — | ± 10 | μA |
| Input current | I_{IN} | — | — | ± 1 | μA |
| Capacitance Ports (as input or output) | C_{Out} C_{In} | — — | — — | 12 8 | pF |
| POR re-arm voltage ⁽⁶⁾ | V_{POR} | 0 | — | 100 | mV |
| POR rise-time ramp rate ⁽⁷⁾ | R_{POR} | 0.035 | — | — | V/ms |
| Monitor mode entry voltage | $V_{DD}+V_{HI}$ | $1.4 \times V_{DD}$ | | $2 \times V_{DD}$ | V |
| Pullup resistors Port A, port B, port C, PTE0–PTE2, \overline{RST} , \overline{IRQ} PTE3–PTE4 (with USB module disabled) D– (with USB module enabled) | R_{PU} | 25 4 1.2 | 40 5 1.5 | 55 6 2.0 | k Ω |
| LVI reset | V_{LVR} | 2.8 (2.4) | 3.3 (2.7) | 3.8 (3.0) ⁽⁸⁾ | V |

- $V_{DD} = 4.0$ to 5.5 Vdc, $V_{SS} = 0$ Vdc, $T_A = T_L$ to T_H , unless otherwise noted.
- Typical values reflect average measurements at midpoint of voltage range, $25^\circ C$ only.
- Run (operating) I_{DD} measured using external square wave clock source ($f_{XCLK} = 6$ MHz). All inputs 0.2 V from rail. No dc loads. Less than 100 pF on all outputs. $C_L = 20$ pF on OSC2. All ports configured as inputs. OSC2 capacitance linearly affects run I_{DD} . Measured with all modules enabled.
- Wait I_{DD} measured using external square wave clock source ($f_{XCLK} = 6$ MHz); all inputs 0.2 V from rail; no dc loads; less than 100 pF on all outputs. $C_L = 20$ pF on OSC2; 15 k $\Omega \pm 5\%$ termination resistors on D+ and D– pins; all ports configured as inputs; OSC2 capacitance linearly affects wait I_{DD}
- STOP I_{DD} measured with USB in suspend mode; OSC1 grounded; transceiver pullup resistor of 1.5 k $\Omega \pm 5\%$ between V_{REG} and D– pins and 15 k $\Omega \pm 5\%$ termination resistor on D+ pin; no port pins sourcing current.
- Maximum is highest voltage that POR is guaranteed.
- If minimum V_{REG} is not reached before the internal POR reset is released, \overline{RST} must be driven low externally until minimum V_{REG} is reached.
- The numbers in parenthesis are MC68HC08JB8 (non-A part) values.

Memory
Characteristics

Table 3. Memory Characteristics

| Characteristic | Symbol | Min | Max | Unit |
|----------------------------|-----------|-----|-----|------|
| RAM data retention voltage | V_{RDR} | 1.3 | — | V |

Notes:

Since MC68HC08JB8A is a ROM device, FLASH memory electrical characteristics do not apply.

**MC68HC08JB8A
Order Numbers**

These part numbers are generic numbers only. To place an order, ROM code must be submitted to the ROM Processing Center (RPC).

Table 4. MC68HC08JB8A Order Numbers

| MC order number | Package | Operating temperature range |
|-----------------|-------------|-----------------------------|
| MC68HC08JB8AJP | 20-pin PDIP | 0 °C to +70 °C |
| MC68HC08JB8AJDW | 20-pin SOIC | 0 °C to +70 °C |
| MC68HC08JB8AADW | 28-pin SOIC | 0 °C to +70 °C |
| MC68HC08JB8AFB | 44-pin QFP | 0 °C to +70 °C |

MC68HC08JB8A and MC68HC08JB8 Differences

The MC68HC08JB8A and MC68HC08JB8 are identical devices, except for the following:

Table 5. MC68HC08JB8A and MC68HC08JB8 Differences

| | MC68HC08JB8A | MC68HC08JB8 |
|---|---|-------------------------------------|
| OSC1 and OSC2 pins | V _{DD} level (5V logic) | V _{REG} level (3.3V logic) |
| Output low current on PTD2–PTD5 in LDD mode | See Table 2 . DC Electrical Characteristics . The numbers in parenthesis are MC68HC08JB8 values. | |
| Operating I _{DD} currents | | |
| LVI trip points | | |

NOTES

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Rev. 0

4/2003

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