TOSHIBA TC7MZ540FK

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

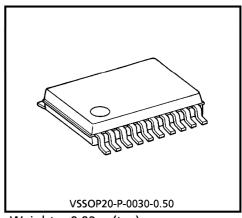
TC7MZ540FK

LOW VOLTAGE OCTAL BUS BUFFER (INVERTED) WITH 5 V TOLERANT INPUTS AND OUTPUTS

The TC7MZ540 is a high parformance CMOS OCTAL BUS BUFFER. Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

The device is designed for low-voltage (3.3 V) V_{CC} applications, but it could be used to interface to 5 V supply environment for both inputs and outputs. The TC7MZ540 is an inverting 3-state buffer having two active-low output enables. When either $\overline{OE}1$ or $\overline{OE}2$ are high, the terminal outputs are in the high-impedance state. This device is designed to be used with 3-state memory address drivers, etc.

All inputs are equipped with protection circuits against static discharge.



Weight: 0.03 g (typ)

Features

• Low voltage operation : $V_{CC} = 2.0 \sim 3.6 \text{ V}$

• High speed operation : $t_{pd} = 6.5 \text{ ns (max)}$

 $(\dot{V}_{CC} = 3.0 \sim 3.6 \text{ V})$

• Output current : $|I_{OH}|/I_{OL} = 24 \text{ mA}$ (min)

 $(V_{CC} = 3.0 V)$

• Latch-up performance : ±500 mA

Available in VSSOP (US20)

- Power down protection is provided on all inputs and outputs.
- Pin and function compatible with the 74 series (74AC/VHC/HC/F/ALS/LS etc.) 540 type.

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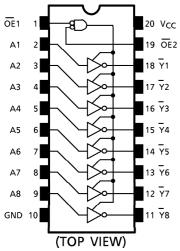
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Pin Assignment



Truth Table

	INPUTS	OUTPUTS	
OE1	OE2	An	0011013
Н	Х	Х	Z
Х	Н	Х	Z
L	L	Н	L
Ĺ	L	L	Н

X : Don't Care Z : High Impedance

IEC Logic Symbol

OE1 (1) N	& EN		
A1 (2) A2 (3) A3 (4) A4 (5) A5 (6) A6 (7) A7 (8) A8 (9)	Δ .	(18) (17) (16) (15) (14) (13) (12) (11)	— Y1 — Y2 — Y3 — Y4 — Y5 — Y6 — Y7 — Y8

Maximum Ratings

PARAMETER	SYMBOL	RATING	UNIT	
Supply Voltage Range	V _{CC}	-0.5~7.0	V	
DC Input Voltage	VIN	-0.5~7.0	V	
DC Output Voltage	\/ - -	-0.5~7.0 (Note 1)	V	
DC Output Voltage	Vout	-0.5~V _{CC} + 0.5 (Note 2)	"	
Input Diode Current	lικ	– 50	mA	
Output Diode Current	loк	± 50 (Note 3)	mA	
DC Output Current	lout	± 50	mA	
Power Dissipation	PD	180	mW	
DC V _{CC} /Ground Current	ICC / IGND	± 100	mA	
Storage Temperature	T _{stg}	- 65∼150	°C	

(Note 1): Output in Off-State

(Note 2): High or Low State. IOUT absolute maximum rating must be observed.

(Note 3): V_{OUT} < GND, V_{OUT} > V_{CC}

Recommended Operating Conditions

PARAMETER	SYMBOL	RATING	UNIT	
Supply Voltage	V	2.0~3.6	V	
Supply Voltage	Vcc	1.5~3.6 (Note 4)	V	
Input Voltage	VIN	0~5.5	V	
Output Voltage	0~5.5 (Note 5)		V	
Output Voltage	Vout	0~ V _{CC} (Note 6)	V	
Output Current	10/10.	± 24 (Note 7)	A	
Output Current	IOH/IOL	± 12 (Note 8)	mA	
Operating Temperature	T _{opr}	- 40~85	°C	
Input Rise And Fall Time	dt/dv	0~10 (Note 9)	ns / V	

(Note 4): Data Retention Only (Note 5): Output in Off-State (Note 6): High or Low State

(Note 7): $V_{CC} = 3.0 \sim 3.6 \text{ V}$ (Note 8): $V_{CC} = 2.7 \sim 3.0 \text{ V}$ (Note 9): $V_{IN} = 0.8 \sim 2.0 \text{ V}$, $V_{CC} = 3.0 \text{ V}$

Electrical Characteristics

DC characteristics (Ta = $-40 \sim 85$ °C)

PARAI	METER	SYMBOL	TEST COI	NDITION	V _{CC} (V)	Min	Max	UNIT
Input	"H" Level	v_{IH}			2.7~3.6	2.0	_	V
Voltage	"L" Level	V _{IL}			2.7~3.6	_	0.8	V
				$I_{OH} = -100 \mu A$	2.7~3.6	V _C C - 0.2		
	"H" Level	Voн	V _{IN} = V _{IH} or V _{IL}	$I_{OH} = -12 \text{ mA}$	2.7	2.2	_	
				$I_{OH} = -18 \text{mA}$	3.0	2.4		
Output				$I_{OH} = -24 \text{mA}$	3.0	2.2	_	V
Voltage			V_{OL} $V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 100 \ \mu\text{A}$	I _{OL} = 100 μA	2.7~3.6	_	0.2	
	"L" Level	VOL ,		I _{OL} = 12 mA	2.7	_	0.4	
			I VIN - VIH OI VIL	I _{OL} = 16 mA	3.0	_	0.4	
				I _{OL} = 24 mA	3.0	_	0.55	
Input Leaka	ge Current	IN	V _{IN} = 0~5.5 V	•	2.7~3.6	_	± 5.0	μΑ
3-State Outp Off-State Cu		loz	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{OUT} = 0 \sim 5.5 \text{ V}$		2.7~3.6	_	± 5.0	μ A
Power Off L Cuurent	-eakage	lOFF	V _{IN} / V _{OUT} = 5.5 V	,	0	_	10.0	μ A
Quiescent Su	upply		$V_{IN} = V_{CC}$ or GND)	2.7~3.6		10.0	^
Current		lcc	V _{IN} / V _{OUT} = 3.6~5.5 V		2.7~3.6	_	± 10.0	μ A
Increase In I Input	CC Per	ΔΙCC	V _{IH} = V _{CC} - 0.6 V		2.7~3.6	_	500	μΑ

AC characteristic (Ta = $-40 \sim 85$ °C)

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	Min	Max	UNIT
Propagation Delay	^t pLH	(Fig.1, 2)	2.7	_	7.5	nc
Time	t _{pHL}	(Fig. 1, 2)	3.3 ± 0.3	1.5	6.5	ns
Outnut Enable Time	t _{pZL}	(Fig.1, 3)	2.7	_	9.5	nc
Output Enable Time	^t pZH		3.3 ± 0.3	1.5	8.5	ns
Output Disable Time	^t pLZ	/Fig. 1 2)	2.7	_	8.5	ne
Output Disable Time	^t pHZ	(Fig.1, 3)	3.3 ± 0.3	1.5	7.5	ns
Output To Output	^t osLH	(Note 10)	2.7	_	_	nc
Skew	tosHL		3.3 ± 0.3	_	1.0	ns

(Note 10): Parameter guaranteed by design. $(t_{OSLH} = |t_{pLHm} - t_{pLHn}|, \ t_{OSHL} = |t_{pHLm} - t_{pHLn}|)$

Dynamic Switching Characteristics (Ta = 25°C, Input $t_{\Gamma} = t_{f} = 2.5 \text{ ns}$, $C_{L} = 50 \text{ pF}$, $R_{L} = 500 \Omega$)

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	Тур.	UNIT
Quiet Output Maximum Dynamic VOL	V _{OLP}	V _{IH} = 3.3 V, V _{IL} = 0 V	3.3	0.8	٧
Quiet Output Minimum Dynamic VOL	V _{OLV}	V _{IH} = 3.3 V, V _{IL} = 0 V	3.3	0.8	٧

Capacitive Characteristics (Ta = 25°C)

PARAMETER	SYMBOL	TEST CONDITION		V _{CC} (V)	Тур.	UNIT
Input Capacitance	C _{IN}			3.3	7	pF
Output Capacitance	COUT	-		3.3	8	рF
Power Dissipation Capacitance	C _{PD}	f _{IN} = 10 MHz	(Note 11)	3.3	40	pF

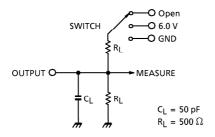
(Note 11): C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation:

 $I_{CC (opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$

Test Circuit

Fig.1



PARAMETER	SWITCH
t _{pLH} , t _{pHL}	Open
t _{pLZ} , t _{pZL}	6.0 V
^t pHZ ^{, t} pZH	GND

AC Waveform

Fig.2 t_{pLH}, t_{pHL}

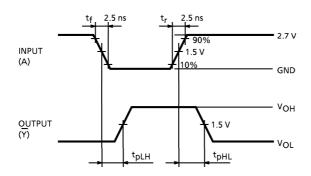
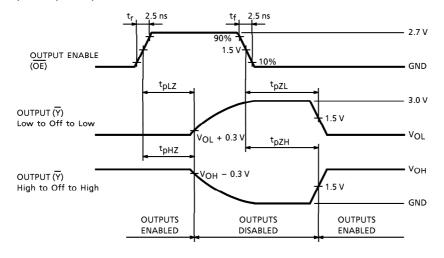


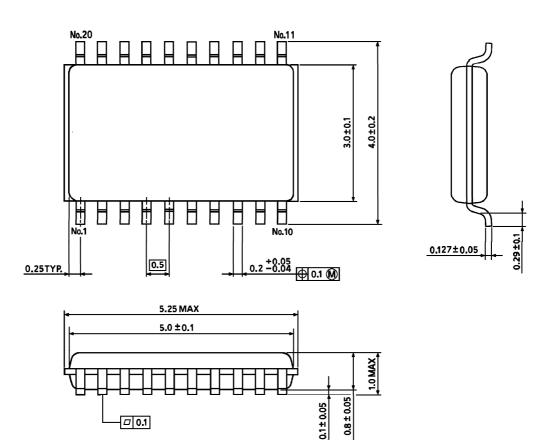
Fig.3 t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}



Unit: mm

Outline Drawing

VSSOP20-P-0030-0.50



Weight: 0.03 g (typ.)