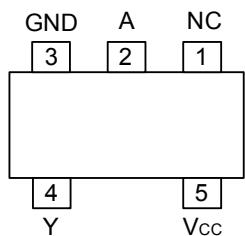




■ PIN CONFIGURATION



■ FUNCTION TABLE (each gate)

INPUT	OUTPUT
A	Y
L	L
H	H

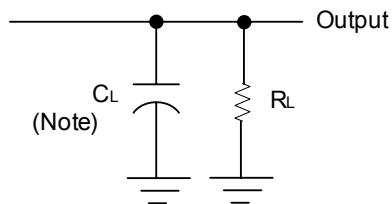
■ LOGIC DIAGRAM (positive logic)





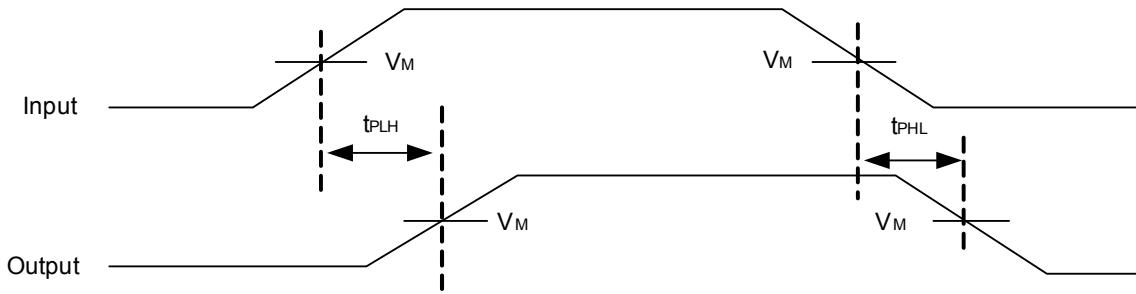


### TEST CIRCUIT AND WAVEFORMS



Note:  $C_L$  includes probe and jig capacitance.

$V_{CC}$	$V_{IN}$	$t_R, t_F$	$V_M$	$C_L$	$R_L$
$1.8V \pm 0.15V$	$V_{CC}$	$\leq 2\text{ns}$	$V_{CC}/2$	15pF	1M
$2.5V \pm 0.2V$	$V_{CC}$	$\leq 2\text{ns}$	$V_{CC}/2$	15pF	1M
$3.3V \pm 0.3V$	3V	$\leq 2.5\text{ns}$	1.5V	15pF	1M
$5V \pm 0.5V$	$V_{CC}$	$\leq 2.5\text{ns}$	$V_{CC}/2$	15pF	1M
$1.8V \pm 0.15V$	$V_{CC}$	$\leq 2\text{ns}$	$V_{CC}/2$	30pF	1K
$2.5V \pm 0.2V$	$V_{CC}$	$\leq 2\text{ns}$	$V_{CC}/2$	30pF	500
$3.3V \pm 0.3V$	3V	$\leq 2.5\text{ns}$	1.5V	50pF	500
$5V \pm 0.5V$	$V_{CC}$	$\leq 2.5\text{ns}$	$V_{CC}/2$	50pF	500



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