FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-16803-1E

32-bit Microcontroller

CMOS

FR60Lite MB91245/S Series

MB91247/247S/248/248S/F248/F248S/MB91V245A

■ OVERVIEW

MB91245/S series is Fujitsu's general-purpose 32-bit RISC microcontroller, which is designed for embedded control applications that require high-speed real-time processing of consumer appliances. This microcontroller uses FR60Lite as its CPU, compatible with other products in the FR* family.

This series incorporates an LCD controller and stepping motor controller.

* : FR, the abbreviation of FUJITSU RISC controller, is a line of products of FUJITSU Limited.

■ FEATURES

- **FR60Lite CPU**
  - 32-bit RISC, load/store architecture, 5-stage pipeline
  - Maximum operating frequency : 32 MHz (Source oscillation is 4 MHz with x8 multiplier – PLL clock multiplier system)
  - 16-bit fixed-length instructions (basic instructions)
  - Instruction execution speed : 1 instruction per cycle
  - Instruction set optimized for embedded application : Memory-to-memory transfer, bit manipulation, barrel shift instructions etc.
  - Instructions adapted for programming C language : Function entry/exit instructions, multiple-register load/store instructions.
  - Register interlock function : Easier assembler coding enabled
  - Built-in multiplier supported at the instruction level
    Signed 32-bit multiplication : 5 cycles
    Signed 16-bit multiplication : 3 cycles

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Be sure to refer to the "Check Sheet" for the latest cautions on development.

"Check Sheet" is seen at the following support page
URL : http://www.fujitsu.com/global/services/microelectronics/product/micom/support/index.html

"Check Sheet" lists the minimal requirement items to be checked to prevent problems beforehand in system development.

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- Interrupt (PC/PS save) : 6 cycles (16 priority levels)
- Harvard architecture allowing program access and data access to be executed simultaneously.
- Instruction set compatible with FR family

• **Internal Peripheral Functions**

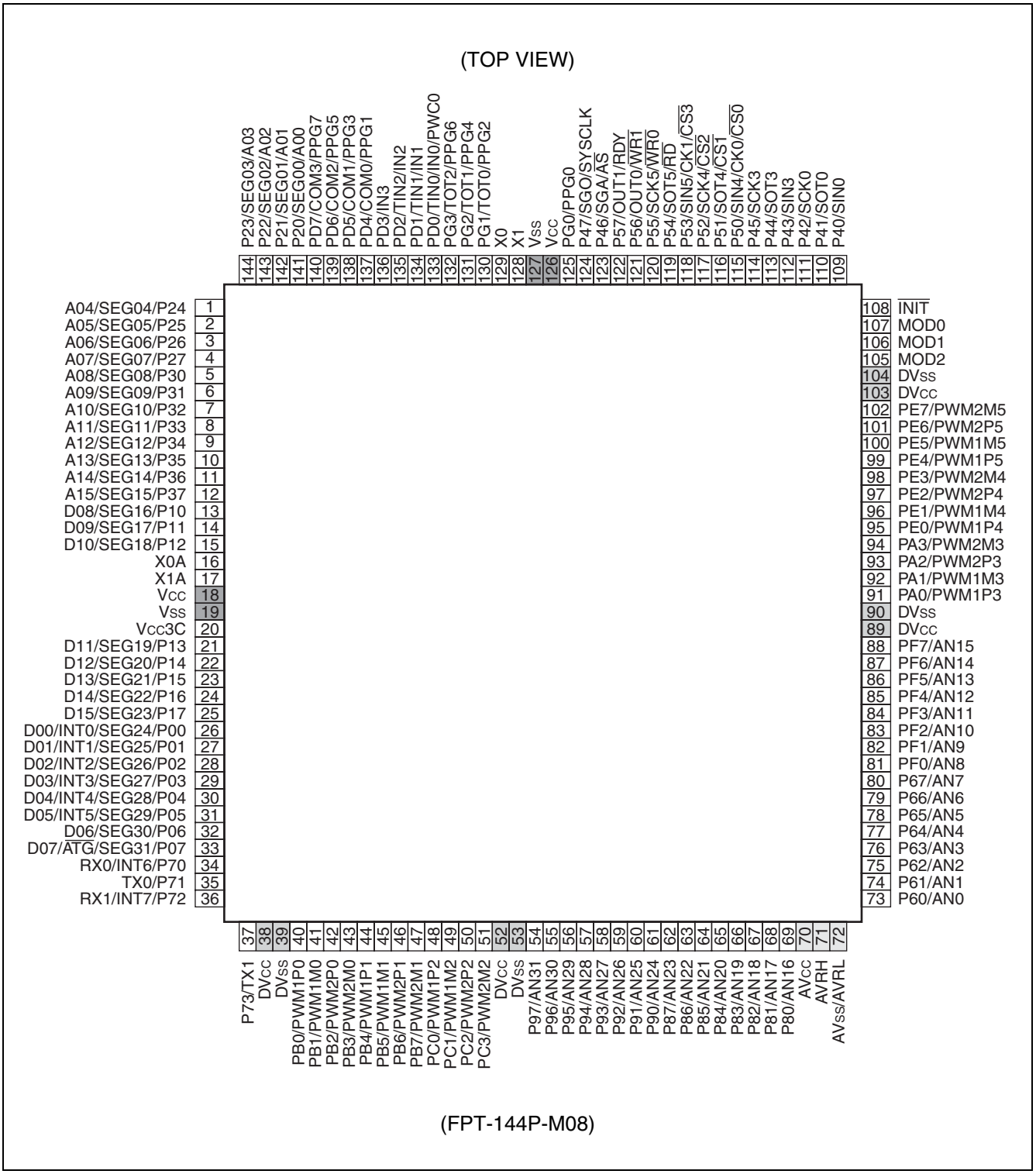
- Internal ROM size & ROM type
  MASK ROM : 256 Kbytes (MB91248/S) / 128 Kbytes (MB91247/S)
  Flash Memory : 256 Kbytes
- Internal RAM size : 16 Kbytes (MB91248/S, MB91F248/S) / 8 Kbytes (MB91247/S) / 32 Kbytes (MB91V245A)
- General-purpose ports : up to 120 ports (includes 4 input-only ports)
- 8/10-bit A/D converter (Sequential comparison type)
  8/10-bit resolution : 32 channels
  Conversion time : 3 µs (16/32 MHz)
  Set the PLL multiplier and the division ratio of peripheral circuit clocks so that the above conversion time is achieved.
  32 MHz : Source oscillation (4 MHz) with x8 multiplier, divided by 1
  16 MHz : Source oscillation with x8 multiplier, divided by 2
- External interrupt input : 8 channels
- Bit search module (for REALOS)
  Search function to locate the position of the first bit that changes from “1” to “0” in one word, from the MSB (Most Significant Bit)
- UART (full duplex double buffer type) : 1 channel
  Parity enable/disable selectable
  Asynchronous clock operation (start-stop synchronization) and synchronous clock operation selectable
  Dedicated baud-rate timer (U-Timer) embedded in each channel
  External clock can be used as transfer clock
  Parity, frame, overrun error detection functions provided
- LIN-UART (full duplex double buffer type) : 3 channels
  Synchronous/asynchronous clock operations selectable
  Sync-break detection
  Dedicated built-in baud-rate generator
- Stepping motor controller (SMC) : 6 channels
  8-bit PWM with 4 high-current outputs for each channel
- 8/16-bit PPG timer : 8/4 channels
- 16-bit reload timer : 3 channels
- 16-bit free-run timer : 2 channels (ICU/OCU linkage)
- 16-bit pulse width counter : 1 channel
- Input capture : 4 channels (linked to ch.0 and ch.1 of free-run timer)
  ch.0 linked to PWC
- Output compare : 2 channels (linked to ch.0 of free-run timer)
- LCD controller : SEG00 to SEG31/COM0 to COM3 (shared with port)
- 16-bit timebase/watch dog timer
- Sound generator
- Real-time clock
- 32 kHz sub clock (not supported in single clock products)
- C-CAN : 2 channels
- Low power consumption modes : sleep mode, stop mode, watch mode
- Package : LQFP-144 (FPT-144P-M08)
- CMOS technology : 0.35 µm
- Power supply voltage : 5 V (Internal logic : 3.3 V, I/O : 5.0 V (step-down circuit used))

■ PRODUCT LINEUP

A table below shows the product lineup of the MB91245/S series. Embedded peripheral functions which are not listed are common functions.

	MB91V245A	MB91247/S	MB91248/S	MB91F248/S
ROM/Flash size	External SRAM	128 Kbytes	256 Kbytes	256 Kbytes
RAM size	32 Kbytes	8 Kbytes	16 Kbytes	16 Kbytes
External interrupt	8 channels			
DMA Controller	5 channels			
A/D Converter	32 channels			
UART	1 channel			
LIN-UART	3 channels			
Stepping Motor Controller	6 channels			
8 /16-bit PPG	8 channels/4 channels			
16-bit Reload Timer	3 channels			
16-bit Free Run Timer	2 channels			
16-bit Pulse Width Counter	1 channel			
Input Capture Unit	4 channels			
Output Compare Unit	2 channels			
LCD Controller	4 COM, 32 SEG			
Sound Generator	1 channel			
Real Time Clock	Yes			
32 kHz Sub Clock	Yes	Yes/No (S series)	Yes/No (S series)	Yes/No (S series)
External bus	Addr 16 bits Data 16 bits			
Others	EVA device	MASK ROM product	MASK ROM product	Flash memory product
On Chip Debug Support Unit	DSU4	—		
C-CAN unit	2 channels 32-message buffer			

■ PIN ASSIGNMENT



■ PIN DESCRIPTIONS

Pin no.	Pin name	I/O circuit type*	Function
1 to 4	P24 to P27	F	General purpose I/O port pins
	SEG04 to SEG07		SEG output pin for LCDC
	A04 to A07		Bits 04 to 07 pins of external address bus
5 to 12	P30 to P37	F	General purpose I/O port pins
	SEG08 to SEG15		SEG output pins for LCDC
	A08 to A15		Bits 08 to 15 pins of external address bus
13 to 15	P10 to P12	G	General purpose I/O port pins
	SEG16 to SEG18		SEG output pins for LCDC
	D08 to D10		Bits 08 to 10 pins of external data bus
16	X0A	B	Sub clock (oscillation) input
17	X1A	B	Sub clock (oscillation) output
18	V_{CC}	—	Power supply pins
19	V_{SS}	—	GND pins
20	$V_{CC}3C$	—	Capacitor connection pin for internal regulator
21 to 25	P13 to P17	G	General purpose I/O port pins
	SEG19 to SEG23		SEG output pins for LCDC
	D11 to D15		Bits 11 to 15 pins of external data bus
26 to 31	P00 to P05	G	General purpose I/O port pins
	SEG24 to SEG29		SEG output pins for LCDC
	INT0 to INT5		External interrupt input pins
	D00 to D05		Bits 00 to 05 pins of external data bus
32	P06	G	General purpose I/O port pin
	SEG30		SEG output pins for LCDC
	D06		Bit 06 pin of external data bus
33	P07	G	General purpose I/O port pin
	SEG31		SEG output pin for LCDC
	$\overline{ATG}$		External trigger input pin at using of A/D converter
	D07		Bit 07 pin of external data bus
34	P70	I	General purpose I/O port pin
	INT6		External interrupt input pin
	RX0		RX0 input pin of CAN0
35	P71	I	General purpose I/O port pin
	TX0		TX0 output pin of CAN0

(Continued)

Pin no.	Pin name	I/O circuit type*	Function
36	P72	I	General purpose I/O port pin
	INT7		External interrupt input pin
	RX1		RX1 input pin of CAN1
37	P73	I	General purpose I/O port pin
	TX1		TX1 output pin of CAN1
38	DV_{CC}	—	Power supply input pins for SMC
39	DV_{SS}	—	GND pins for SMC
40	PB0	H	General purpose I/O port pin
	PWM1P0		PWM output pin of stepping motor controller
41	PB1	H	General purpose I/O port pin
	PWM1M0		PWM output pin of stepping motor controller
42	PB2	H	General purpose I/O port pin
	PWM2P0		PWM output pin of stepping motor controller
43	PB3	H	General purpose I/O port pin
	PWM2M0		PWM output pin of stepping motor controller
44	PB4	H	General purpose I/O port pin
	PWM1P1		PWM output pin of stepping motor controller
45	PB5	H	General purpose I/O port pin
	PWM1M1		PWM output pin of stepping motor controller
46	PB6	H	General purpose I/O port pin
	PWM2P1		PWM output pin of stepping motor controller
47	PB7	H	General purpose I/O port pin
	PWM2M1		PWM output pin of stepping motor controller
48	PC0	H	General purpose I/O port pin
	PWM1P2		PWM output pin of stepping motor controller
49	PC1	H	General purpose I/O port pin
	PWM1M2		PWM output pin of stepping motor controller
50	PC2	H	General purpose I/O port pin
	PWM2P2		PWM output pin of stepping motor controller
51	PC3	H	General purpose I/O port pin
	PWM2M2		PWM output pin of stepping motor controller
52	DV_{CC}	—	Power supply input pins for SMC
53	DV_{SS}	—	GND pins for SMC

(Continued)

Pin no.	Pin name	I/O circuit type*	Function
54 to 61	P97 to P90	E	General-purpose I/O port pins : Valid when analog input is prohibited
	AN31 to AN24		Analog input pins of A/D converter : Valid when ADER register is set to analog input
62 to 69	P87 to P80	E	General-purpose I/O port pins : Valid when analog input is prohibited
	AN23 to AN16		Analog input pins of A/D converter : Valid when ADER register is set to analog input
70	AV_{CC}	—	Analog power supply input pin for A/D converter
71	AVRH	—	Analog base voltage input pin for A/D converter
72	AV_{SS}/AVRL	—	Analog GND/analog base low voltage input pin for A/D converter
73 to 80	P60 to P67	E	General-purpose I/O port pins : Valid when analog input is prohibited
	AN0 to AN7		Analog input pins of A/D converter : Valid when ADER register is set to analog input
81 to 88	PF0 to PF7	E	General-purpose I/O port pins : Valid when analog input is prohibited
	AN8 to AN15		Analog input pins of A/D converter : Valid when ADER register is set to analog input
89	DV_{CC}	—	Power supply input pins for SMC
90	DV_{SS}	—	GND pins for SMC
91	PA0	H	General purpose I/O port pin
	PWM1P3		PWM output pin of stepping motor controller
92	PA1	H	General purpose I/O port pin
	PWM1M3		PWM output pin of stepping motor controller
93	PA2	H	General purpose I/O port pin
	PWM2P3		PWM output pin of stepping motor controller
94	PA3	H	General purpose I/O port pin
	PWM2M3		PWM output pin of stepping motor controller
95	PE0	H	General purpose I/O port pin
	PWM1P4		PWM output pin of stepping motor controller
96	PE1	H	General purpose I/O port pin
	PWM1M4		PWM output pin of stepping motor controller
97	PE2	H	General purpose I/O port pin
	PWM2P4		PWM output pin of stepping motor controller
98	PE3	H	General purpose I/O port pin
	PWM2M4		PWM output pin of stepping motor controller

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Pin no.	Pin name	I/O circuit type*	Function
99	PE4	H	General purpose I/O port pin
	PWM1P5		PWM output pin of stepping motor controller
100	PE5	H	General purpose I/O port pin
	PWM1M5		PWM output pin of stepping motor controller
101	PE6	H	General purpose I/O port pin
	PWM2P5		PWM output pin of stepping motor controller
102	PE7	H	General purpose I/O port pin
	PWM2M5		PWM output pin of stepping motor controller
103	DV_{CC}	—	Power supply input pins for SMC
104	DV_{SS}	—	GND pins for SMC
105	MOD2	D	Mode pin 2 : Used to set basic operating mode and required to be connected to V_{CC} or V_{SS}
106	MOD1	D	Mode pin 1 : Used to set basic operating mode and required to be connected to V_{CC} or V_{SS}
107	MOD0	D	Mode pin 0 : Used to set basic operating mode and required to be connected to V_{CC} or V_{SS}
108	$\overline{INIT}$	C	External reset input pin
109	P40	I	General-purpose I/O port pin : Valid when UART0 data input is prohibited
	SIN0		UART0 serial data input pin, requiring output by ports to be stopped while UART0 is performing input operation, except when executed intentionally, as this input is always in use
110	P41	I	General-purpose I/O port pin : Valid when UART0 data output is prohibited
	SOT0		UART0 serial data output pin : Valid when UART0 data output is permitted
111	P42	I	General-purpose I/O port pin : Valid when clock output of UART0 is prohibited
	SCK0		UART0 clock input and output pin for serial communication : Valid when clock output of UART0 is permitted
112	P43	I	General-purpose I/O port pin : Valid when LIN-UART0 data input is prohibited
	SIN3		LIN-UART0 serial data input pin, requiring output by ports to be stopped while LIN-UART0 is performing input operation, except when executed intentionally, as this input is always in use
113	P44	I	General-purpose I/O port pin : Valid when LIN-UART0 data output is prohibited
	SOT3		LIN-UART0 serial data output pin : Valid when data output of LIN-UART0 is permitted

(Continued)

Pin no.	Pin name	I/O circuit type*	Function
114	P45	I	General-purpose I/O port pin : Valid when clock output of LIN-UART0 is prohibited
	SCK3		LIN-UART0 clock input and output pin for serial communication : Valid when clock output of LIN-UART0 is permitted
115	P50	I	General-purpose I/O port pin
	SIN4		Serial data input pin of LIN-UART1 : LIN-UART1, requiring output by ports to be stopped while LIN-UART1 is performing input operation, except when executed intentionally, as this input is always in use
	CK0		External clock input pin of free-run timer 0
	$\overline{CS0}$		Output pin of chip select 0 : Valid when external bus mode is selected
116	P51	I	General-purpose I/O port pin
	SOT4		LIN-UART1 serial data output pin : Valid when data output of LIN-UART1 is permitted
	$\overline{CS1}$		Output pin of chip select 1 : Valid when output of chip select 1 is permitted
117	P52	I	General-purpose I/O port pin
	SCK4		LIN-UART1 clock input and output pin for serial communication : Valid when clock output of LIN-UART1 is permitted
	$\overline{CS2}$		Output pin of chip select 2 : Valid when output of chip select 2 is permitted
118	P53	I	General-purpose I/O port pin
	SIN5		Serial data input pin of LIN-UART2 : LIN-UART2, requiring output by ports to be stopped while LIN-UART2 is performing input operation, except when executed intentionally, as this input is always in use
	CK1		External clock input pin of free-run timer 1
	$\overline{CS3}$		Output of chip select 3 : Valid when output of chip select 3 is permitted
119	P54	I	General-purpose I/O port pin
	SOT5		Serial data output pin of LIN-UART2 : Valid when data output of LIN-UART2 is permitted
	$\overline{RD}$		Read strobe output pin of external bus : Valid when external bus mode is selected
120	P55	I	General-purpose I/O port pin
	SCK5		LIN-UART2 clock input and output pin for serial communication : Valid when clock output of LIN-UART2 is permitted
	$\overline{WR0}$		Write strobe output pin of external bus : Valid when $\overline{WR0}$ output is permitted in external bus mode

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Pin no.	Pin name	I/O circuit type*	Function
121	P56	I	General-purpose I/O port pin
	OUT0		Output compare output pin
	$\overline{WR1}$		Write strobe output pin of external bus : Valid when $\overline{WR1}$ output is permitted in external bus mode
122	P57	J	General-purpose I/O port pin
	OUT1		Output compare output pin
	RDY		External ready input pin : Valid when external ready input is permitted
123	P46	I	General-purpose I/O port pin
	SGA		Sound generator pin
	$\overline{AS}$		External address strobe output pin : Valid when address strobe output is permitted
124	P47	I	General-purpose I/O port pin
	SGO		Sound generator pin
	SYSCLK		System clock output pin : Valid when system clock output is permitted and outputs the same clock as the operating frequency of external bus (Output is stopped in STOP mode)
125	PG0	I	General-purpose I/O port pin
	PPG0		Output of PPG timer 0 : Valid when output of PPG timer 0 is permitted
126	V_{CC}	—	Power supply pins
127	V_{SS}	—	GND pins
128	X1	A	Main clock (oscillation) output pin
129	X0	A	Main clock (oscillation) input pin
130	PG1	I	General-purpose I/O port pin
	TOT0		Output pin for reload timer
	PPG2		Output pin of PPG timer 2 : Valid when output of PPG timer 2 is permitted
131	PG2	I	General-purpose I/O port pin
	TOT1		Output pin for reload timer
	PPG4		Output pin of PPG timer 4 : Valid when output of PPG timer 4 is permitted
132	PG3	I	General-purpose I/O port pin
	TOT2		Output pin for reload timer
	PPG6		Output pin of PPG timer 6 : Valid when output of PPG timer 6 is permitted

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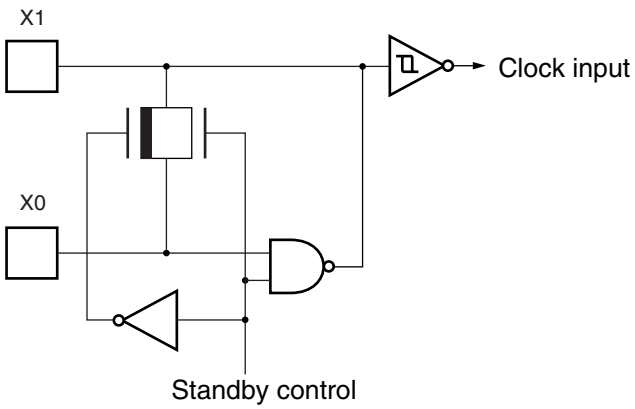
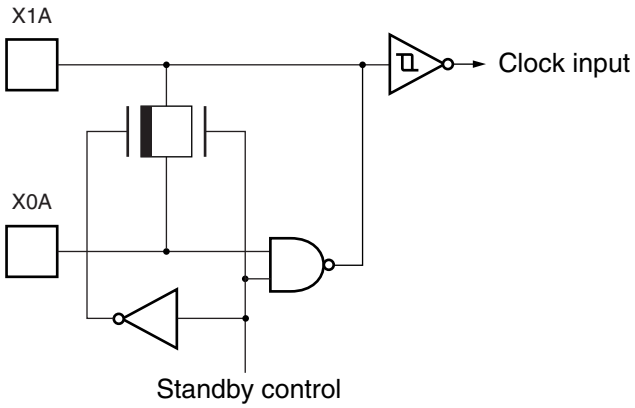
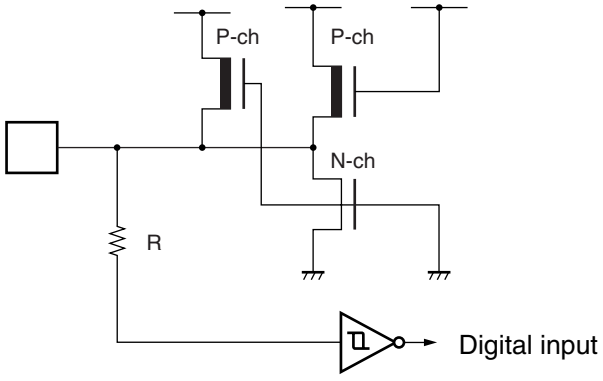
Pin no.	Pin name	I/O circuit type*	Function
133	PD0	K	General-purpose I/O port pin
	TIN0		Event input pin for reload timer
	IN0		Trigger input pin of input capture 0 : This sets input capture to trigger input and is enabled when input port is set up. When set as input capture input, it requires output by ports to be stopped, except when executed intentionally, as this input is always used.
	PWC0		Input pin of pulse width counter 0 of PWC0 : Valid when input of pulse width counter 0 of PWC0 is permitted
134	PD1	K	General-purpose I/O port pin
	TIN1		Event input pin for reload timer
	IN1		Trigger input pin of input capture 1 : This sets input capture to trigger input and is enabled when input port is set up. When set as input capture input, it requires output by ports to be stopped, except when executed intentionally, as this input is always used.
135	PD2	K	General-purpose I/O port pin
	TIN2		Event input pin for reload timer
	IN2		Trigger input pin of input capture 2 : This sets input capture to trigger input and is enabled when input port is set up. When set as input capture input, it requires output by ports to be stopped, except when executed intentionally, as this input is always used.
136	PD3	K	General-purpose I/O port pin
	IN3		Trigger input pin of input capture 3 : This sets input capture to trigger input and is enabled when input port is set up. When set as input capture input, it requires output by ports to be stopped, except when executed intentionally, as this input is always used.
137 to 140	PD4 to PD7	F	General-purpose I/O port pin
	COM0 to COM3		Output pin of COM0 to COM3 of LCDC
	PPG1, PPG3, PPG5, PPG7		Output pin of PPG timer 1, 3, 5 and 7 : Valid when output of PPG timer 1, 3, 5 and 7 is permitted
141 to 144	P20 to P23	F	General purpose I/O port pins
	SEG00 to SEG03		SEG output pins for LCDC
	A00 to A03		Bits 00 to 03 pins of external address bus

* : For information about the I/O circuit type, refer to “■ I/O CIRCUIT TYPE”.

■ I/O CIRCUIT TYPE

Group	Circuit Type	Remarks
A		For high speed (source oscillation of main clock) • Oscillation circuit • Feedback resistance X0 : approx. 1 MΩ
B		For low speed (source oscillation of sub clock) • Oscillation circuit • Feedback resistance X0A : approx. 7 MΩ
C		• CMOS hysteresis input • Pull-up resistor provided • No standby control

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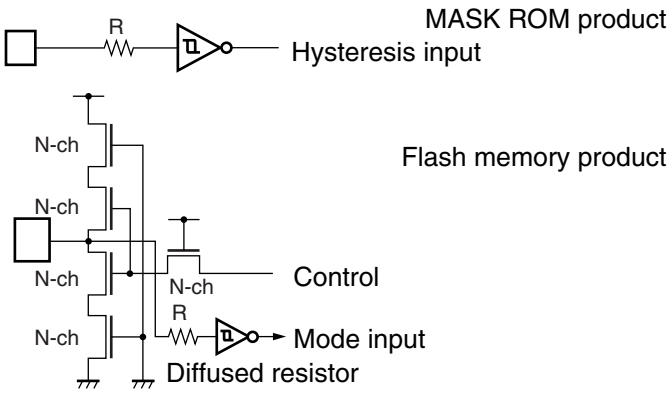
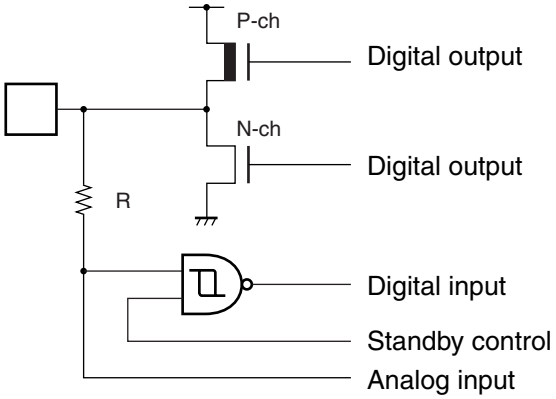
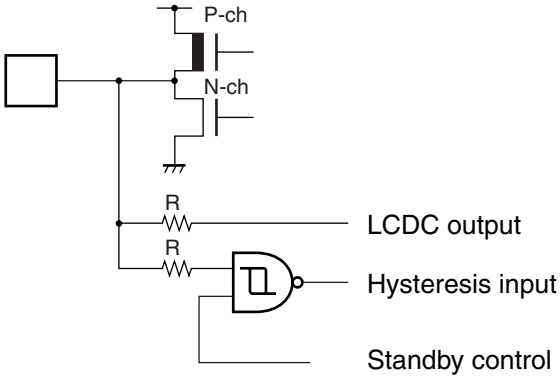
Group	Circuit Type	Remarks
D		• MASK ROM product Hysteresis input Pull-down resistor provided only for MOD2 & MOD1 • Flash memory product Hysteresis input High-voltage control for Flash test provided
E		• CMOS output (4 mA) • Hysteresis (Automotive level) input (Standby control provided) • Analog input (Analog input is valid when the corresponding ADER bit is set to 1.)
F		• CMOS output (4 mA) • LCDC output • Hysteresis (Automotive level) input (Standby control provided)

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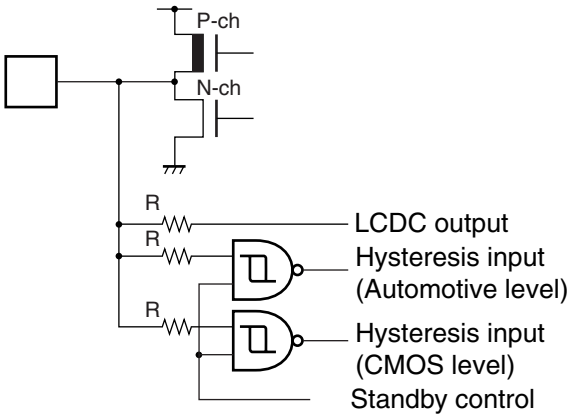
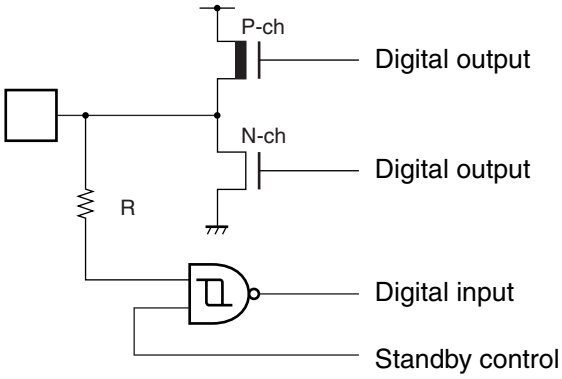
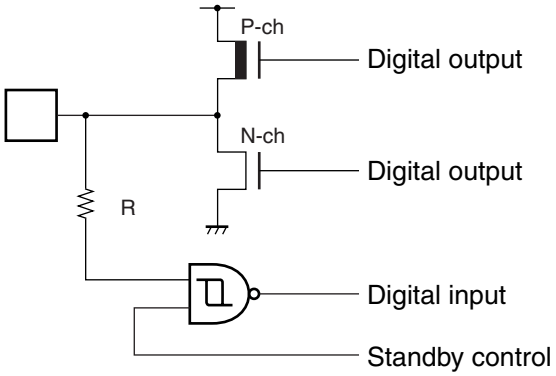
Group	Circuit Type	Remarks
G		• CMOS output (4 mA) • LCDC output • Hysteresis (Automotive level) input (Standby control provided) • Hysteresis (CMOS level) input (Standby control provided)
H		• CMOS output High current output for PWM (30 mA) • Hysteresis (Automotive level) input (Standby control provided)
I		• CMOS output (4 mA) • Hysteresis (Automotive level) input (Standby control provided)

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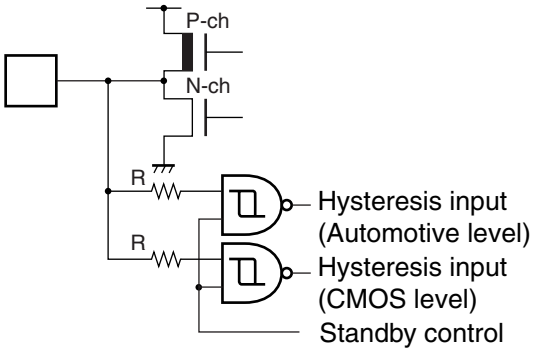
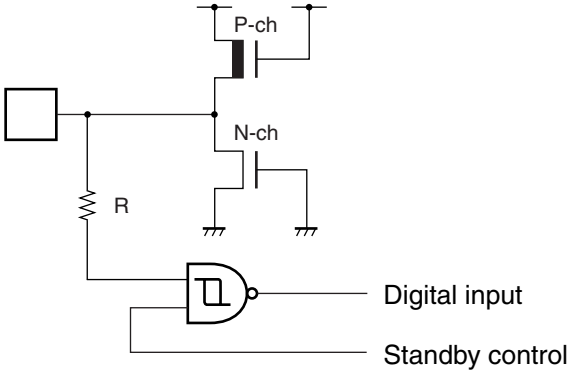
Group	Circuit Type	Remarks
J		• CMOS output (4 mA) • Hysteresis (Automotive level) input (Standby control provided) • Hysteresis (CMOS level) input (Standby control provided)
K		• Hysteresis (Automotive level) input (Standby control provided)

■ HANDLING DEVICES

• Preventing Latch-up

Latch-up may occur in a CMOS IC, if a voltage greater than V_{CC} pin or less than V_{SS} pin is applied to input and output pin, or if an above-rating voltage is applied between V_{CC} and V_{SS}. When latch-up occurs, it may significantly increase the power supply current, and may cause thermal destruction of an element. When you use a CMOS IC, be very careful not to exceed the maximum rating.

• Treatment of Unused Input Pins

Do not leave an unused input pin open, since it may cause a malfunction. Handle by performing a pull-up or pull-down with a resistance of 2 kΩ or more. An unused I/O pin should be set to the output status and left open. When set to the input status, it should be handled in the same way as an input pin.

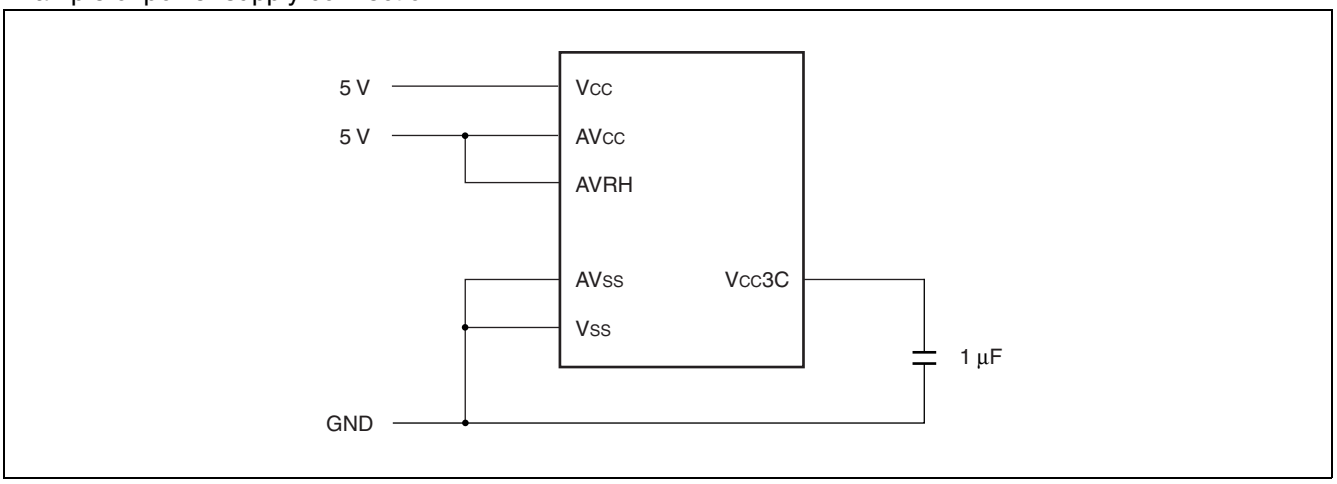
• About power supply pins

If there are multiple V_{CC} and V_{SS} pins, from the point of view of device design pins to be of the same potential are connected inside the device to prevent such malfunctioning as latch-up. However, you must connect all the pins to external power supply and a ground line to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating. Moreover, connect the current supply source with the V_{CC} and V_{SS} pins of this device at the low impedance.

Furthermore, it is also advisable to connect a ceramic bypass capacitor of approximately 0.1 µF between V_{CC} and V_{SS} near this device.

This device incorporates a regulator. When using the device with 5V power supply, apply that power supply to the V_{CC} pin and always connect a 1 µF or greater capacitor to the $V_{CC}3C$ for the regulator.

Example of power supply connection



- Crystal oscillator circuit

  Noise near the X0/X1 pins and X0A/X1A pins may cause the device to malfunction. Design the PC board such that X0/X1 pins, X0A/X1A pins, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to the ground are placed as near one another as possible. When routing the X0 and X1 signals, they should be shielded for use on the board. Caution must be taken especially when using a pin next to the X0.

  It is strongly recommended to design the PC board artwork with the X0, X1, X0A and X1A pins surrounded by ground plane because stable operation can be expected with such a layout.

  In addition, a sub clock is required even when a dual clock product is used as a single clock product.

  When using MB91F248S/248S/247S, connect the X0A pin to GND and leave the X1A pin open.

  Please ask the crystal maker to evaluate the oscillational characteristics of the crystal and this device.

- Mode pins (MOD0 to MOD2)

  These pins should be connected directly to V_{CC} or V_{SS} pins. To prevent the device erroneously switching to test mode due to noise, design the PC board such that the distance between the mode pins and V_{CC} or V_{SS} pins is as short as possible and the connection impedance is now.

- Operation at start-up

  Always use the $\overline{INIT}$ pin to perform a setting initialization reset (INIT) after power-on. Immediately after power-on, hold the low level input to the $\overline{INIT}$ pin for the stabilization wait time required for the oscillator circuit, to take the oscillation stabilization wait time for the oscillator circuit.

  For INIT via the $\overline{INIT}$ pin, the oscillation stabilization wait time setting is initialized to the minimum value.

- Source oscillation input upon power-on

  When power-on, always input the clock for the duration of the oscillation stabilization delay time.

- Treatment of power supply pins on A/D converter

  Connect to ensure “AV_{CC} = AVRH = V_{CC} and AV_{SS} = V_{SS}” even if the A/D converter is not in use.

- Power-on sequence for power supply analog input of A/D converter

  Always supply power to the A/D converter (AV_{CC} and AVRH) and apply analog input (AN0 to AN 31) after turning on the digital power supply (V_{CC}). Also, turn off the power supply for the A/D converter and analog input before turning off the digital power supply (V_{CC}). In so doing, the power supply must be turn on and off so that AVRH does not exceed AV_{CC}. Even when using a pin shared with analog input as an input port, ensure that the input voltage does not exceed AV_{CC} (There is no problem in turning on or off the analog and digital power supplies at the same time).

- Handling of power supply for high-current output buffer pin (DV_{CC}, DV_{SS})

  Always apply power to high-current output buffer pins (DV_{CC}) after turning on the digital power supply (V_{CC}). In addition, turn off the power supply for the high-current output buffer pins before turning off the digital power supply (V_{CC}).

  Apply the same power as for high-current output buffer pins even when using such pins as general-purpose ports. (There is no problem in turning on or off the power supply for the high-current output buffer pins and the digital power supply at the same time.)

  Always use the GND pin (DV_{SS}) for the high-current output buffer pin at the same potential as the digital GND (V_{SS}).

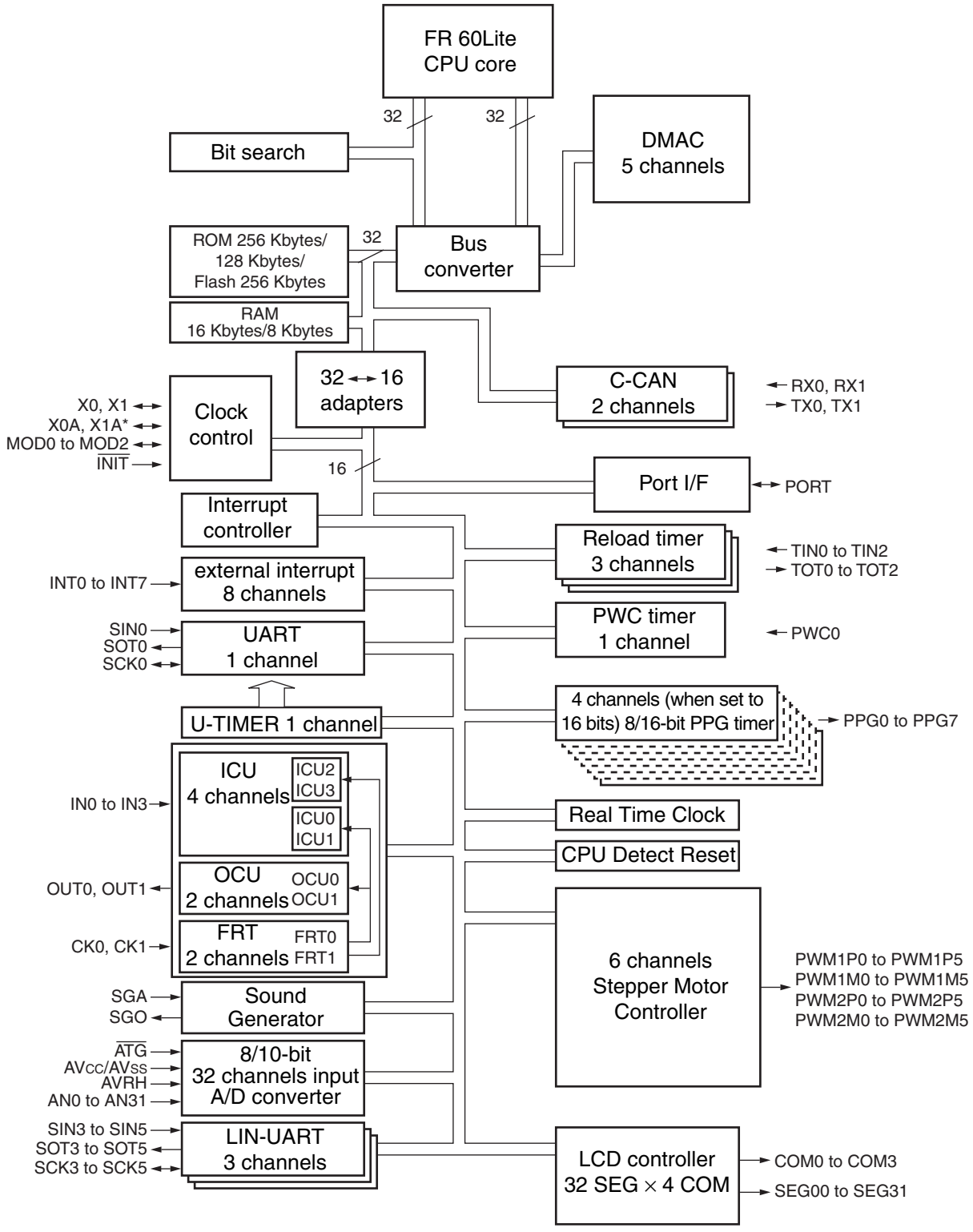
- About switching from main clock mode to sub clock mode or stop mode

  Always stop the main clock after switching the main clock mode to the sub clock mode or stop mode. Also secure the oscillation stabilization wait time when returning from the sub clock mode or stop mode to the main clock mode.

- About Flash write

  Note that Flash write is not possible in the sub mode.

■ BLOCK DIAGRAM



* : The sub clock is not supported in single clock products.

■ MEMORY SPACE

• Memory space

The FR family has of 4 Gbytes logical address space (2^{32} addresses) linearly accessible to the CPU space.

• Direct addressing area

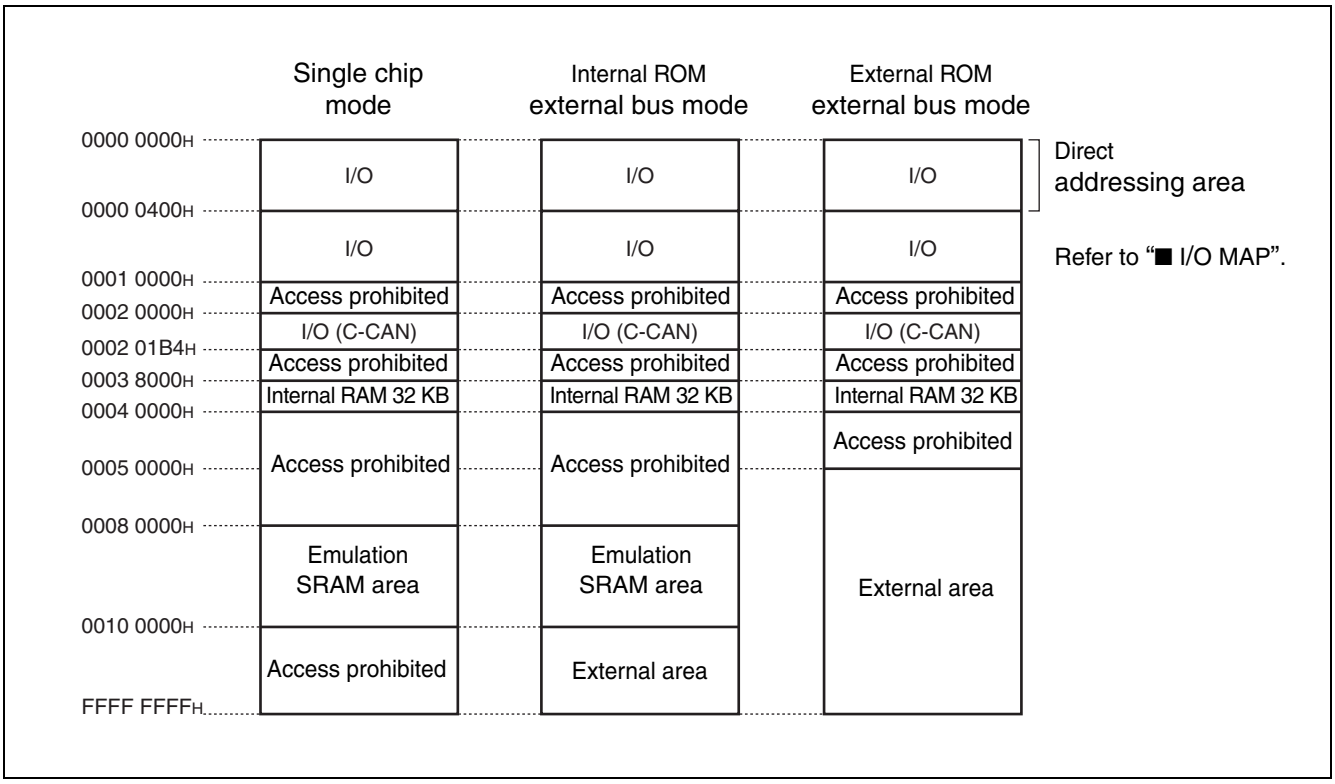
The following address space areas are used as I/O areas.

These areas are called direct addressing areas, in which the address of an operand can be specified directly during on instruction.

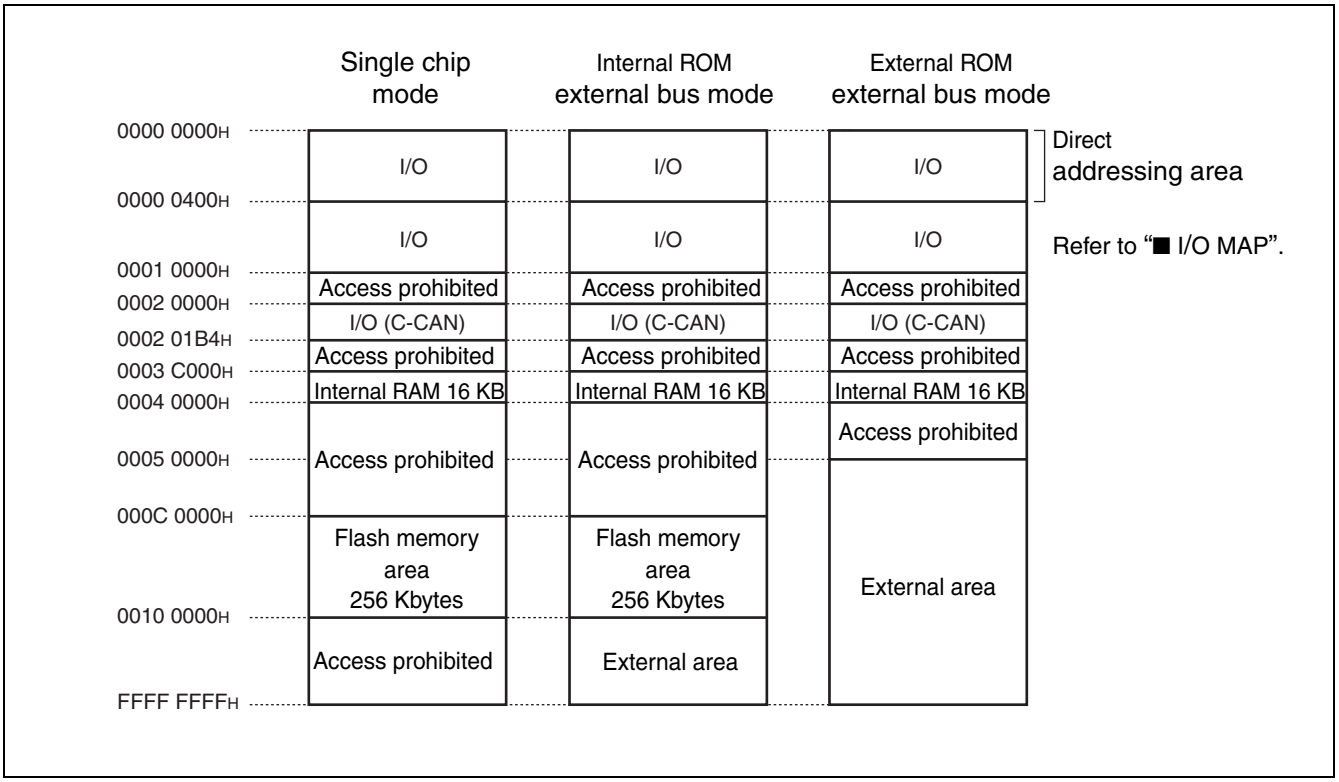
The direct area varies depending on the size of data to be accessed as follows.
→ Byte data access : 000_H to $0FF_H$
→ Halfword data access : 000_H to $1FF_H$
→ Word data access : 000_H to $3FF_H$

■ MEMORY MAP

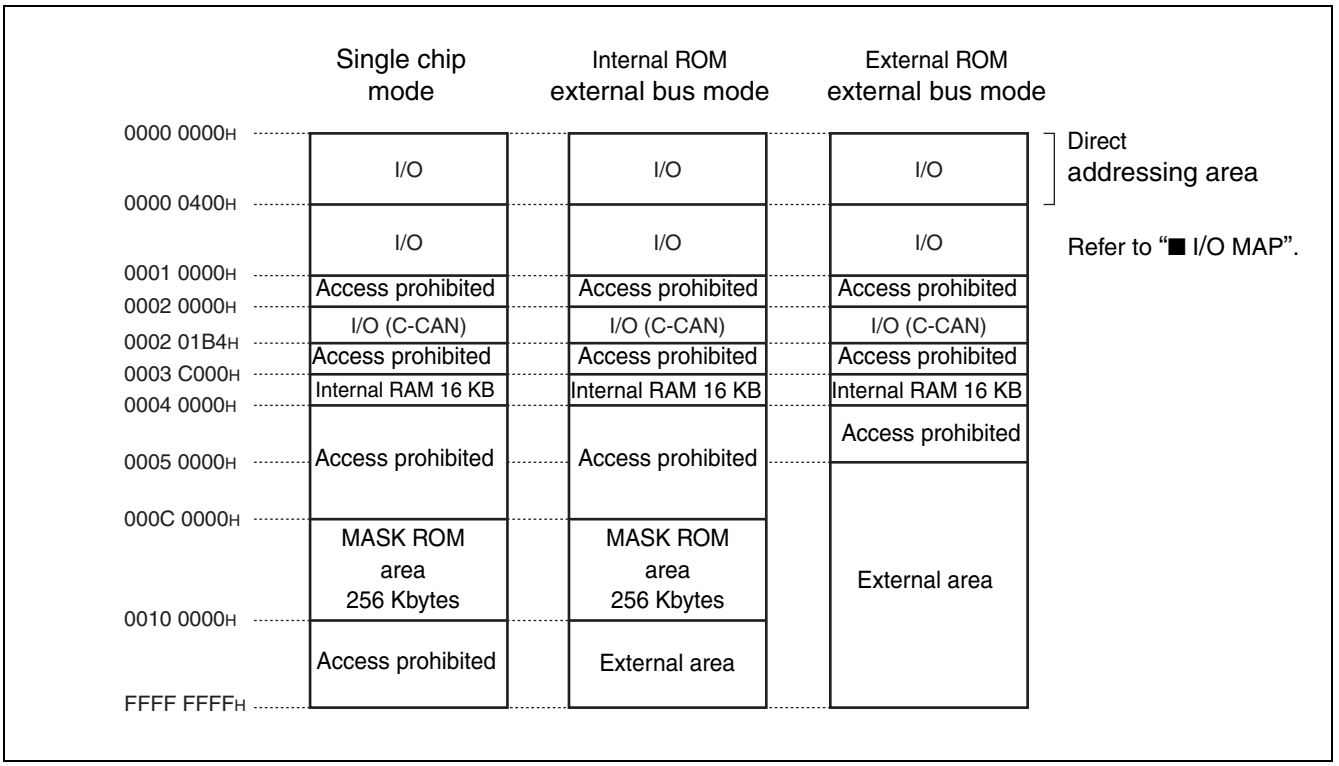
MB91V245A



MB91F248/S

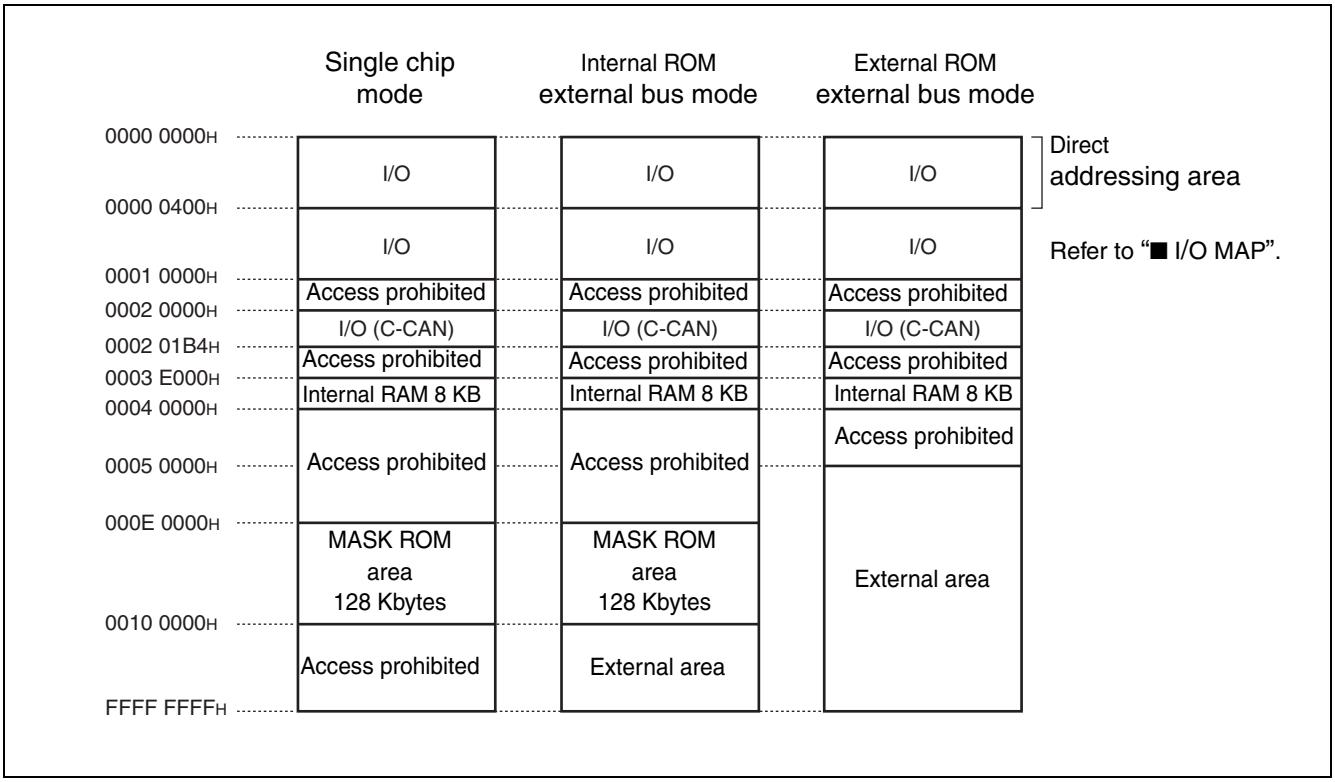


MB91248/S



Note : Each mode is set depending on the mode vector fetch after $\overline{\text{INIT}}$ is negated (For mode settings, refer to "■ MODE SETTINGS").

MB91247/S



Note : Each mode is set depending on the mode vector fetch after $\overline{\text{INIT}}$ is negated (For mode settings, refer to "■ MODE SETTINGS").

■ MODE SETTINGS

The FR family, sets the operation mode using mode pins (MOD2 to MOD0) and mode data.

• Mode pins

The mode pins (MOD2 to MOD0) specify how the mode vector fetch and reset vector fetch is performed.

Other settings than these in the table are prohibited.

Mode pin			Mode name	Reset vector access area
MOD2	MOD1	MOD0		
0	0	0	Internal ROM mode vector	Internal
0	0	1	External ROM mode vector	External

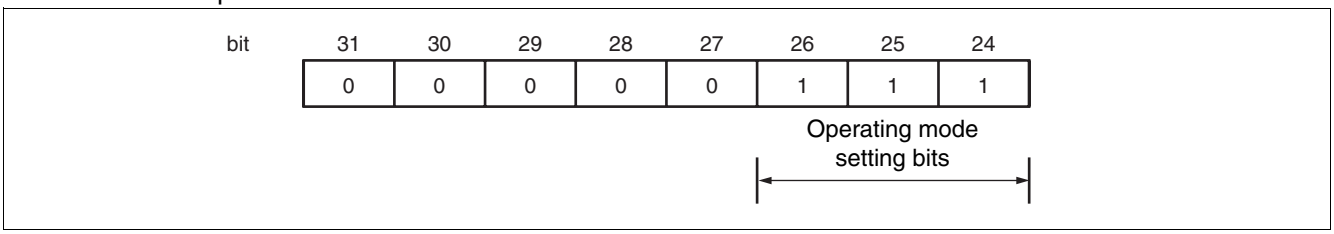
• Mode data

Data written to the internal mode register (MODR) by mode vector fetch is called mode data.

After an operating mode has been set in the mode register the device operates in that operating mode.

The mode data is set by all reset sources. User programs cannot set data to the mode register.

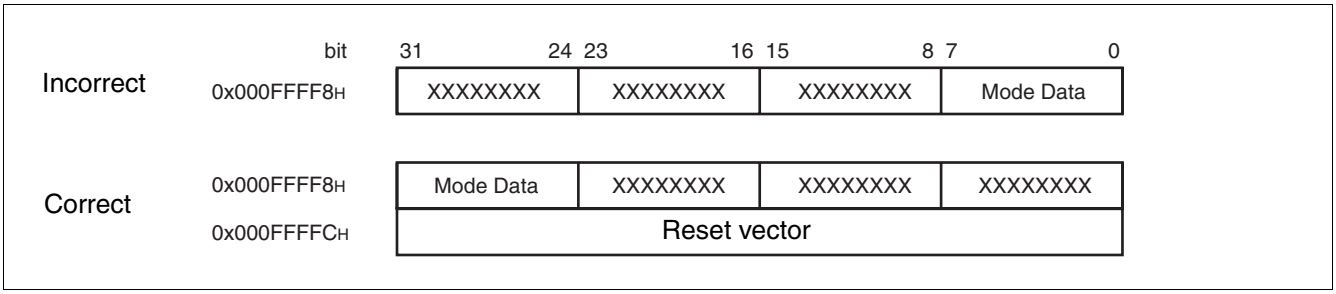
Detailed description of mode data



Bit 31 to bit 24 are reserved.

Always set the value to “00000111$_B$”. Normal operation is not guaranteed when a value other than “00000111$_B$” is set.

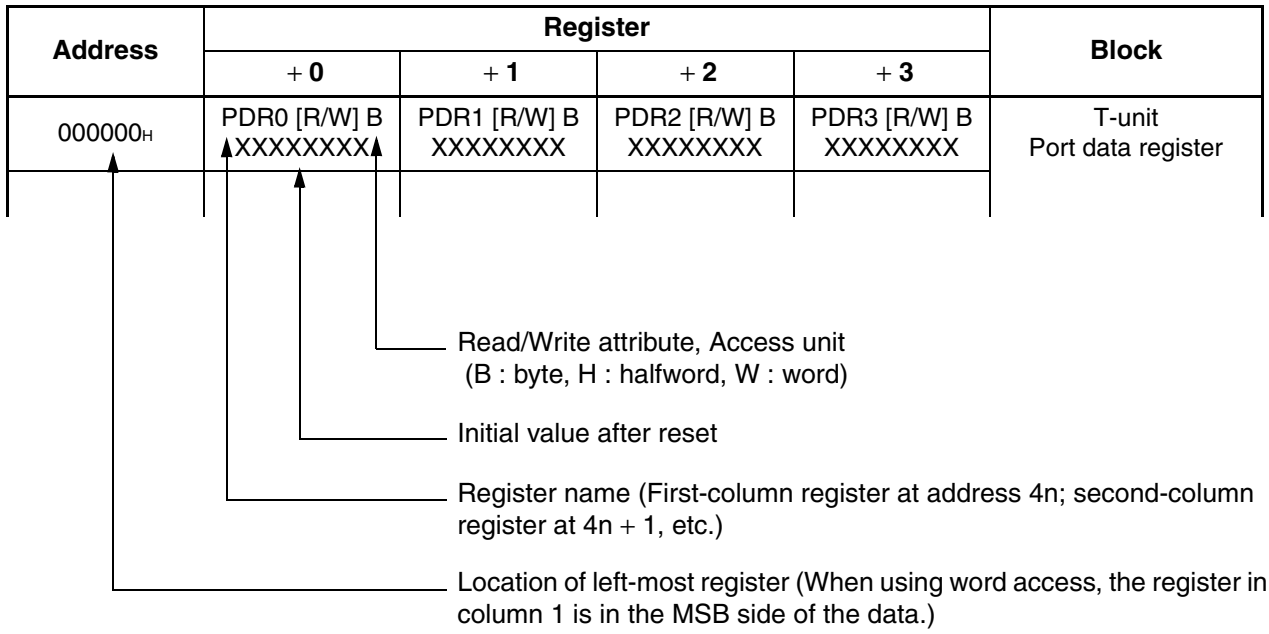
Note : Mode data set in the mode vector must be placed as byte data at 0x000FFFF8$_H$.
Place the data in the most significant byte from bit 31 to bit 24 as the FR family uses the big endian system for byte endian.



■ I/O MAP

The following table shows the correspondence between the memory space area and each register of the peripheral resource.

[How to read the map]



Note :

Initial values of register bits are represented as follows :

“ 1 ” : Initial value “1”

“ 0 ” : Initial value “0”

“ X ” : Initial value “undefined”

“ - ” : No physical register present at this location

Access by any undescribed data access attribute is prohibited.

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
00000000H	PDR0 [R/W] B, H XXXXXXXX	PDR1 [R/W] B, H XXXXXXXX	PDR2 [R/W] B, H 00000000	PDR3 [R/W] B, H XXXX0000	Port Data Register
00000004H	PDR4 [R/W] B, H XXXXXXXX	PDR5 [R/W] B, H XXXXXXXX	PDR6 [R/W] B, H XXXXXXXX	PDR7 [R/W] B, H ----XXXX	
00000008H	PDR8 [R/W] B, H XXXXXXXX	PDR9 [R/W] B, H XXXXXXXX	PDRA [R/W] B, H ----XXXX	PDRB [R/W] B, H XXXXXXXX	
0000000CH	PDRC [R/W] B, H ----XXXX	PDRD [R/W] B, H 0000XXXX	PDRE [R/W] B, H XXXXXXXX	PDRF [R/W] B, H XXXXXXXX	
00000010H	PDRG [R/W] B, H ----XXXX	—			
00000014H to 0000003CH	—				Reserved
00000040H	EIRR0 [R/W] B, H, W 00000000	ENIR0 [R/W] B, H, W 00000000	ELVR0 [R/W] B, H, W 00000000 00000000		External Interrupt Control (INT0 to INT7)
00000044H	DICR [R/W] B, H, W -------0	HRCL [R/W] B 0--11111	—		Delay Interrupt Module
00000048H	TMRLR0 [W] H, W XXXXXXXX XXXXXXXX		TMR0 [R] H, W XXXXXXXX XXXXXXXX		Reload Timer 0
0000004CH	—	00001000	TMCSR0 [R/W] B, H, W ----0000 00000000		
00000050H	TMRLR1 [W] H, W XXXXXXXX XXXXXXXX		TMR1 [R] H, W XXXXXXXX XXXXXXXX		Reload Timer 1
00000054H	—		TMCSR1 [R/W] B, H, W ----0000 00000000		
00000058H	TMRLR2 [W] H, W XXXXXXXX XXXXXXXX		TMR2 [R] H, W XXXXXXXX XXXXXXXX		Reload Timer 2
0000005CH	—		TMCSR2 [R/W] B, H, W ----0000 00000000		
00000060H	SSR [R/W] B, H, W 00001000	SIDR [R/W] B, H, W XXXXXXXX	SCR [R/W] B, H, W 00000100	SMR [R/W] B, H, W 00--0-0-	UART0
00000064H	UTIM [R] H (UTIMR [W] H) 00000000 00000000		DRCL [W] B --------	UTIMC [R/W] B 0--00001	U-TIMER0
00000068H to 0000008CH	—				Reserved
00000090H	—	SGDBL [R/W] B -------0	SGCR [R/W] B, H, W 0-----00 000--000		Sound Generator
00000094H	SGAR [R/W] B, H, W 00000000	SGFR [R/W] B, H, W XXXXXXXX	SGTR [R/W] B, H, W XXXXXXXX	SGDR [R/W] B, H, W XXXXXXXX	

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
00000098H	LCDCMR [R/W] B, H, W ----0000	—	LCR0 [R/W] B, H, W 00010000	LCR1 [R/W] B, H, W 00000000	LCD Controller Driver
0000009CH	VRAM0 [R/W] B, H, W XXXXXXXX	VRAM1 [R/W] B, H, W XXXXXXXX	VRAM2 [R/W] B, H, W XXXXXXXX	VRAM3 [R/W] B, H, W XXXXXXXX	
000000A0H	VRAM4 [R/W] B, H, W XXXXXXXX	VRAM5 [R/W] B, H, W XXXXXXXX	VRAM6 [R/W] B, H, W XXXXXXXX	VRAM7 [R/W] B, H, W XXXXXXXX	
000000A4H	VRAM8 [R/W] B, H, W XXXXXXXX	VRAM9 [R/W] B, H, W XXXXXXXX	VRAM10 [R/W] B, H, W XXXXXXXX	VRAM11 [R/W] B, H, W XXXXXXXX	
000000A8H	VRAM12 [R/W] B, H, W XXXXXXXX	VRAM13 [R/W] B, H, W XXXXXXXX	VRAM14 [R/W] B, H, W XXXXXXXX	VRAM15 [R/W] B, H, W XXXXXXXX	
000000A8H to 000000AFH	—				Reserved
000000B0H	SCR3 [R/W] B, H, W 00000000	SMR3 [R/W] B, H, W 00000000	SSR3 [R/W] B, H, W 00001000	RDR3/TDR3 [R/W] B, H, W --------	LIN-UART0
000000B4H	ESCR3 [R/W] B, H, W 00000X00	ECCR3 [R/W] B, H, W 000000XX	BGR13 [R/W] B, H, W XXXXXXXX	BGR03 [R/W] B, H, W XXXXXXXX	
000000B8H	SCR4 [R/W] B, H, W 00000000	SMR4 [R/W] B, H, W 00000000	SSR4 [R/W] B, H, W 00001000	RDR4/TDR4 [R/W] B, H, W --------	LIN-UART1
000000BCH	ESCR4 [R/W] B, H, W 00000X00	ECCR4 [R/W] B, H, W 000000XX	BGR14 [R/W] B, H, W XXXXXXXX	BGR04 [R/W] B, H, W XXXXXXXX	
000000C0H	SCR5 [R/W] B, H, W 00000000	SMR5 [R/W] B, H, W 00000000	SSR5 [R/W] B, H, W 00001000	RDR5/TDR5 [R/W] B, H, W --------	LIN-UART2
000000C4H	ESCR5 [R/W] B, H, W 00000X00	ECCR5 [R/W] B, H, W 000000XX	BGR15 [R/W] B, H, W XXXXXXXX	BGR05 [R/W] B, H, W XXXXXXXX	
000000C8H to 000000D0H	—				Reserved
000000D4H	TCDT0 [R/W] H, W 00000000 00000000		—	TCCS0 [R/W] B, H, W 00000000	16-bit Free Run Timer0
000000D8H	TCDT1 [R/W] H, W 00000000 00000000		—	TCCS1 [R/W] B, H, W 00000000	16-bit Free Run Timer1

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000000DCH to 000000E0H	—				Reserved
000000E4H	IPCP1 [R] H, W XXXXXXXX XXXXXXXX		IPCP0 [R] H, W XXXXXXXX XXXXXXXX		16-bit Input Capture 0, 1
000000E8H	—			ICS01 [R/W] B, H, W 00000000	
000000ECH	IPCP3 [R] H, W XXXXXXXX XXXXXXXX		IPCP2 [R] H, W XXXXXXXX XXXXXXXX		16-bit Input Capture 2, 3
000000F0H	—			ICS23 [R/W] B, H, W 00000000	
000000F4H to 00000104H	—				Reserved
00000108H	OCCP1 [R/W] H, W XXXXXXXX XXXXXXXX		OCCP0 [R/W] H, W XXXXXXXX XXXXXXXX		16-bit Output Compare
0000010CH	—				
00000110H	—		OCS01 [R/W] B, H, W 11101100 00001100		
00000114H to 0000012CH	—				Reserved
00000130H	PWCSR0 [R/W] B, H, W 0000000X 00000000		PWCR0 [R] H, W 00000000 00000000		16-bit PWC
00000134H	—				
00000138H	—	PDIVR0 [R/W] B, H, W -----000	—		
0000013CH to 00000140H	—				Reserved
00000144H	—	WTDBL [R/W] B -------0	WTCR [R/W] B, H 00000000 000-00-0		Real Time Clock
00000148H	—	WTBR [R/W] B ---XXXXX XXXXXXXX XXXXXXXX			
0000014CH	WTHR [R/W] B, H ---XXXXX	WTMR [R/W] B, H --XXXXXX	WTSR [R/W] B --XXXXXX	—	
00000150H	ADERH [R/W] B, H, W 00000000 00000000		ADERL [R/W] B, H, W 00000000 00000000		A/D Converter
00000154H	ADCS1 [R/W] B, H, W 00000000	ADCS0 [R/W] B, H, W 00000000	ADCR1 [R] B, H, W ------XX	ADCR0 [R] B, H, W XXXXXXXX	

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
00000158H	ADCT1 [R/W] B, H, W 00010000	ADCT0 [R/W] B, H, W 00101100	ADSCH [R/W] B, H, W ---00000	ADECH [R/W] B, H, W ---00000	A/D Converter
0000015CH	CUCR [R/W] B, H, W -------- ---0--00		CUTD [R/W] B, H, W 10000000 00000000		Clock Caliblator
00000160H	CUTR1 [R] B, H, W -------- 00000000		CUTR2 [R] B, H, W 00000000 00000000		
00000164H	PWC20 [R/W] B, H, W XXXXXXXX	PWC10 [R/W] B, H, W XXXXXXXX	—	Reserved	Stepping Motor Controller
00000168H	—	PWC0 [R/W] B -0000--0	PWS20 [R/W] B, H, W -0000000	PWS10 [R/W] B, H, W --000000	
0000016CH	PWC21 [R/W] B, H, W XXXXXXXX	PWC11 [R/W] B, H, W XXXXXXXX	—		
00000170H	—	PWC1 [R/W] B -0000--0	PWS21 [R/W] B, H, W -0000000	PWS11 [R/W] B, H, W --000000	
00000174H	PWC22 [R/W] B, H, W XXXXXXXX	PWC12 [R/W] B, H, W XXXXXXXX	—		
00000178H	—	PWC2 [R/W] B -0000--0	PWS22 [R/W] B, H, W -0000000	PWS12 [R/W] B, H, W --000000	
0000017CH	PWC23 [R/W] B, H, W XXXXXXXX	PWC13 [R/W] B, H, W XXXXXXXX	—		
00000180H	—	PWC3 [R/W] B -0000--0	PWS23 [R/W] B, H, W -0000000	PWS13 [R/W] B, H, W --000000	
00000184H	PWC24 [R/W] B, H, W XXXXXXXX	PWC14 [R/W] B, H, W XXXXXXXX	—		
00000188H	—	PWC4 [R/W] B -0000--0	PWS24 [R/W] B, H, W -0000000	PWS14 [R/W] B, H, W --000000	
0000018CH	PWC25 [R/W] B, H, W XXXXXXXX	PWC15 [R/W] B, H, W XXXXXXXX	—		
00000190H	—	PWC5 [R/W] B -0000--0	PWS25 [R/W] B, H, W -0000000	PWS15 [R/W] B, H, W --000000	

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
00000194H to 000001A4H	—				Reserved
000001A8H	CANPRE [R/W] B, H, W 00000000	Reserved	—		CAN Prescaler
000001ACH	—				Reserved
000001B0H	—	TRG [R/W] B, H, W 00000000	—	REVC [R/W] B, H, W 00000000	PPG0
000001B4H	PRLH0 [R/W] B, H, W XXXXXXXX	PRLL0 [R/W] B, H, W XXXXXXXX	PRLH1 [R/W] B, H, W XXXXXXXX	PRLL1 [R/W] B, H, W XXXXXXXX	
000001B8H	PRLH2 [R/W] B, H, W XXXXXXXX	PRLL2 [R/W] B, H, W XXXXXXXX	PRLH3 [R/W] B, H, W XXXXXXXX	PRLL3 [R/W] B, H, W XXXXXXXX	
000001BCH	PPGC0 [R/W] B, H, W 0000000X	PPGC1 [R/W] B, H, W 0000000X	PPGC2 [R/W] B, H, W 0000000X	PPGC3 [R/W] B, H, W 0000000X	
000001C0H	PRLH4 [R/W] B, H, W XXXXXXXX	PRLL4 [R/W] B, H, W XXXXXXXX	PRLH5 [R/W] B, H, W XXXXXXXX	PRLL5 [R/W] B, H, W XXXXXXXX	PPG0
000001C4H	PRLH6 [R/W] B, H, W XXXXXXXX	PRLL6 [R/W] B, H, W XXXXXXXX	PRLH7 [R/W] B, H, W XXXXXXXX	PRLL7 [R/W] B, H, W XXXXXXXX	
000001C8H	PPGC4 [R/W] B, H, W 0000000X	PPGC5 [R/W] B, H, W 0000000X	PPGC6 [R/W] B, H, W 0000000X	PPGC7 [R/W] B, H, W 0000000X	
000001CCH to 000001FCH	—				Reserved
00000200H	DMACA0 [R/W] B, H, W *1 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
00000204H	DMACB0 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
00000208H	DMACA1 [R/W] B, H, W *1 00000000 0000XXXX XXXXXXXX XXXXXXXX				
0000020CH	DMACB1 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
00000210H	DMACA2 [R/W] B, H, W *1 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00000214H	DMACB2 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
00000218H	DMACA3 [R/W] B, H, W *1 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
0000021CH	DMACB3 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
00000220H	DMACA4 [R/W] B, H, W *1 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00000224H	DMACB4 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
00000228H to 0000023CH	—				
00000240H	DMACR [R/W] B 0XX00000 XXXXXXXX XXXXXXXX XXXXXXXX				
00000244H to 000003ECH	—				Reserved
000003F0H	BSD0 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit Search Module
000003F4H	BSD1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000003F8H	BSDC [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000003FCH	BSRR [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00000400H	DDR0 [R/W] B, H, W 00000000	DDR1 [R/W] B, H, W 00000000	DDR2 [R/W] B, H, W 11111111	DDR3 [R/W] B, H, W 00001111	Port Direction Register
00000404H	DDR4 [R/W] B, H, W 00000000	DDR5 [R/W] B, H, W 00000000	DDR6 [R/W] B, H, W 00000000	DDR7 [R/W] B, H, W ----0000	
00000408H	DDR8 [R/W] B, H, W 00000000	DDR9 [R/W] B, H, W 00000000	DDRA [R/W] B, H, W ----0000	DDRB [R/W] B, H, W 00000000	
0000040CH	DDRC [R/W] B, H, W ----0000	DDRD [R/W] B, H, W 1111----	DDRE [R/W] B, H, W 00000000	DDRF [R/W] B, H, W 00000000	
00000410H	DDRG [R/W] B, H, W ----0000	—			
00000414H to 0000041CH	—				Reserved
00000420H	PFR0 [R/W] B, H, W 00000000	PFR1 [R/W] B, H, W 00000000	PFR2 [R/W] B, H, W 00000000	PFR3 [R/W] B, H, W 00000000	Port Function Register
00000424H	PFR4 [R/W] B, H, W 00000000	PFR5 [R/W] B, H, W 00000000	—	PFR7 [R/W] B, H, W ----0000	

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
00000428H	—		PFRA [R/W] B, H, W ----0000	PFRB [R/W] B, H, W 00000000	Port Function Register
0000042CH	PFRC [R/W] B, H, W ----0000	PFRD [R/W] B, H, W 00000000	PFRE [R/W] B, H, W 00000000	—	
00000430H	PFRG [R/W] B, H, W ----0000	—			
00000434H to 0000043CH	—				Reserved
00000440H	ICR00 [R/W] B, H, W ---11111	ICR01 [R/W] B, H, W ---11111	ICR02 [R/W] B, H, W ---11111	ICR03 [R/W] B, H, W ---11111	Interrupt Control Unit
00000444H	ICR04 [R/W] B, H, W ---11111	ICR05 [R/W] B, H, W ---11111	ICR06 [R/W] B, H, W ---11111	ICR07 [R/W] B, H, W ---11111	
00000448H	ICR08 [R/W] B, H, W ---11111	ICR09 [R/W] B, H, W ---11111	ICR10 [R/W] B, H, W ---11111	ICR11 [R/W] B, H, W ---11111	
0000044CH	ICR12 [R/W] B, H, W ---11111	ICR13 [R/W] B, H, W ---11111	ICR14 [R/W] B, H, W ---11111	ICR15 [R/W] B, H, W ---11111	
00000450H	ICR16 [R/W] B, H, W ---11111	ICR17 [R/W] B, H, W ---11111	ICR18 [R/W] B, H, W ---11111	ICR19 [R/W] B, H, W ---11111	
00000454H	ICR20 [R/W] B, H, W ---11111	ICR21 [R/W] B, H, W ---11111	ICR22 [R/W] B, H, W ---11111	ICR23 [R/W] B, H, W ---11111	
00000458H	ICR24 [R/W] B, H, W ---11111	ICR25 [R/W] B, H, W ---11111	ICR26 [R/W] B, H, W ---11111	ICR27 [R/W] B, H, W ---11111	
0000045CH	ICR28 [R/W] B, H, W ---11111	ICR29 [R/W] B, H, W ---11111	ICR30 [R/W] B, H, W ---11111	ICR31 [R/W] B, H, W ---11111	
00000460H	ICR32 [R/W] B, H, W ---11111	ICR33 [R/W] B, H, W ---11111	ICR34 [R/W] B, H, W ---11111	ICR35 [R/W] B, H, W ---11111	
00000464H	ICR36 [R/W] B, H, W ---11111	ICR37 [R/W] B, H, W ---11111	ICR38 [R/W] B, H, W ---11111	ICR39 [R/W] B, H, W ---11111	
00000468H	ICR40 [R/W] B, H, W ---11111	ICR41 [R/W] B, H, W ---11111	ICR42 [R/W] B, H, W ---11111	ICR43 [R/W] B, H, W ---11111	
0000046CH	ICR44 [R/W] B, H, W ---11111	ICR45 [R/W] B, H, W ---11111	ICR46 [R/W] B, H, W ---11111	ICR47 [R/W] B, H, W ---11111	
00000470H to 0000047CH	—				Reserved
00000480H	RSRR [R/W] B, H, W 10000000	STCR [R/W] B, H, W 00110011	TBCR [R/W] B, H, W 00XXXX11	CTBR [W] B, H, W XXXXXXXX	Clock Control Unit
00000484H	CLKR [W] B, H, W 00000000	WPR [R/W] B, H, W XXXXXXXX	DIVR0 [R/W] B, H, W 00000011	DIVR1 [R/W] B, H, W 00000000	
00000488H	—		OSCCR [R/W] B X000XXX0	—	

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000048CH	—				Clock Control Unit
00000490H	OSCR [R/W] B 000--001	—			
00000494H to 000004F8H	—				Reserved
000004FCH	PSCR [W] B XXXXXXXX	—			Port Input Level Select Register
00000500H to 0000053CH	—				Reserved
00000540H	PILR0 [R/W] B, H, W 00000000	PILR1 [R/W] B, H, W 00000000	—		Port Input Level Select Register
00000544H	—	PILR5 [R/W] B, H, W 0-------	—		
00000548H to 00000550H	—				
00000554H to 00000578H	—				Reserved
0000057CH	Reserved	LVRC [R/W] B, H, W 00011000	Reserved	Reserved	CPU Detection of operation
00000580H to 000005FCH	—				Reserved
00000600H	—		EPFR2 [R/W] B, H, W 00000000	EPFR3 [R/W] B, H, W 00000000	Extended Port Function Register
00000604H	EPFR4 [R/W] B, H, W 00000000	EPFR5 [R/W] B, H, W 00000000	—		
00000608H	—				
0000060CH	—	EPFRD [R/W] B, H, W 00000000	—		Extended Port Function Register
00000610H	EPFRG [R/W] B, H, W ----0000	—			
00000614H to 0000063CH	—				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
00000640H	ASR0 [R/W] B, H, W 00000000 00000000		ACR0 [R/W] B, H, W 1111XX00 00000000		External Bus Control Unit
00000644H	ASR1 [R/W] B, H, W XXXXXXXX XXXXXXXX		ACR1 [R/W] B, H, W XXXXXXXX XXXXXXXX		
00000648H	ASR2 [R/W] B, H, W XXXXXXXX XXXXXXXX		ACR2 [R/W] B, H, W XXXXXXXX XXXXXXXX		
0000064CH	ASR3 [R/W] B, H, W XXXXXXXX XXXXXXXX		ACR3 [R/W] B, H, W XXXXXXXX XXXXXXXX		
00000650H to 0000065CH	—				
00000660H	AWR0 [R/W] B, H, W 01110000 01011011		AWR1 [R/W] B, H, W XXXX0000 XX0X1XXX		
00000664H	AWR2 [R/W] B, H, W 0XXX0000 XX0X1XXX		AWR3 [R/W] B, H, W 0XXX0000 0X0X1XXX		
00000668H to 0000067CH	—				Reserved
00000680H	CSER [R/W] B, H, W XXXX0001	—			External Bus Control Unit
00000684H to 000007F8H	—				Reserved
000007FCH	—	MODR *2	—		Mode register
00000800H to 00000FFCH	—				Reserved
00001000H	DMASA0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
00001004H	DMADA0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00001008H	DMASA1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000100CH	DMADA1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00001010H	DMASA2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00001014H	DMADA2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00001018H	DMASA3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000101C$_H$	DMADA3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
00001020$_H$	DMASA4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00001024$_H$	DMADA4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00001028$_H$ to 00006FFC$_H$	—				Reserved
00007000$_H$	FLCR [R/W] 01XX1000	—			Flash I/F (Only Mass Production Product)
00007004$_H$	FLWC [R/W] 00000011	—			
00007008$_H$ to 0000FFFC$_H$	—				Reserved
00020000$_H$	CTRLR0		STATR0		CAN0
00020004$_H$	ERRCNT0		BTR0		
00020008$_H$	INTR0		TESTR0		
0002000C$_H$	BRPER0		—		
00020010$_H$	IF1CREQ0		IF1CMSK0		
00020014$_H$	IF1MSK20		IF1MSK10		
00020018$_H$	IF1ARB20		IF1ARB10		
0002001C$_H$	IF1MCTR0		—		
00020020$_H$	IF1DTA10		IF1DTA20		
00020024$_H$	IF1DTB10		IF1DTB20		
00020028$_H$, 0002002C$_H$	—				
00020030$_H$	Reserved (IF1 data A mirror, little endian byte ordering)				
00020034$_H$	Reserved (IF1 data B mirror, little endian byte ordering)				
00020038$_H$, 0002003C$_H$	—				
00020040$_H$	IF2CREQ0		IF2CMSK0		
00020044$_H$	IF2MSK20		IF2MSK10		
00020048$_H$	IF2ARB20		IF2ARB10		
0002004C$_H$	IF2MCTR0		—		
00020050$_H$	IF2DTA10		IF2DTA20		
00020054$_H$	IF2DTB10		IF2DTB20		

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
00020058H, 0002005CH	—				CAN0
00020060H	Reserved (IF2 data A mirror, little endian byte ordering)				
00020064H	Reserved (IF2 data B mirror, little endian byte ordering)				
00020068H, 0002007CH	—				
00020080H	TREQR20		TREQR10		
00020084H	Reserved (> 32..128 Message buffer)				
00020088H, 0002008CH	—				
00020090H	NEWDT20		NEWDT10		
00020094H	Reserved (> 32..128 Message buffer)				
00020098H, 0002009CH	—				
000200A0H	INTPEND20		INTPEND10		
000200A4H	Reserved (> 32..128 Message buffer)				
000200A8H, 000200ACH	—				
000200B0H	MESVAL20		MESVAL10		
000200B4H	Reserved (> 32..128 Message buffer)				
000200B8H, 000200FCH	—				
00020100H	CTRLR1		STATR1		CAN1
00020104H	ERRCNT1		BTR1		
00020108H	INTR1		TESTR1		
0002010CH	BRPER1		—		
00020110H	IF1CREQ1		IF1CMSK1		
00020114H	IF1MSK21		IF1MSK11		
00020118H	IF1ARB21		IF1ARB11		
0002011CH	IF1MCTR1		—		
00020120H	IF1DTA11		IF1DTA21		
00020124H	IF1DTB11		IF1DTB21		
00020128H, 0002012CH	—				
00020130H	Reserved (IF1 data A mirror, little endian byte ordering)				
00020134H	Reserved (IF1 data B mirror, little endian byte ordering)				
00020138H, 0002013CH	—				

(Continued)

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
00020140H	IF2CREQ1		IF2CMSK1		CAN1
00020144H	IF2MSK21		IF2MSK11		
00020148H	IF2ARB21		IF2ARB11		
0002014CH	IF2MCTR1		—		
00020150H	IF2DTA11		IF2DTA21		
00020154H	IF2DTB11		IF2DTB21		
00020158H, 0002015CH	—				
00020160H	Reserved (IF2 data A mirror, little endian byte ordering)				
00020164H	Reserved (IF2 data B mirror, little endian byte ordering)				
00020168H, 0002017CH	—				
00020180H	TREQR21		TREQR11		
00020184H	Reserved (> 32..128 Message buffer)				
00020188H, 0002018CH	—				
00020190H	NEWDT21		NEWDT11		
00020194H	Reserved (> 32..128 Message buffer)				
00020198H, 0002019CH	—				
000201A0H	INTPND21		INTPND11		
000201A4H	Reserved (> 32..128 Message buffer)				
000201A8H, 000201ACH	—				
000201B0H	MESVAL21		MESVAL11		
000201B4H	Reserved (> 32..128 Message buffer)				
000201B8H, 000201FCH	—				
00038000H to 003FFFFCH	—				F-bus RAM 32 Kbytes
0003C000H to 003FFFFCH	—				F-bus RAM 16 Kbytes
0003E000H to 003FFFFCH	—				F-bus RAM 8 Kbytes

*1 : The lower 16 bits (DTC [15 : 0]) of DMACA0 to DMACA4 cannot be accessed in bytes.

*2 : This register is set by a mode vector fetch and cannot be accessed by the user.

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000C0000H to 000FFFFCH	—				User ROM 256 Kbytes (Only Mass Production Product)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000E0000H to 000FFFFCH	—				User ROM 128 Kbytes (MB91247)

■ VECTOR TABLE

Interrupt source	Interrupt number		Interrupt level	Offset	TBR default address	DMA start source
	Decimal	Hexa-decimal				
Reset	0	00	—	$3FC_H$	$000FFFFC_H$	—
Mode vector	1	01	—	$3F8_H$	$000FFFF8_H$	—
System reserved	2	02	—	$3F4_H$	$000FFFF4_H$	—
System reserved	3	03	—	$3F0_H$	$000FFFF0_H$	—
System reserved	4	04	—	$3EC_H$	$000FFFEC_H$	—
System reserved	5	05	—	$3E8_H$	$000FFFE8_H$	—
System reserved	6	06	—	$3E4_H$	$000FFFE4_H$	—
Coprocessor absent trap	7	07	—	$3E0_H$	$000FFFE0_H$	—
Coprocessor error trap	8	08	—	$3DC_H$	$000FFFDC_H$	—
INTE instruction	9	09	—	$3D8_H$	$000FFFD8_H$	—
System reserved	10	0A	—	$3D4_H$	$000FFFD4_H$	—
System reserved	11	0B	—	$3D0_H$	$000FFFD0_H$	—
Step trace trap	12	0C	—	$3CC_H$	$000FFFCC_H$	—
NMI request (ICE)	13	0D	—	$3C8_H$	$000FFFC8_H$	—
Undefined instruction exception	14	0E	—	$3C4_H$	$000FFFC4_H$	—
NMI instruction	15	0F	15 (F_H) Fixed	$3C0_H$	$000FFFC0_H$	—
External interrupt 0	16	10	ICR00	$3BC_H$	$000FFFBC_H$	6
External interrupt 1	17	11	ICR01	$3B8_H$	$000FFFB8_H$	7
External interrupt 2	18	12	ICR02	$3B4_H$	$000FFFB4_H$	—
External interrupt 3	19	13	ICR03	$3B0_H$	$000FFFB0_H$	—
External interrupt 4	20	14	ICR04	$3AC_H$	$000FFFAC_H$	—
External interrupt 5	21	15	ICR05	$3A8_H$	$000FFFA8_H$	—
External interrupt 6	22	16	ICR06	$3A4_H$	$000FFFA4_H$	—
External interrupt 7	23	17	ICR07	$3A0_H$	$000FFFA0_H$	—
Reload timer 0 (Underflow)	24	18	ICR08	$39C_H$	$000FFF9C_H$	—
Reload timer 1 (Underflow)	25	19	ICR09	398_H	$000FFF98_H$	9
Reload timer 2 (Underflow)	26	1A	ICR10	394_H	$000FFF94_H$	10
UART0 (Reception completed/error)	27	1B	ICR11	390_H	$000FFF90_H$	0
UART0 (Transmission completed)	28	1C	ICR12	$38C_H$	$000FFF8C_H$	3
LIN-UART0 (Reception completed/ error, LIN Sync break, bus idle)	29	1D	ICR13	388_H	$000FFF88_H$	1

(Continued)

Interrupt source	Interrupt number		Interrupt level	Offset	TBR default address	DMA start source
	Decimal	Hexa-decimal				
LIN-UART0 (Transmission completed)	30	1E	ICR14	384_H	$000FFF84_H$	4
LIN-UART1 (Reception completed/ error, LIN Sync break, bus idle)	31	1F	ICR15	380_H	$000FFF80_H$	2
LIN-UART1 (Transmission completed)	32	20	ICR16	$37C_H$	$000FFF7C_H$	5
LIN-UART2 (Reception completed/ error, LIN Sync break, bus idle)	33	21	ICR17	378_H	$000FFF78_H$	—
LIN-UART2 (Transmission completed)	34	22	ICR18	374_H	$000FFF74_H$	—
CAN0 Reception/Transmission completed Node status transition	35	23	ICR19	370_H	$000FFF70_H$	—
CAN1 Reception/Transmission completed Node status transition	36	24	ICR20	$36C_H$	$000FFF6C_H$	—
System reserved	37	25	ICR21	368_H	$000FFF68_H$	—
System reserved	38	26	ICR22	364_H	$000FFF64_H$	—
System reserved	39	27	ICR23	360_H	$000FFF60_H$	—
PWC (Measurement completed)	40	28	ICR24	$35C_H$	$000FFF5C_H$	—
PWC (Overflow)	41	29	ICR25	358_H	$000FFF58_H$	—
DMAC transfer completed/error	42	2A	ICR26	354_H	$000FFF54_H$	—
A/D converter	43	2B	ICR27	350_H	$000FFF50_H$	14
Real-time clock Hour/minute/second overflow, corrected	44	2C	ICR28	$34C_H$	$000FFF4C_H$	—
System reserved	45	2D	ICR29	348_H	$000FFF48_H$	—
Main oscillation stabilization wait timer	46	2E	ICR30	344_H	$000FFF44_H$	—
Timebase timer overflow	47	2F	ICR31	340_H	$000FFF40_H$	—
PPG0/1 underflow	48	30	ICR32	$33C_H$	$000FFF3C_H$	—
PPG2/3 underflow	49	31	ICR33	338_H	$000FFF38_H$	—
PPG4/5 underflow	50	32	ICR34	334_H	$000FFF34_H$	—
PPG6/7 underflow	51	33	ICR35	330_H	$000FFF30_H$	—
16-bit free-run timer 0 Overflow & OCU0 Compare match clear	52	34	ICR36	$32C_H$	$000FFF2C_H$	—

(Continued)

(Continued)

Interrupt source	Interrupt number		Interrupt level	Offset	TBR default address	DMA start source
	Decimal	Hexa-decimal				
16-bit free-run timer 1 Overflow	53	35	ICR37	328_H	$000FFF28_H$	—
ICU0 (Capture)	54	36	ICR38	324_H	$000FFF24_H$	—
ICU1 (Capture)	55	37	ICR39	320_H	$000FFF20_H$	—
ICU2 (Capture)	56	38	ICR40	$31C_H$	$000FFF1C_H$	—
ICU3 (Capture)	57	39	ICR41	318_H	$000FFF18_H$	—
OCU0 (Match)	58	3A	ICR42	314_H	$000FFF14_H$	—
OCU1 (Match)	59	3B	ICR43	310_H	$000FFF10_H$	—
System reserved	60	3C	ICR44	$30C_H$	$000FFF0C_H$	—
System reserved	61	3D	ICR45	308_H	$000FFF08_H$	—
Sound generator setup count completed	62	3E	ICR46	304_H	$000FFF04_H$	—
Delay interrupt source bit	63	3F	ICR47	300_H	$000FFF00_H$	—
System reserved (Used by REALOS)	64	40	—	$2FC_H$	$000FFEFC_H$	—
System reserved (Used by REALOS)	65	41	—	$2F8_H$	$000FFEF8_H$	—
System reserved	66 to 79	42 to 4F	—	$2F4_H$ to $2C0_H$	$000FFEF4_H$ to $000FFEC0_H$	—
Used by INT instruction	80 to 255	50 to FF	—	$2BC_H$ to 000_H	$000FFEBC_H$ to $000FFC00_H$	—

■ TABLE OF PIN STATUS IN EACH MODE

• Single chip mode

Pin name	Function name	Initial value		In sleep state	In stop state	
		$\overline{INIT}$ = "L"	$\overline{INIT}$ = "H"		HIZ = 0	HIZ = 1
$\overline{INIT}$	$\overline{INIT}$	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
X0	X0				Hi-Z or input enabled	Hi-Z or input enabled
X1	X1				"H" output or input enabled	"H" output or input enabled
X0A	X0A				Hi-Z or input enabled	Hi-Z or input enabled
X1A	X1A				"H" output or input enabled	"H" output or input enabled
MOD0	MOD0				Input enabled	Input enabled
MOD1	MOD1					
MOD2	MOD2					
P00	P00/SEG24/INT0/D00	Output Hi-Z input enabled	Output Hi-Z input enabled	P : Immediately preceding status held F : Operation or output held during LCDC output; INT0 to INT5 input enabled when PFR0 register is set to "0"	P : Immediately preceding status held F : Operation or output held during LCDC output; INT0 to INT5 input enabled when PFR0 register is set to "0"	Operation or output held during LCDC output, otherwise output Hi-Z / INT0 to INT5 input enabled when PFR0 register is set to "0"
P01	P01/SEG25/INT1/D01					
P02	P02/SEG26/INT2/D02					
P03	P03/SEG27/INT3/D03					
P04	P04/SEG28/INT4/D04					
P05	P05/SEG29/INT5/D05					
P06	P06/SEG30/D06				P : Immediately preceding status held F : Operation or output held during LCDC output; Otherwise Hi-Z	Operation or output held during LCDC output; Otherwise output Hi-Z/ Input fixed to "0"
P07	P07/SEG31/$\overline{ATG}$/D07					
P10 to P17	P10 to P17/ SEG16 to SEG23/ D08 to D15					
P20 to P27	P20 to P27/ SEG00 to SEG07/ A00 to A07	"L" output	"L" output			
P30 to P33	P30 to P33/ SEG08 to SEG11/ A08 to A11					
P34 to P37	P34 to P37/ SEG12 to SEG15/ A12 to A15	Output Hi-Z input enabled	Output Hi-Z input enabled			

(Continued)

Pin name	Function name	Initial value		In sleep state	In stop state	
		$\overline{INIT}$ = "L"	$\overline{INIT}$ = "H"		HIZ = 0	HIZ = 1
P40	P40/SIN0	Output Hi-Z input enabled	Output Hi-Z input enabled	P : Immediately preceding status held F : Normal operation performed	P : Immediately preceding status held F : Output held or Hi-Z	Output Hi-Z / Input fixed to "0"
P41	P41/SOT0					
P42	P42/SCK0					
P43	P43/SIN3					
P44	P44/SOT3					
P45	P45/SCK3					
P46	P46/SGA/$\overline{AS}$					
P47	P47/SGO/SYSCLK					
P50	P50/SIN4/CK0/$\overline{CS0}$					
P51	P51/SOT4/$\overline{CS1}$					
P52	P52/SCK4/$\overline{CS2}$					
P53	P53/SIN5/CK1/$\overline{CS3}$					
P54	P54/SOT5/$\overline{RD}$					
P55	P55/SCK5/$\overline{WR0}$					
P56	P56/OUT0/$\overline{WR1}$					
P57	P57/OUT1/RDY					
P60 to P67	P60 to P67/AN0 to AN7					
P70	P70/RX0/INT6				P : Immediately preceding status held F : Output held, INT6 input enabled	Output Hi-Z / INT6 input enabled when PFR7 register is set to "1"
P71	P71/TX0				P : Immediately preceding status held, F : Hi-Z	Output Hi-Z / Input fixed to "0"
P72	P72/RX1/INT7				P : Immediately preceding status held F : Output held, INT7 input enabled	Output Hi-Z / INT7 input enabled when PFR7 register is set to "1"

(Continued)

(Continued)

Pin name	Function name	Initial value		In sleep state	In stop state	
		$\overline{\text{INIT}}$ = "L"	$\overline{\text{INIT}}$ = "H"		HIZ = 0	HIZ = 1
P73	P73/TX0	Output Hi-Z input enabled	Output Hi-Z input enabled	P : Immediately preceding status held F : Normal operation performed	P : Immediately preceding status held F : Output held or Hi-Z	Output Hi-Z / Input fixed to "0"
P80 to P87	P80 to P87/AN16 to AN23					
P90 to P97	P90 to P97/AN24 to AN31					
PA0 to PA3	PA0 to PA3/ PWMxxx to PWMxxx					
PB0 to PB7	PB0 to PB7/ PWMxxx to PWMxxx					
PC0 to PC3	PC0 to PC3/ PWMxxx to PWMxxx					
PD0	PD0/TIN0/IN0/PWC0	Input enabled	Input enabled	Input enabled	Hi-Z	Input fixed to "0"
PD1	PD1/TIN1/IN1					
PD2	PD2/TIN2/IN2					
PD3	PD3/IN3					
PD4	PD4/COM0/PPG1	"L" output	"L" output	P : Immediately preceding status held F : Normal operation performed	P : Immediately preceding status held LCDC : Output or hold PPG : Output held	
PD5	PD5/COM1/PPG3					
PD6	PD6/COM2/PPG5					
PD7	PD7/COM3/PPG7					
PE0 to PE7	PE0 to PE7/ PWMxxx to PWMxxx	Output Hi-Z Input enabled	Output Hi-Z Input enabled		P : Immediately preceding status held F : Output held or Hi-Z	Output Hi-Z / Input fixed to "0"
PF0 to PF7	PF0 to PF7/AN8 to AN15					
PG0	PG0/ (WOT) /PPG0					
PG1	PG1/TOT0/PPG2					
PG2	PG2/TOT1/PPG4					
PG3	PG3/TOT2/PPG6					

• **External bus mode (8-bit)**

Pin name	Function name	Initial value		In sleep mode	In stop mode	
		$\overline{INIT}$ = "L"	$\overline{INIT}$ = "H"		HIZ = 0	HIZ = 1
$\overline{INIT}$	$\overline{INIT}$	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
X0	X0				Hi-Z or input enabled	Hi-Z or input enabled
X1	X1				"H" output or input enabled	"H" output or input enabled
X0A	X0A				Hi-Z or input enabled	Hi-Z or input enabled
X1A	X1A				"H" output or input enabled	"H" output or input enabled
MOD0	MOD0				Input enabled	Input enabled
MOD1	MOD1					
MOD2	MOD2					
P00	P00/SEG24/INT0	Output Hi-Z input enabled	Output Hi-Z input enabled	P : Immediately preceding status held F : Normal operation performed	P : Immediately preceding status held F : Operation or output held during LCDC output; INT0 to INT5 input enabled when PFR0 register is set to "0"	Operation or output held during LCDC output, otherwise output Hi-Z / INT0 to INT5 input enabled when PFR0 register is set to "0"
P01	P01/SEG25/INT1					
P02	P02/SEG26/INT2					
P03	P03/SEG27/INT3					
P04	P04/SEG28/INT4					
P05	P05/SEG29/INT5					
P06	P06/SEG30				P : Immediately preceding status held F : Operation or output held during LCDC output, otherwise Hi-Z	Operation or output held during LCDC output, otherwise output Hi-Z / Input fixed to "0"
P07	P07/SEG31/$\overline{ATG}$					
P10 to P17	D08 to D15			Hi-Z	Hi-Z	Output Hi-Z / Input fixed to "0"
P20 to P27	A00 to A07	"L" output	"H" output	F : Address output	F : Address output	Output Hi-Z / Input fixed to "0"
P30 to P33	A08 to A11					

(Continued)

Pin name	Function name	Initial value		In sleep mode	In stop mode	
		$\overline{INIT}$ = "L"	$\overline{INIT}$ = "H"		HIZ = 0	HIZ = 1
P34 to P37	A12 to A15	Output Hi-Z input enabled	"H" output	F : Address output	F : Address output	Output Hi-Z / Input fixed to "0"
P40	P40/SIN0	Output Hi-Z input enabled	Output Hi-Z input enabled	P : Immediately preceding status held F : Normal operation performed	P : Immediately preceding status held F : Output held or Hi-Z	
P41	P41/SOT0					
P42	P42/SCK0					
P43	P43/SIN3					
P44	P44/SOT3					
P45	P45/SCK3					
P46	P46/SGA/$\overline{AS}$		"H" output	P : Immediately preceding status held, $\overline{AS}$: "H" output, F : Normal operation performed	P : Immediately preceding status held, $\overline{AS}$: "H" output, F : Output held	
P47	P47/SGO/SYSCLK		CLK output	P : Immediately preceding status held, CLK : CLK output, F : Normal operation performed	P : Immediately preceding status held, CLK : "H" or "L" output, F : Output held	
P50	P50/SIN4/CK0/$\overline{CS0}$		"H" output	Bus control : "H" output P : Immediately preceding status held F : Normal operation performed	Bus control : "H" output P : Immediately preceding status held F : Output held or Hi-Z	
P51	P51/SOT4/$\overline{CS1}$					
P52	P52/SCK4/$\overline{CS2}$					
P53	P53/SIN5/CK1/$\overline{CS3}$					
P54	P54/SOT5/$\overline{RD}$					
P55	P55/SCK5/$\overline{WR0}$					

(Continued)

Pin name	Function name	Initial value		In sleep mode	In stop mode	
		$\overline{INIT}$ = "L"	$\overline{INIT}$ = "H"		HIZ = 0	HIZ = 1
P56	P56/OUT0	Output Hi-Z input enabled	"H" output	P : Immediately preceding status held F : Normal operation performed; "H" output when EPFR is set to "0"	P : Immediately preceding status held F : Output held; "H" output when EPFR is set to "0"	Output Hi-Z / Input fixed to "0"
P57	P57/OUT1/ RDY		RDY input	P : Immediately preceding status held F : Normal status, RDY input	P : Immediately preceding status held F : Output held, RDY input	
P60 to P67	P60 to P77/ AN0 to AN7	Output Hi-Z input enabled	Output Hi-Z input enabled	P : Immediately preceding status held F : Normal operation performed	P : Immediately preceding status held F : Output held or Hi-Z	Output Hi-Z / Input fixed to "0"
P70	P70/RX0/ INT6				P : Immediately preceding status held F : Output held, INT6 input enabled	Output Hi-Z / INT6 input enabled when PFR7 register is set to "1"
P71	P71/TX0				P : Immediately preceding status held, F : Hi-Z	Output Hi-Z / Input fixed to "0"
P72	P72/RX1/ INT7				P : Immediately preceding status held F : Output held, INT7 input enabled	Output Hi-Z / INT7 input enabled when PFR7 register is set to "1"

(Continued)

(Continued)

Pin name	Function name	Initial value		In sleep mode	In stop mode	
		$\overline{INIT}$ = "L"	$\overline{INIT}$ = "H"		HIZ = 0	HIZ = 1
P80 to P87	P80 to P87/ AN16 to AN23	Output Hi-Z input enabled	Output Hi-Z input enabled	P : Immediately preceding status held F : Normal operation performed	P : Immediately preceding status held F : Normal operation performed	Output Hi-Z / Input fixed to "0"
P90 to P97	P90 to P97/ AN24 to AN31					
PA0 to PA3	PA0 to PA3/ PWMxxx to PWMxxx					
PB0 to PB7	PB0 to PB7/ PWMxxx to PWMxxx					
PC0 to PC3	PC0 to PC3/ PWMxxx to PWMxxx					
PD0	PD0/TIN0/ IN0/PWC0	Input enabled	Input enabled	Input enabled	Hi-Z	Input fixed to "0"
PD1	PD1/TIN1					
PD2	PD2/TIN2					
PD3	PD3/IN3					
PD4	PD4/COM0/ PPG1	"L" output	"L" output	P : Immediately preceding status held F : Normal operation performed	P : Immediately preceding status held LCDC : Output or hold PPG : Output held	
PD5	PD5/COM1/ PPG3					
PD6	PD6/COM2/ PPG5					
PD7	PD7/COM3/ PPG7					
PE0 to PE7	PE0 to PE7/ PWMxxx to PWMxxx	Output Hi-Z Input enabled	Output Hi-Z Input enabled		P : Immediately preceding status held F : Output held or Hi-Z	Output Hi-Z / Input fixed to "0"
PF0 to PF7	PF0 to PF7/ AN8 to AN15					
PG0	PG0/ (WOT) / PPG0					
PG1	PG1/TOT0/ PPG2					
PG2	PG2/TOT1/ PPG4					
PG3	PG3/TOT2/ PPG6					

• **External bus mode (16-bit)**

Pin name	Function name	Initial value		In sleep mode	In stop mode	
		$\overline{\text{INIT}}$ = "L"	$\overline{\text{INIT}}$ = "H"		HIZ = 0	HIZ = 1
$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
X0	X0				Hi-Z or input enabled	Hi-Z or input enabled
X1	X1				"H" output or input enabled	"H" output or input enabled
X0A	X0A				Hi-Z or input enabled	Hi-Z or input enabled
X1A	X1A				"H" output or input enabled	"H" output or input enabled
MOD0	MOD0				Input enabled	Input enabled
MOD1	MOD1					
MOD2	MOD2					
P00	D00	Output Hi-Z input enabled	Output Hi-Z input enabled	Hi-Z	Hi-Z	Output Hi-Z Input fixed to "0"
P01	D01					
P02	D02					
P03	D03					
P04	D04					
P05	D05					
P06	D06					
P07	D07					
P10 to P17	D08 to D15					
P20 to P27	A00 to A07	"L" output	"H" output	F : Address output	F : Address output	
P30 to P33	A08 to A11					
P34 to P37	A12 to A15	Output Hi-Z input enabled				
P40	P40/SIN0		Output Hi-Z input enabled	P : Immediately preceding status held F : Normal operation performed	P : Immediately preceding status held F : Output held or Hi-Z	
P41	P41/SOT0					
P42	P42/SCK0					
P43	P43/SIN3					
P44	P44/SOT3					
P45	P45/SCK3					

(Continued)

Pin name	Function name	Initial value		In sleep mode	In stop mode	
		$\overline{INIT}$ = "L"	$\overline{INIT}$ = "H"		HIZ = 0	HIZ = 1
P46	P46/SGA/$\overline{AS}$	Output Hi-Z input enabled	"H" output	P : Immediately preceding status held, $\overline{AS}$: "H" output, F : Normal operation performed	P : Immediately preceding status held, $\overline{AS}$: "H" output, F : Output held	Output Hi-Z Input fixed to "0"
P47	P47/SGO/ SYSCLK		CLK output	P : Immediately preceding status held, CLK : CLK output, F : Normal operation performed	P : Immediately preceding status held, CLK : "H" or "L" output, F : Output held	
P50	P50/SIN4/ CK0/$\overline{CS0}$		"H" output	Bus control : "H" output P : Immediately preceding status held F : Normal operation performed	Bus control : "H" output P : Immediately preceding status held F : Output held or Hi-Z	
P51	P51/SOT4/ $\overline{CS1}$					
P52	P52/SCK4/ $\overline{CS2}$					
P53	P53/SIN5/ CK1/$\overline{CS3}$					
P54	P54/SOT5/ $\overline{RD}$	Output Hi-Z input enabled	"H" output	Bus control : "H" output P : Immediately preceding status held F : Normal operation performed	Bus control : "H" output P : Immediately preceding status held F : Output held or Hi-Z	Output Hi-Z / Input fixed to "0"
P55	P55/SCK5/ $\overline{WR0}$					
P56	P56/OUT0/ $\overline{WR1}$					
P57	P57/OUT1/ RDY		RDY input	P : Immediately preceding status held F : Normal status, RDY input	P : Immediately preceding status held F : Output held, RDY input	
P60 to P67	P60 to P77/ AN0 to AN7	Output Hi-Z input enabled	Output Hi-Z input enabled	P : Immediately preceding status held F : Normal operation performed	P : Immediately preceding status held F : Output held or Hi-Z	Output Hi-Z / Input fixed to "0"

(Continued)

Pin name	Function name	Initial value		In sleep mode	In stop mode	
		$\overline{INIT}$ = "L"	$\overline{INIT}$ = "H"		HIZ = 0	HIZ = 1
P70	P70/RX0/ INT6	Output Hi-Z input enabled	Output Hi-Z input enabled	P : Immediately preceding status held F : Normal operation performed	P : Immediately preceding status held F : Output held, INT6 input enabled	Output Hi-Z / INT6 input enabled when PFR7 register is set to "1"
P71	P71/TX0				P : Immediately preceding status held, F : Hi-Z	Output Hi-Z / Input fixed to "0"
P72	P72/RX1/ INT7				P : Immediately preceding status held F : Output held, INT7 input enabled	Output Hi-Z / INT7 input enabled when PFR7 register is set to "1"
P80 to P87	P80 to P87/ AN16 to AN23	Output Hi-Z input enabled	Output Hi-Z input enabled	P : Immediately preceding status held F : Normal operation performed	P : Immediately preceding status held F : Normal operation performed	Output Hi-Z/ Input fixed to "0"
P90 to P97	P90 to P97/ AN24 to AN31					
PA0 to PA3	PA0 to PA3/ PWMxxx to PWMxxx					
PB0 to PB7	PB0 to PB7/ PWMxxx to PWMxxx					
PC0 to PC3	PC0 to PC3/ PWMxxx to PWMxxx					
PD0	PD0/TIN0/ IN0/PWC0	Input enabled	Input enabled	Input enabled	Hi-Z	Input fixed to "0"
PD1	PD1/TIN1					
PD2	PD2/TIN2					
PD3	PD3/IN3					

(Continued)

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Pin name	Function name	Initial value		In sleep mode	In stop mode	
		$\overline{\text{INIT}}$ = "L"	$\overline{\text{INIT}}$ = "H"		HIZ = 0	HIZ = 1
PD4	PD4/COM0/ PPG1	"L" output	"L" output	P : Immediately preceding status held F : Normal operation performed	P : Immediately preceding status held LCDC : Output or hold PPG : Output held	Input fixed to "0"
PD5	PD5/COM1/ PPG3					
PD6	PD6/COM2/ PPG5					
PD7	PD7/COM3/ PPG7					
PE0 to PE7	PE0 to PE7/ PWMxxx to PWMxxx	Output Hi-Z Input enabled	Output Hi-Z Input enabled		P : Immediately preceding status held F : Output held or Hi-Z	Output Hi-Z / Input fixed to "0"
PF0 to PF7	PF0 to PF7/ AN8 to AN15					
PG0	PG0/ (WOT) / PPG0					
PG1	PG1/TOT0/ PPG2					
PG2	PG2/TOT1/ PPG4					
PG3	PG3/TOT2/ PPG6					

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	$AV_{CC} = V_{CC}$*2
	V_{AVRH}	V_{SS} – 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq V_{AVRH}$
	DV_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	$DV_{CC} = V_{CC}$*2
Input voltage*1	V_I	V_{SS} – 0.3	V_{CC} + 0.3	V	
Output voltage*1	V_O	V_{SS} – 0.3	V_{CC} + 0.3	V	
"L" level maximum output current*3	I_{OL1}	—	15	mA	*5
	I_{OL2}	—	40	mA	*6
"L" level average output current*4	I_{OLAV1}	—	4	mA	*5
	I_{OLAV2}	—	30	mA	*6
"L" level total maximum output current	ΣI_{OL1}	—	120	mA	*5
	ΣI_{OL2}	—	330	mA	*6
"L" level total average output current	ΣI_{OLAV1}	—	50	mA	*5
	ΣI_{OLAV2}	—	240	mA	*6
"H" level maximum output current	I_{OH1}*3	—	–15	mA	*5
	I_{OH2}*3	—	–40	mA	*6
"H" level average output current	I_{OHAV1}*4	—	–4	mA	*5
	I_{OHAV2}*4	—	–30	mA	*6
"H" level total maximum output current	ΣI_{OH1}	—	–120	mA	*5
	ΣI_{OH2}	—	–330	mA	*6
"H" level total average output current	ΣI_{OHAV1}*7	—	–50	mA	*5
	ΣI_{OHAV2}*7	—	–240	mA	*6
Power consumption	P_D	—	660	mW	
Operating temperature	T_A	–40	+105	°C	MASK ROM product (in single chip operation)
		–40	+105	°C	Flash memory product (in single chip operation)
		–40	+85	°C	MASK ROM/Flash memory product (in external bus operation)
Storage temperature	Tstg	–55	+150	°C	
+B input standard (Maximum clamp current)	I_{IHH}	—	2	mA	Exclusive of dedicated input pins*8
+B input standard (Total maximum clamp current)	ΣI_{IHH}	—	20	mA	

(Continued)

(Continued)

*1 : The parameter is base on V_{SS} = AV_{SS} = DV_{SS} = 0.0 V.

*2 : Caution must be taken that AV_{CC} and DV_{CC} do not exceed V_{CC} upon power-on and under other circumstances.

*3 : The maximum output current defines the peak current value of each of the corresponding pins.

*4 : The average output current defines the average value of the current (100 ms) which passes through each of the corresponding pins. The average value represents a value calculated by multiplying the operating current by the operating rate.

*5 : Output other than PA0 to PA3 pins, PB0 to PB7 pins, PC0 to PC3 pins, and PE0 to PE7 pins

*6 : (PA0 to PA3 pins, PE0 to PE7 pins) + (PB0 to PB7 pins, PC0 to PC3 pins)
The SMC pins are divided into two groups (12 pins each) and the value is calculated as the total current per group.

*7 : The total average output current defines the average value of the current (100 ms) which passes through all the corresponding pins. The average value represents a value calculated by multiplying the operating current by the operating rate.

*8 : +B input standard defines the current value for each of the corresponding pins.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = DV_{SS} = AV_{SS} = 0.0 V)

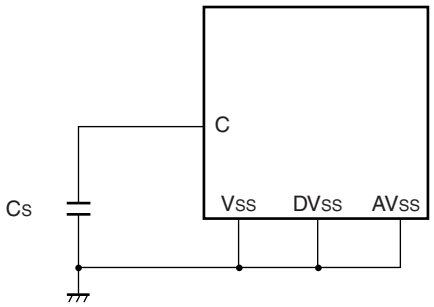
Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC} AV_{CC} DV_{CC}	4.5	5.5	V	Recommended guaranteed operating range (MB91F248, MB91248)
		3.5	5.5	V	Guaranteed operating range*1 (MB91F248, MB91248)
		2.0	5.5	V	Guaranteed operating range for holding stop operation status*2 (MB91F248, MB91248)
Smoothing capacitor*3	C_S	1		µF	Use a ceramic capacitor or a capacitor with similar frequency characteristics.
Operating temperature	T_A	–40	+105	°C	MASK ROM product (in single chip operation)
		–40	+105	°C	Flash memory product (in single chip operation)
		–40	+85	°C	MASK ROM/Flash memory product (in external bus operation)

*1 : Exclusive of A/D operation

*2 : Internal voltage held in RAM : 1.8 V (Min) /3.6 V (Max)

*3 : For how to connect the smoothing capacitor C_S, refer to the figure below.

• C Pin Connection Diagram



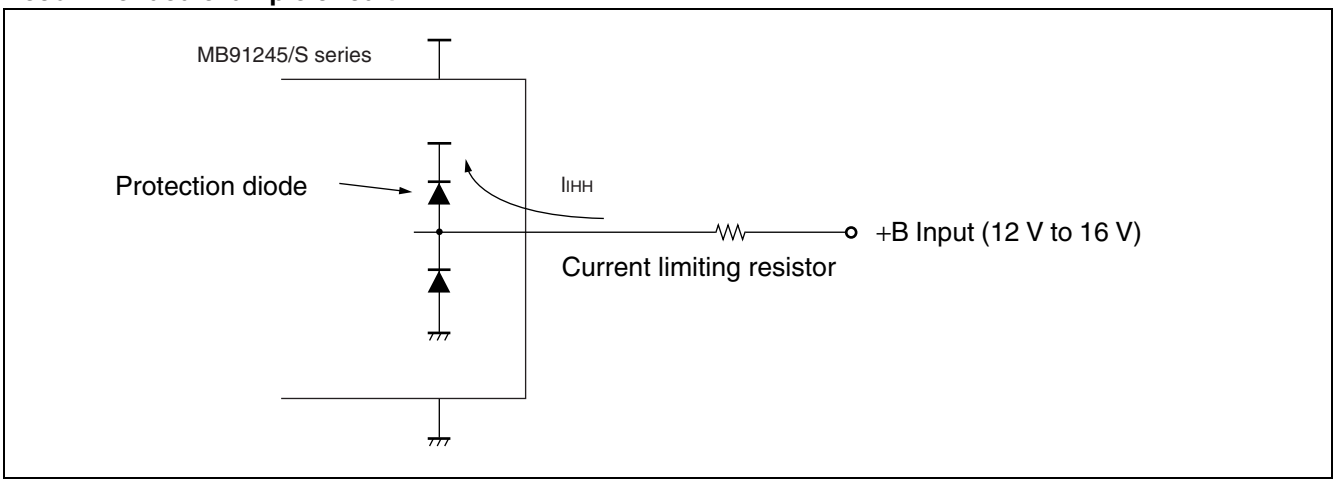
< + B input (12 V to 16 V) conditions>

- Do not connect +B potential directly to a microcontroller pin.
- Always connect a resistor between the microcontroller pin and +B signal to limit the current.

  I_{IHH} = 2 mA per pin (Max.) [In the steady state and transient state between power-on and power-off, etc.]

  It can be connected to any general-purpose input port except the output pin for LCDC.
- The protection diode in the microcontroller turns the potential upon +B input between the limiting resistor and microcontroller pin into "V_{CC} + protection diode ON voltage". Configure the circuit so that these are not interfered and the potential is not exceeded.

Recommended example circuit



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Specifications

(T_A : Recommended operating conditions; Vcc = 5.0 V ±10%, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IHS}	—	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Automotive level input pins*1
	V_{IH}	P00 to P07, P10 to P17, P57	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	CMOS hysteresis input pins*2
	V_{IHM}	—	—	V_{CC} – 0.3	—	V_{CC} + 0.3	V	MOD pins*3
	V_{IHX}	X0, X1, X0A, X1A, $\overline{INIT}$	—	0.8 V_{CC}	—	—	V	
"L" level input voltage	V_{ILS}	—	—	V_{SS} – 0.3	—	0.5 V_{CC}	V	Automotive level input pins*1
	V_{IL}	P00-P07, P10-P17, P57	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	CMOS hysteresis input pins*2
	V_{ILM}	—	—	V_{SS} – 0.3	—	Vss + 0.3	V	MOD pins*3
	V_{ILX}	X0, X1, X0A, X1A, $\overline{INIT}$	—	—	—	0.2 V_{CC}	V	
Power supply current*4	I_{CC}	V_{CC}	Operating frequency : F_{CP} = 32 MHz in main mode	—	55	85	mA	Flash memory product
				—	55	85	mA	MASK ROM product
				—	100	150	mA	In Flash-Write mode
	I_{CCL}		Operating frequency : F_{CP} = 32 kHz, T_A = +25 °C in sub mode	—	290	450	µA	
	I_{CCH}		T_A = +25 °C, Vcc = 5V in stop mode (oscillation stopped)	—	95	150	µA	
	I_{CTS}		T_A = +25 °C, Vcc = 5V in stop mode (RTC in use)	—	390	500	µA	At 4 MHz
Input leak current	I_{IL}	All input pins	V_{CC} = DV_{CC} = AV_{CC} = 5.5 V V_{SS} < V_I < V_{CC}	–5	—	+5	µA	
Input capacity 1	C_{IN1}	Other than V_{cc}, V_{SS}, DV_{cc}, DV_{SS}, AV_{cc}, AV_{SS}, PA0 to PA3, PB0 to PB7, PC0 to PC3, PE0 to PE7	—	—	5	15	pF	
Input capacity 2	C_{IN2}	PA0 to PA3, PB0 to PB7, PC0 to PC3, PE0 to PE7	—	—	15	45	pF	
Pull-up resistance	R_{UP}	$\overline{INIT}$	—	25	50	100	kΩ	

(Continued)

(Continued)

(T_A : Recommended operating conditions; Vcc = 5.0 V ±10%, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Pull-down resistance	R_{DOWN}	MOD1, MOD2	—	25	50	100	kΩ	MASK ROM products only
Output "H" voltage 1	V_{OH1}	Other than PA0 to PA3, PB0 to PB7, PC0 to PC3, PE0 to PE7	Vcc = 4.5 V I_{OH} = –4.0 mA	V_{CC} – 0.5	—	—	V	
Output "H" voltage 2	V_{OH2}	PA0 to PA3, PB0 to PB7, PC0 to PC3, PE0 to PE7	Vcc = 4.5 V I_{OH} = –30.0 mA	V_{CC} – 0.5	—	—	V	
Output "L" voltage 1	V_{OL1}	Other than PA0 to PA3, PB0 to PB7, PC0 to PC3, PE0 to PE7	Vcc = 4.5 V I_{OL} = 4.0 mA	—	—	0.4	V	
Output "L" voltage 2	V_{OL2}	PA0 to PA3, PB0 to PB7, PC0 to PC3, PE0 to PE7	Vcc = 4.5 V I_{OL} = 30.0 mA	—	—	0.55	V	
High current output Drive capacity Phase-to-phase deviation 1	ΔV_{OH2}	PWM1Pn, PWM1Mn, PWM2Pn, PWM2Mn, n = 0 to 5	Vcc = 4.5 V I_{OH} = 30.0 mA Maximum deviation of V_{OH2}	0	—	90	mV	*5
High current output Drive capacity Phase-to-phase deviation 2	ΔV_{OL2}	PWM1Pn, PWM1Mn, PWM2Pn, PWM2Mn, n = 0 to 5	Vcc = 4.5 V I_{OL} = 30.0 mA Maximum deviation of V_{OL2}	0	—	90	mV	*5
COM0 to COM3 Output impedance	R_{VCOM}	COMm (m = 0 to 3)	—	—	—	2.5	kΩ	
SEG00 to SEG31 Output impedance	R_{VSEG}	SEGn (n = 00 to 31)	—	—	15	30	kΩ	
LCDC leak current	I_{LCDC}	COMm (m = 0 to 3) , SEGn, (n = 00 to 31)	T_A = +25 °C	–0.5	—	+0.5	µA	

*1 : All input pins except X0, X1, X0A, X1A, MOD0, MOD1, MOD2 and $\overline{INIT}$ pins

*2 : Can be selected by the input level select register (PILR).

*3 : MOD0, MOD1 and MOD2

*4 : They represent current values used when supplying power to the external clock from pin X1.

*5 : Defined by the maximum deviation of V_{OH2}/V_{OL2} of each pin, when PWM1P0, PWM1M0, PWM2P0 and PWM2M0 in ch.0 are simultaneously turned on. The same applies to other channels.

4. Flash Memory Write/Erase Characteristics

Parameter	Condition	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	T_A = +25 °C, Vcc = 5.0 V	—	1	15	s	Exclusive of internal write time prior to erase
Chip erase time	T_A = +25 °C, Vcc = 5.0 V	—	5	—	s	Exclusive of internal write time prior to erase
Halfword write time	T_A = +25 °C, Vcc = 5.0 V	—	16	3600	µs	Exclusive of overhead time at system level
Chip write time	T_A = +25 °C, Vcc = 5.0 V	—	2.1	—	s	Exclusive of overhead time at system level
Erase/write cycle	—	10000	—	—	cycle	
Flash memory data retain time	T_A = +85 °C (average)	10	—	—	year	*

* : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85 °C) .

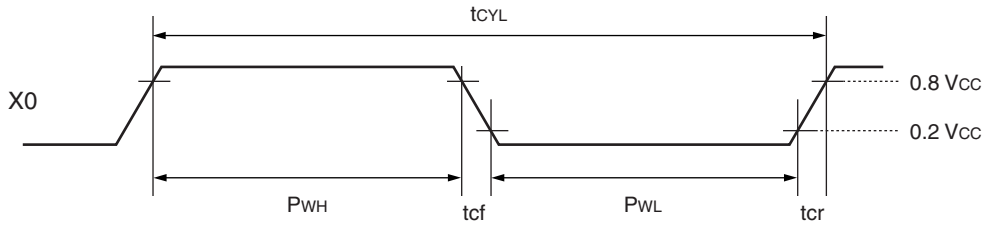
5. AC Specifications

(1) Clock timing

(T_A : Recommended operating conditions; Vcc = 5.0 V ±10%, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Frequency of source oscillation clock	F_C	X0, X1	—	—	4	—	MHz	
	Fca	X0A, X1A		—	32	—	kHz	
Source oscillation clock Cycle time	t_{CYL}	X0, X1		—	250	—	ns	
Input clock pulse width	P_{WH} , P_{WL}	X0		100	—	—	ns	The duty ratio normally ranges from 40% to 60%.
Frequency of internal operating clock	f_{CPB}	—	—	0.0312	—	32	MHz	CPU based (CLKB)
	f_{CPT}			0.0312	—	16	MHz	External bus based (CLKT)
	f_{CPP}			0.0312	—	32	MHz	Peripheral based (CLKP)
Internal operating clock cycle	t_{CPB}	—	—	31.25	—	32000	ns	CPU based (CLKB)
	t_{CPT}			62.5	—	32000	ns	External bus based (CLKT)
	t_{CPP}			31.25	—	32000	ns	Peripheral based (CLKP)
Input clock Rise/fall time	tcr tcf	X0	—	—	—	5	ns	When external clock is used
Frequency of internal base clock	F_{CP}	—		—	—	32	MHz	When main oscillation is at 4 MHz and PLL multiplied by 8 is used
Internal base clock Cycle time	t_{CP}	—	—	31.25	—	—	ns	When main oscillation is at 4 MHz and PLL multiplied by 8 is used

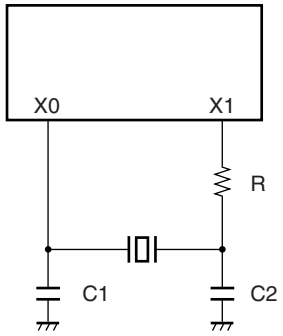
• X0/X1 Clock Timing



• Operations

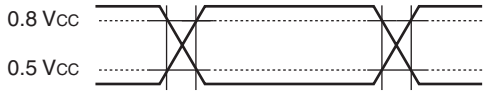
Oscillation should be performed as described below :
[Source oscillation] : X0/X1 : 4 MHz, PLL : multiplied by 8, Internal frequency : 32 MHz
: X0A/X1A : 32 kHz, PLL : no multiplied, Internal frequency : 32 kHz
Note that the PLL oscillation stabilization wait time should be set to 500 µs or more.

Example oscillation circuit

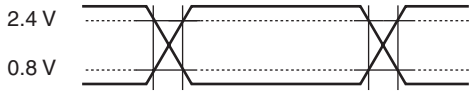


AC specifications are defined by the following measurement standard voltage values :

• Input signal waveform
Hysteresis input pin



• Output signal waveform
Output pin

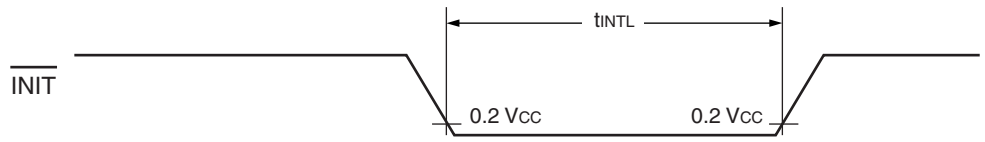


(2) Reset input

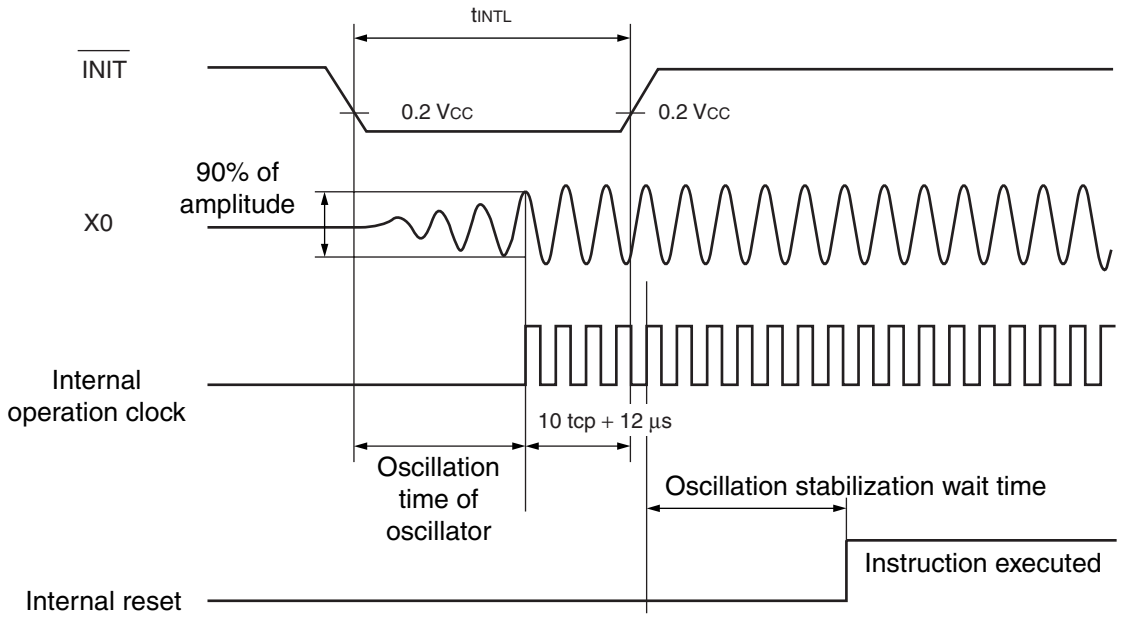
(T_A : Recommended operating conditions; Vcc = 5.0 V ±10%, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
$\overline{INIT}$ input time	t_{INTL}	$\overline{INIT}$	—	500	—	ns	Flash memory product
				10 t_{CP}	—	ns	MASK ROM product
				Oscillation time of oscillator* + 10 tcp + 12 µs	—	ms	In stop mode

* : The oscillation time of the oscillator refers to the time when the amplitude has reached 90%. The oscillation time of the crystal oscillator ranges from several ms to tens of ms. The oscillation time of the ceramic oscillator ranges from several hundreds to several ms, while that of the external clock is 0 ms.



• In stop mode

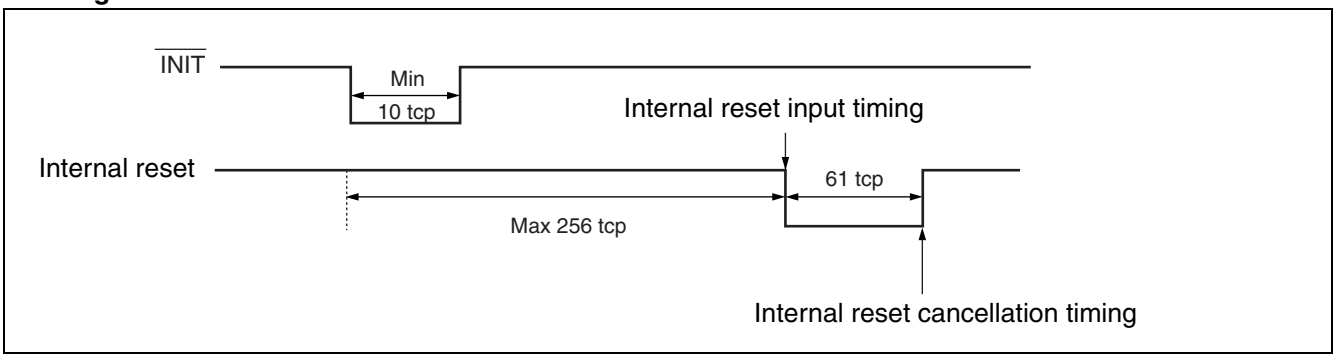


[External reset input specifications ($\overline{\text{INIT}}$) and internal reset signal cancellation timing]

- When an external reset input is generated, a maximum of 256 tcp is designed to be spent until it reaches the internal reset signal to transmit all reset signals to the internal logic.
  (Max 8 μs at 32 MHz)
- The following chart shows how to set the timing for instruction execution start (start of application operation) after external reset input.

Time from external reset input to instruction start = Max 256 tcp + 61 tcp

• Timing Chart

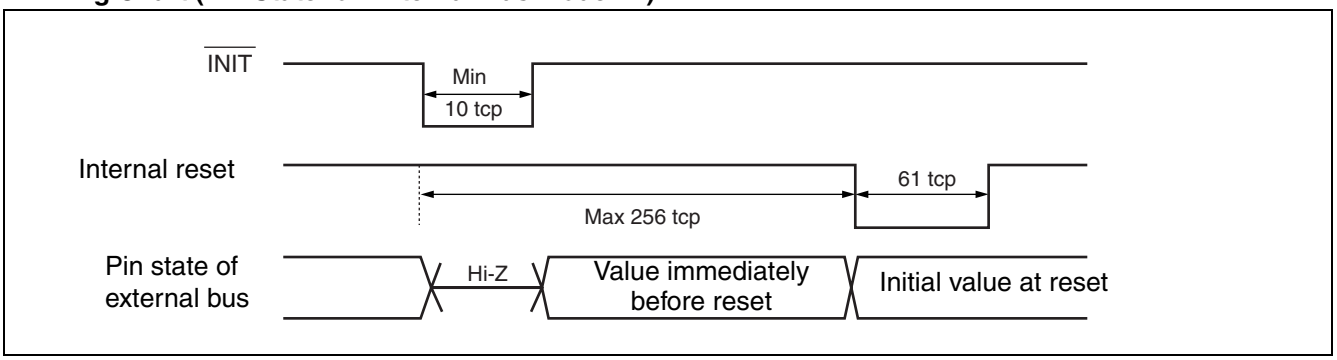


[Pin state in external bus mode]

In the external bus mode, it is not guaranteed to hold the RAM value upon external reset ($\overline{\text{INIT}}$ = “0”) input.

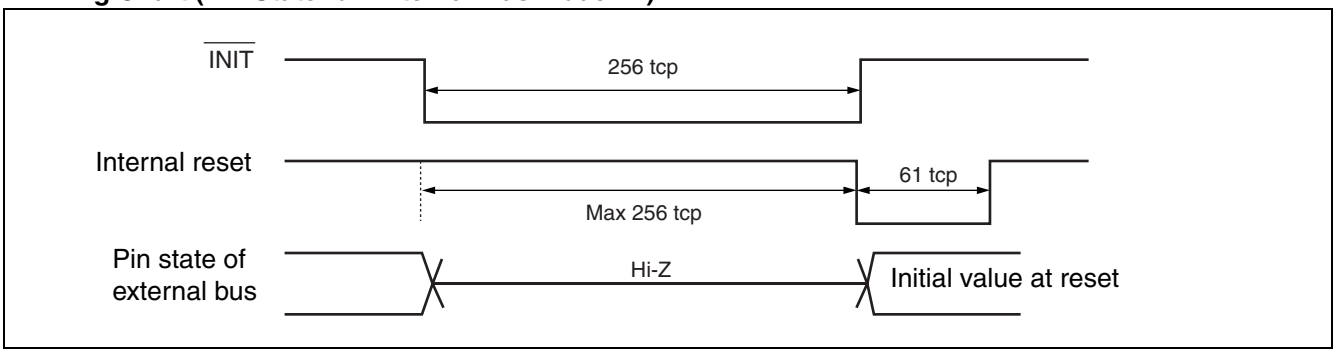
In the external bus mode, the value of the internal bus is output to each pin during the time from the internal reset input to its cancellation as well as the RAM value is not guaranteed to be held.

• Timing Chart (Pin State for External Bus Mode : 1)



It can be avoided by the following external reset input to continue Hi-Z.

• **Timing Chart (Pin State for External Bus Mode : 2)**



(3) Power-on Conditions

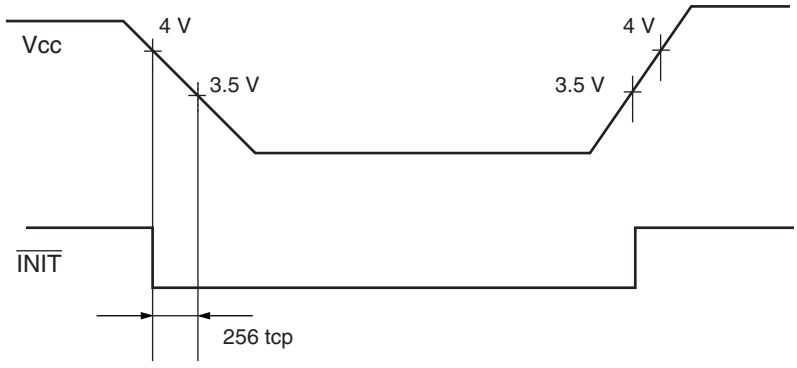
(T_A : Recommended operating conditions; V_{SS} = 0.0 V)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Power supply rising time	t_R	Vcc	—	0.05	30	ms	
Power supply start voltage	V_{OFF}			—	0.2	V	
Power supply peak voltage	V_{ON}			3.5	—	V	
Power supply cut-off time	t_{OFF}			50	—	ms	Due to repetitive operation

Power supply drop time, power supply voltages and external reset input to retain RAM data in MB91245/S

Satisfy the following reset input standard to retain the RAM data used in the single chip mode.

Vcc (V)	Voltage drop time	External reset input standard ($\overline{INIT}$)
4.0 V → 3.5 V dropped	Min 256 tcp	Min 256 tcp

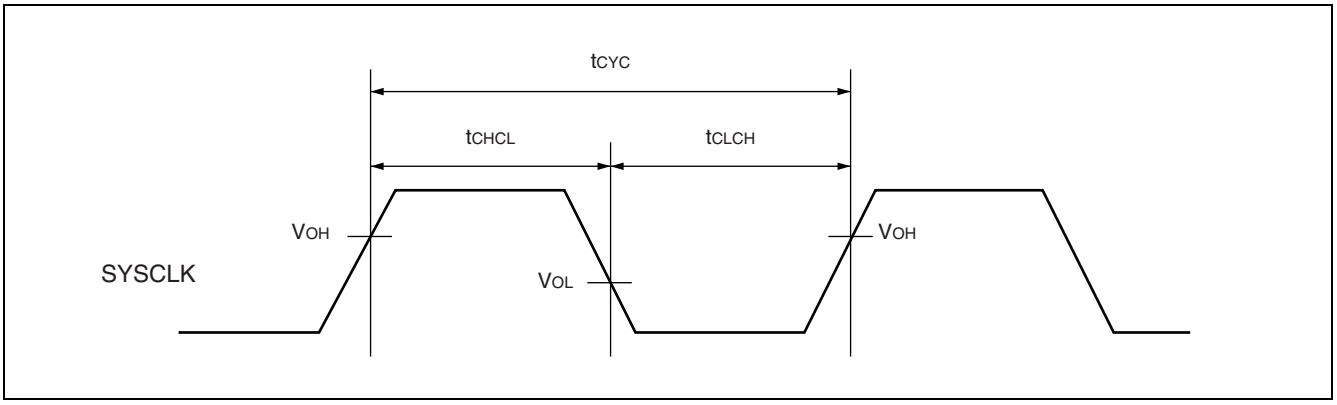


To retain RAM data, enter 256 tcp of $\overline{INIT}$ or more before dropping V_{CC} to 3.5 V or lower.

(4) Clock Output Timing

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	SYSCLK	—	t_{CPT}	—	ns	*1
SYSCLK↑→SYSCLK↓	t_{CHCL}	SYSCLK		t_{CYC} / 2 – 10	t_{CYC} / 2 + 10	ns	*2
SYSCLK↓→SYSCLK↑	t_{CLCH}	SYSCLK		t_{CYC} / 2 – 10	t_{CYC} / 2 + 10	ns	*3



*1 : t_{CYC} is the frequency of one clock cycle including the gear cycle.

*2 : The ratings are based on conditions with “gear cycle × 1”.
When the gear cycle is set to 1/2, 1/4 or 1/8, perform calculation by substituting 1/2, 1/4 or 1/8 for “n” in the following formula, respectively.

$$(1 / 2 \times 1 / n) \times t_{CYC} - 10$$

*3 : This is the value for the gear cycle × 1.

(5) Normal Bus Access : Read/Write Operation

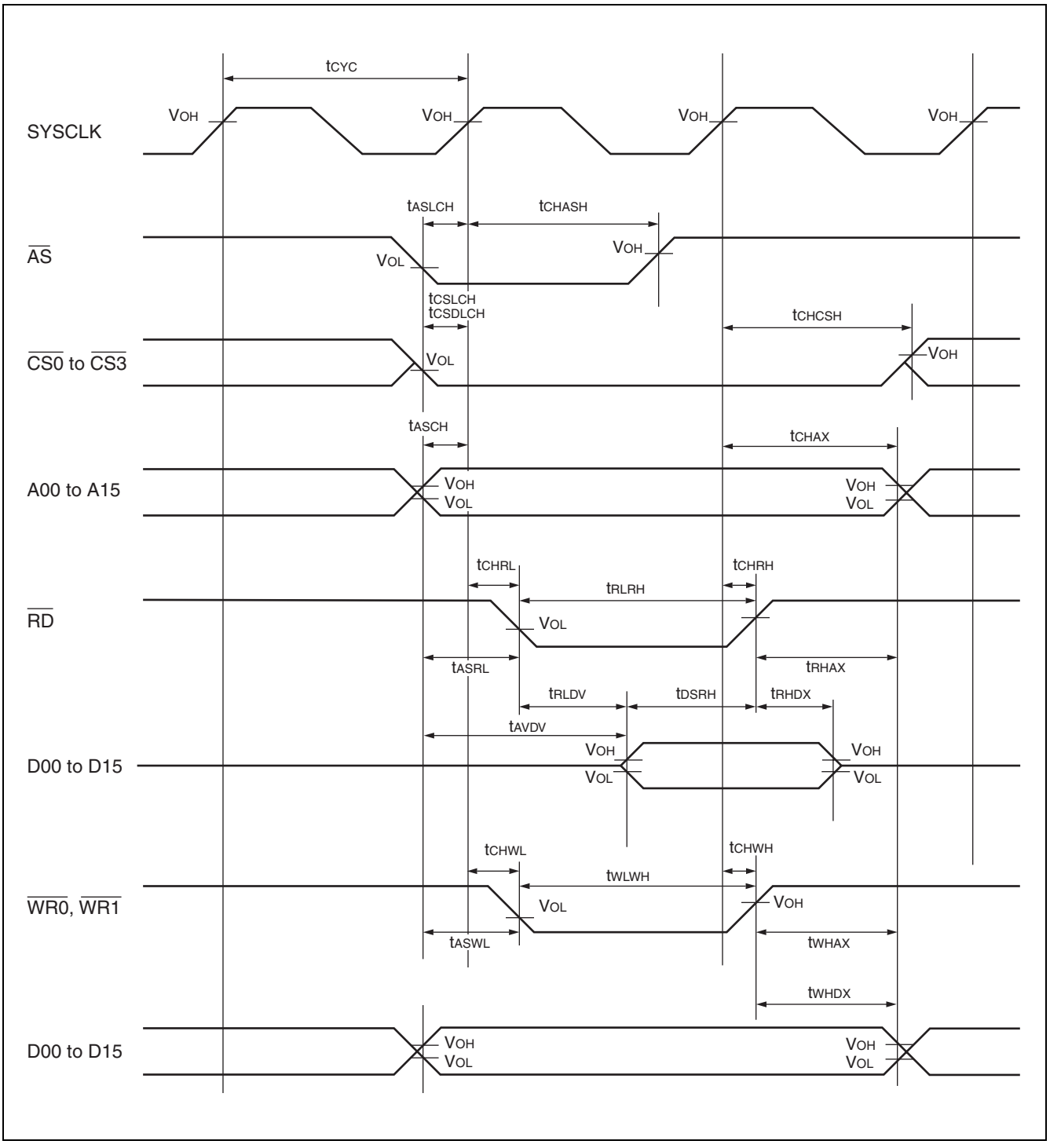
(V_{CC} = 4.0 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, T_A = 0 °C to + 70 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
$\overline{CS0}$ to $\overline{CS3}$ setup	t_{CSLCH}	SYSCLK $\overline{CS0}$ to $\overline{CS3}$	AWRxL : W02 = 0	3	—	ns	
	t_{CSDLCH}		AWRxL : W02 = 1	–8	—	ns	
$\overline{CS0}$ to $\overline{CS3}$ hold	t_{CHCSH}			3	t_{CYC} / 2 + 25	ns	
Address setup	t_{ASCH}	SYSCLK A00 to A15		3	—	ns	
	t_{ASWL}	$\overline{WR0}$, $\overline{WR1}$ A00 to A15		3	—	ns	
	t_{ASRL}	$\overline{RD}$ A00 to A15		3	—	ns	
Address hold	t_{CHAX}	SYSCLK A00 to A15		3	t_{CYC} / 2 + 25	ns	
	t_{WHAX}	$\overline{WR0}$, $\overline{WR1}$ A00 to A15		3	—	ns	
	t_{RHAX}	$\overline{RD}$ A00 to A15		3	—	ns	
Valid address → valid data input time	t_{AVDV}	A00 to A15 D00 to D15		—	3 / 2 × t_{CYC} + 45	ns	*1, *2
$\overline{WR0}$, $\overline{WR1}$ delay time	t_{CHWL}	SYSCLK $\overline{WR0}$, $\overline{WR1}$		—	8	ns	
$\overline{WR0}$, $\overline{WR1}$ delay time	t_{CHWH}			—	8	ns	
$\overline{WR0}$, $\overline{WR1}$ minimum pulse width	t_{WLWH}	$\overline{WR0}$, $\overline{WR1}$		t_{CYC} – 5	—	ns	
$\overline{WR0}$, $\overline{WR1}$↑→ data hold time	t_{WHDX}	D00 to D15		3	—	ns	
$\overline{RD}$ delay time	t_{CHRL}	SYSCLK $\overline{RD}$		—	6	ns	
$\overline{RD}$ delay time	t_{CHRH}			—	6	ns	
$\overline{RD}$ ↓ → valid data input time	t_{RLDV}	$\overline{RD}$ D00 to D15		—	t_{CYC} – 30	ns	*1
Data setup → $\overline{RD}$ ↑ time	t_{DSRH}			20	—	ns	
$\overline{RD}$ ↑ → data hold time	t_{RHDX}			0	—	ns	
$\overline{RD}$ minimum pulse width	t_{RLRH}	$\overline{RD}$		t_{CYC} – 5	—	ns	
$\overline{AS}$ setup	t_{ASLCH}	SYSCLK $\overline{AS}$		3	—	ns	
$\overline{AS}$ hold	t_{CHASH}			3	t_{CYC} / 2 + 25	ns	

*1 : If the bus is expanded by automatic wait insertion or RDY input, add time (t_{CYC} × the number of expanded cycles) to the rated value.

*2 : The ratings are based on conditions with “gear cycle × 1”. If the gear cycle is set to 1/2 to 1/16, perform calculation by substituting the corresponding value for “n” in the following formula.

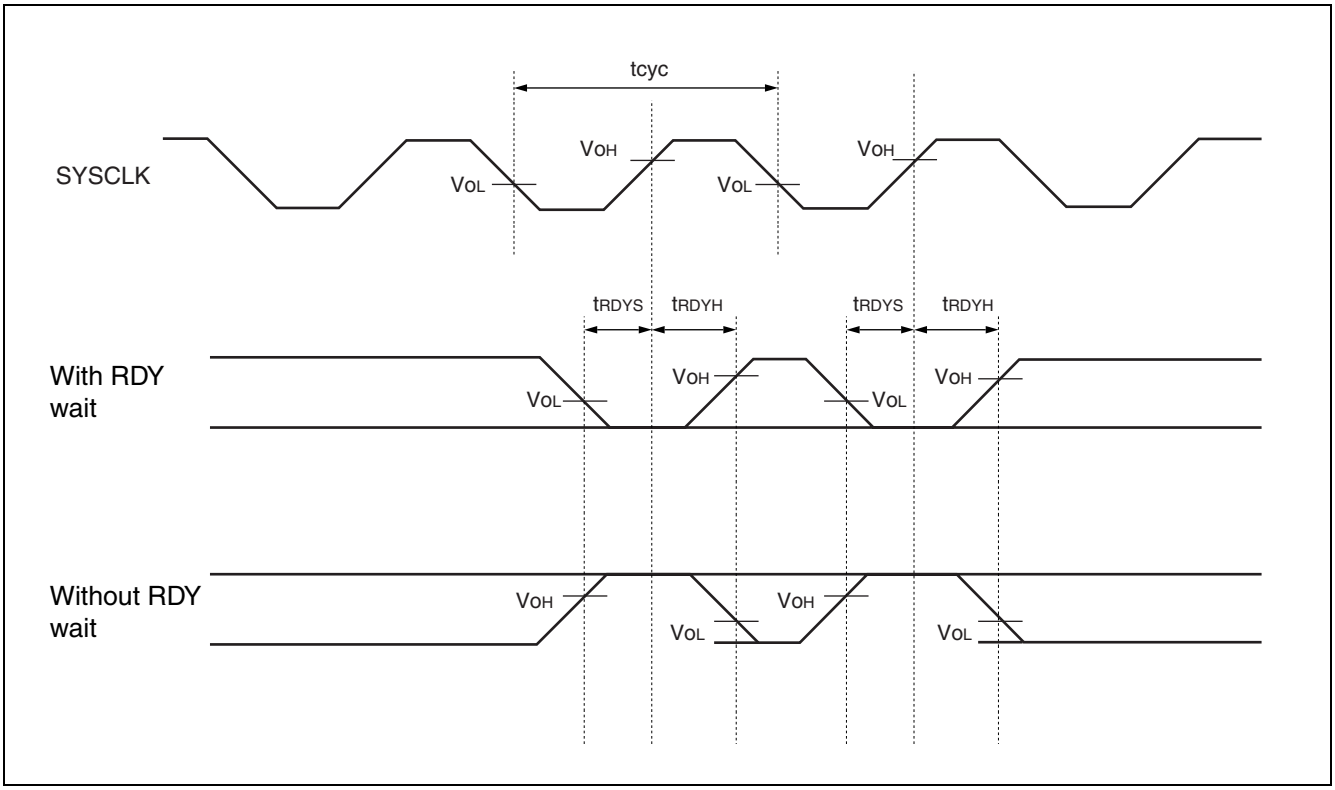
Formula : 3/ (2n) × t_{CYC} + 45


tCYC
SYSCLK
VOH
VOH
VOH
VOH
tASLCH
tCHASH
AS
VOL
VOH
tCSLCH
tCSDLCH
tCHCSH
CS0 to CS3
VOL
VOH
tASCH
tCHAX
A00 to A15
VOH
VOL
VOH
VOL
tCHRL
tCHRH
tRLRH
RD
VOL
tASRL
tRHAX
tRLDV
tDSRH
tRHDX
tAVDV
D00 to D15
VOH
VOL
VOH
VOL
tCHWL
tCHWH
tWLWH
WR0, WR1
VOL
VOH
tASWL
tWHAX
tWHDX
D00 to D15
VOH
VOL
VOH
VOL

(6) Ready Input Timing

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
RDY setup time →SYSCLK↓	t_{RDYS}	SYSCLK RDY	—	10	—	ns	
SYSCLK↑→ RDY hold time	t_{RDYH}	SYSCLK RDY		0	—	ns	



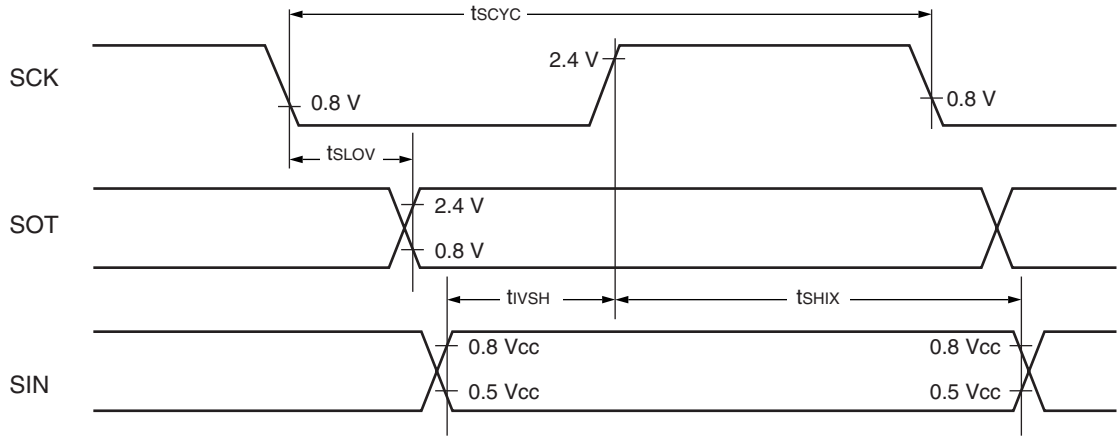
(7) UART Timing

(T_A : Recommended operating conditions; V_{CC} = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V)

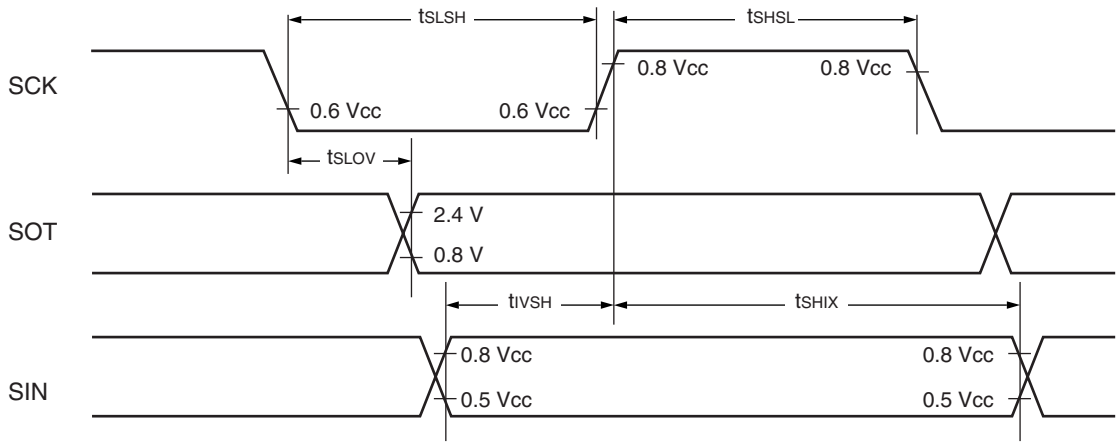
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock Cycle time	t_{SCYC}	SCK0	—	8 t_{CP}	—	ns	For internal shift clock mode output pin, C_L = 80 pF+1·TTL
SCK↓→ SOT delay time	t_{SLOV}	SCK0, SOT0		–80	+80	ns	
Valid SIN→ SCK↑	t_{IVSH}	SCK0, SIN0		100	—	ns	
SCK↑→ Valid SIN hold time	t_{SHIX}			60	—	ns	
Serial clock “H” pulse width	t_{SHSL}	SCK0	—	4 t_{CP}	—	ns	For external shift clock mode output pin, C_L = 80 pF+1·TTL
Serial clock “L” pulse width	t_{SLSH}			4 t_{CP}	—	ns	
SCK↓→ SOT delay time	t_{SLOV}	SCK0, SOT0		—	150	ns	
Valid SIN→ SCK↑	t_{IVSH}	SCK0, SIN0		60	—	ns	
SCK↑→ Valid SIN hold time	t_{SHIX}			60	—	ns	

Notes : • The above ratings are the values for clock synchronous mode.
• C_L is a load capacitance connected to pins during testing.

• Internal Shift Clock Mode



• External Shift clock Mode

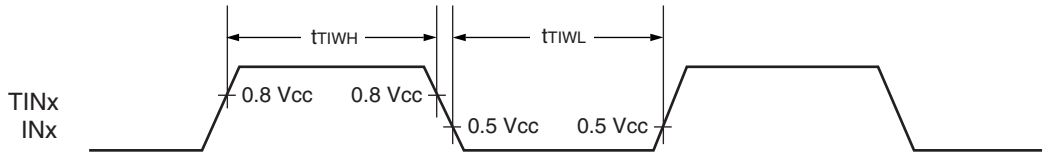


(8) Timer Input Timing

(T_A : Recommended operating conditions; V_{CC} = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH} t_{TIWL}	TIN0 to TIN2, PWC IN0 to IN3	—	4 t_{CP}	—	ns	

• Timer Input Timing

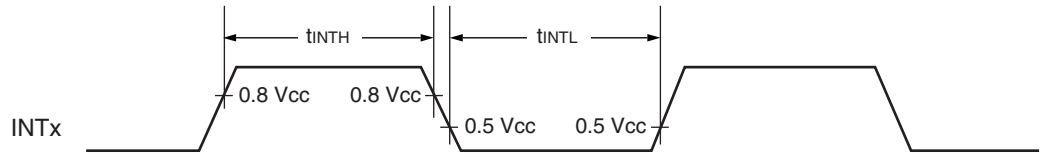


(9) External Interrupt Timing

(T_A : Recommended operating conditions; V_{CC} = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{INTH}, $_{INTL}$	INT0 to INT7	—	3 t_{CP}	—	ns	

• External interrupt input timing



Note : For INTx level detection time required to recover from the stop mode, add the stabilization time for the internal step-down circuit (12 µs).

6. A/D Converter Electrical Characteristics

(1) Electrical Characteristics

(T_A : Recommended operating conditions; $V_{CC} = AV_{CC} = 5.0$ V ±10%, $V_{SS} = AV_{SS} = 0.0$ V)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	±3.0	LSB	
Non-linearity error	—	—	—	—	±2.5	LSB	
Differential linearity error	—	—	—	—	±1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN31	AV_{SS} − 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	V	1 LSB = (AVRH − AV_{SS}) / 1024
Full-scale transition voltage	V_{FST}	AN0 to AN31	AVRH − 3.5 LSB	AVRH − 1.5 LSB	AVRH + 0.5 LSB	V	
Sampling time	t_{SMP}	—	1.375	—	—	µs	*1
Compare time	t_{CMP}	—	1.375	—	—	µs	*2
A/D conversion time	t_{CNV}	—	2.750	—	—	µs	*3
Analog port input current	I_{AIN}	AN0 to AN31	—	—	10	µA	$V_{AVSS} \leq V_{AIN} \leq V_{AVCC}$
Analog input voltage	V_{AIN}	AN0 to AN31	0	—	AVRH	V	
Standard voltage	AVR+	AVRH	4.0	—	AVcc	V	
Power supply current*4	I_A	AV_{CC}	—	2.4	4.7	mA	
	I_{AH}		—	—	5	µA	*5
Standard voltage supply current	I_R	AVRH	—	500	900	µA	V_{AVRH} = 5.0 V
	I_{RH}	AVRH	—	—	5	µA	*5
Variation between channels	—	AN0 to AN31	—	—	5	LSB	

*1 : When F_{CP} is 32 MHz : $t_{SMP} = (R_{ext} + Rin) \times Cin \times 7 = ST \times CLKP$ cycle = 2 channels × 31.25 ns = 1.375 µs

*2 : When F_{CP} is 32 MHz : $t_{CMP} = CKIN \times 11 = CT \times CLKP$ cycle × 11 = 4 h × 31.25 ns × 11 = 1.375 µs

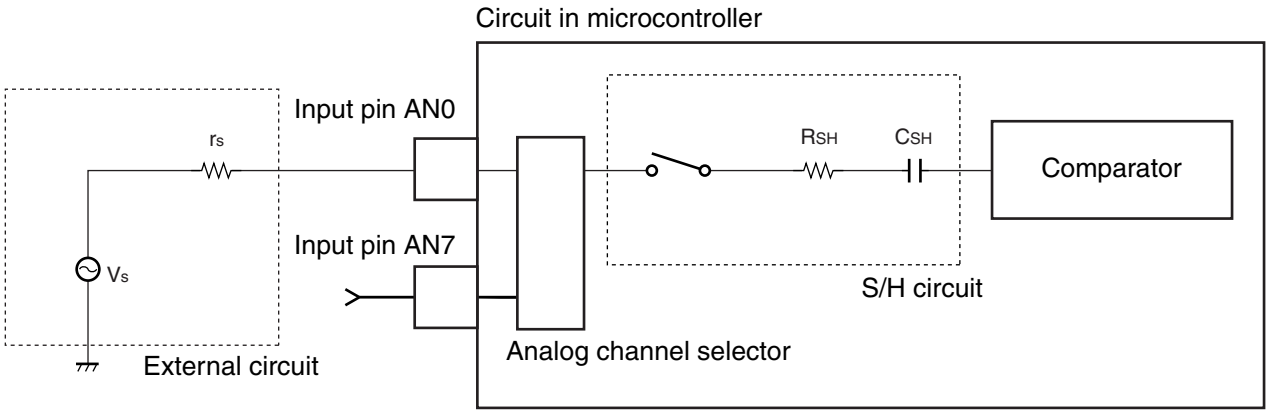
*3 : This represents the conversion time per channel when t_{SMP} and t_{CMP} are selected while F_{CP} is 32 MHz.

*4 : The current values are targeted temporary ratings.

*5 : This defines the power supply current when the A/D converter is not in operation and the CPU is stopped (at "Vcc = AVcc = AVRH = 5.0 V")

Notes :
- As AVRH becomes smaller, the error becomes greater.
- Use the output impedance r_S of the external circuit for analog input under the following conditions :
  Output impedance r_S of the external circuit = 5 kΩ (Max)
- If the output impedance of the external circuit is too high, the sampling time of the analog voltage may not be sufficient.
  When placing a DC blocking capacitor between the external circuit and input pin, set the capacitance to the value calculated by multiplying C_{SH} by several thousands as a guideline in order to minimize the impact from dividing voltage capacitance with C_{SH}.

• Analog Input Equivalent Circuit



<Recommended parameter values and tentative guideline for each element>

r_S = 5 kΩ or less

R_{SH} = approx. 2.5 kΩ

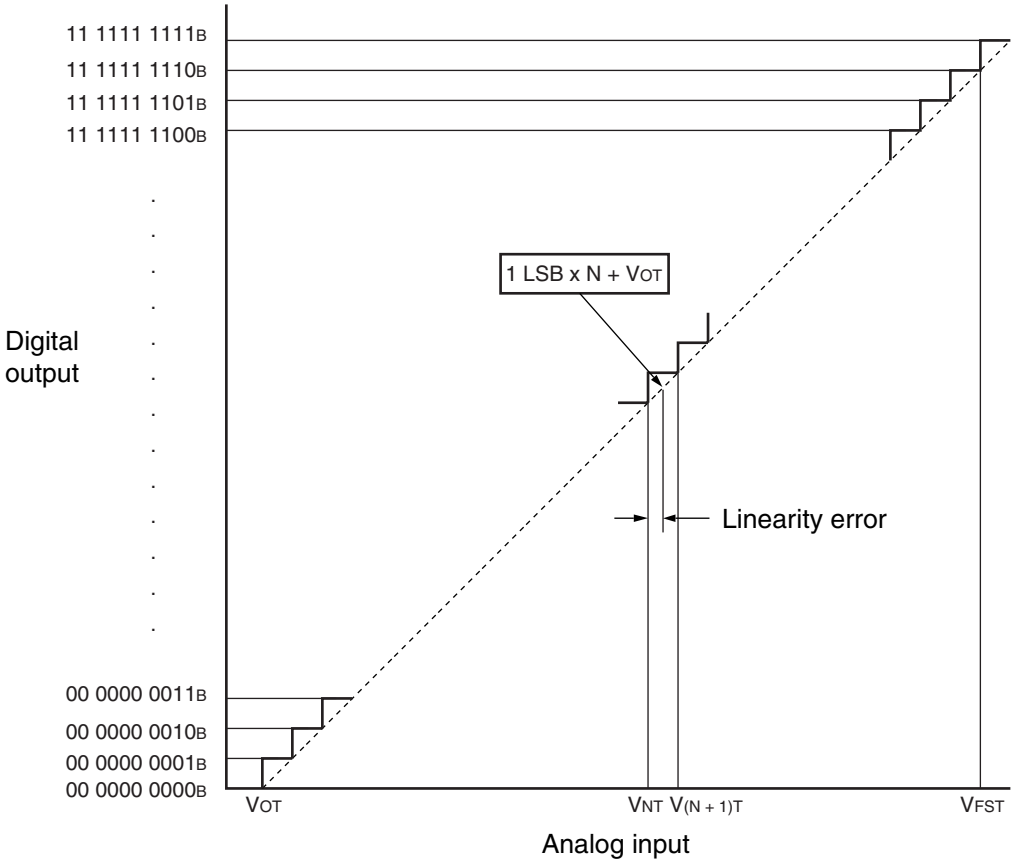
C_{SH} = approx. 10 pF

Note : These element parameters should be regarded as tentative values used only for design purposes. They are not guaranteed values.

(2) Term Definitions

- Resolution
  Level of analog variation that can be distinguished by the A/D converter.
  When the number of bits is 10, the analog voltage can be resolved into $2^{10} = 1024$.
- Total error
  Difference between actual and theoretical values, which is a total value derived from an offset error, gain error, non-linearity error and noise.
- Linearity error
  Deviation between the value along a straight line connecting the zero transition point (“00 0000 0000”←→ “00 0000 0001”) of a device and the full-scale transition point (“11 1111 1110”←→“11 1111 1111”) compared with the actual conversion values obtained.
- Differential linearity error
  Deviation of input voltage, which is required for changing output code by1 LSB, from an ideal value.

• 10-bit A/D Converter- Conversion Characteristics



$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}$$

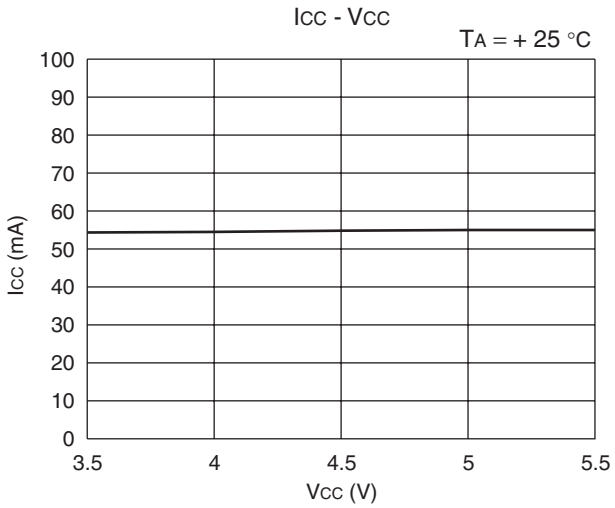
$$\text{Linearity error} = \frac{V_{NT} - (1\ \text{LSB} \times N + V_{OT})}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linearity error} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1 \quad [\text{LSB}]$$

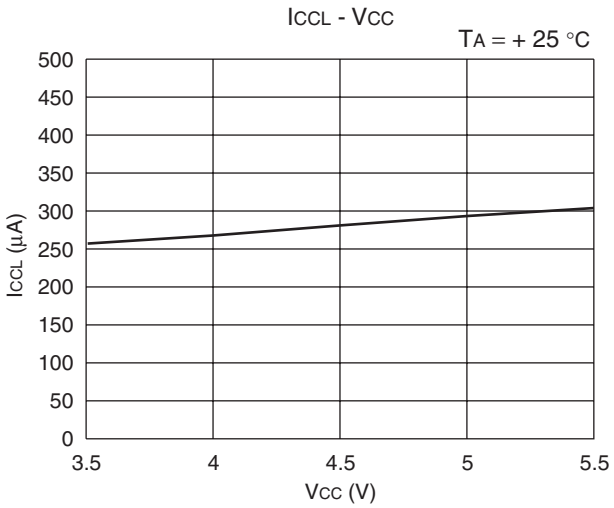
N : A/D converter digital output value.
V_{OT} : Voltage at which digital output transits from 000_H to 001_H.
V_{FST} : Voltage at which digital output transits from $3FE_H$ to $3FF_H$.
V_{NT} : A voltage at which digital output transits from (N – 1) to N.

■ EXAMPLE CHARACTERISTICS

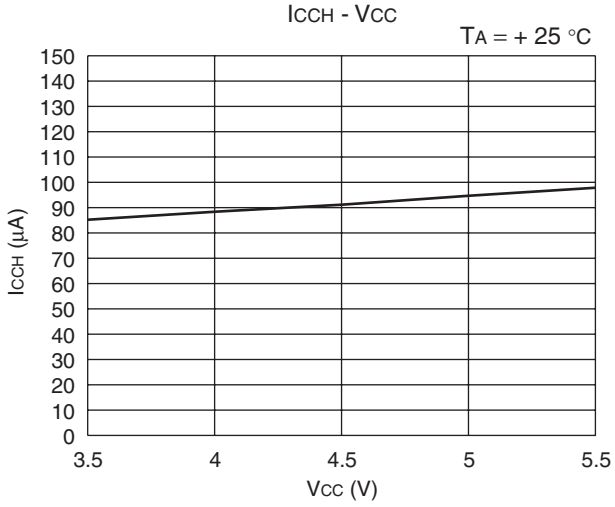
(1) Power supply current (at main RUN)



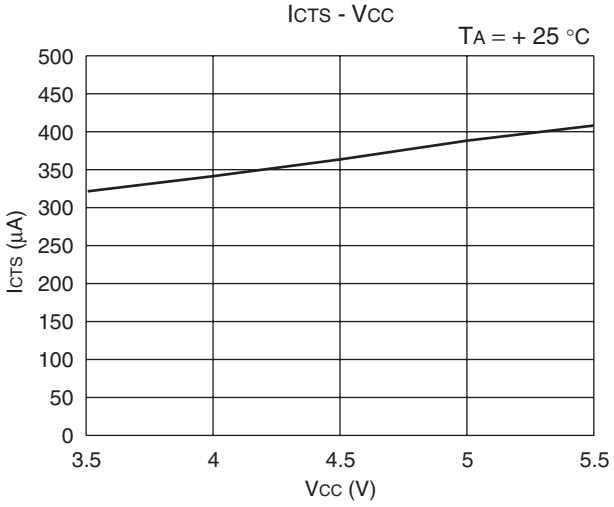
(2) Power supply current (at sub RUN)



(3) Power supply current (at stop : when oscillation stops)

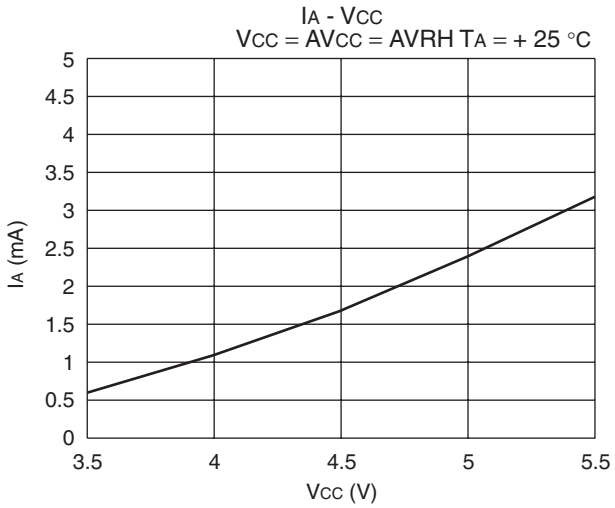


(4) Power supply current (at stop : when using RTC 4 MHz)

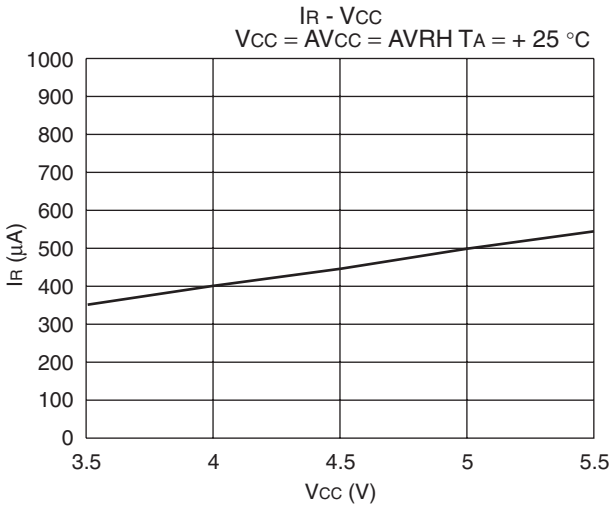


(Continued)

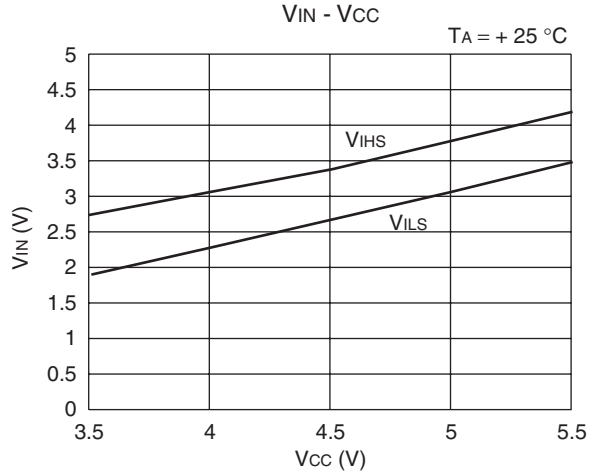
(5) A/D power supply current



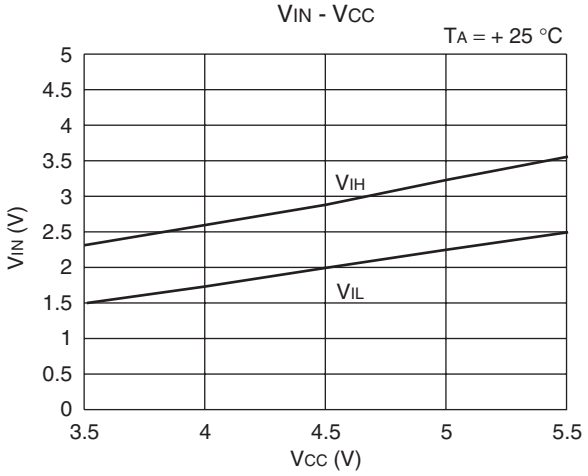
(6) A/D reference voltage supply current



(7) "H" level input voltage/"L" level input voltage (Automotive input)



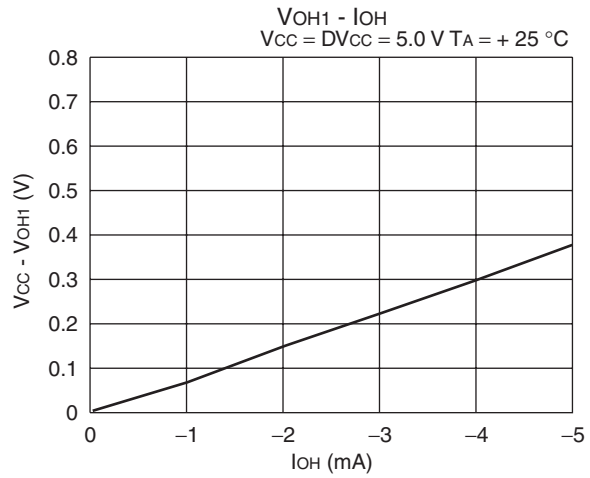
(8) "H" level input voltage/"L" level input voltage (CMOS hysteresis input)



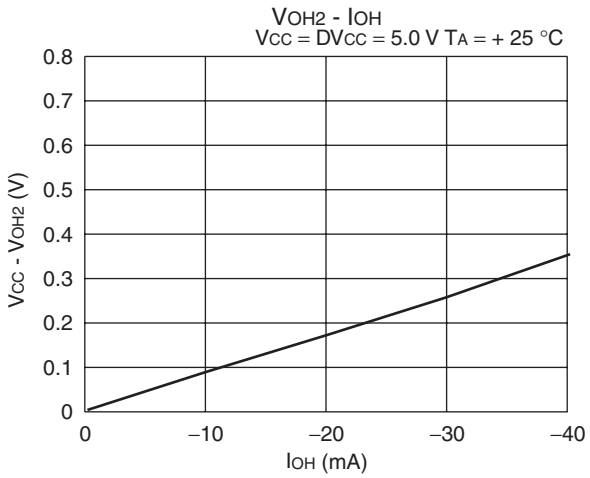
(Continued)

(Continued)

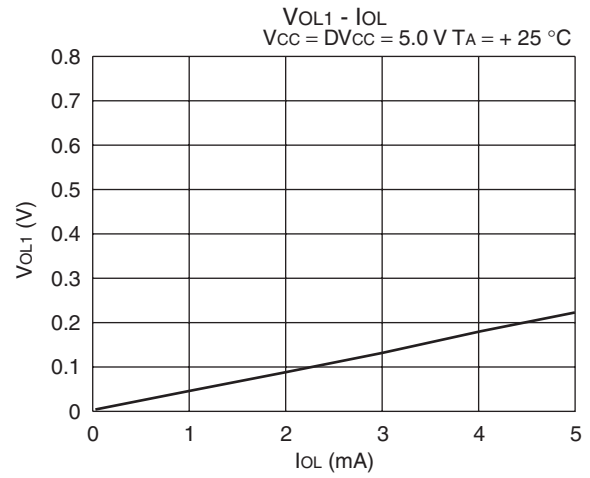
(9) “H” level output voltage



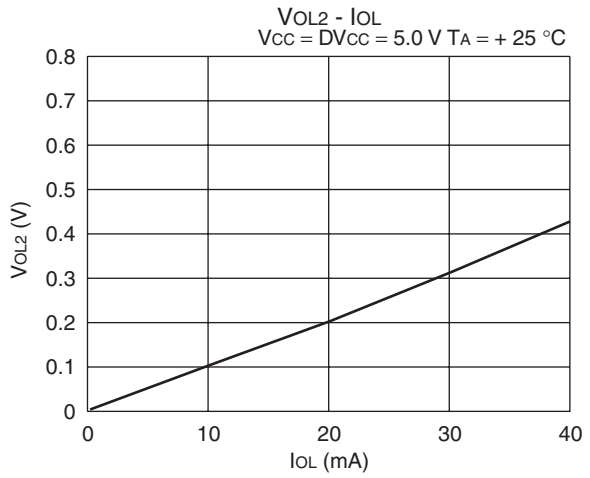
(10) “H” level output voltage



(11) “L” level output voltage



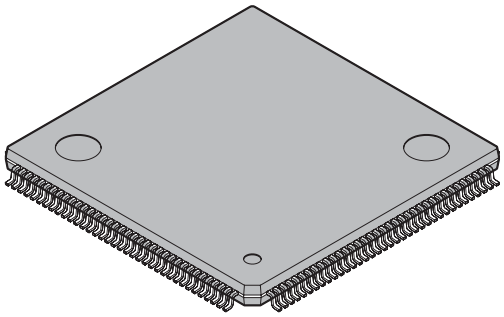
(12) “L” level output voltage



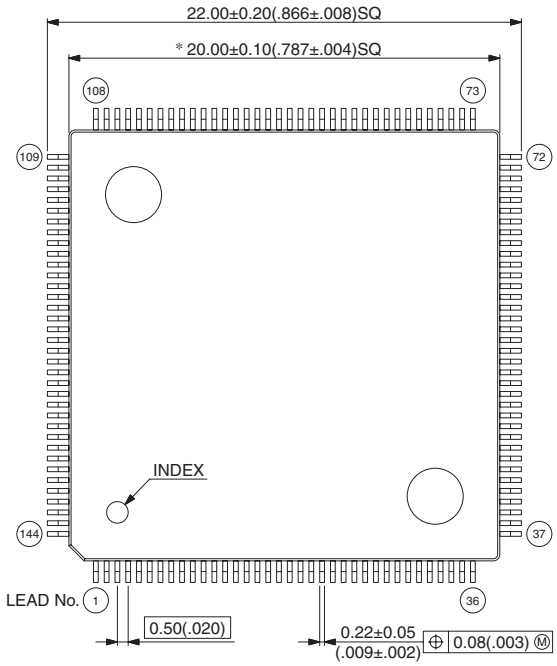
■ ORDERING INFORMATION

Part number	Package	Remarks
MB91V245ACR-ES	401-pin ceramic PGA (PGA-401C-A02)	Evaluation product
MB91F248PFV-GSE1	144-pin plastic LQFP (FPT-144P-M08)	Dual clock product
MB91F248SPFV-GSE1	144-pin plastic LQFP (FPT-144P-M08)	Single clock product
MB91247PFV-GSE1	144-pin plastic LQFP (FPT-144P-M08)	Dual clock product
MB91247SPFV-GSE1	144-pin plastic LQFP (FPT-144P-M08)	Single clock product
MB91248PFV-GSE1	144-pin plastic LQFP (FPT-144P-M08)	Dual clock product
MB91248SPFV-GSE1	144-pin plastic LQFP (FPT-144P-M08)	Single clock product

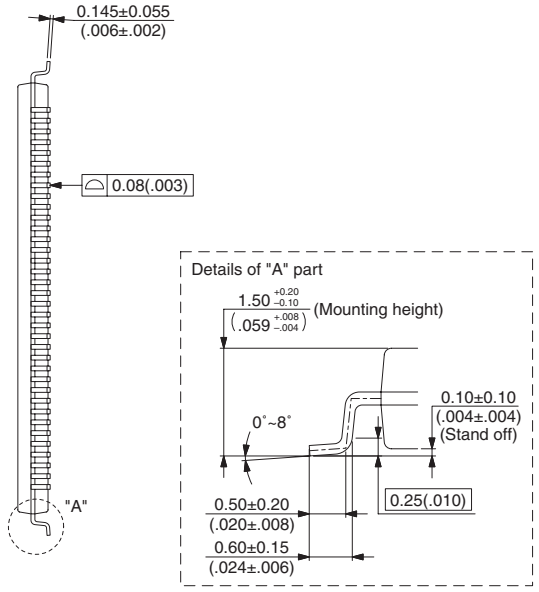
■ PACKAGE DIMENSION

144-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	20.0 × 20.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	1.20g
(FPT-144P-M08)	Code (Reference)	P-LFQFP144-20×20-0.50

144-pin plastic LQFP
(FPT-144P-M08)



Note 1) *:Values do not include resin protrusion.
Resin protrusion is +0.25(.010)Max(each side).
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

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Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/fj/DATASHEET/ef-ovpklv.html

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