OXFORD SEMICONDUCTOR

Data Sheet

OXU140CM
USB On-The-Go Full Speed Host, High Speed Peripheral with Multi-Storage Interface

Features

- Single-chip USB OTG full-speed host and high-speed peripheral controller
  - Reduces system cost and board space
  - Minimizes system design complexity and power
  - Simultaneous USB host, peripheral, and CE-ATA/MMC/SD interface operation
  - USB peripheral to CE-ATA/MMC/SD bridging
- Compatible with the USB 2.0 and OTG specifications
- CE-ATA 1.1 command support with built-in flow control
- MMC 4.1 compatible
  - Configurable 1-/4-/8-bit data bus at up to 48 MHz clock frequency
  - Dual-voltage (3.3 V and 1.8 V) I/O support
  - Integrated smart clock control for reduced power consumption
- 3.3 V power supply, flexible I/O voltage of 1.65 V to 3.6 V (LVCMOS/TTL) to interface to a wide range of MCUs
- Low-power sleep mode to minimize power consumption when not in use
- Integrated on-chip charge pump, supports up to 100 mA of current, enables support for broad range of USB devices
- Packaging
  - 8 × 8 mm BGA, 100 ball, RoHS compliant
  - 14 × 14 mm LQFP, 128 pin, RoHS compliant
- 16-bit memory mapped interface can gluelessly interface to most popular microprocessors and DSPs
- Fast microprocessor access cycle and double/multi buffering support for all four types of USB transfers
- Two DMA (slave) channel support for peripheral controller and CE-ATA/MMC/SD controller lowers CPU utilization
- Integrated PLL supports external crystal or crystal oscillators of 12 MHz or 30 MHz, for system flexibility

- 16 Kbytes of on-chip SRAM, optimized buffer size for performance and cost
- USB peripheral allows up to 8 bi-directional endpoints and transfers to enable support for multi-function systems
- Host Negotiation Protocol and Session Request Protocol implemented in hardware
- Transaction scheduling and transfer level protocol implemented in hardware (including data toggle, retry, and bandwidth management) for high performance

Device Overview

The Oxford Semiconductor OXU140CM is a single-chip USB On-The-Go (OTG) controller that incorporates a full-speed host, a high-speed peripheral controller, and a multi-storage interface that supports the following technologies:

- Consumer electronics advanced technology attachment (CE-ATA) HDDs
- MultiMediaCard (MMC)
- Secure Digital (SD)

The high-speed peripheral port offers high-data-rate transfers to and from host PCs. This is essential for devices such as smart phones, portable media players, car audio/navigation units, and personal storage devices, where media transfer times greatly impact the user experience. The full-speed host port enables the connection of a wide range of devices, such as flash drives, keyboards, mice, and digital still cameras. The OXU140CM low-power design is ideal for extending the battery life in mobile applications.

The multi-storage interface provides glueless support for CE-ATA hard drives. This new class of drives is designed for lower pin count, better power utilization, and a more efficient command protocol than existing hard drives, making it ideal for portable applications. The interface also supports MMC and SD flash memory devices, providing additional product flexibility in memory capacity expansion. The OXU140CM implements fast bridging between the USB peripheral port and the multi-storage interface, improving data transfer rates and minimizing CPU utilization.

The OXU140CM allows for simultaneous host and peripheral operation. The ports can be configured in one of two modes:

- One OTG port and one full-speed host port
- One high-speed peripheral port and two full-speed host ports

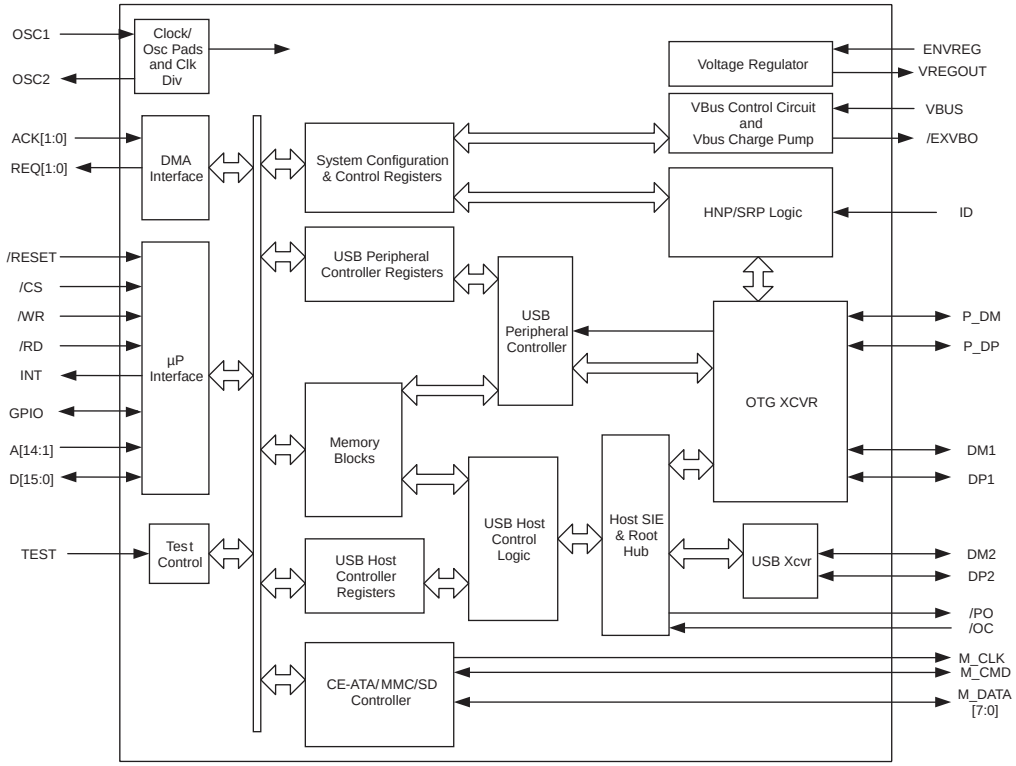
The multi-storage interface can be used in conjunction with either mode.

The OXU140CM is supported with USB device drivers and the Oxford Semiconductor USBLink™ product suite. The USBLink host, peripheral, and OTG stacks have been ported to a wide variety of real time operating system including VxWorks®, ThreadX®, and Nucleus®.

In addition, Oxford Semiconductor also makes available low-level controller drivers for other native USB stacks such as those included with Windows® CE and Linux® 2.6.x.

Figure 1 shows a block diagram of the OXU140CM.

Figure 1 OXU140CM Architectural Diagram



Development Support

The OXU140CM product suite includes the USB controller as well as the protocol stacks and the driver software that enable a wide variety of USB applications. This unique ability to deliver a total hardware and software solution sets Oxford Semiconductor apart from other semiconductor companies and benefits customers by:

- Shortening time to market
- Reducing risk
- Offering a single source for hardware & software, thereby reducing the number of suppliers the customer has to deal with

Oxford Semiconductor is a Microsoft® Windows® Embedded Partner and has developed host and peripheral controller drivers for Windows CE 5.0. Similar software support is also available for Linux® 2.6.x.

For customers using an RTOS such as VxWorks®, ThreadX®, Nucleus®, OSE, LynxOS®, and AMX™, among others, Oxford Semiconductor offers its USBLink host, peripheral and On-The-Go software solutions.

The USBLink Product Suite is a modularized approach to providing USB connectivity for a wide variety of embedded products. Due to its flexible architecture and broad based support for USB host, peripheral and OTG applications, Oxford Semiconductor can tailor the USBLink software deliverables to meet each customer's USB requirements.

The USBLink solutions are configurable and can support systems with:

- Big or little endian processors
- DMA or non-DMA USB controllers
- A wide variety of USB controllers, including the OXU140CM
- Complex to simple operating systems

Oxford Semiconductor has over eight years of experience developing embedded USB technology. Its USBLink software has been ported to twenty different operating systems and a wide variety of embedded architectures. USBLink is shipping in many millions of units.

Electrical Characteristics

Tables 1 to 11 detail the required operating conditions for the device and the DC and AC electrical characteristics.

Table 1 Absolute Maximum Device Ratings

Symbol	Parameter	Min	Max	Unit
$V_{DD3.3}$	3.3 V power supply	-0.3	4.0	V
$V_{DD1.8}$	1.8 V power supply	-0.3	2.16	V
V_{DDW}	1.8 V to 3.3 V wide-range I/O power supply	-0.3	4.0	V
V_I	DC input voltage	-0.3	4.0	V
T_S	Storage temperature	-40	+150	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the normal operating conditions specified in the following section. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2 Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
$V_{DD3.3}$	3.3 V power supply	2.97	3.63	V
$V_{DD1.8}$	1.8 V power supply	1.62	1.98	V
V_{DDW}	1.8 to 3.3 V wide-range I/O power supply	1.62	3.63	V
$V_{I3.3}$	DC input voltage of 3.3 V pins	0	3.6	V
V_{IW}	DC input voltage of wide-range pins	0	$1.1*V_{DDW}$	V
T_O	Operating temperature	-40	+85	°C

Table 3 DC Characteristics, Full-Speed USB I/O Signals: DP_N, DM_N

Symbol	Parameter	Condition	Min	Max	Unit
V_{DI}	Differential input sensitivity	$\|V_{I(DP_N)} - V_{I(DM_N)}\|$ (where N = 1 or 2)	0.2		V
V_{CM}	Differential comm. mode range		0.8	2.5	V
V_{OL}	Static output low		0.0	0.3	V
V_{OH}	Static output high		2.8	3.6	V
V_{CRS}	Output signal crossover		1.3	2.0	V
C_{IN}	Input capacitance			20	pF

Table 4 DC Characteristics, High-Speed USB I/O Signals: DP_P and DM_P Only

Symbol	Parameter	Condition	Min	Max	Unit
V_{HSDIFF}	High-speed differential input sensitivity	$\|V_{I(DP^P)} - V_{I(DM^P)}\|$	300		mV
V_{HSCM}	High-speed data signaling common mode range		-50	500	mV
V_{HSSQ}	High-speed squelch detection threshold	Squelch detected		100	mV
		No squelch detected	150		mV
V_{HSIO}	High-speed idle output voltage (differential)		-10	10	mV
V_{HSOL}	High-speed low-level output voltage (differential)		-10	10	mV
V_{HSOH}	High-speed high-level output voltage (differential)		-360	400	mV
V_{CHIRPK}	Chirp-K output voltage (differential)		-900	-500	mV

Table 5 DC Characteristics, Logic Signals

Symbol	Parameter	Condition	Min	Max	Unit
V_{OL}	Low-level output voltage			0.4	V
V_{OH}	High-level output voltage	V_{DDW} = 3.3 V	2.4		V
		V_{DDW} = 1.8 V	$0.75*V_{DDW}$		V
V_{IL}	Low-level input voltage	V_{DDW} = 3.3 V		0.8	V
		V_{DDW} = 1.8 V		$0.3*V_{DDW}$	V
V_{IH}	High-level input voltage	V_{DDW} = 3.3 V	2.0		V
		V_{DDW} = 1.8 V	$0.7*V_{DDW}$		V
C_{IN}	Input capacitance		2.2 (typical)		pF
C_{OUT}	Output capacitance		2.2 (typical)		pF
C_{BI}	Bi-directional capacitance		2.2 (typical)		pF
I_{IN}	Input leakage current	No pull up or pull down	-10	10	μA

Note: The capacitances listed above do not include pad capacitance and package capacitance. One can estimate pin capacitance by adding pad capacitance of about 0.5 pF; and the package capacitance, which is about 0.86 pF max for QFP and 0.42 pF max for BGA.

Table 6 DC Characteristics, ID Resistance

Symbol	Parameter	Condition	Min	Max	Unit
$R_{B\text{-}PLUG\text{-}ID}$	Resistance to ground on mini-B plug		100 K		Ω
$R_{A\text{-}PLUG\text{-}ID}$	Resistance to ground on mini-A plug			10	Ω

Table 7 DC Characteristics, Regulator

Symbol	Parameter	Condition	Min	Max	Unit
RV_{out}	Output voltage	Driving current <= 100 mA	1.8 (typical)		V
RI_{drive}	Driving current	$V_{DD3.3A}$ = 3.3 V Output voltage = 1.8 V		150	mA
Rt_{st}	Start-up time when enabled	$V_{DD3.3A}$ = 3.3 V RV_{out} = 1.62 V (90%)	25 (typical)		µs

Note: The $V_{DD3.3A}$ pin that corresponds to the regulator supply is QFP pin 106 and BGA pin B7.

Table 8 DC Characteristics, Charge Pump

Symbol	Parameter	Condition	Min	Max	Unit
CV_{out}	Output voltage	Driving current <= 100 mA	4.75	5.07	V
$V_{DD1.8}$	Driving current	$V_{CPSUPPLY}$ = 3.3 V Output voltage = 5 V		100	mA
V_{DDW}	Start-up time when enabled	$V_{CPSUPPLY}$ = 3.3 V RV_{out} = 4.5 V (90%)	400 (typical)		µs

Note: The charge pump supply $V_{CPSUPPLY}$ supplies the external components of the charge pump circuit.

Table 9 AC Characteristics, High-Speed DP_P and DM_P Driver Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
t_{HSR}	High-speed differential rise time		500		ps
t_{HSF}	High-speed differential fall time		500		ps
R_{DRV}	Driver output impedance	Equivalent resistance used as internal chip	40.5	49.5	Ω

Table 10 AC Characteristics, Full-Speed DP_1, DP_2, DM_1, DM_2 Driver Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
t_{FR}	Rise time	C_L = 50 pF	4	20	ns
t_{FF}	Fall time	C_L = 50 pF	4	20	ns
t_{FRFM}	T_R/T_F matching		90	110	%
Z_{DRV}	Driver output resistance	Steady state drive with external 33 Ω series resistor	3	9	Ω

Table 11 AC Characteristics, Low-Speed DP_1, DP_2, DM_1, DM_2 Driver Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
t_{LR}	Rise time	C_L = 200 - 600 pF	75	300	ns
t_{LF}	Fall time	C_L = 200 - 600 pF	75	300	ns
t_{FRFM}	T_R/T_F matching		80	125	%

Power Consumption

Table 12 gives typical power consumption figures for the OXU140CM.

Table 12 OXU140CM Power Consumption

	Condition	Min	Max	Unit
Host operational current	ENVREG = 1		30	mA
Peripheral operational current	High-speed, ENVREG = 1		75	mA
	Full-speed, ENVREG = 1		50	mA
Host suspend state current	ENVREG = 1	150 (typical)		µA
Peripheral suspend state current	ENVREG = 1	400 (typical)		µA
MMC host operational current	ENVREG = 1		45	mA
MMC host suspend current	ENVREG = 1	150 (typical)		µA
Power save state current	ENVREG = 1	150 (typical)		µA

The above measurements are at typical process corner and room temperature and do not account for process and temperature variations.

Peripheral operational current is measured with a 5 m cable with maximum switching and BULK OUT transfers at 400 Mbps with 92.6% bus utilization during one microframe. The actual average current in customer applications will be lower.

MMC host operation current is measured with 8-bit at 48 MHz writing 55AA pattern to an MMC 4.1 card at 15 Mbps throughput. The actual average operational current will vary base on the data pattern and throughput rates supported by the attached device.

ENVREG = 1 enables the internal voltage regulator.

Pin Layout

The OXU140CM is supplied as a 128-pin LQFP package and as a 100-ball BGA package. Figure 2 shows the chip layout of the 128-pin LQFP package.

Figure 2 OXU140CM 128-Pin LQFP Package (Top View)

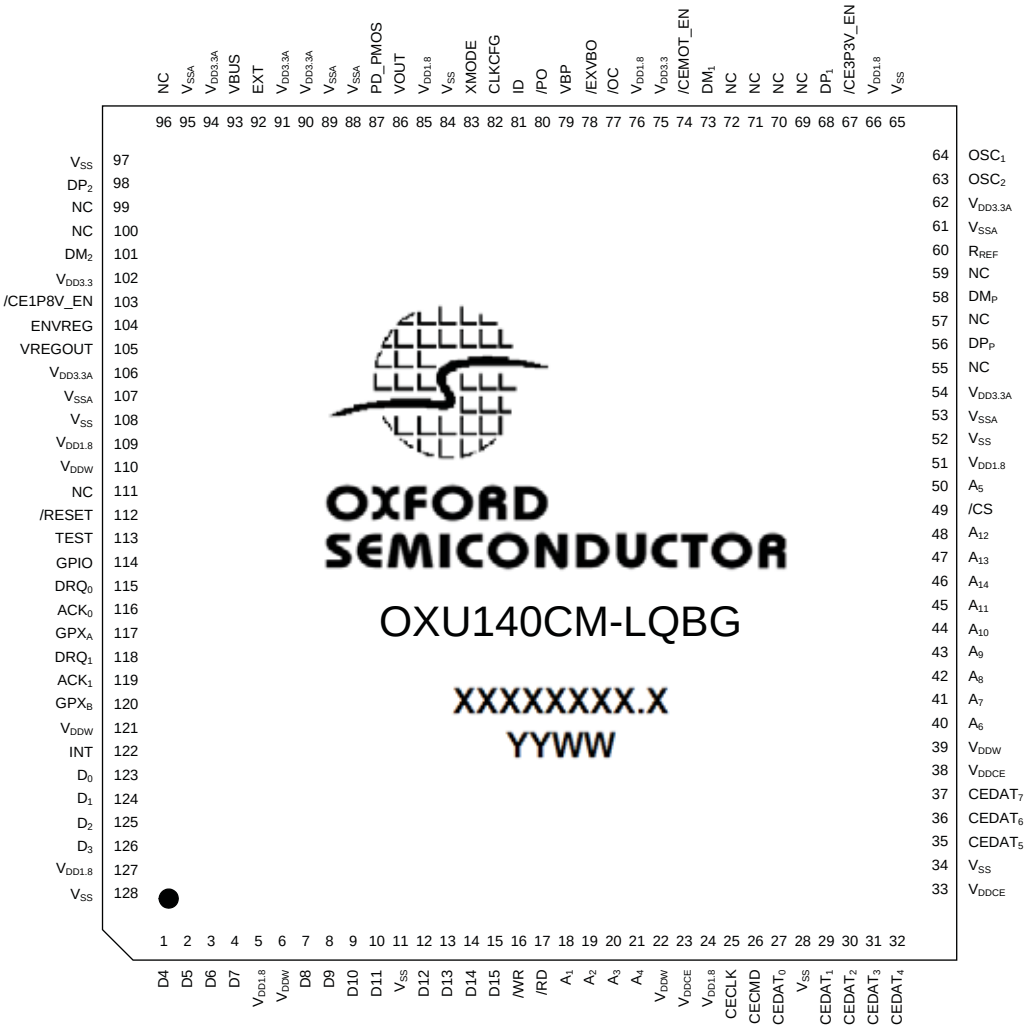


Table 13 lists the LQFP pin allocations.

*Table 13 OXU140CM **128-Pin LQFP** Pin Allocations (Sheet 1 of 3)*

Pin	No. Pins	Type(1)	Name	Description
Processor Interface (39 pins)				
1, 2, 3, 4, 7, 8, 9, 10, 12, 13, 14, 15, 123, 124, 125, 126	16	MSBCT	D_0 - D_{15}	16-bit data bus
18, 19, 20, 21, 40, 41, 42, 43, 44, 45, 46, 47, 48, 50	14	MSI	A_1 - A_{14}	Address bus for direct address space
16	1	MSIU	/WR	Write strobe
17	1	MSIU	/RD	Read strobe
49	1	MSIU	/CS	Chip select
122	1	MOCT	/INT	Interrupt to the MCU.This pin can be software configured as a driven output or open drain. Open drain is the default
112	1	MSIVI	/RESET	Hardware reset
118, 115	2	MOCT	DRQ_1, DRQ_0	DMA request outputs to support two channels
119, 116	2	MSI	ACK_1, ACK_0	DMA acknowledge
General Purpose I/O (3 pins)				
114, 117, 120	3	MSBC	GPIO, GPX_A, GPX_B	General purpose I/O
Power & Ground (39 pins)				
54, 62, 90, 91, 94, 106	6		$V_{DD3.3A}$	Analog +3.3 V power
53, 61, 88, 89, 95, 107	6		V_{SSA}	Analog ground
75, 102	2		$V_{DD3.3}$	Digital +3.3 V power
5, 24, 51, 66, 76, 85, 109, 127	8		$V_{DD1.8}$	1.8 V core power. VREGOUT may be used for the supplies
6. 22, 39, 110, 121	5		V_{DDW}	Wide-range I/O +1.65 V to +3.6 V for the processor interface
23, 33, 38	3		V_{DDCE}	Wide-range I/O +1.65 V to +3.6 V for the media port
11, 28, 34, 52, 65, 84, 97, 108, 128	9		V_{SS}	Digital/wide-range I/O ground
USB Interface (13 pins)				
58, 56	2	B	DM_P, DP_P	Data lines for USB peripheral port, which may serve as an OTG port in combination with host port 1. If not used, these two pins should be left floating
73, 68	2	B	DM_1, DP_1	Data lines for Host Port 1, which may serve as a USB host or an OTG port in combination with the peripheral port. If not used, these two pins should be left floating

*Table 13 OXU140CM **128-Pin LQFP** Pin Allocations (Sheet 2 of 3)*

Pin	No. Pins	Type[(1)]	Name	Description
101, 98	2	B	DM_2, DP_2	Data lines for Host Port 2, a dedicated USB host port. If not used, these two pins should be left floating
60	1	B	R_{REF}	Connect external reference resistor (12 KΩ +/- 1%) to V_{SSA}
93	1	5I	VBUS	VBUS input used by the voltage comparators of the OTG port for connection. This pin should be left floating in a host-only application
79	1	O	VBP	V_{BUS} pulsing control. This pin is used only when Port 1 is an OTG port for a B-DEVICE.
78	1	O	/EXVBO	Turn on/off the external V_{BUS} (5 V) for OTG operation (1:V_{BUS} off, 0: V_{BUS} on) when using the external charge pump
77	1	IU	/OC	Over current condition indicator for powered host ports
81	1	IU	ID	Connected to the ID pin of the mini-AB connector for OTG applications. With the help of an internal pull-up resistor, this pin determines the chip's responsibility in an OTG application (0: A-device, 1:B-device)
80	1	O	/PO	Turn on/off gang power for all host ports
Clock Interface (3 pins)				
82	1	I	CLKCFG	The state of this pin is used to indicate whether a 12 MHz or a 30 MHz crystal/oscillator is being used. CLKCFG -- Frequency 0--12-MHz crystal; 12-MHz 3.3 V oscillator input on OSC1 1--30-MHz crystal; 30-MHz 3.3 V oscillator input on OSC1
64	1	I	OSC_1	A 12-MHz or 30-MHz passive crystal should be connected across the two pins. Optionally, a 12 MHz or 30-MHz oscillator can be connected to OSC1 while keeping OSC2 unconnected
63	1	O	OSC_2	
MMC/CE-ATA (13 pins)				
25	1	MO	CECLK	SD/MMC/CE-ATA CLK output (0-48 MHz)
26	1	MBUS	CECMD	SD/MMC/CE-ATA CMD
37, 36, 35, 32, 31, 30, 29, 27	8	MBUS	CEDAT[7:0]	SD/MMC/CE-ATA 1,4 or 8-bit data bus
67	1	O	/CE3P3V_EN	On/off control for MMC 3.3 V interface power
103	1	O	/CE1P8V_EN	On/off control for MMC 1.8 V interface power
74	1	O	/CEMOT_EN	On/off control for HDD motor power
Internal VBUS Charge Pump (3 pins)				
87	1	O	PD_PMOS	Internal charge pump output for P-MOSFET (optional switch on the VOUT)
92	1	O	EXT	Internal charge pump output for N-MOSFET
86	1	I	VOUT	Internal charge pump output voltage feedback pin

*Table 13 OXU140CM **128-Pin LQFP** Pin Allocations (Sheet 3 of 3)*

Pin	No. Pins	Type(1)	Name	Description
Internal Voltage Regulator (2 pins)				
104	1	I	ENVREG	Enables the internal voltage regulator if asserted. If not used, this pin should be tied to V_{SS}
105	1	O	VREGOUT	Internal voltage regulator output of 1.8 V. If enabled, this output should be connected to the $V_{DD1.8}$ supplies of the chip. If the regulator is disabled, this pin should be treated as another $V_{DD1.8}$ supply input to the chip
Test (2 pins)				
83	1	I	XMODE	Xcrv test mode. This pin should be grounded for normal operation
113	1	ID	TEST	Factory test mode. This pin should be grounded or left floating (has an internal pull-down) for normal operation
Miscellaneous (11 pins)				
55, 57, 59, 69, 70, 71 72, 96, 99, 100,111	1		NC	No connection. These pins should be left floating

Note to Table 13: 1 Type key: format is [(L)(W_)X(Y)(_Z(T))] where the following conventions apply:

L—Logic Level		W—Tolerance		X—Type		Y—Pull		Z—Drive	T—Tristate	
M(2)	Multi-voltage: 3.3 V CMOS 2.5 V CMOS 1.8 V CMOS	5	5 V	I	Input	U	Pull up	C(3)	T	Tristate
			3.3 V	O	Output	D	Pull down			Normal
S	Schmitt Trigger			B	Bidirectional		None			

2 Program to 3.3 V, 2.5 V, or 1.8 V by setting the V_{IO} voltage level.

3 Program to 2 mA, 4 mA, 6 mA, 8 mA, 10 mA, 12 mA, 14 mA, or 16 mA.

Figure 3 shows the chip layout of the 100-ball BGA package.

Figure 3 OXU140CM 100-Ball BGA Package (Top View)

	A	B	C	D	E	F	G	H	J	K
10	DP_2	V_{SSA}	VBUS	V_{SSA}	ID	/OC	/EXVBO	/CPE3P3V_EN	V_{SSA}	OSC_2
9	DM_2	/CPE1P8V_EN	$V_{DD3.3A}$	VOUT	CLKCFG	/PO	/CEMOT_EN	DP_1	DP_P	$V_{DD3.3A}$
8	VREGOUT	ENVREG	$V_{DD3.3A}$	EXT	XMODE	VBP	DM_1	DM_P	$V_{DD3.3A}$	OSC_1
7	GPIO	$V_{DD3.3A}$	V_{SSA}	$V_{DD3.3}$	PD_PMOS	$V_{DD1.8}$	$V_{DD1.8}$	V_{SSA}	A_5	R_{REF}
6	TEST	NC (GP12)	/RESET	$V_{DD3.3}$	V_{SS}	V_{SS}	A_{14}	A_{12}	A_{13}	/CS
5	GPX_A	DRQ_0	DRQ_1	V_{DDW}	V_{DDW}	V_{SS}	V_{DDCE}	A_9	A_{11}	A_{10}
4	ACK_0	ACK_1	GPX_B	/INT	D_{12}	$V_{DD1.8}$	$CEDAT_2$	A_6	A_7	A_8
3	D_1	D_0	D_3	D_{10}	D_{13}	/WR	A_1	$CEDAT_0$	$CEDAT_7$	$CEDAT_6$
2	D_5	D_2	D_8	D_{11}	D_{14}	A_2	A_4	CECLK	$CEDAT_1$	$CEDAT_4$
1	D_7 ●	D_4	D_6	D_9	D_{15}	/RD	A_3	CECMD	$CEDAT_3$	$CEDAT_5$

Table 14 lists the BGA pin allocations.

*Table 14 OXU140CM **100-Ball BGA** Pin Allocations (Sheet 1 of 3)*

Pin	No. Pins	Type[(1)]	Name	Description
Processor Interface (39 pins)				
B3, A3, B2, C3, B1, A2, C1, A1, C2, D1, D3, D2, E4, E3, E2, E1	16	MSBCT	D_0 - D_{15}	16-bit data bus
G3, F2, G1, G2, J7, H4, J4, K4, H5, K5, J5, H6, J6, G6	14	MSID	A_1 - A_{14}	Address bus for direct address space
F3	1	MSIU	/WR	Write strobe
F1	1	MSIU	/RD	Read strobe
K6	1	MSIU	/CS	Chip select
D4	1	MOCT	/INT	Interrupt to the MCU.This pin can be software configured as a driven output or open drain. Open drain is the default
C6	1	MSIU	/RESET	Hardware reset
C5, B5	2	MOCT	DRQ_1, DRQ_0	DMA request outputs to support two channels
B4, A4	2	MSI	ACK_1, ACK_0	DMA acknowledge
General Purpose I/O (3 pins)				
A7, A5, C4	3	MSBC	GPIO, GPX_A, GPX_B	General purpose I/O
Power & Ground (21 pins)				
B7, C8, C9, J8, K9	5		$V_{DD3.3A}$	Analog +3.3 V power
B10, C7, D10, H7, J10	5		V_{SSA}	Analog ground
D6, D7	2		$V_{DD3.3}$	Digital +3.3 V power
F4, F7, G7	3		$V_{DD1.8}$	1.8 V core power. VREGOUT may be used for the supplies
D5. E5	2		V_{DDW}	Wide-range I/O +1.65 V to +3.6 V for the processor interface
G5	1		V_{DDCE}	Wide-range I/O +1.65 V to +3.6 V for the media port
E6, F5, F6	3		V_{SS}	Digital/wide-range I/O ground
USB Interface (13 pins)				
H8 J9	2	B	DM_P, DP_P	Data lines for USB peripheral port, which may serve as an OTG port in combination with host port 1. If not used, these two pins should be left floating
G8, H9	2	B	DM_1, DP_1	Data lines for Host Port 1, which may serve as a USB host or an OTG port in combination with the peripheral port. If not used, these two pins should be left floating

*Table 14 OXU140CM **100-Ball BGA** Pin Allocations (Sheet 2 of 3)*

Pin	No. Pins	Type[(1)]	Name	Description
A9, A10	2	B	DM_2, DP_2	Data lines for Host Port 2, a dedicated USB host port. If not used, these two pins should be left floating
K7	1	B	R_{REF}	Connect external reference resistor (12 KΩ +/- 1%) to V_{SSA}
C10	1	5I	VBUS	VBUS input used by the voltage comparators of the OTG port for connection. This pin should be left floating in a host-only application
F8	1	O	VBP	V_{BUS} pulsing control. This pin is used only when Port 1 is an OTG port for a B-DEVICE.
G10	1	O	/EXVBO	Turn on/off the external V_{BUS} (5 V) for OTG operation (1:V_{BUS} off, 0: V_{BUS} on) when using the external charge pump
F10	1	P5IU	/OC	Over current condition indicator for powered host ports
E10	1	IU	ID	Connected to the ID pin of the mini-AB connector for OTG applications. With the help of an internal pull-up resistor, this pin determines the chip's responsibility in an OTG application (0: A-device, 1:B-device)
F9	1	O	/PO	Turn on/off gang power for all host ports
Clock Interface (3 pins)				
E9	1	I	CLKCFG	The state of this pin is used to indicate whether a 12 MHz or a 30 MHz crystal/oscillator is being used. CLKCFG -- Frequency 0--12-MHz crystal; 12-MHz 3.3 V oscillator input on OSC1 1--30-MHz crystal; 30-MHz 3.3 V oscillator input on OSC1
K8	1	I	OSC_1	A 12-MHz or 30-MHz passive crystal should be connected across the two pins. Optionally, a 12 MHz or 30-MHz oscillator can be connected to OSC1 while keeping OSC2 unconnected
K10	1	O	OSC_2	
MMC/CE-ATA (13 pins)				
J3, K3, K1, K2, J1, G4, J2, H3	8	MBUS	CEDAT[7:0]	SD/MMC/CE-ATA 1,4 or 8-bit data bus
H10	1	O	/CE3P3V_EN	On/off control for MMC 3.3 V interface power
B9	1	O	/CE1P8V_EN	On/off control for MMC 1.8 V interface power
G9	1	O	/CEMOT_EN	On/off control for HDD motor power
H2	1	MO	CECLK	SD/MMC/CE-ATA CLK output (0-48 MHz)
H1	1	MBUS	CECMD	SD/MMC/CE-ATA CMD
Internal VBUS Charge Pump (3 pins)				
E7	1	O	PD_PMOS	Internal charge pump output for P-MOSFET (optional switch on the VOUT)
D8	1	O	EXT	Internal charge pump output for N-MOSFET
D9	1	I	VOUT	Internal charge pump output voltage feedback pin

*Table 14 OXU140CM **100-Ball BGA** Pin Allocations (Sheet 3 of 3)*

Pin	No. Pins	Type(1)	Name	Description
Internal Voltage Regulator (2 pins)				
B8	1	I	ENVREG	Enables the internal voltage regulator if asserted. If not used, this pin should be tied to V_{SS}
A8	1	O	VREGOUT	Internal voltage regulator output of 1.8 V. If enabled, this output should be connected to the $V_{DD1.8}$ supplies of the chip. If the regulator is disabled, this pin should be treated as another $V_{DD1.8}$ supply input to the chip
Test (2 pins)				
E8	1	I	XMODE	Xcrv test mode. This pin should be grounded for normal operation
A6	1	ID	TEST	Factory test mode. This pin should be grounded or left floating (has an internal pull-down) for normal operation
Miscellaneous (1 pin)				
B6	1		NC	No connection. These pins should be left floating

Note to Table 14: 1 Type key: format is [(L)(W_)X(Y)(_Z(T))] where the following conventions apply:

L—Logic Level		W—Tolerance		X—Type		Y—Pull		Z—Drive	T—Tristate	
M(2)	Multi-voltage: 3.3 V CMOS 2.5 V CMOS 1.8 V CMOS	5	5 V	I	Input	U	Pull up	C(3)	T	Tristate
			3.3 V	O	Output	D	Pull down			Normal
S	Schmitt Trigger			B	Bidirectional		None			

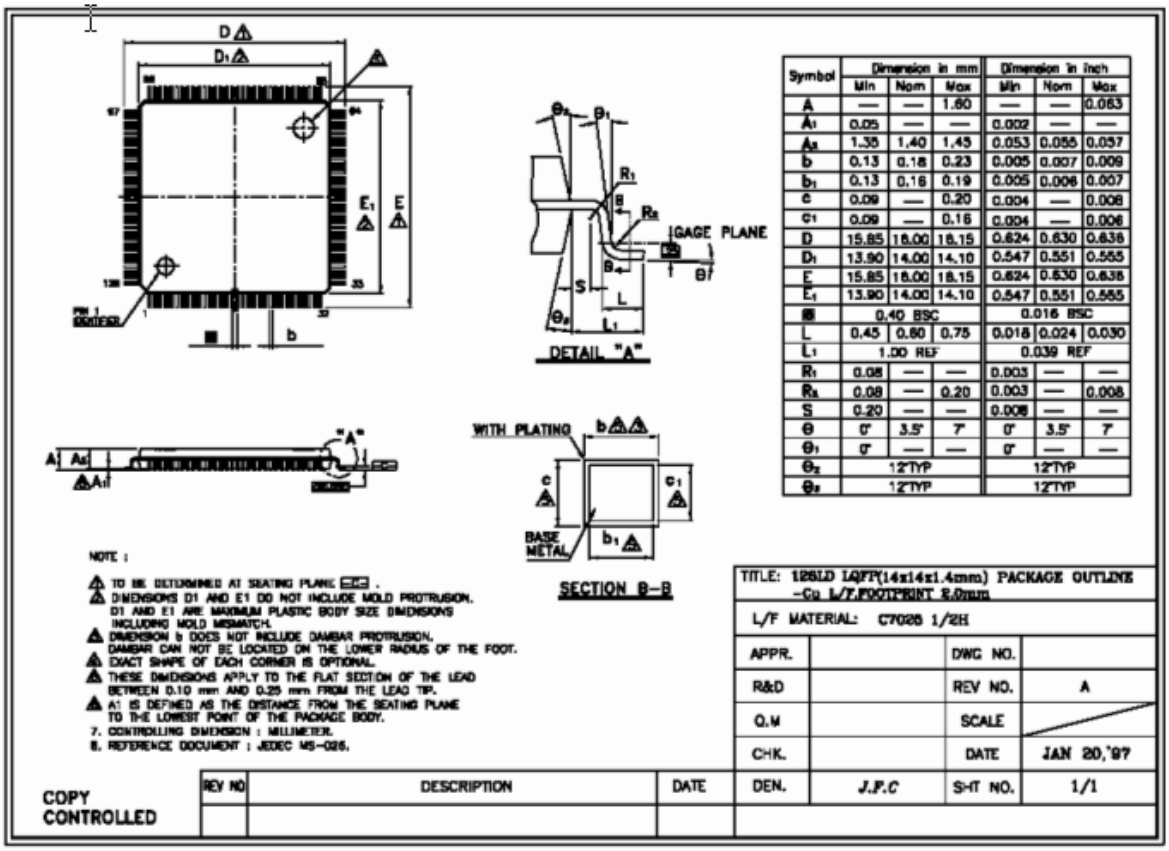
2 Program to 3.3 V, 2.5 V, or 1.8 V by setting the V_{IO} voltage level.

3 Program to 2 mA, 4 mA, 6 mA, 8 mA, 10 mA, 12 mA, 14 mA, or 16 mA.

Package Layout

Figure 4 shows the package layout for the 128-pin LQFP package.

Figure 4 128-Pin LQFP Package



Symbol	Dimension in mm			Dimension in Inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	—	0.002	—	—
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	—	0.16	0.004	—	0.006
D	15.85	16.00	16.15	0.624	0.630	0.636
D1	13.90	14.00	14.10	0.547	0.551	0.555
E	15.85	16.00	16.15	0.624	0.630	0.636
E1	13.90	14.00	14.10	0.547	0.551	0.555
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	12°TYP			12°TYP		
θ3	12°TYP			12°TYP		

Figure 5 shows the layout for the 100-ball TFBGA.

Figure 5 100-Ball TFBGA Package

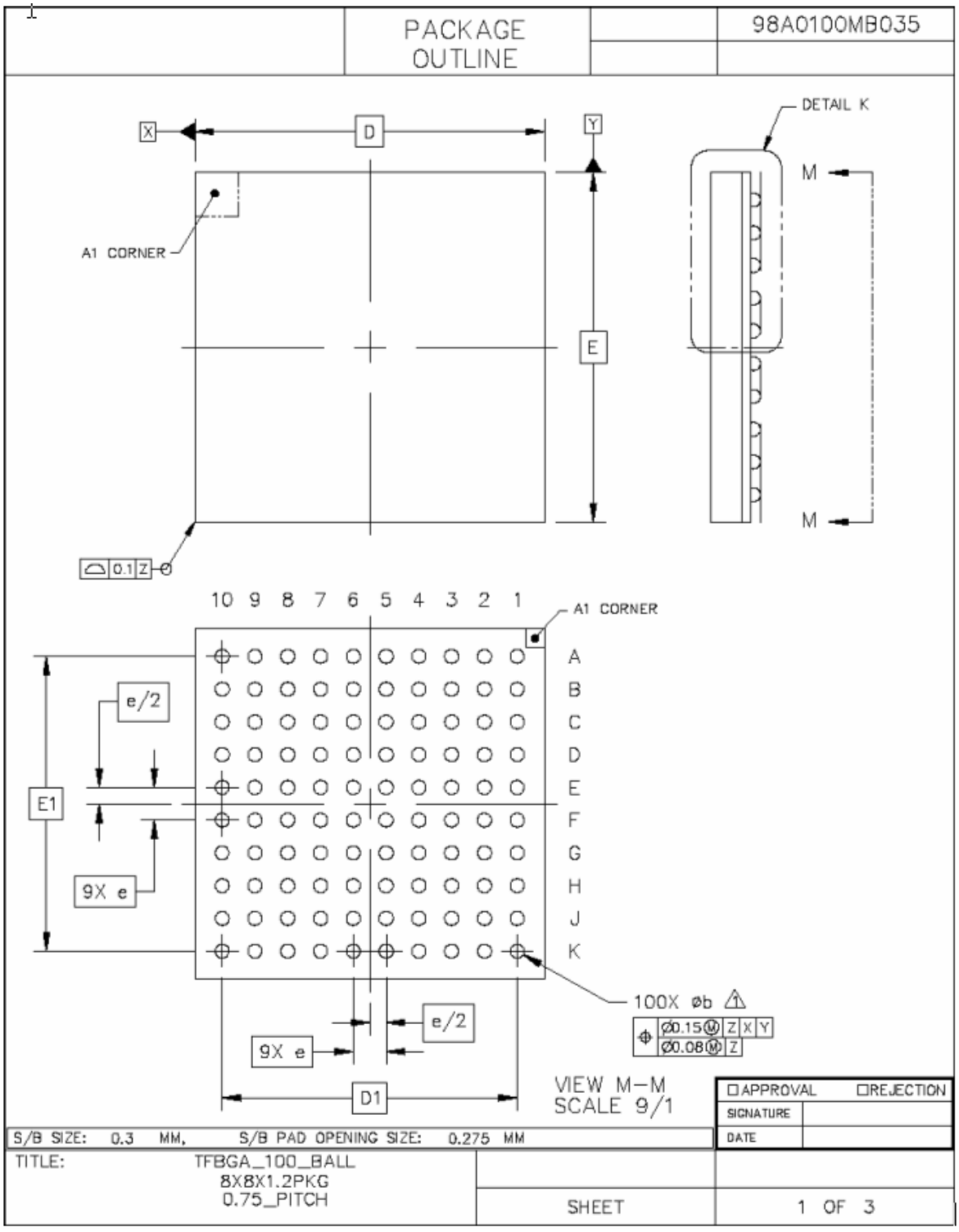
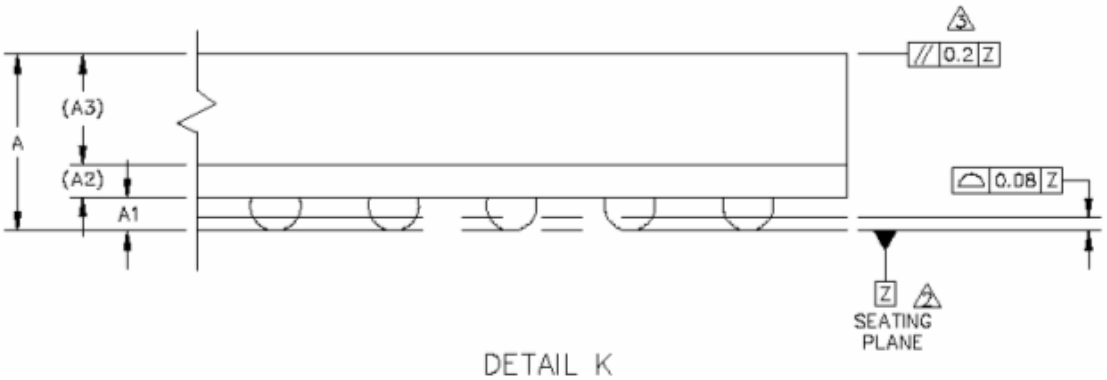


Figure 5 100-Ball TFBGA Package (continued)

	PACKAGE OUTLINE		98A0100MB035
			001



DETAIL K
SCALE 25/1
(ROTATE 90°)

DIM	MIN.	NOR.	MAX.
A	---		1.2
A1	0.16		0.26
A2		0.21 REF	
A3		0.7 REF	
b	0.27		0.37
D		8 BSC	
E		8 BSC	
e		0.75 BSC	
D1		6.75 BSC	
E1		6.75 BSC	

NOTES

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
2. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

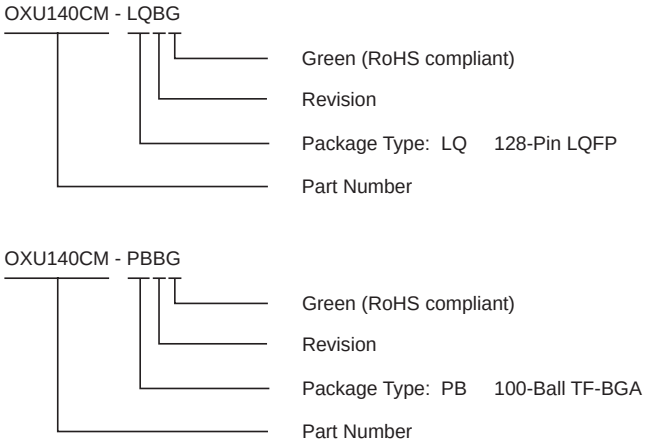
UNIT	DIMENSION AND TOLERANCES	REFERENCE DOCUMENT
UNIT	ASME_Y14.5M	REFERENCE_DOCUMENT

TITLE: TFBGA_100_BALL 8X8X1.2PKG 0.75_PITCH

SHEET 2 OF 3

Ordering Information

The following conventions are used to identify Oxford Semiconductor products:



Contacting Oxford Semiconductor

See the Oxford Semiconductor website (http://www.oxsemi.com) for further details about Oxford Semiconductor devices, or email sales@oxsemi.com.

Revision Information

Table 15 documents the revisions of this guide.

Table 15 Revision Information

Revision	Modification
Jul 06	First publication

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