256MB – 32Mx64 SDRAM, UNBUFFERED

FEATURES

- Burst Mode Operation
- Auto and Self Refresh capability
- LVTTL compatible inputs and outputs
- Serial Presence Detect with EEPROM
- Fully synchronous: All signals are registered on the positive edge of the system clock
- Programmable Burst Lengths: 1, 2, 4, 8 or Full Page
- 3.3V± 0.3V Power Supply
- 144 Pin SO-DIMM
  - D1: 27.94mm (1.10")

NOTE: Consult factory for availability of:
- Lead-Free Products
- Vendor source control options
- Industrial temperature option

DESCRIPTION

The W3DG6433V is a 32Mx64 synchronous DRAM module which consists of four 32Mx16 SDRAM components in TSOP II package, and one 2Kb EEPROM in an 8 pin TSSOP package for Serial Presence Detect which are mounted on a 144 pin SO-DIMM multilayer FR4 Substrate.

* This product is subject to change without notice.

PIN CONFIGURATIONS (FRONT SIDE/BACK SIDE)

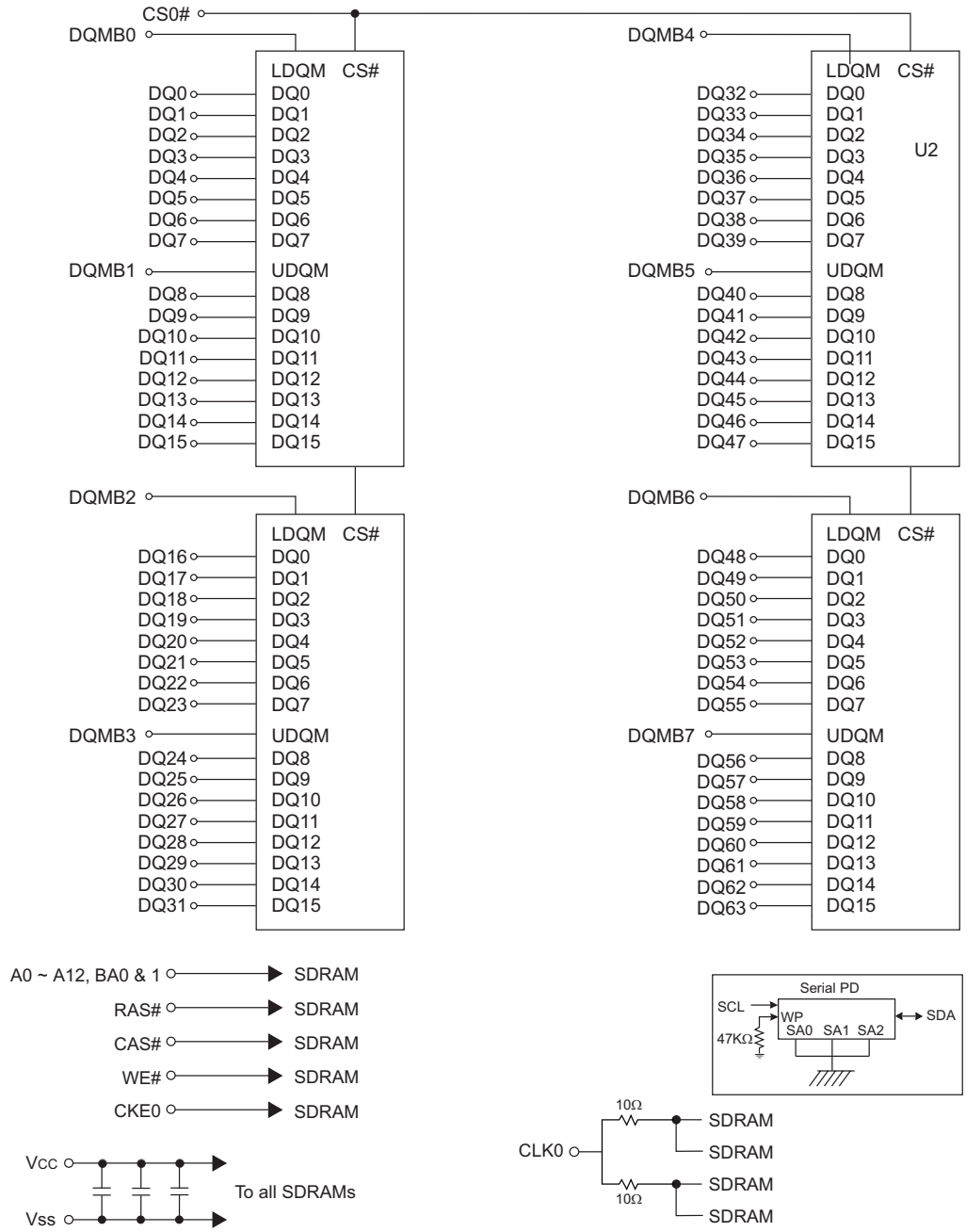
PINOUT											
PIN	FRONT	PIN	BACK	PIN	FRONT	PIN	BACK	PIN	BACK	PIN	BACK
1	V_{SS}	2	V_{SS}	49	DQ13	50	DQ45	97	DQ22	98	DQ54
3	DQ0	4	DQ32	51	DQ14	52	DQ46	99	DQ23	100	DQ55
5	DQ1	6	DQ33	53	DQ15	54	DQ47	101	V_{CC}	102	V_{CC}
7	DQ2	8	DQ34	55	V_{SS}	56	V_{SS}	103	A6	104	A7
9	DQ3	10	DQ35	57	NC	58	NC	105	A8	106	BA0
11	V_{CC}	12	V_{CC}	59	NC	60	NC	107	V_{SS}	108	V_{SS}
13	DQ4	14	DQ36	61	CLK0	62	CKE0	109	A9	110	BA1
15	DQ5	16	DQ37	63	V_{CC}	64	V_{CC}	111	A10/AP	112	A11
17	DQ6	18	DQ38	65	RAS#	66	CAS#	113	V_{CC}	114	V_{CC}
19	DQ7	20	DQ39	67	WE#	68	NC	115	DQMB2	116	DQMB6
21	V_{SS}	22	V_{SS}	69	CS0#	70	A12	117	DQMB3	118	DQMB7
23	DQMB0	24	DQMB4	71	NC	72	NC	119	V_{SS}	120	V_{SS}
25	DQMB1	26	DQMB5	73	DNU	74	NC	121	DQ24	122	DQ56
27	V_{CC}	28	V_{CC}	75	V_{SS}	76	V_{SS}	123	DQ25	124	DQ57
29	A0	30	A3	77	NC	78	NC	125	DQ26	126	DQ58
31	A1	32	A4	79	NC	80	NC	127	DQ27	128	DQ59
33	A2	34	A5	81	V_{CC}	82	V_{CC}	129	V_{CC}	130	V_{CC}
35	V_{SS}	36	V_{SS}	83	DQ16	84	DQ48	131	DQ28	132	DQ60
37	DQ8	38	DQ40	85	DQ17	86	DQ49	133	DQ29	134	DQ61
39	DQ9	40	DQ41	87	DQ18	88	DQ50	135	DQ30	136	DQ62
41	DQ10	42	DQ42	89	DQ19	90	DQ51	137	DQ31	138	DQ63
43	DQ11	44	DQ43	91	V_{SS}	92	V_{SS}	139	V_{SS}	140	V_{SS}
45	V_{CC}	46	V_{CC}	93	DQ20	94	DQ52	141	SDA**	142	SCL**
47	DQ12	48	DQ44	95	DQ21	96	DQ53	143	V_{CC}	144	V_{CC}

PIN NAMES

A0 – A12	Address Input (Multiplexed)
BA0-1	Select Bank
DQ0-63	Data Input/Output
CLK0	Clock Input
CKE0	Clock Enable Input
CS0#	Chip Select Input
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
DQMB0-7	DQM
V_{CC}	Power Supply (3.3V)
V_{SS}	Ground
SDA	Serial Data I/O
SCL	Serial Clock
DNU	Do Not Use
NC	No Connect

** These pins should be NC in the system which does not support SPD.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}, V_{CCQ}	-1.0 ~ 4.6	V
Storage Temperature	T_{STG}	-55 ~ +150	°C
Power Dissipation	P_D	4	W
Short Circuit Current	I_{OS}	50	mA

Note:

Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

Voltage Referenced to: V_{SS} = 0V, T_A = 0°C to +70°C

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	3.0	3.3	3.6	V	
Input High Voltage	V_{IH}	2.0	3.0	$V_{CCQ+0.3}$	V	1
Input Low Voltage	V_{IL}	-0.3	—	0.8	V	2
Output High Voltage	V_{OH}	2.4	—	—	V	I_{OH}= -2mA
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL}= -2mA
Input Leakage Current	I_{LI}	-10	—	10	µA	3

Note:

1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{CCQ}
   Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE

T_A = 25°C, f = 1MHz, V_{CC} = 3.3V, V_{REF} = 1.4V ± 200mV

Parameter	Symbol	Max	Unit
Input Capacitance (A0-A12)	C_{IN1}	21	pF
Input Capacitance (RAS#,CAS#,WE#)	C_{IN2}	21	pF
Input Capacitance (CKE0)	C_{IN3}	21	pF
Input Capacitance (CLK0)	C_{IN4}	16	pF
Input Capacitance (CS0#)	C_{IN5}	21	pF
Input Capacitance (DQM0-DQM7)	C_{IN6}	11	pF
Input Capacitance (BA0-BA1)	C_{IN7}	21	pF
Data Input/Output Capacitance (DQ0-DQ63)	C_{OUT}	9	pF

OPERATING CURRENT CHARACTERISTICS

V_{CC} = 3.3V, 0°C ≤ T_A ≤ +70°C

			Version			
Parameter	**Symbol**	**Conditions**	**133**	**100**	**Units**	**Note**
Operating Current (One bank active)	I_{CC1}	Burst Length = 1 t_{RC} ≤ t_{RC}(min) I_{OL} = 0mA	440	440	mA	1
Precharge Standby Current in Power Down Mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	14		mA	
Active Standby Current in Non-Power Down Mode	I_{CC3N}	CKE ≥ V_{IH}(min), CS ≥ V_{IH}(min), tcc = 10ns Input signals are changed one time during 20ns	180		mA	
Operating Current (Burst mode)	I_{CC4}	Io = mA Page burst 4 Banks activated t_{CCD} = 2CK	520	520	mA	1
Refresh Current	I_{CC5}	t_{RC} ≥ t_{RC}(min)	980	980	mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V	24		mA	

Notes:
1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS

V_{CC} = 3.3V ± 0.3V, 0 ≤ T_A ≤ 70°C

Parameter	Value	Unit
AC input levels (V_{IH}/V_{IL})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	t_R/t_F = 1/1	ns
Output timing measurement reference level	1.4	V

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version	Unit	Note
			7.5, 10		
Row active to row active delay		t_{RRD} (min)	15	ns	1
RAS# to CAS# delay		t_{RCD} (min)	20	ns	1
Row precharge time		t_{RP} (min)	20	ns	1
Row active time		t_{RAS} (min)	45	ns	1
		t_{RAS} (max)	100	us	
Row cycle time		t_{RC} (min)	65	ns	1
Last data in to row precharge		t_{RDL} (min)	2	CLK	2
Last data in to Active delay		t_{DAL} (min)	2 CLK + t_{RP}	—	
Last data in to new col. address delay		t_{CDL} (min)	1	CLK	2
Last data in to burst stop		t_{BDL} (min)	1	CLK	2
Col. address to col. address delay		t_{CCD} (min)	1	CLK	3
Number of valid output data	CAS latency=3		2	ea	4
	CAS latency=2		1		

Notes :

1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

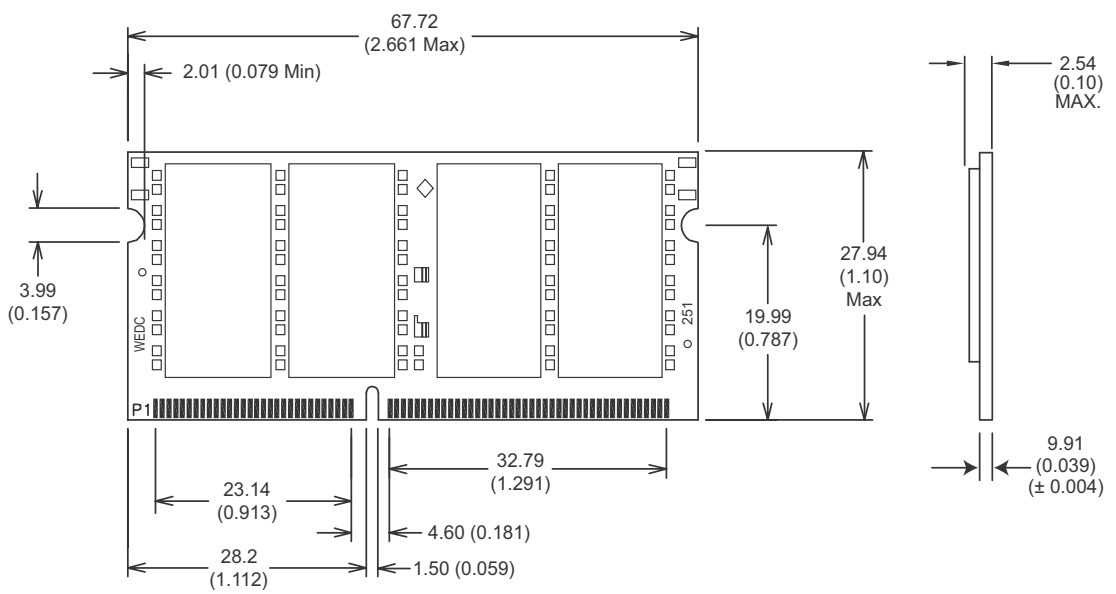
PACKAGE DIMENSIONS FOR D1

Ordering Information	Speed	CAS Latency	Height*
W3DG6433V10D1	100MHz	CL=2	27.94 (1.10")
W3DG6433V75D1	133MHz	CL=3	27.94 (1.10")

NOTES:

- Consult Factory for availability of Lead-Free products. (F = Lead-Free, G = RoHS Compliant)
- Product specific part numbers are available for source control if needed, please consult factory for the correct part number if a specific component vendor is preferred. Please add "-M" for Micron or "-S" for Samsung to the back of the part number for the specific component vendor preferred.
- Consult factory for availability of industrial temperature (-40°C to 85°C) option

PACKAGE DIMENSIONS FOR D1



* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES).

Document Title

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Revision History

Rev #	History	Release Date	Status
Rev 0	Created	11-01	Advanced
Rev 1	1.1 Removed “ED” from part number 1.2 Updated CAP and I_{DD} specs	6-04	Preliminary
Rev 2	2.1 Updated block diagram 2.2 Updated package dimensions 2.3 Added lead-free and RoHS notes 2.4 Added source control options 2.5 Added industrial temperature option 2.6 Added AC Specs	1-05	Preliminary
Rev 3	3.1 Updated ICC Specs 3.2 Move from Preliminary to Final	3-05	Final