ARIZONA MICROTEK, INC.

AZP92

ECL/PECL ÷1, ÷2 Clock Generation Chip with Selectable Enable

FEATURES

- Green and RoHS Compliant / Lead (Pb) Free Package Available
- 3.0V to 5.5V Operation
- Selectable Divide Ratio
- Selectable Enable Polarity and Threshold (CMOS/TTL or PECL)
- Selectable Input Biasing
- High Bandwidth for ≥1GHz
- Available in a MLP 8 (2x2) Package

PACKAGE AVAILABILITY

PACKAGE	PART NO.	MARKING	NOTES
MLP 8 (2x2) Green / RoHS Compliant / Lead (Pb) Free	AZP92NAG	P1G <Date Code>	1,2
DIE	AZP92X	N/A	3,4

1 Add R1 at end of part number for 7 inch (1K parts), R2 for 13 inch (2.5K parts) Tape & Reel.
2 Date code format: "Y" for year followed by "WW" for week.
3 Waffle Pack
4 Contact factory for availability

DESCRIPTION

The AZP92 is a specialized ÷1 or ÷2 clock generation part including an enable/reset function. The divide ratio is selected with the DIV-SEL pin/pad. When DIV-SEL is open (NC), the AZP92 functions as a standard receiver. If DIV-SEL is connected to V_{EE}, it functions as a ÷2 divider.

A selectable enable is provided which also functions as a reset when the ÷2 mode is selected. Enable (EN) functionality is selected with the EN-SEL pin/pad which has three valid states: open (NC), V_{EE}, or connected to V_{EE} via a 20kΩ resistor. Leaving EN-SEL open or connecting it to V_{EE} will select the EN pin/pad to function as an active high CMOS/TTL enable. When EN-SEL is open, an internal 75kΩ pull-up resistor is selected which enables the outputs whenever EN is left open. When EN-SEL is connected to V_{EE}, an internal 75kΩ pull-down resistor is selected which disables the outputs whenever EN is left open.

Connecting the EN-SEL to V_{EE} with a 20kΩ resistor will select the EN pin/pad to function as an active low PECL/ECL enable with an internal 75kΩ pull-down resistor. In this mode, outputs are enabled when EN is left open (NC). This default logic condition can be overridden by connecting the EN to V_{CC} with an external resistor of ≤20kΩ. Refer to the enable truth table on the next page for detailed operation.

DIE (AZP92X)

The AZP92X provides a V_{BB} and a BIAS pad with 940Ω internal resistors from D to BIAS and $\overline{D}$ to BIAS. Connecting the BIAS pad to V_{BB} allows D and $\overline{D}$ to be AC coupled with minimal external components. For single ended applications, D or $\overline{D}$ may be connected directly to V_{BB} to form a single 1880Ω bias resistor. The V_{BB} pin supports 1.5mA sink/source current. Whenever used, the V_{BB} should be bypassed to ground or V_{CC} with a 0.01 µF capacitor.

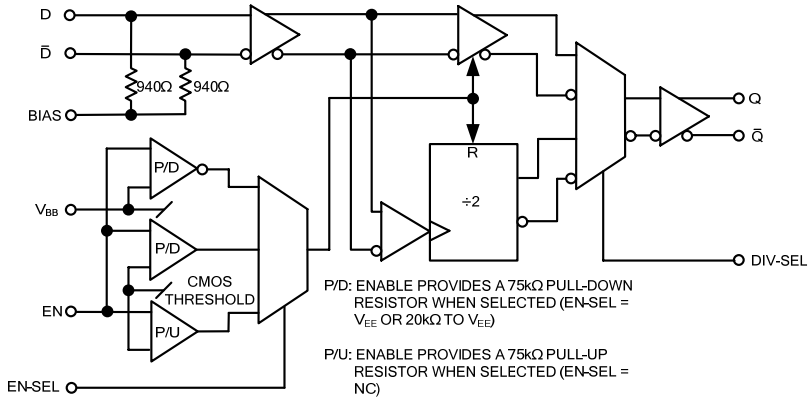
MLP 8, 2x2 mm Package (AZP92NA)

The AZP92NA provides a V_{BB} with an 1880Ω internal bias resistor from D to V_{BB}. This feature allows AC coupling with minimal external components. The V_{BB} pin supports 1.5mA sink/source current and should be bypassed to ground or V_{CC} with a 0.01 µF capacitor.

NOTE: The specifications in the ECL/PECL tables are valid when thermal equilibrium has been established.

SIGNAL DESCRIPTION

PIN/PAD	FUNCTION
D/$\overline{D}$	Data Inputs
Q/$\overline{Q}$	Data Outputs
V_{BB}	Reference Voltage Output
BIAS	Input Bias Return
EN	Enable/Reset Input
EN-SEL	Enable Logic Select
DIV-SEL	Divide Ratio Select
V_{EE}	Negative Supply
V_{CC}	Positive Supply



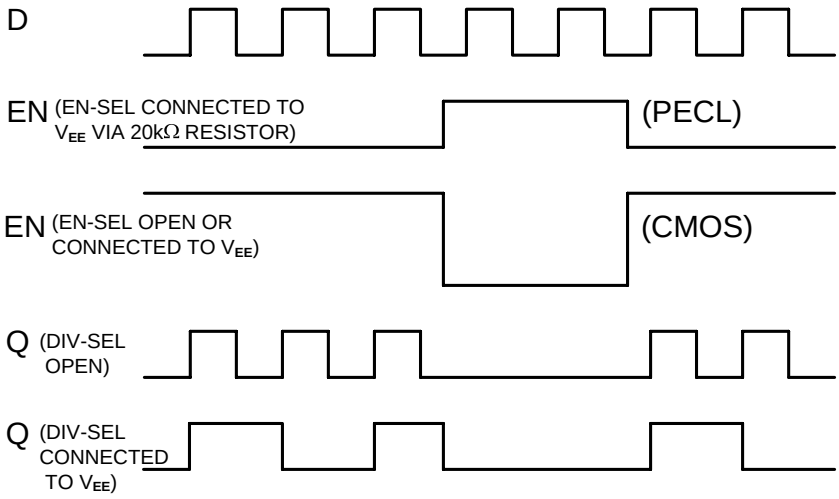
ENABLE TRUTH TABLE

EN-SEL	EN	Q	$\overline{Q}$
NC	CMOS Low or V_{EE}	Low	High
NC	CMOS High, V_{CC} or NC	Data	Data
V_{EE}	CMOS Low, V_{EE} or NC	Low	High
V_{EE}	CMOS High or V_{CC}	Data	Data
20kΩ to V_{EE}	PECL Low, V_{EE} or NC	Data	Data
20kΩ to V_{EE}	PECL High or V_{CC}	Low	High

DIVIDE TRUTH TABLE

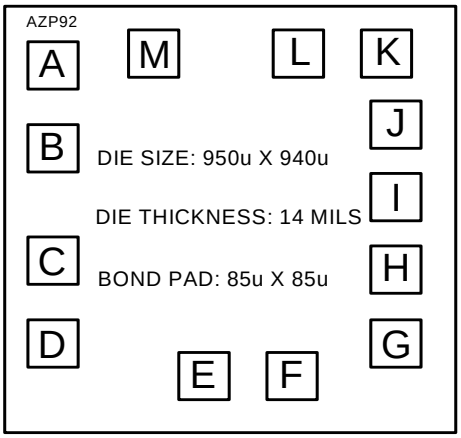
DIV-SEL	DIVIDE RATIO
NC	÷1
V_{EE} [1]	÷2

[1] DIV-SEL connection must be ≤1Ω.



TIMING DIAGRAM

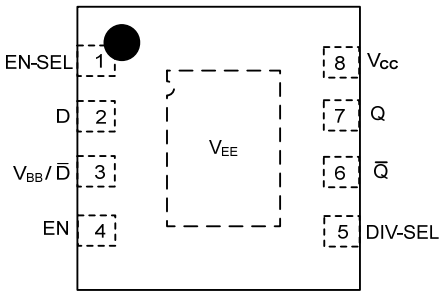
DIE PAD COORDINATES



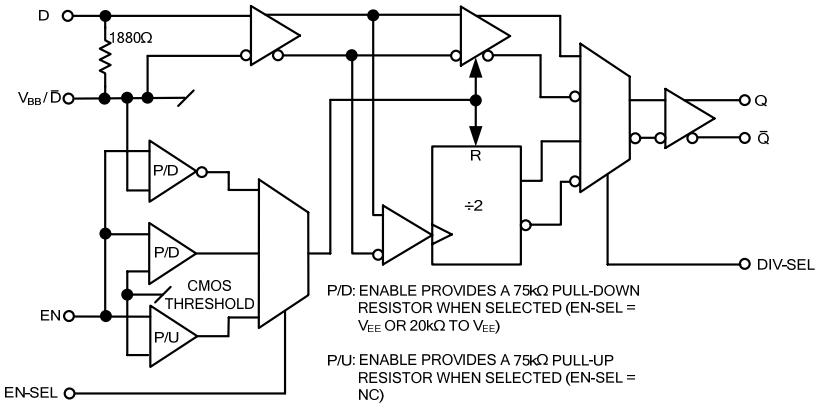
NAME	SIGNAL	X (Microns)	Y (Microns)
A	D	-342.5	312.5
B	$\overline{D}$	-342.5	144.5
C	BIAS	-342.5	-87.0
D	V_{BB}	-342.5	-255.0
E	EN	-33.5	-312.5
F	V_{EE}	126.5	-312.5
G	DIV-SEL	312.5	-248.5
H	$\overline{Q}$	312.5	-98.5
I	Q	312.5	51.5
J	NC	312.5	201.5
K	V_{CC}	302.5	342.5
L	V_{CC}	142.5	342.5
M	EN-SEL	-140.5	342.5

Notes:
1. Other die thicknesses available. Contact factory for further information.
2. The die backside may be left open or connected to V_{EE}.

AZP92NA
MLP 8, 2x2 mm



TOP VIEW



Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic		Rating	Unit
V_{CC}	PECL Power Supply	(V_{EE} = 0V)	0 to +6.0	Vdc
V_I	PECL Input Voltage	(V_{EE} = 0V)	0 to +6.0	Vdc
V_{EE}	ECL Power Supply	(V_{CC} = 0V)	-6.0 to 0	Vdc
V_I	ECL Input Voltage	(V_{CC} = 0V)	-6.0 to 0	Vdc
I_{HGOUT}	Output Current	— Continuous — Surge	50 100	mA
T_A	Operating Temperature Range		-40 to +85	°C
T_{STG}	Storage Temperature Range		-65 to +150	°C

100K ECL DC Characteristics (V_{EE} = -3.0V to -5.5V, V_{CC} = GND)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage[1]	-1085	-880	-1025	-880	-1025	-880	-1025	-880	mV
V_{OL}	Output LOW Voltage[1]	-1900	-1555	-1900	-1620	-1900	-1620	-1900	-1620	mV
V_{IH}	Input HIGH Voltage D/$\overline{D}$, EN (ECL)[2] EN (CMOS)[3]	 -1165 V_{EE}+2000	 -390 V_{CC}	 -1165 V_{EE}+2000	 -390 V_{CC}	 -1165 V_{EE}+2000	 -390 V_{CC}	 -1165 V_{EE}+2000	 -390 V_{CC}	mV
V_{IL}	Input LOW Voltage D/$\overline{D}$, EN (ECL)[2] EN (CMOS)[3]	 -2250 V_{EE}	 -1475 V_{EE} + 800	 -2250 V_{EE}	 -1475 V_{EE} + 800	 -2250 V_{EE}	 -1475 V_{EE} + 800	 -2250 V_{EE}	 -1475 V_{EE} + 800	mV
V_{BB}	Reference Voltage	-1390	-1250	-1390	-1250	-1390	-1250	-1390	-1250	mV
I_{IH}	Input HIGH Current EN		150		150		150		150	µA
I_{IL}	Input LOW Current EN (ECL)[2] EN (CMOS)[3]	 0.5 -150		 0.5 -150		 0.5 -150		 0.5 -150		µA
I_{EE}	Power Supply Current[4]		31		31		31		34	mA

1. Specified with outputs terminated through 50Ω resistors to V_{CC} - 2V.
2. EN-SEL connected to V_{EE} through a 20kΩ resistor.
3. EN-SEL connected V_{EE} or left open (NC).
4. DIV-SEL left open (NC).

100K LVPECL DC Characteristics (V_{EE} = GND, V_{CC} = +3.3V)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage[1,2]	2215	2420	2275	2420	2275	2420	2275	2420	mV
V_{OL}	Output LOW Voltage[1,2]	1400	1745	1400	1680	1400	1680	1400	1680	mV
V_{IH}	Input HIGH Voltage[1] D/$\overline{D}$, EN (PECL)[3] EN (CMOS)[4]	 2135 2000	 2910 V_{CC}	 2135 2000	 2910 V_{CC}	 2135 2000	 2910 V_{CC}	 2135 2000	 2910 V_{CC}	mV
V_{IL}	Input LOW Voltage[1] D/$\overline{D}$, EN (PECL)[3] EN (CMOS)[4]	 1050 GND	 1825 800	 1050 GND	 1825 800	 1050 GND	 1825 800	 1050 GND	 1825 800	mV
V_{BB}	Reference Voltage[1]	1910	2050	1910	2050	1910	2050	1910	2050	mV
I_{IH}	Input HIGH Current EN		150		150		150		150	µA
I_{IL}	Input LOW Current EN (PECL)[3] EN (CMOS)[4]	 0.5 -150		 0.5 -150		 0.5 -150		 0.5 -150		µA
I_{EE}	Power Supply Current[5]		31		31		31		34	mA

1. For supply voltages other that 3.3V, use the ECL table values and ADD supply voltage value.
2. Specified with outputs terminated through 50Ω resistors to V_{CC} - 2V.
3. EN-SEL connected to V_{EE} through a 20kΩ resistor.
4. EN-SEL connected V_{EE} or left open (NC).
5. DIV-SEL left open (NC).

100K PECL DC Characteristics (V_{EE} = GND, V_{CC} = +5.0V)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage[1,2]	3915	4120	3975	4120	3975	4120	3975	4120	mV
V_{OL}	Output LOW Voltage[1,2]	3100	3445	3100	3380	3100	3380	3100	3380	mV
V_{IH}	Input HIGH Voltage[1] D/$\overline{D}$, EN (PECL)[3] EN (CMOS)[4]	 3835 2000	 4610 V_{CC}	 3835 2000	 4610 V_{CC}	 3835 2000	 4610 V_{CC}	 3835 2000	 4610 V_{CC}	mV
V_{IL}	Input LOW Voltage[1] D/$\overline{D}$, EN (PECL)[3] EN (CMOS)[4]	 2750 GND	 3525 800	 2750 GND	 3525 800	 2750 GND	 3525 800	 2750 GND	 3525 800	mV
V_{BB}	Reference Voltage[1]	3610	3750	3610	3750	3610	3750	3610	3750	mV
I_{IH}	Input HIGH Current EN		150		150		150		150	µA
I_{IL}	Input LOW Current EN (PECL)[3] EN (CMOS)[4]	 0.5 -150		 0.5 -150		 0.5 -150		 0.5 -150		µA
I_{EE}	Power Supply Current[5]		31		31		31		34	mA

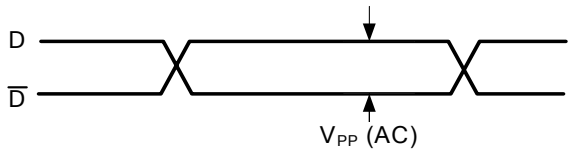
1. For supply voltages other that 5.0V, use the ECL table values and ADD supply voltage value.
2. Specified with outputs terminated through 50Ω resistors to V_{CC} - 2V.
3. EN-SEL connected to V_{EE} through a 20kΩ resistor.
4. EN-SEL connected V_{EE} or left open (NC).
5. DIV-SEL left open (NC).

AC Characteristics (V_{EE} = -3.0V to -5.5V; V_{CC} = GND or V_{EE} = GND; V_{CC} = +3.0V to +5.5V)

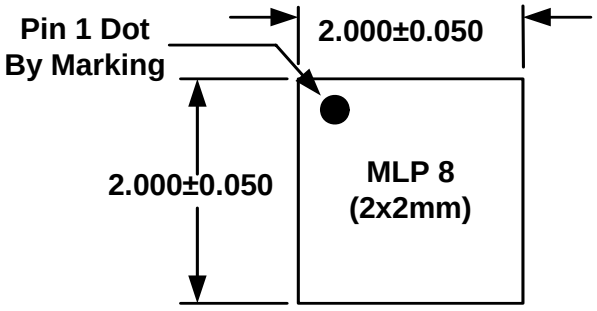
Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PLH} / t_{PHL}	Propagation Delay D to Q/$\overline{Q}$ Outputs[1] (SE) EN to Q/$\overline{Q}$ Outputs[1]			 450 600			 450 600			 450 600			 450 600	ps
t_{SKEW}	Duty Cycle Skew[2] (SE)		5	20		5	20		5	20		5	20	ps
V_{PP} (AC)	Input Swing[3] Differential (D/$\overline{D}$) Single Ended (D)[4]	 150 300		 1000 2000	 150 300		 1000 2000	 150 300		 1000 2000	 150 300		 1000 2000	mV
t_r / t_f	Output Rise/Fall[1] (20% - 80%)	80		200	80		200	80		200	80		200	ps

1. Specified with outputs terminated through 50Ω resistors to V_{CC} - 2V.
2. Duty cycle skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device.
3. The peak-to-peak input swing is the range for which AC parameters are guaranteed.
4. Range valid for AC coupled signals only.

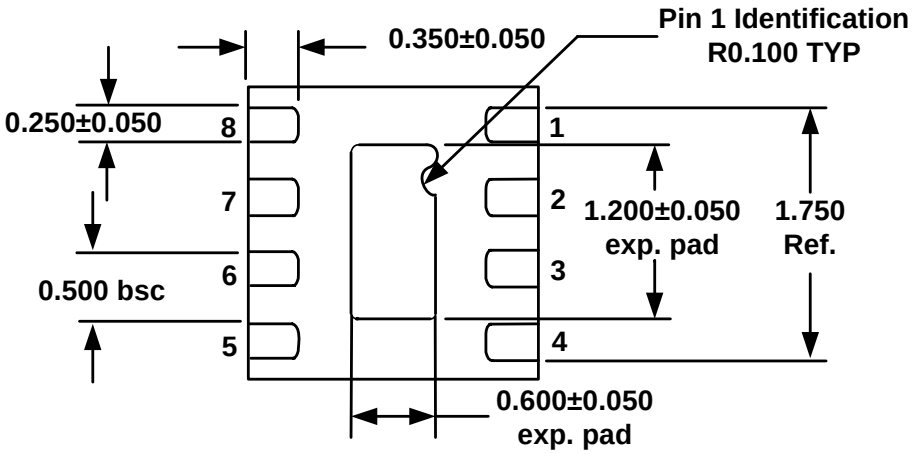
AC PP INPUT (Differential)



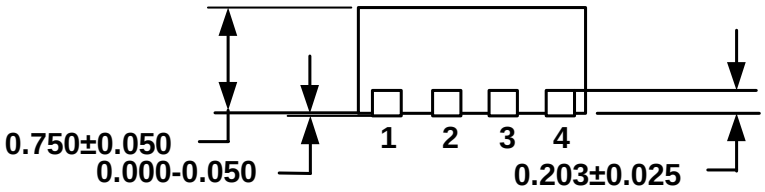
PACKAGE DIAGRAM
MLP 8 2x2mm



TOP VIEW



BOTTOM VIEW



SIDE VIEW

Note: All dimensions are in mm