2.4 Gbit/s ATM Layer Solution

FEATURES

- Monolithic single chip device which handles ATM Layer functions for one direction including VPI/VCI address translation, cell appending, cell rate policing, cell counting and OAM requirements for 64 k VCs (virtual connections). Two or more PM7325 S/UNI®-ATLAS-3200 devices can be cascaded to support additional VC's.
- Instantaneous transfer rate of 3200 Mbit/s supports a cell transfer rate of $5.68x10^6$ cells/s.
- Can be configured as an Ingress mode device or an Egress mode device.
- POS-PHY/UTOPIA Level 3 PHY and Switch interface supports a 32-bit 104 MHz interface. Extended cell format is supported (52 - 64 byte cell). Packets are not processed and are buffered and passed through transparently. Handles up to 48 logical PHY ports.
- Supports a full duplex 16 bit 5 2MHz SCI-PHY™ Backwards Cell Interface Port which allows an Ingress mode device and an Egress mode device to communicate and behave as a single bi-directional device.
- Supports a 64-bit (with or without parity) 125 MHz External Pipelined ZBT SRAM interface.
- Includes a FIFO buffered 32-bit microprocessor bus interface for cell insertion and extraction, deterministic VC Table access, status monitoring and configuration of the device.
- Per-PHY output buffering scheme resolves the head-of-line blocking issue.
- Ingress and Egress functions include flexible search engines that cover the entire PHYID/VPI/VCI address range, dual leaky-bucket policing, per-VC cell counts, OAM-FM and OAM-PM processing.

POLICING

- ITU-I.371, ATM Forum TM4.1 compliant, per-VC programmable dual leaky-bucket policing with a programmable action (tag, discard, or count only) for each bucket, each with three programmable 16 bit non-compliant cell counts.
- Per-PHY single leaky-bucket policing with a programmable action (tag, discard, or count only).
- Guaranteed Frame Rate (GFR) Policing with Minimum Cell Rate Frame Tagging.

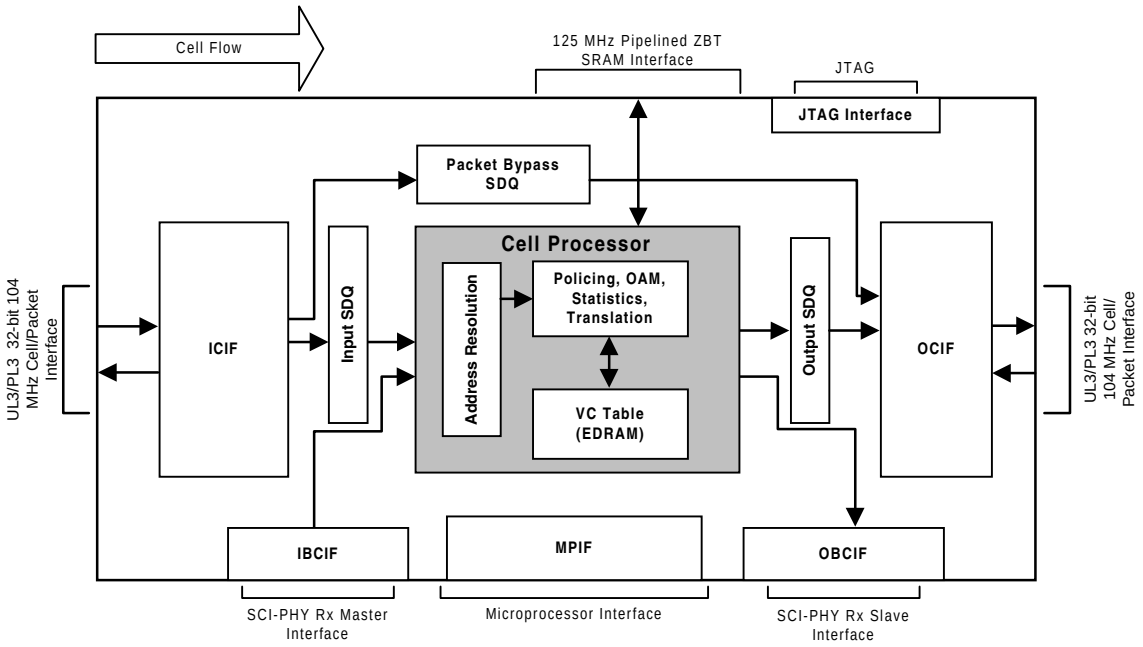
OAM

- ITU-I.610 (1999) compliant OAM on both Ingress and Egress directions.
- Complete Fault Management (AIS, RDI, CC) processing, for VP/VC, Segment/End-to-end flows on all VCs.
- Complete Performance Monitoring processing, for VP/VC, Segment/End-to-end, Forward/Backward flows, on 512 Uni-directional VCs.
- Per-PHY AIS/RDI generation.

CELL COUNTING

- Per-VC counts include CLP0 cells, CLP1 cells, OAM cells, RM cells, and invalid cells, cells violating the contract and total AAL5 frames.
- Per-PHY counts include CLP0 cells, CLP1 cells, OAM cells, errored OAM cells, unassigned/invalid cells and policing violations.
- Per-device counts include total cells received/transmitted, and physical layer cells.

BLOCK DIAGRAM



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2.4 Gbit/s ATM Layer Solution

PACKAGING

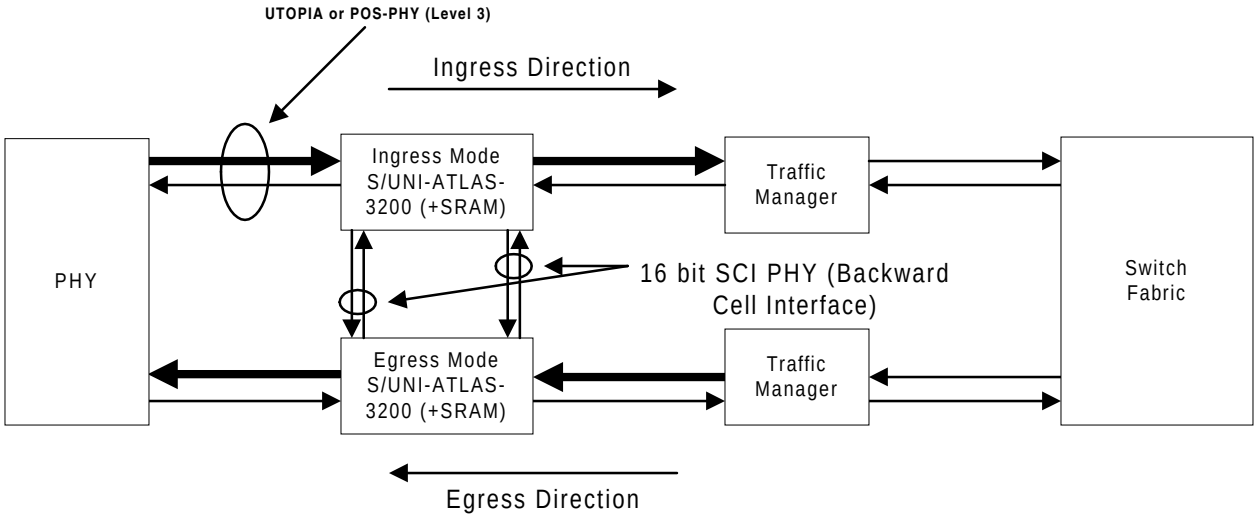
- Provides a standard five signal P1149.1 JTAG test port for boundary scan board test purposes.
- Implemented in low power, 0.18 micron, 1.5 V CMOS technology with 2.5 V embedded DRAM, 2.5 V external SRAM interface, and 3.3 V external interfaces (excluding the SRAM interface).
- Packaged in a 768 pin Tape Ball Grid Array (TBGA) package.

APPLICATIONS

- Core ATM switches.
- Wide Area Network ATM Core and Edge Switches.
- ATM Enterprise and Workgroup Switches.
- Broadband Access Multiplexers.

TYPICAL APPLICATION

S/UNI-ATLAS-3200 OC-48 PORT CARD APPLICATION



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