

GENERAL DESCRIPTION

EM19110 is a 10-bit, 5 MHz CMOS A/D converter for high speed and high resolution use. The 2-step parallel structures accompanying with an average technique that external generated reference voltage, the users can tune transfer curve to meet their application.

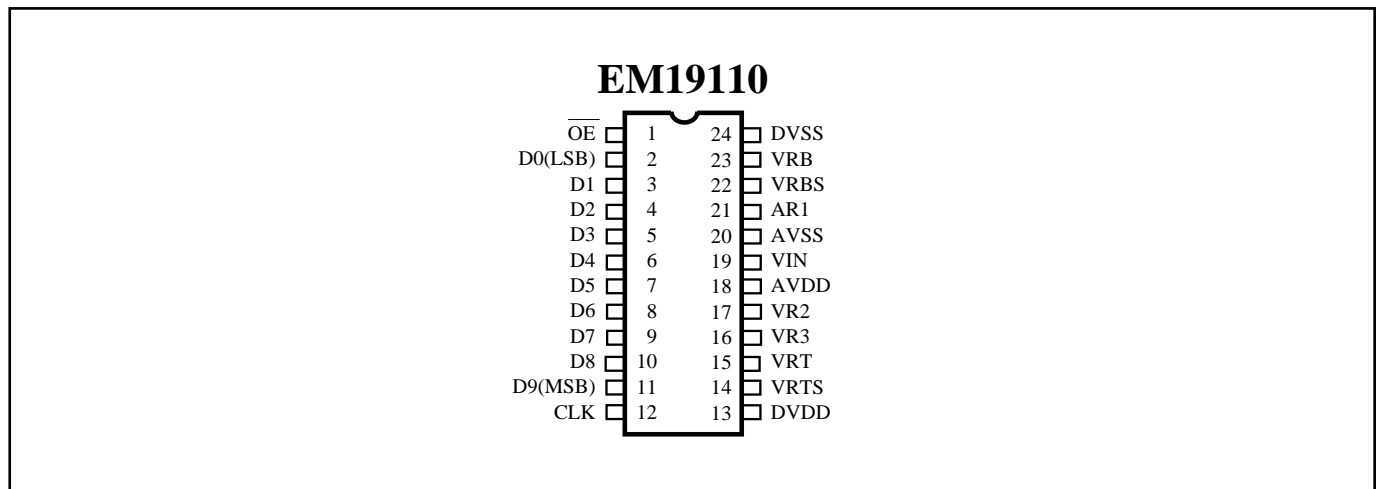
FEATURES

- 5 MSPS maximum conversion speed
- High resolution up to 10 bit
- Built-in sampling and hold circuit
- Internal self-bias reference voltage
- 115 mW low power dissipation at 5MSPS
- +5V single power supply
- Available in 24 pin SOP
- Series
EM19110M for 300 mil SOP

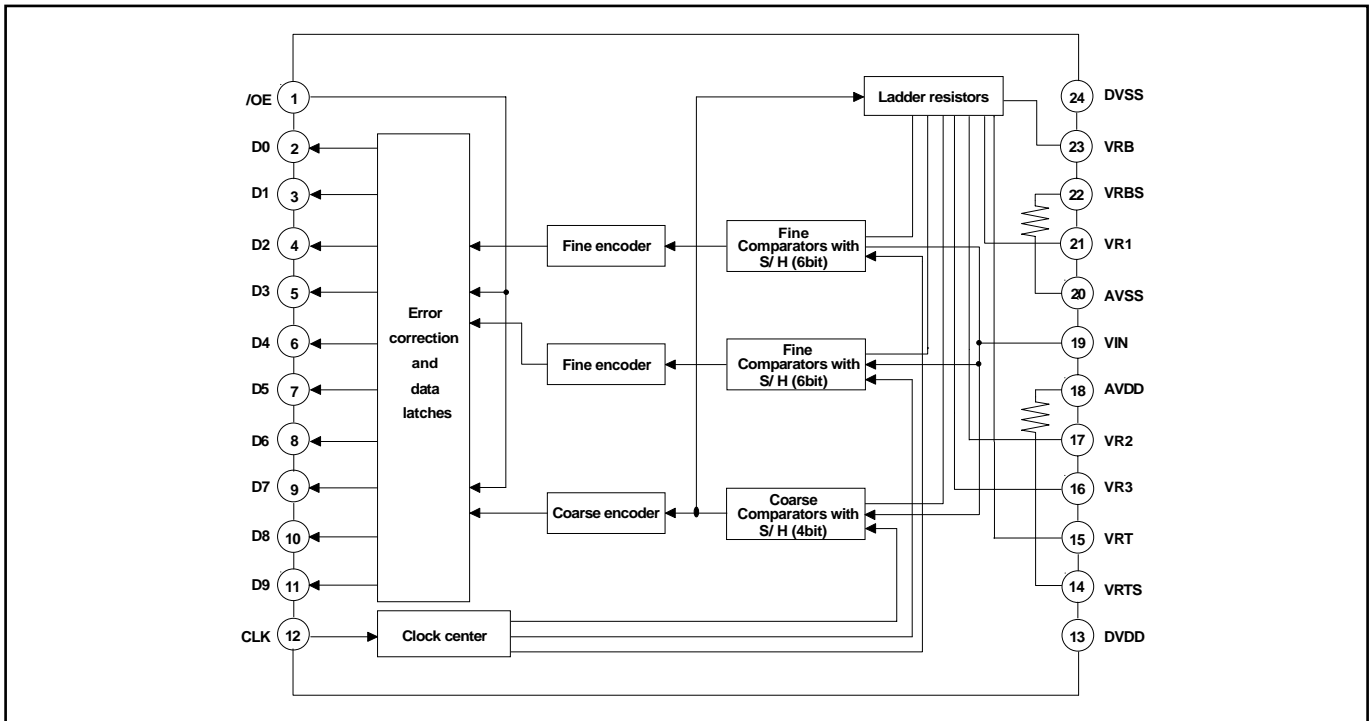
APPLICATION

Precision scanner, digital cellular phone and a wide range of fields where high speed and high resolution A/D conversion is required in the digital communication.

PIN ASSIGNMENT



FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

Symbol	Function
\overline{OE}	Output enable
D0	Data output bit 0 (LSB)
D1	Data output bit 1
D2	Data output bit 2
D3	Data output bit 3
D4	Data output bit 4
D5	Data output bit 5
D6	Data output bit 6
D7	Data output bit 7
D8	Data output bit 8
D9	Data output bit 9 (MSB)
CLK	Clock input
DVDD	Digital power supply
VRTS	Top internal reference voltage
VRT	Top reference voltage
VR3	Tap-3 reference voltage
VR2	Tap-2 reference voltage
AVDD	Analog power supply
VIN	Analog input voltage
AVSS	Analog ground
VR-1	Tap-1 reference voltage
VRBS	Bottom internal reference voltage
VRB	Bottom reference voltage
DVSS	Digital ground

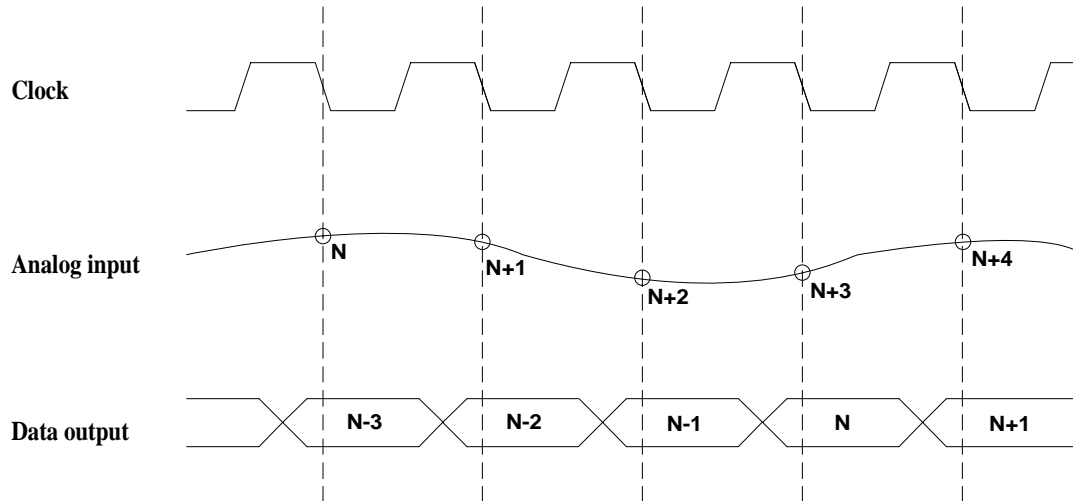
ABSOLUTE MAXIMUM RATINGS ($T_A=25^\circ\text{C}$)

Items	Sym.	Rating	Unit
Supply voltage	V_{DD}	7	V
Analog input voltage	V_{IN}	V_{SS} to V_{DD}	V
Reference input voltage	V_{RT}, V_{RB}	V_{SS} to V_{DD}	V
Operating temperature	T_{OPR}	-20 to 65	$^\circ\text{C}$

 $(F_C=5\text{MSPS}, AV_{DD}=DV_{DD}=5\text{V}, V_{RB}=1.0\text{V}, V_{RT}=4.0\text{V}, T_a=25^\circ\text{C})$

Parameter	Sym.	Conditions	Min.	Typ.	Max.	Unit
Maximum Conversion Speed	F_C			5	8	MSPS
Supply current	I_{DD}	$F_C=5\text{MSPS}$		23	28	mA
Reference pin current	I_{REF}		7.5	8.5	9.4	mA
Analog input bandwidth	BW			1		MHz
Analog input capacitance	C_{IN}			5		pF
Reference resistance	R_{REF}		320	355	400	Ω
Differential reference voltage	$V_{RT}-V_{RB}$	External bias $AV_{SS} \leq V_{RB} \leq V_{RT} \leq AV_{DD}$	1.0			V_{DD}
Internal bias reference voltage	V_{RB}	Internal bias short V_{RB} and V_{RBS}	0.95	1.0	1.05	V
	$V_{RT}-V_{RB}$	Internal bias short V_{RT} and V_{RTS}	2.9	3.0	3.1	
Digital input voltage	V_{IH}		4.0			V
	V_{IL}				1.0	
Digital input current	I_{IH}	$V_{DD}=\text{max.}$			5	μA
	I_{IL}				5	
Digital output current	I_{OH}	$\overline{OE}=V_{SS}$				V
	I_{OL}	$V_{DD}=\text{min.}$				V
Digital output current	I_{OZH}	$\overline{OE}=V_{DD}$			16	V
					16	V
Output data delay	TDL			20	30	ns
Integral nonlinearity	EL				± 2.0	LSB
Differential nonlinearity	ED				± 1.0	LSB
Aperture jitter	t_{aj}			50		ps
Sampling delay	t_{ds}			4		ns

TIMING DIAGRAM



Application Note

1. AVDD ,DVDD ,VSS

To reduce noise effects, separate the analog and digital systems close to the device. For both the digital and analog VDD pins, use a ceramic capacitor of about 0.1 μ F set as close as possible to the pin to bypass to the respective GND's.

2. Signal input V_i

Compared with the flash type A/D converter, the input capacitance of the analog input is rather small. However it is necessary to conduct the drive with an amplifier featuring sufficient band and drive capability. When driving with an amplifier of low output impedance, parasite oscillation may occur. That may be prevented by inserting a resistance of about 100 Ω in series between the amplifier output and A/D input.

3. Clock input

The clock line wiring should be as short as possible also, to avoid any interference with other signals, separate it from other circuits.

4. Reference voltage

Voltage between VRT to VRB is compatible with the dynamic range of the analog input. Bypassing VRT and VRB pins to GND, by means of a capacitor about 0.1 μ F, stable characteristics are obtained. By shorting VRT and VRTS, VRB and VRBS, the self bias function that generates VRT=4.0V and VRB=1.0V, is activated. Also, the users can setup external reference voltage by just connecting VRT and VRB to desired DC voltage under spec.

5. Clock timing

Analog input is sampled with the falling edge of CLK and output as digital data with a delay of 2.5 clocks and with the following rising edge. The delay from the clock rising edge to the data output is the output data delay about 20ns.

6. /OE

By connecting /OE to GND output mode is obtained. By connecting to VDD high impedance is obtained.

7. About latch up

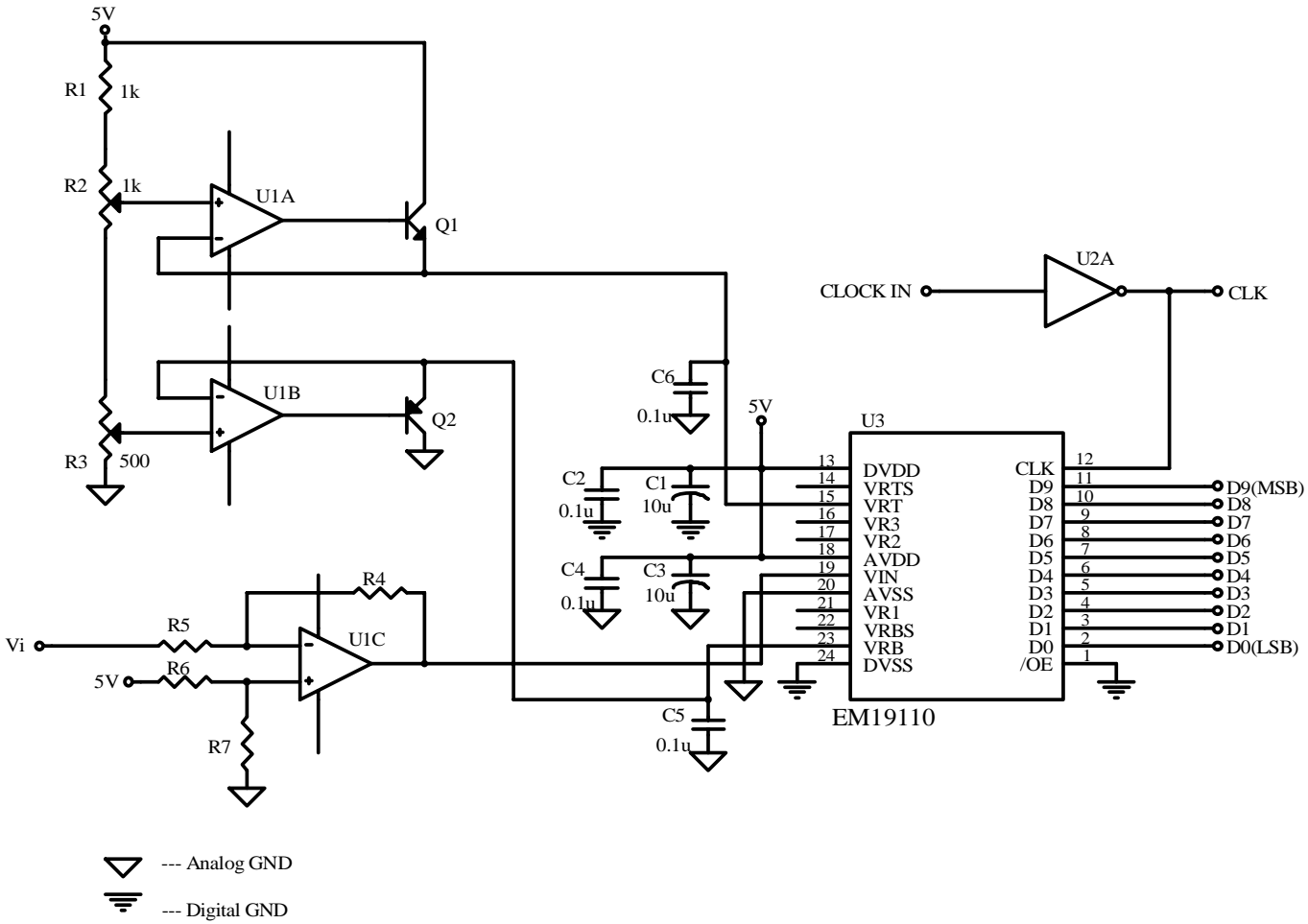
It is necessary that AVDD and DVDD pins be the common source of power supply. This is to avoid latch up due to the voltage difference between AVDD and DVDD pins when power is ON.

8. Tap reference voltage

Tap reference voltage VR1 thru VR3 connect to eighth point along the reference ladder; VR1 is 1/4th up from VRB, VR2 is 2/4th up from VRB, VR3 is 3/4th up from VRB. These pins connecting 0.1uF capacitor to VSS can stabilize the transfer characteristic. By connecting these pins to voltage sources, the piece wise linear transfer curve can be attained.



APPLICATION CIRCUIT



* This specification are subject to be changed without notice.