

μPD789304, 789306, 789314, 789316

8-BIT SINGLE-CHIP MICROCONTROLLER

The μPD789304, 789306, 789314, and 789316 belong to the μPD789306, 789316 Subseries (for LCD drivers) in the 78K/0S Series.

Flash memory versions (μPD78F9306, 78F9316) that can be operated using the same power supply voltage as mask ROM versions are available, along with various development tools.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD789306, 789316 Subseries User's Manual: U14800E
78K/0S Series User's Manual Instructions: U11047E

FEATURES

- ROM and RAM capacities

Part Number	Item	Program Memory (ROM)	Data Memory	
			Internal High-Speed RAM	LCD Display RAM
μPD789304, 789314		8 KB	512 bytes	24 bytes
μPD789306, 789316		16 KB		

- Main system clock
Ceramic/crystal oscillation: μPD789304, 789306
RC oscillation: μPD789314, 789316
- I/O ports: 23
- Serial interface: 2 channels
Switchable between 3-wire serial I/O mode and UART mode: 1 channel
3-wire serial I/O mode: 1 channel
- LCD controller/driver
Segment signals: 24, common signals: 4
- Timer: 5 channels
- Power supply voltage: V_{DD} = 1.8 to 5.5 V

APPLICATIONS

Remote control devices, healthcare equipment, etc.

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

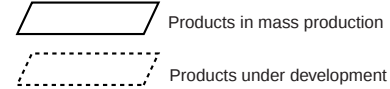
ORDERING INFORMATION

Part Number	Package
μ PD789304GC-xxx-AB8	64-pin plastic QFP (14 × 14)
μ PD789304GK-xxx-9ET	64-pin plastic TQFP (12 × 12)
μ PD789306GC-xxx-AB8	64-pin plastic QFP (14 × 14)
μ PD789306GK-xxx-9ET	64-pin plastic TQFP (12 × 12)
μ PD789314GC-xxx-AB8	64-pin plastic QFP (14 × 14)
μ PD789314GK-xxx-9ET	64-pin plastic TQFP (12 × 12)
μ PD789316GC-xxx-AB8	64-pin plastic QFP (14 × 14)
μ PD789316GK-xxx-9ET	64-pin plastic TQFP (12 × 12)

Remark xxx indicates ROM code suffix.

78K/0S SERIES LINEUP

The products in the 78K/0S Series are listed below. The names enclosed in boxes are subseries names.



Y subseries products support SMB.

Small-scale package, general-purpose applications

44-pin	μPD789046	μPD789074 with added subsystem clock
42-/44-pin	μPD789026	μPD789014 with enhanced timer and increased ROM, RAM capacity
30-pin	μPD789074	μPD789026 with enhanced timer
28-pin	μPD789014	On-chip UART and capable of low voltage (1.8 V) operation

Small-scale package, general-purpose applications and A/D converter

44-pin	μPD789177	μPD789167 with enhanced A/D converter
44-pin	μPD789167	μPD789104A with enhanced timer
30-pin	μPD789156	μPD789146 with enhanced A/D converter
30-pin	μPD789146	μPD789104A with added EEPROM™
30-pin	μPD789134A	μPD789124A with enhanced A/D converter
30-pin	μPD789124A	RC oscillation version of the μPD789104A
30-pin	μPD789114A	μPD789104A with enhanced A/D converter
30-pin	μPD789104A	μPD789026 with added A/D converter and multiplier

Inverter control

44-pin	μPD789842	On-chip inverter controller and UART
--------	-----------	--------------------------------------

VFD drive

52-pin	μPD789871	Total display outputs: 25
--------	-----------	---------------------------

LCD drive

80-pin	μPD789488	A/D converter and on-chip voltage booster type LCD (28 × 4)
80-pin	μPD789417A	μPD789407A with enhanced A/D converter
80-pin	μPD789407A	A/D converter and resistance division type LCD (28 × 4)
64-pin	μPD789456	μPD789446 with enhanced A/D converter
64-pin	μPD789446	A/D converter and on-chip voltage booster type LCD (15 × 4)
64-pin	μPD789436	μPD789426 with enhanced A/D
64-pin	μPD789426	A/D converter and on-chip voltage booster type LCD (5 × 4)
64-pin	μPD789316	RC oscillation version of the μPD789306
64-pin	μPD789306	On-chip voltage booster type LCD (24 × 4)

Dot LCD drive

144-pin	μPD789835	Segment/common outputs: 96
88-pin	μPD789830	Segments: 40, commons: 16

ASSP

80-pin	μPD789477	μPD789488 with added remote control receiver and resistance division type LCD
52-pin	μPD789467	For remote controller, with A/D converter and on-chip voltage booster type LCD
52-pin	μPD789327	For remote controller, with SIO and resistance division type LCD
64-pin	μPD789803	For PC keyboard, on-chip USB HUB function
44-pin	μPD789800	For PC keyboard, on-chip USB function
44-pin	μPD789840	For keypad, on-chip POC
20-pin	μPD789861	RC oscillation version of the μPD789860
20-pin	μPD789860	For keyless entry, on-chip POC and key return circuit

The major functional differences among the subseries are listed below.

Function Subseries Name		ROM Capacity	8-Bit	16-Bit	Watch	WDT	8-Bit A/D	10-Bit A/D	Serial Interface	I/O	V _{DD}	Remarks
											MIN. Value	
Small-scale package, general- purpose applications	μPD789046	16 K	1 ch	1 ch	1 ch	1 ch	–	–	1 ch (UART: 1 ch)	34	1.8 V	–
	μPD789026	4 K to 16 K	2 ch	–	–		8 ch	–	1 ch (UART: 1 ch)	31		
	μPD789074	2 K to 8 K		24								
	μPD789014	2 K to 4 K		–								
Small-scale package, general- purpose applications and A/D converter	μPD789177	16 K to 24 K	3 ch	1 ch		1 ch					–	8 ch
	μPD789167	8 K to 16 K	1 ch	–	8 ch	–	1 ch (UART: 1 ch)	20				
	μPD789156				–	4 ch						
	μPD789146				4 ch	–						
	μPD789134A	2 K to 8 K			–	4 ch			RC-oscillation version			
	μPD789124A	4 ch	–									
	μPD789114A	–	4 ch									
	μPD789104A	4 ch	–									
Inverter control	μPD789842	8 K to 16 K	3 ch	Note	1 ch	1 ch	8 ch	–	1 ch (UART: 1 ch)	30	4.0 V	–
VFD drive	μPD789871	4 K to 8 K	3 ch	–	1 ch	1 ch	–	–	1 ch	33	2.7 V	–
LCD drive	μPD789488	32 K	3 ch	1 ch	1 ch	1 ch	–	8 ch	2 ch (UART: 1 ch)	45	1.8 V	–
	μPD789417A	12 K to 24 K	2 ch	1 ch	1 ch	–	7 ch	1 ch (UART: 1 ch)	43			
	μPD789407A	–					–	30				
	μPD789456	12 K to 16 K					–	6 ch	–	40		
	μPD789446	–					6 ch	–				
	μPD789436	–					6 ch	–				
	μPD789426	–					6 ch	–				
	μPD789316	8 K to 16 K					–	–	2 ch (UART: 1 ch)	23		
	μPD789306	–					–	–	–	–		
Dot LCD drive	μPD789835	24 K to 60 K	6 ch			–	1 ch	1 ch	3 ch	–	1 ch (UART: 1 ch)	28
	μPD789830	24 K	1 ch	1 ch	–	–	–	–	1 ch (UART: 1 ch)	30	2.7 V	
ASSP	μPD789477	24 K	3 ch	1 ch	1 ch	1 ch	8 ch	–	2 ch (UART: 1 ch)	45	1.8 V	On-chip LCD
	μPD789467	4 K to 24 K	2 ch	–	–	1 ch	–	–	18			
	μPD789327	–	–	–	1 ch	21						
	μPD789803	8 K to 16 K	2 ch	–	–	1 ch	–	2 ch (USB: 1 ch)	41	3.6 V	–	
	μPD789800	8 K							31	4.0 V		
	μPD789840	–							4 ch	1 ch	29	2.8 V
	μPD789861	4 K							–	–	14	1.8 V
	μPD789860	–	–	–	–	On-chip EEPROM						

Note 10-bit timer: 1 channel

OVERVIEW OF FUNCTIONS

Item		μPD789304	μPD789306	μPD789314	μPD789316
Internal memory	ROM	8 KB	16 KB	8 KB	16 KB
	High-speed RAM	512 bytes			
	LCD display RAM	24 bytes			
Main system clock (oscillation frequency)		Ceramic/crystal oscillation (1.0 to 5.0 MHz)		RC oscillation (2.0 to 4.0 MHz)	
Subsystem clock (oscillation frequency)		Crystal oscillation (32.768 kHz)			
Minimum instruction execution time		0.4 μs/1.6 μs (@ 5.0 MHz operation with main system clock)		0.5 μs/2.0 μs (@ 4.0 MHz operation with main system clock)	
		122 μs (@ 32.768 kHz operation with subsystem clock)			
General-purpose registers		8 bits × 8 registers			
Instruction set		• 16-bit operation • Bit manipulation (set, reset, test)			
I/O ports		Total: 23 • CMOS I/O: 19 • N-ch open drain: 4			
Timers		• 16-bit timer: 1 channel • 8-bit timer/event counter: 2 channels • Watch timer: 1 channel • Watchdog timer: 1 channel			
Serial interface		• Switchable between 3-wire serial I/O mode and UART mode: 1 channel • 3-wire serial I/O mode: 1 channel			
LCD controller/driver		• Segment signal outputs: 24 (Max.) • Common signal outputs: 4 (Max.)			
Vectored interrupt sources	Maskable	Internal: 9, External: 5			
	Non-maskable	Internal: 1			
Power supply voltage		V _{DD} = 1.8 to 5.5 V			
Operating ambient temperature		T _A = −40 to +85°C			
Package		• 64-pin plastic QFP (14 × 14) • 64-pin plastic TQFP (12 × 12)			

CONTENTS

1. PIN CONFIGURATION (TOP VIEW)	7
2. BLOCK DIAGRAM	9
3. PIN FUNCTIONS	10
3.1 Port Pins	10
3.2 Non-Port Pins	11
3.3 Pin I/O Circuits and Recommended Connection of Unused Pins	12
4. MEMORY SPACE.....	14
5. PERIPHERAL HARDWARE FUNCTIONS	15
5.1 Ports	15
5.2 Clock Generator.....	16
5.3 Timer.....	17
5.4 Serial Interface.....	22
5.5 LCD Controller/Driver.....	25
6. INTERRUPT FUNCTIONS.....	27
7. STANDBY FUNCTION	29
8. RESET FUNCTION.....	29
9. MASK OPTIONS	29
10. OVERVIEW OF INSTRUCTION SET	30
10.1 Conventions.....	30
10.2 List of Operations.....	32
11. ELECTRICAL SPECIFICATIONS	37
★ 12. CHARACTERISTICS CURVES OF LCD CONTROLLER/DRIVER (REFERENCE VALUES).....	54
13. PACKAGE DRAWINGS	56
★ 14. RECOMMENDED SOLDERING CONDITIONS.....	58
APPENDIX A. DEVELOPMENT TOOLS	59
APPENDIX B. RELATED DOCUMENTS.....	61

1. PIN CONFIGURATION (TOP VIEW)

64-pin plastic QFP (14 × 14)

μPD789304GC-xxx-AB8

μPD789306GC-xxx-AB8

μPD789314GC-xxx-AB8

μPD789316GC-xxx-AB8

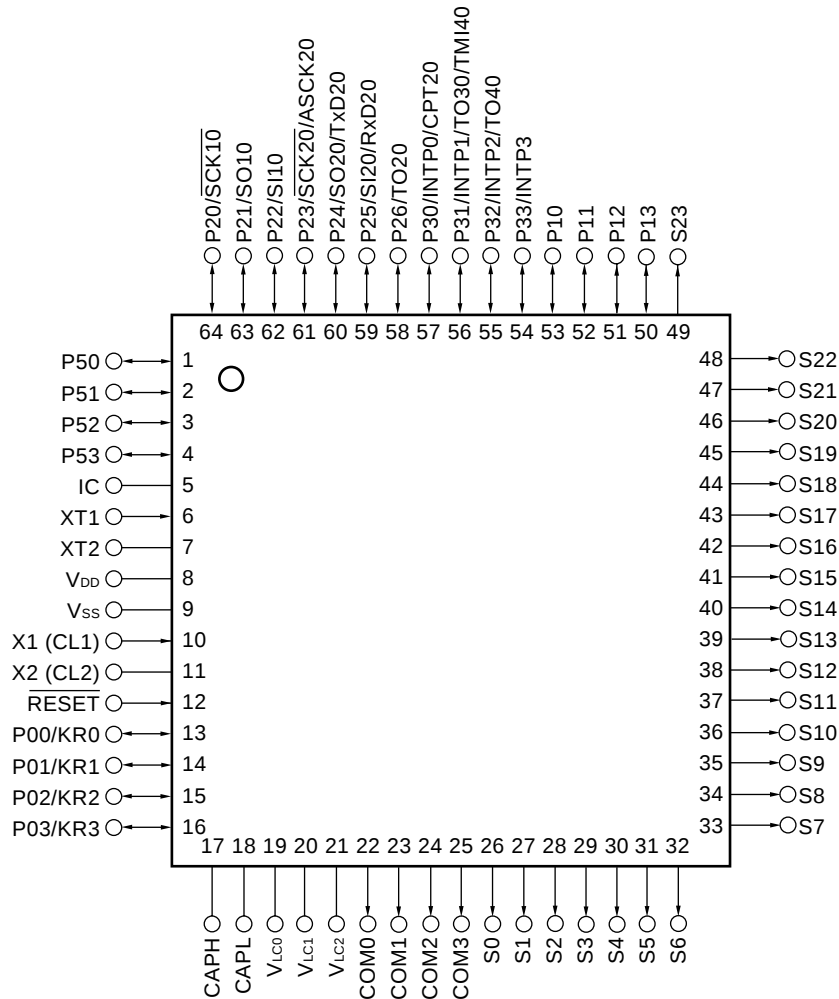
64-pin plastic TQFP (12 × 12)

μPD789304GK-xxx-9ET

μPD789306GK-xxx-9ET

μPD789314GK-xxx-9ET

μPD789316GK-xxx-9ET

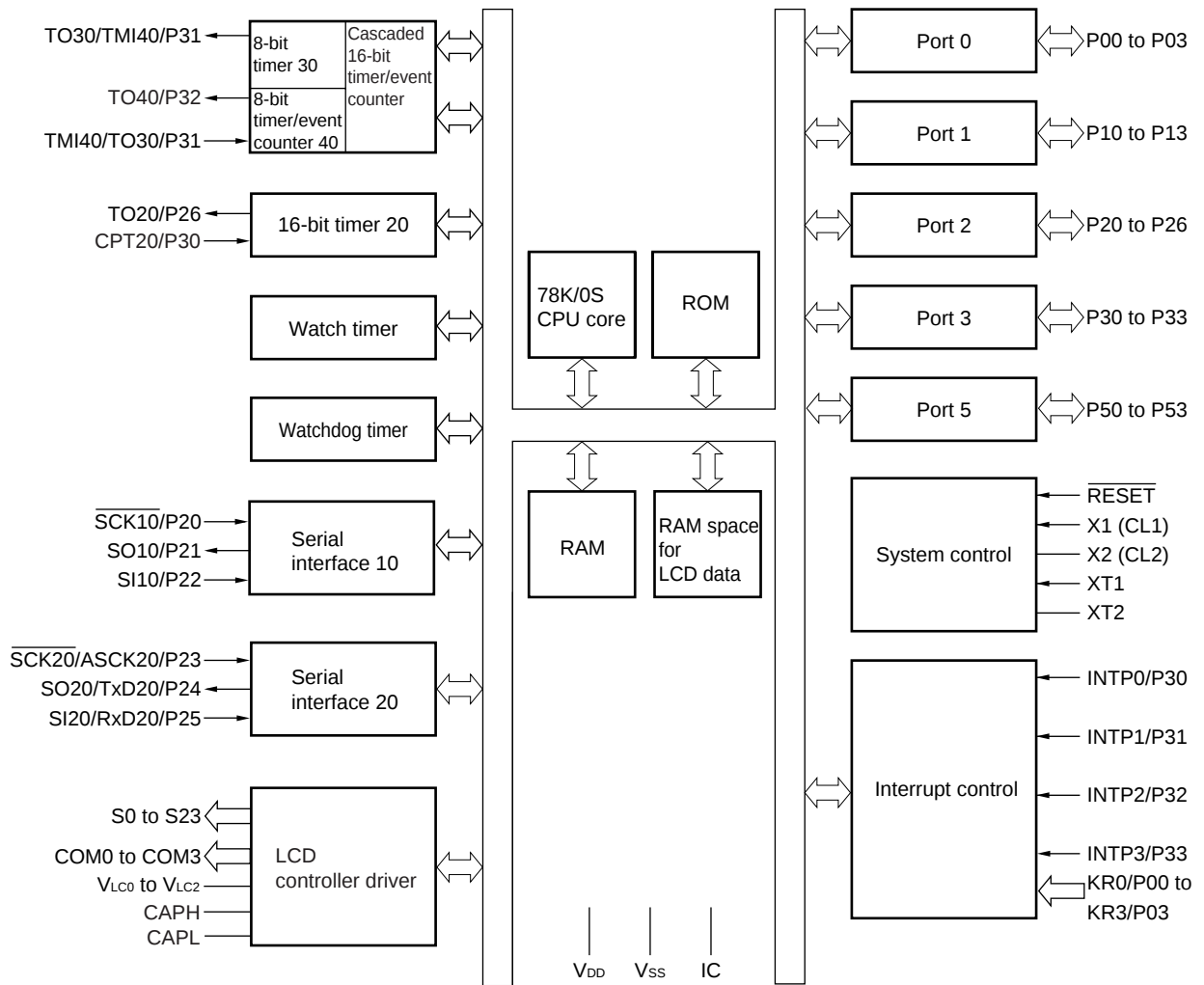


Caution Connect the IC (Internally Connected) pin directly to the Vss pin.

Remark Pin names enclosed in parentheses are when using the μPD789314, 789316.

ASCK20:	Asynchronous serial input	RESET:	Reset
CAPH, CAPL:	LCD power supply capacitance control	RxD20:	Receive data
CL1, CL2:	RC oscillator	S0 to S23:	Segment output
COM0 to COM3:	Common output	SCK10, SCK20:	Serial clock
CPT20:	Capture trigger input	SI10, SI20:	Serial input
IC:	Internally connected	SO10, SO20:	Serial output
INTP0 to INTP3:	External interrupt input	TMI40:	Timer input
KR0 to KR3:	Key return	TO20, TO30, TO40:	Timer output
P00 to P03:	Port 0	TxD20:	Transmit data
P10 to P13:	Port 1	VDD:	Power supply
P20 to P26:	Port 2	V _{LC0} to V _{LC2} :	LCD power supply
P30 to P33:	Port 3	VSS:	Ground
P50 to P53:	Port 5	X1, X2:	Crystal/ceramic oscillator
		XT1, XT2:	Crystal oscillator

2. BLOCK DIAGRAM



Remark Pin names enclosed in parentheses are when using the μPD789314, 789316.

3. PIN FUNCTIONS

3.1 Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
P00 to P03	I/O	Port 0. 4-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified in port units by software.	Input	KR0 to KR3
P10 to P13	I/O	Port 1. 4-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified in port units by software.	Input	—
P20	I/O	Port 2. 7-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified in 1-bit units by software.	Input	SCK10
P21				SO10
P22				SI10
P23				SCK20/ASCK20
P24				SO20/TxD20
P25				SI20/RxD20
P26				TO20
P30	I/O	Port 3. 4-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified in 1-bit units by software.	Input	INTP0/CPT20
P31				INTP1/TO30/TMI40
P32				INTP2/TO40
P33				INTP3
P50 to P53	I/O	Port 5. 4-bit I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified in bit units by the mask option.	Input	—

3.2 Non-Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input	P30/CPT20
INTP1				P31/TO30/TMI40
INTP2				P32/TO40
INTP3				P33
KR0 to KR3	Input	Key return signal detection	Input	P00 to P03
SCK10	I/O	Serial clock input/output for serial interface (SIO10)	Input	P20
SCK20		Serial clock input/output for serial interface (SIO20)		P23/ASCK20
SI10	Input	Serial data input for SIO10 serial interface	Input	P22
SI20		Serial data input for SIO20 serial interface		P25/RxD20
SO10	Output	Serial data output for SIO10 serial interface	Input	P21
SO20		Serial data output for SIO20 serial interface		P24/TxD20
ASCK20	Input	Serial clock input for asynchronous serial interface	Input	P23/SCK20
RxD20	Input	Serial data input for asynchronous serial interface	Input	P25/SI20
TxD20	Output	Serial data output for asynchronous serial interface	Input	P24/SO20
TO20	Output	16-bit timer (TM20) output	Input	P26
CPT20	Input	Capture edge input	Input	P30/INTP0
TO30	Output	8-bit timer (TM30) output	Input	P31/INTP1/TMI40
TO40	Output	8-bit timer (TM40) output	Input	P32/INTP2
TMI40	Input	External count clock input to 8-bit timer (TM40)	Input	P31/INTP1/TO30
S0 to S23	Output	Segment signal output for LCD controller/driver	Output	—
COM0 to COM3	Output	Common signal output for LCD controller/driver	Output	—
V _{LC0} to V _{LC2}	—	LCD drive voltage	—	—
CAPH	—	Connection pin for LCD driver's capacitor	—	—
CAPL	—		—	—
X1 ^{Note 1}	Input	Connecting crystal resonator for main system clock oscillation	—	—
X2 ^{Note 1}	—		—	—
CL1 ^{Note 2}	Input	Connections to resistor (R) and capacitor (C) for main system clock oscillation	—	—
CL2 ^{Note 2}	—		—	—
XT1	Input	Connecting crystal resonator for subsystem clock oscillation	—	—
XT2	—		—	—
RESET	Input	System reset input	Input	—
V _{DD}	—	Positive power supply	—	—
V _{SS}	—	Ground potential	—	—
IC	—	Internally connected. Connect directly to V _{SS} .	—	—

Notes 1. μPD789304, 789306 only

2. μPD789314, 789316 only

3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

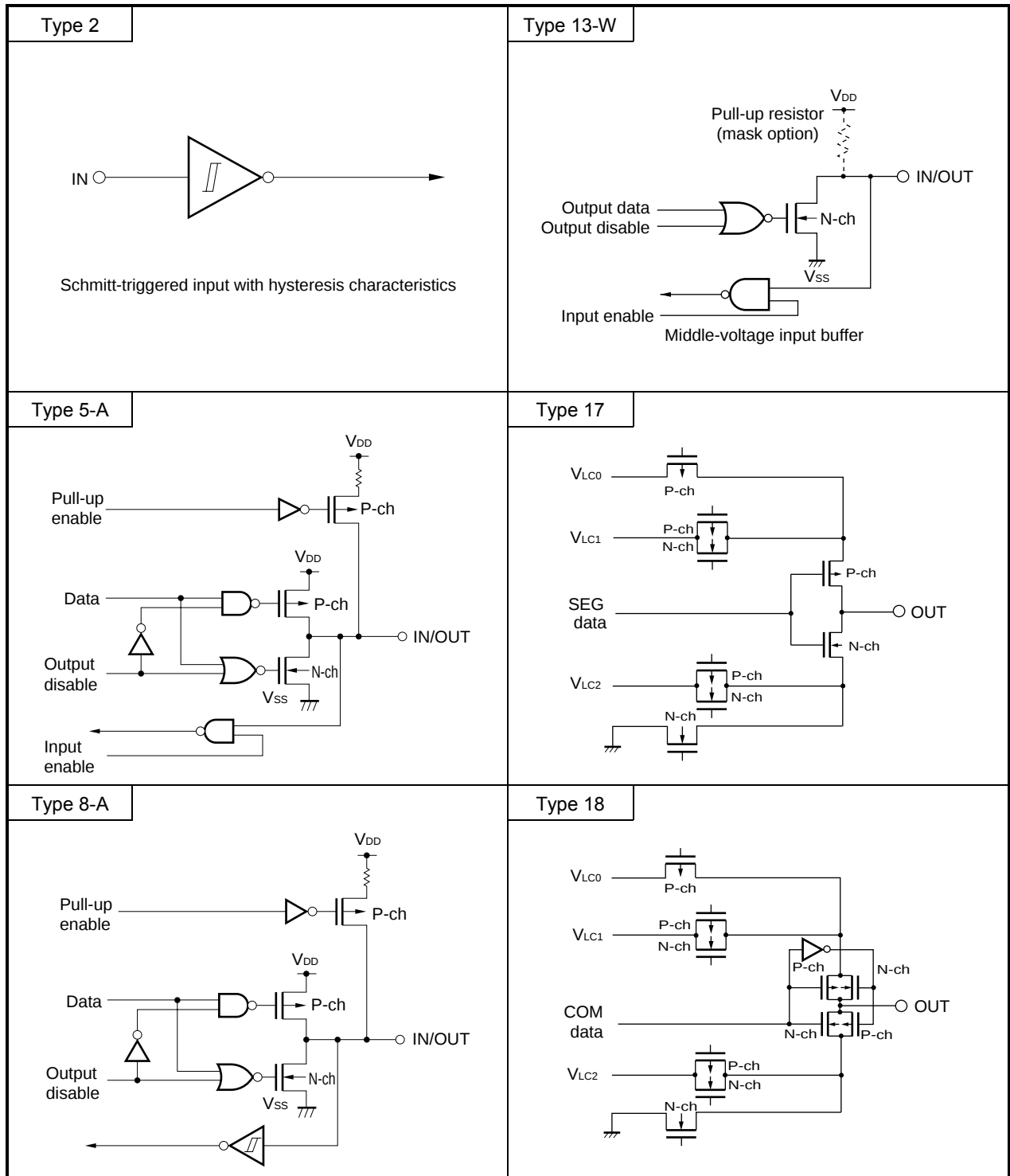
The I/O circuit type of each pin and recommended connection of unused pins are shown in Table 3-1.

For the I/O circuit configuration of each type, refer to Figure 3-1.

Table 3-1. Types of Pin I/O Circuits and Recommended Connection of Unused Pins

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00/KR0 to P03/KR3	8-A	I/O	Input: Independently connect to V _{DD} or V _{SS} via a resistor. Output: Leave open.
P10 to P13	5-A		
P20/SCK10	8-A		
P21/SO10			
P22/SI10			
P23/SCK20/ASCK20			
P24/SO20/TxD20			
P25/SI20/RxD20			
P26/TO20			
P30/INTP0/CPT20			Input: Independently connect to V _{SS} via a resistor. Output: Leave open.
P31/INTP1/TO30/ TMI40			
P32/INTP2/TO40			
P33/INTP3			
P50 to P53	13-W		Input: Independently connect to V _{DD} via a resistor. Output: Leave open.
S0 to S23	17	Output	Leave open.
COM0 to COM3	18		
V _{LC0} to V _{LC2}	—	—	
CAPH, CAPL	—		
XT1	—	Input	Connect to V _{SS} .
XT2		—	Leave open.
RESET	2	Input	—
IC	—	—	Directly connect to V _{SS} .

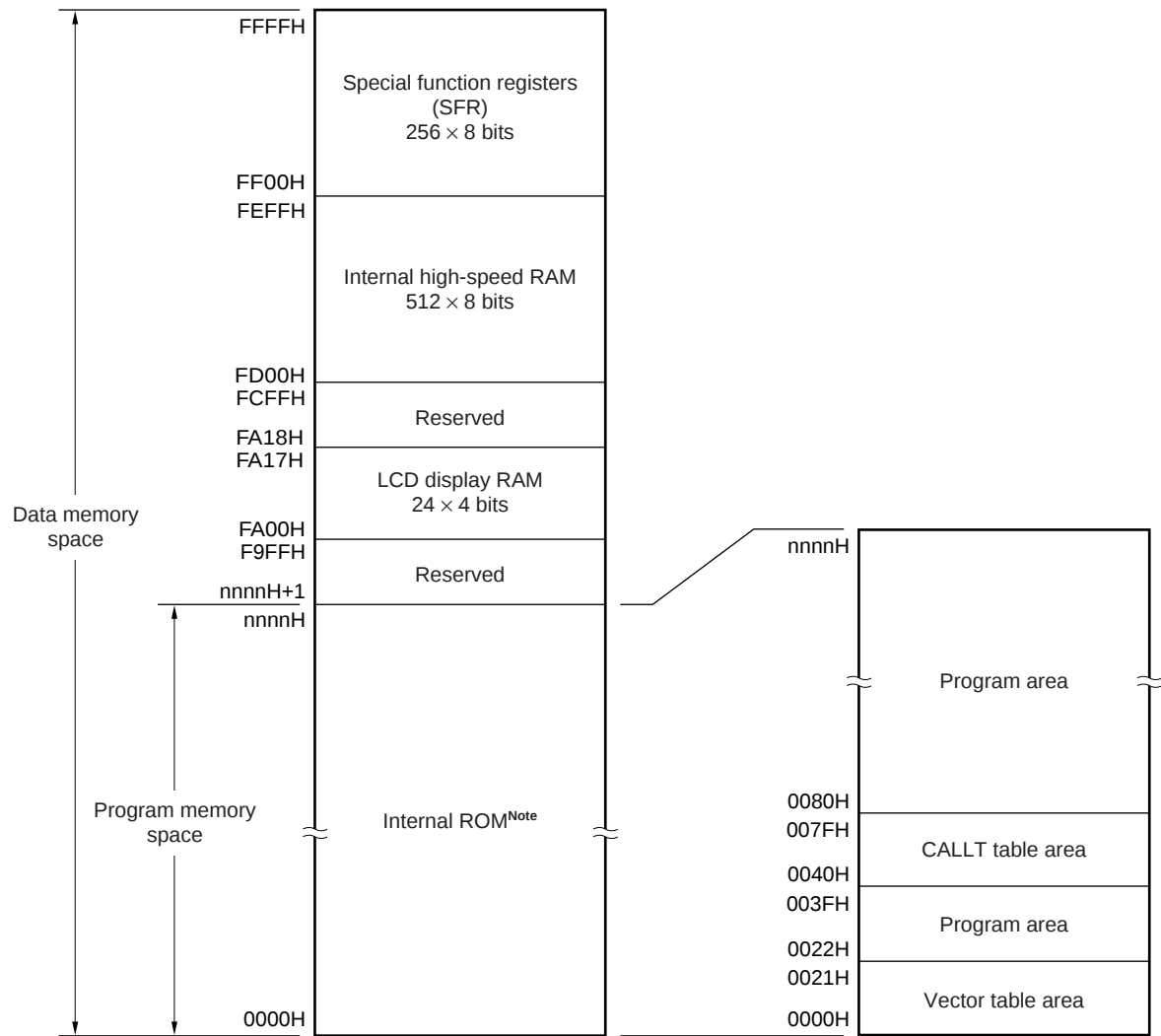
Figure 3-1. Pin I/O Circuits



4. MEMORY SPACE

Figure 4-1 shows the memory map of the μPD789304, 789306, 789314, and 789316.

Figure 4-1. Memory Map



Note The internal ROM capacity depends on the product (see the following table).

Part Number	Last Address of Internal ROM nnnnH
μPD789304, 789314	1FFFH
μPD789306, 789316	3FFFH

5. PERIPHERAL HARDWARE FUNCTIONS

5.1 Ports

The I/O ports are listed below.

- CMOS I/O: 19
- N-ch open-drain I/O: 4

Table 5-1. Port Functions

Port Name	Pin Name	Function
Port 0	P00 to P03	I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by software.
Port 1	P10 to P13	I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by software.
Port 2	P20 to P26	I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by software.
Port 3	P30 to P33	I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by software.
Port 5	P50 to P53	I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by the mask option.

5.2 Clock Generator

The specifications of the main system clock generator differ depending on the product as shown below.

(1) Main system clock generator

- Ceramic/crystal oscillation: μ PD789304, 789306

This generator's oscillation frequency range is 1.0 to 5.0 MHz. The minimum instruction execution time can be changed from 0.4 to 1.6 μ s (@ 5.0 MHz operation).

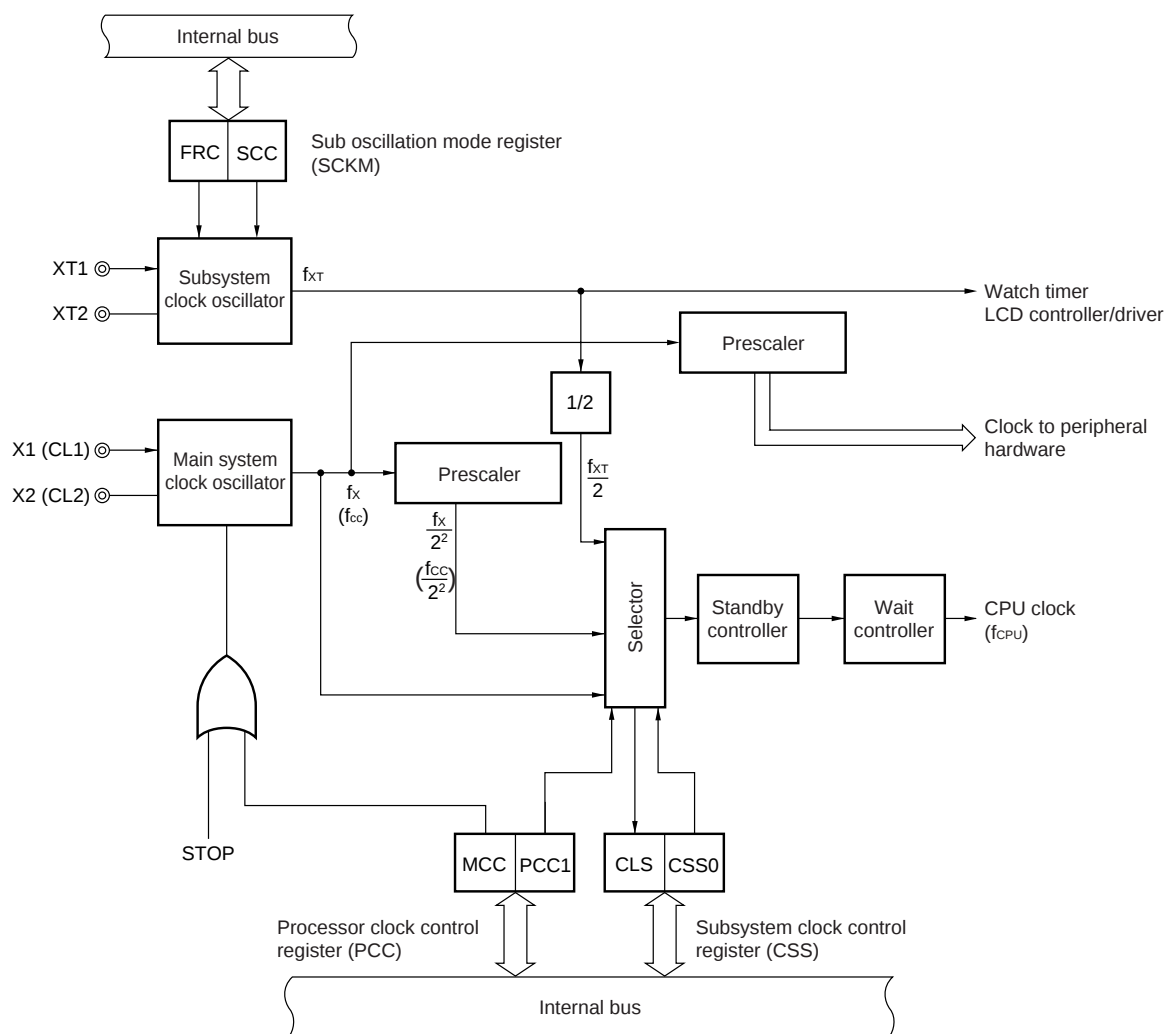
- RC oscillation: μ PD789314, 789316

This generator's oscillation frequency range is 2.0 to 4.0 MHz. The minimum instruction execution time can be changed from 0.5 to 2.0 μ s (@ 4.0 MHz operation).

(2) Subsystem clock generator (crystal oscillation)

This generator's oscillation frequency is 32.768 kHz. The minimum instruction execution time is 122 μ s (@ 32.768 kHz operation).

Figure 5-1. Block Diagram of Clock Generator



Remark Pins names enclosed in parentheses are when using the RC oscillation (μ PD789314, 789316).

5.3 Timer

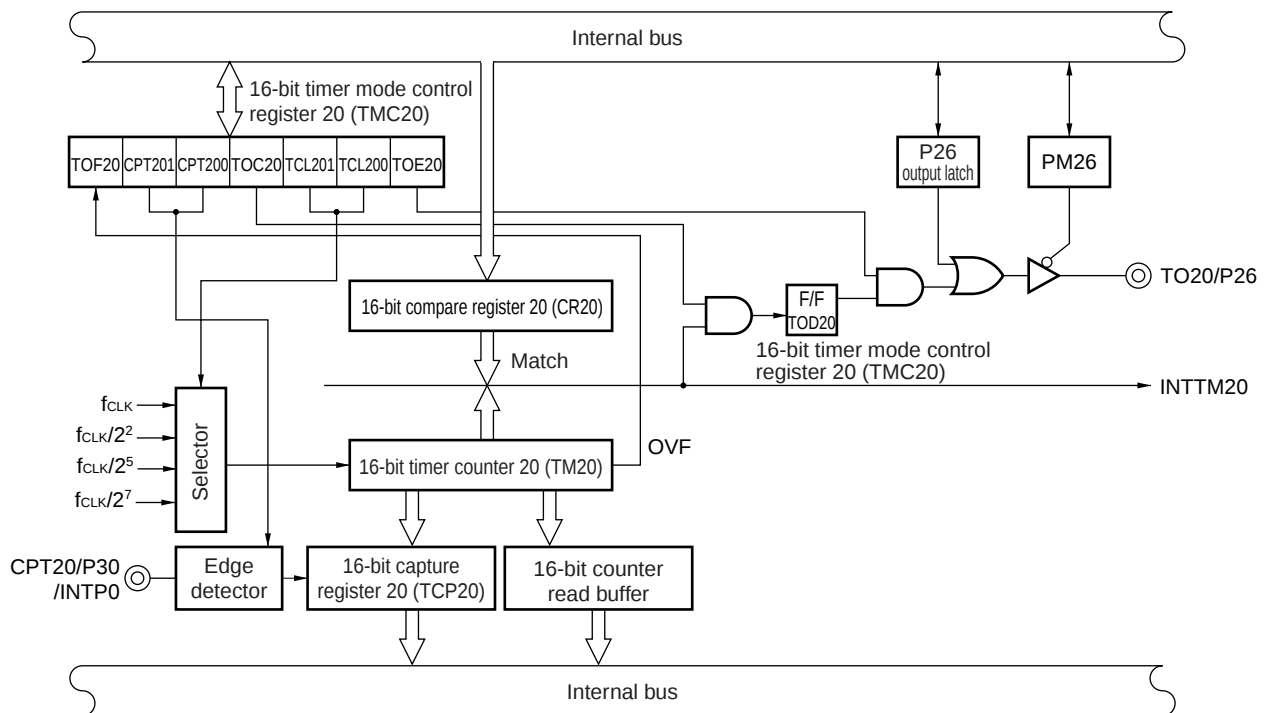
Five timer channels are incorporated.

- 16-bit timer (TM20): 1 channel
- 8-bit timer (TM30, TM40): 2 channels
- Watch timer (WT): 1 channel
- Watchdog timer (WTM): 1 channel

Table 5-2. Timer Operation

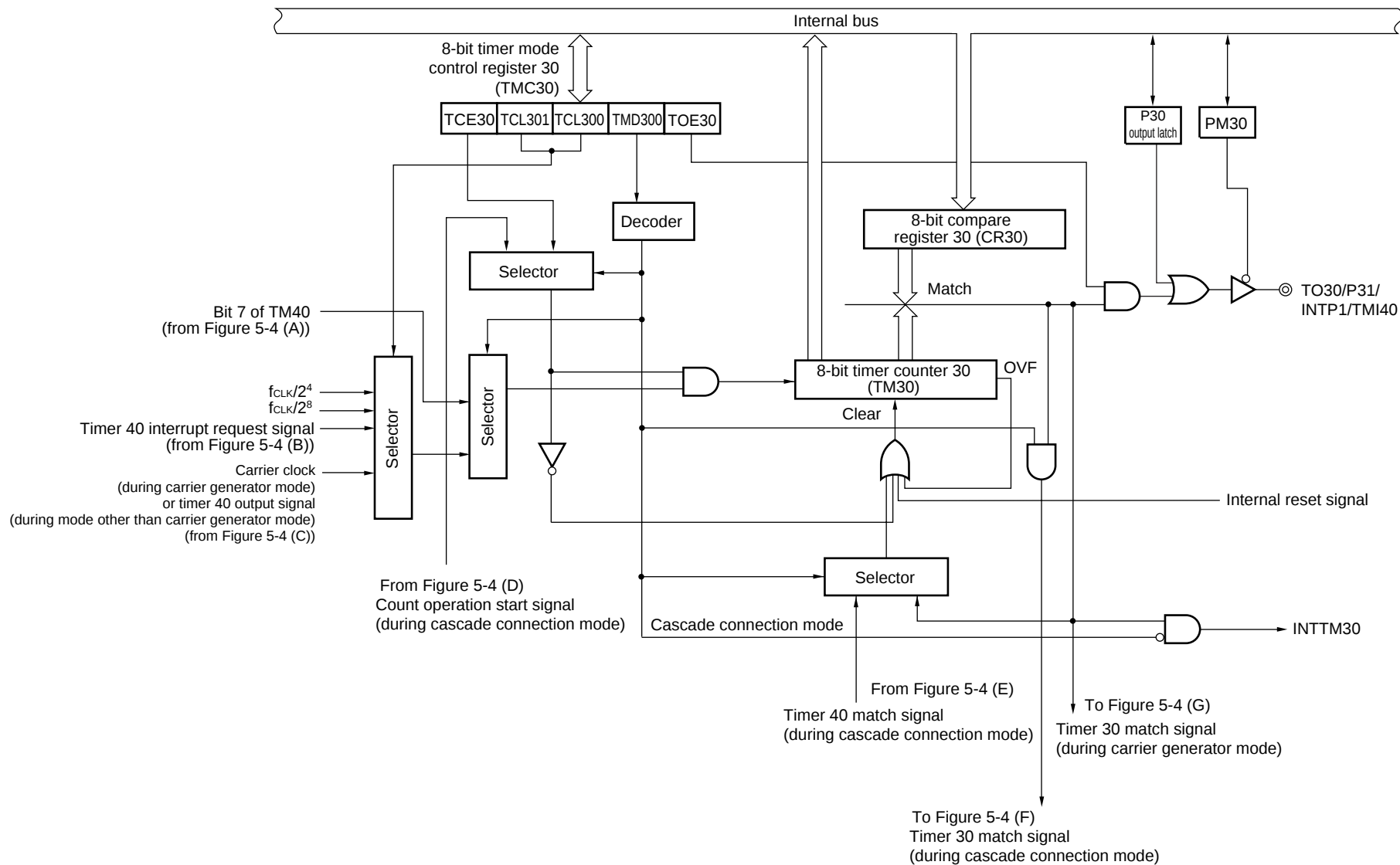
		TM20	TM30	TM40	WT	WTM
Operation mode	Interval time	1 channel	1 channel	1 channel	1 channel	1 channel
	External event counter	—	1 channel	1 channel	—	—
Function	Timer output	1 output	1 output	1 output	—	—
	Square wave output	—	1 output	1 output	—	—
	Interrupt request	1	1	1	1	1

Figure 5-2. Block Diagram of 16-Bit Timer (TM20)



Remark f_{CLK}: f_x or f_{cc}

Figure 5-3. Block Diagram of Timer 30 (TM30)



Remark fCLK: fx or fcc

The diagram illustrates the internal architecture of the 8-bit timer counter 40 (TM40). Key components and their connections include:

- Registers:**
 - 8-bit timer mode control register 40 (TMC40):** Contains bits TCE40, TCL402, TCL401, TCL400, TMD401, TMD400, and TOE40.
 - 8-bit compare register H40 (CRH40) and 8-bit compare register 40 (CR40):** Connected to the internal bus and a Selector.
 - Carrier generator output control register 40 (TCA40):** Contains bits RMC40, NRZB40, and NRZ40.
- Logic and Control:**
 - Decoder:** Receives inputs from TMD401 and TMD400.
 - Selector:** Receives inputs from TCE40, TMD401, TMD400, and the internal bus. It selects between different clock sources for the timer counter.
 - 8-bit timer counter 40 (TM40):** The core counting unit, receiving a clock signal from the Selector. It has a Match output and an OVF (overflow) output.
 - Match Logic:** The Match signal is compared with CRH40 and CR40. If they match, it triggers the F/F (flip-flop) and the Output control circuit.
 - Output control circuit:** Receives inputs from the Match signal, RMC40, NRZB40, and NRZ40. It generates the TO40/P32/INTP2 output signal.
 - Reset Logic:** The Reset signal is generated by an OR gate combining the OVF signal, the Match signal, and the internal reset signal.
- External Connections and Modes:**
 - Carrier generator mode:** Enabled by TCE40, it uses the carrier generator output control register (TCA40) to generate a carrier wave.
 - PWM mode:** Enabled by TMD401, it generates a pulse-width modulated signal.
 - Cascade connection mode:** Enabled by TMD400, it allows the timer to be cascaded with other timers. It uses the TMD401 and TMD400 signals to generate a count operation start signal to timer 30 and a TM40 timer counter match signal.
 - Interrupts:** The INTTM40 signal is generated by the OVF signal, and the timer 40 interrupt request signal is generated by the Match signal.

Remark f_{CLK} : f_X or f_{CC}

Data Sheet U14384EJ1V0DS

Figure 5-5. Block Diagram of Output Controller (Timer 40)

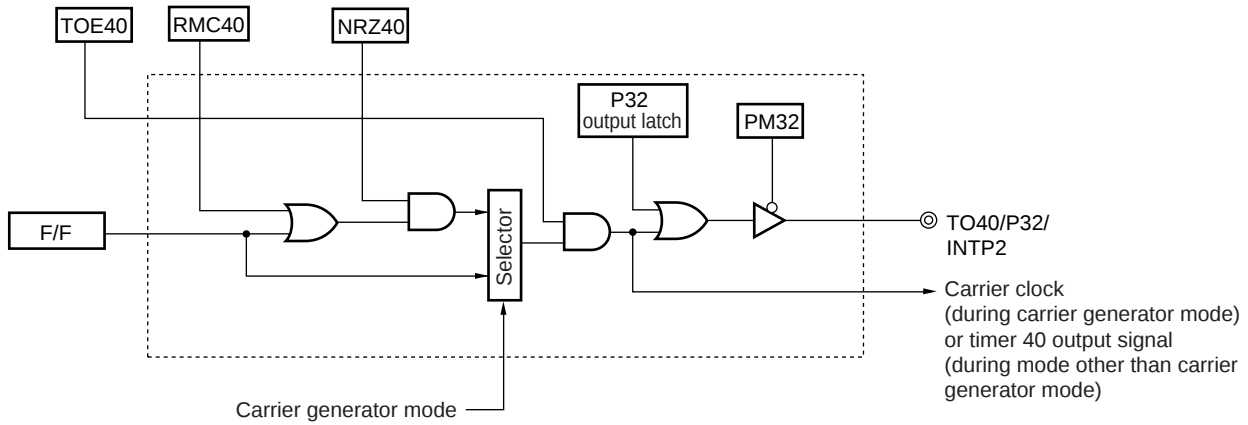
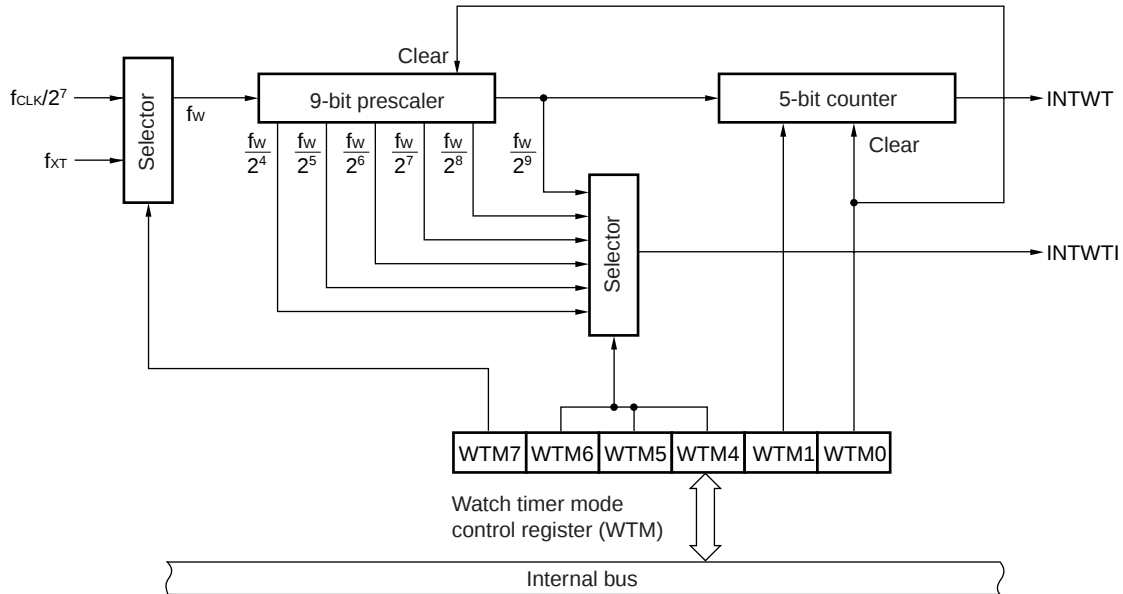
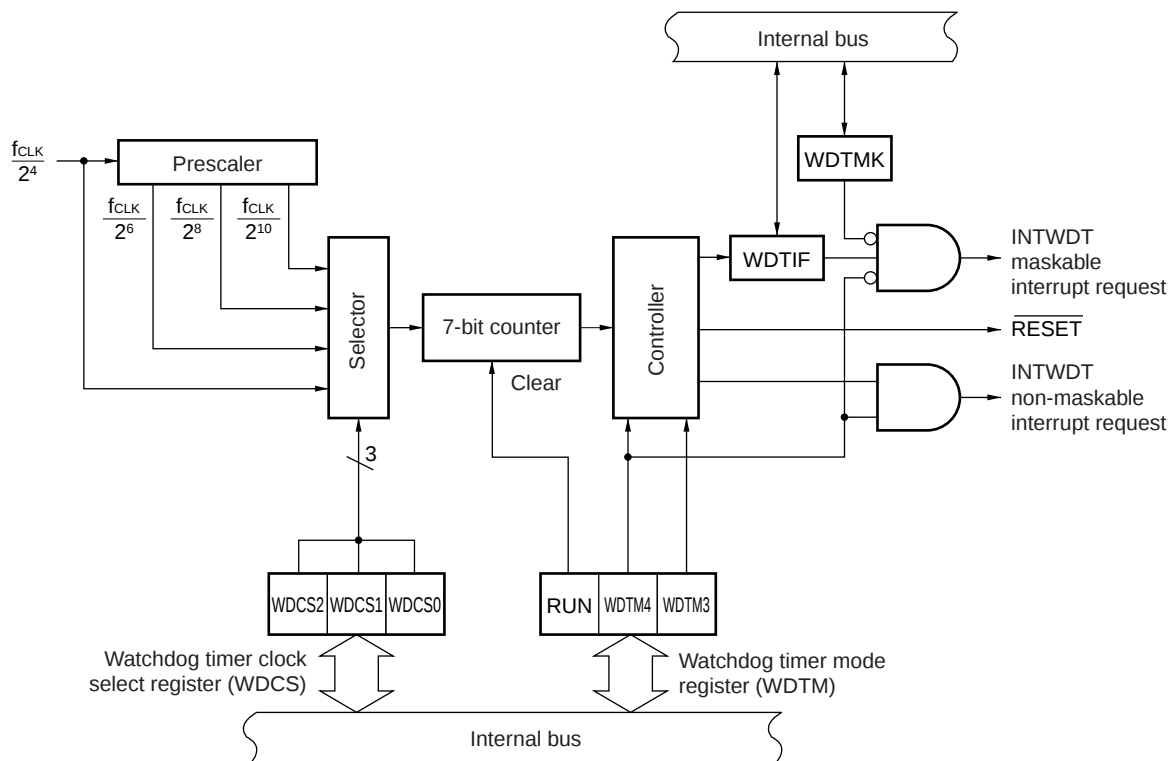


Figure 5-6. Block Diagram of Watch Timer (WT)



Remark f_{CLK} : f_X or f_{CC}

Figure 5-7. Block Diagram of Watchdog Timer (WTM)



Remark f_{CLK} : f_x or f_{CC}

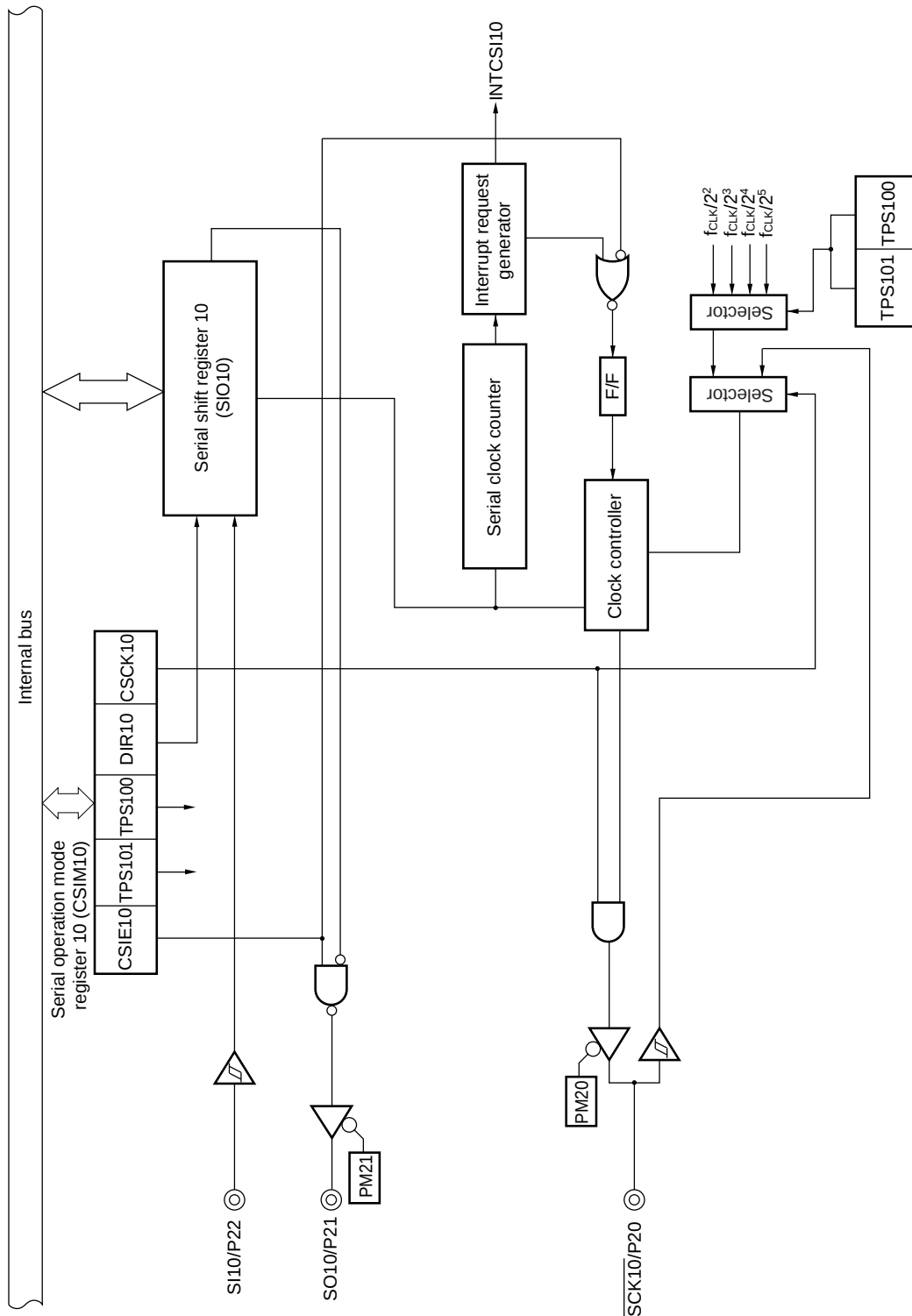
5.4 Serial Interface

5.4.1 Serial interface 10 (SIO10)

Serial interface 10 (SIO10) has the following two types of modes.

- Operation stop mode
- 3-wire serial I/O mode

Figure 5-8. Block Diagram of Serial Interface 10

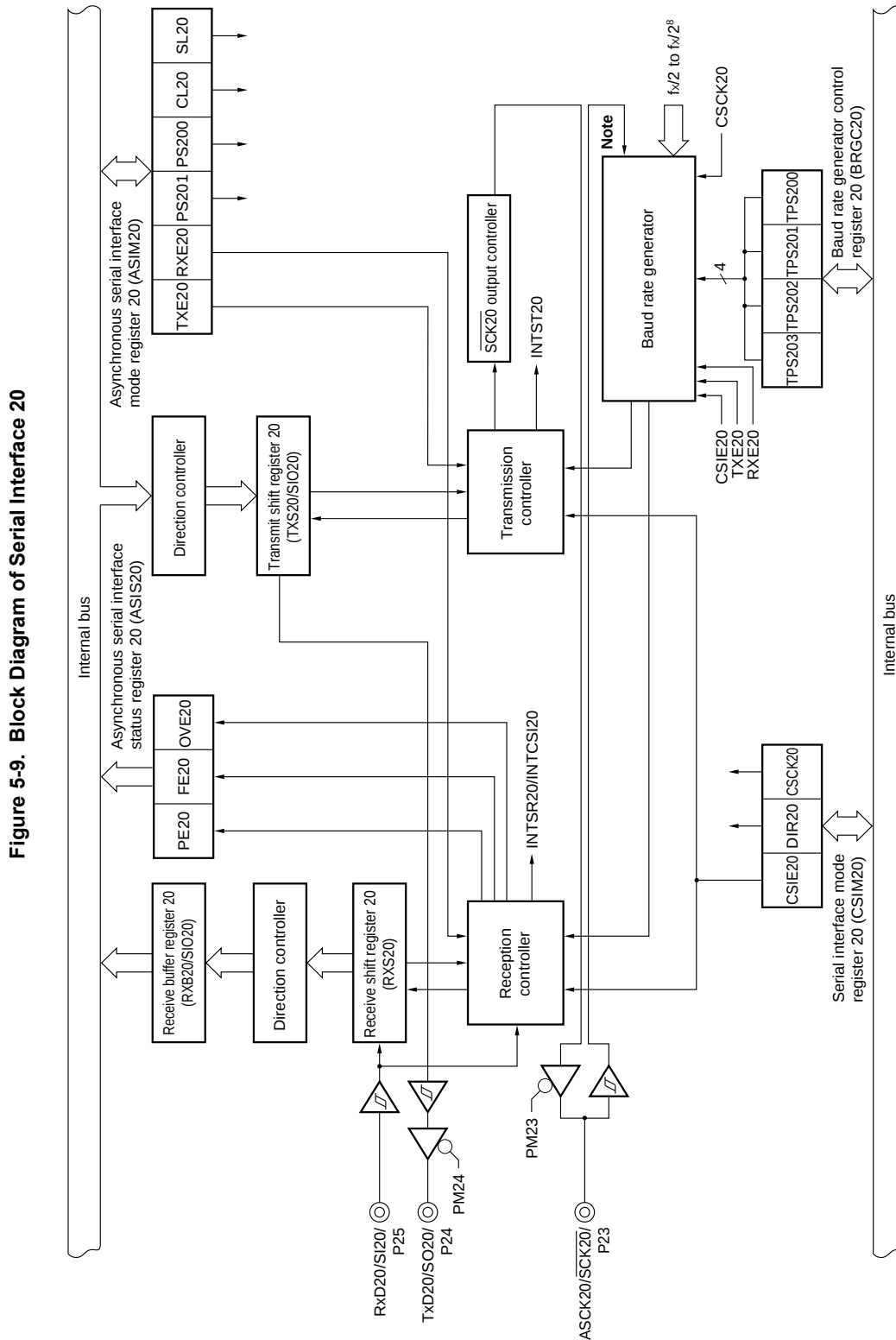


Remark f_{CLK}: fx or fcc

5.4.2 Serial interface 20 (SIO20)

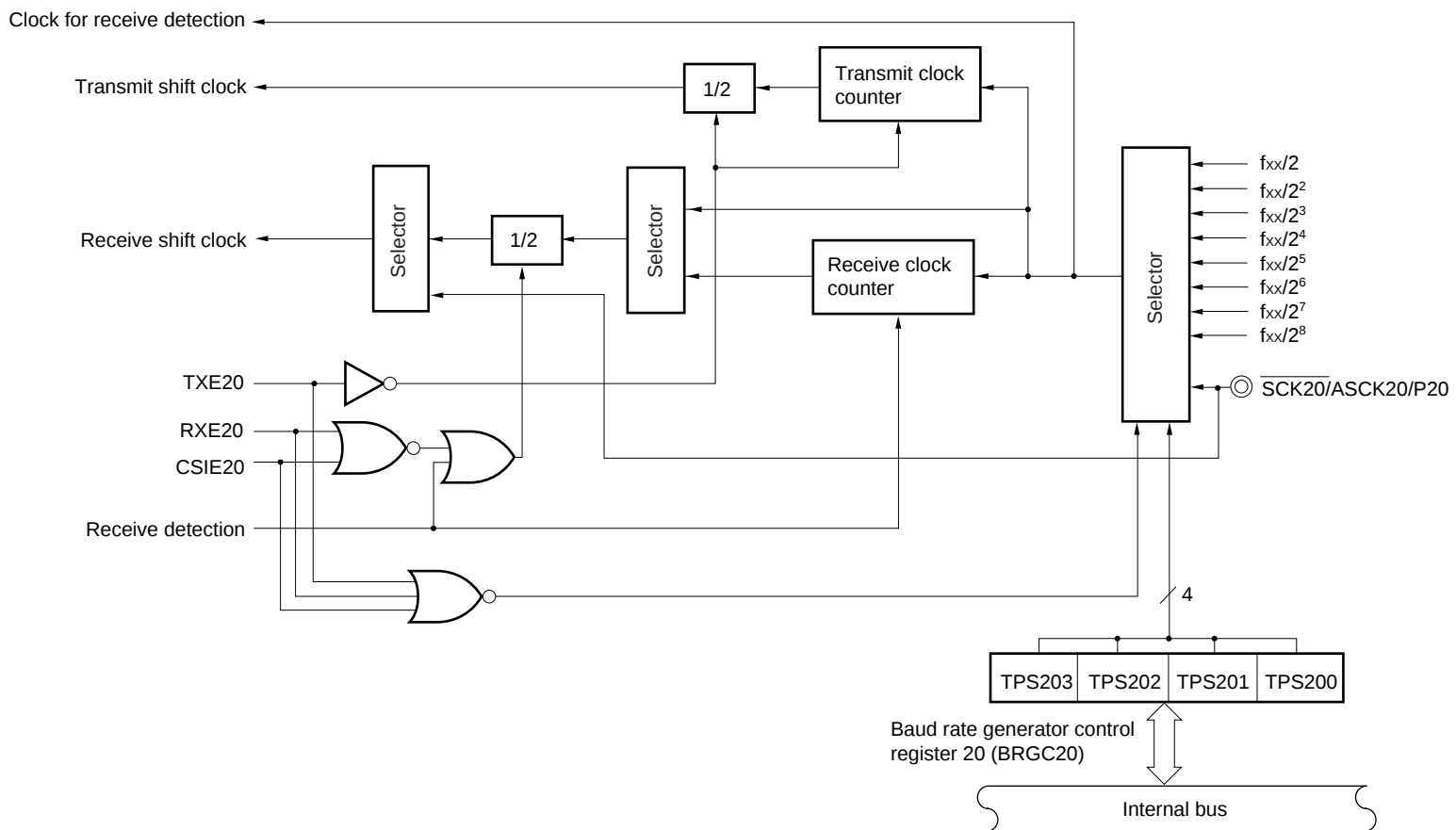
Serial interface 20 (SIO20) has the following three types of modes.

- Operation stop mode
- Asynchronous serial interface (UART) mode
- 3-wire serial I/O mode



Note See Figure 5-10 for the configuration of the baud rate generator.

Figure 5-10. Block Diagram of Baud Rate Generator 20

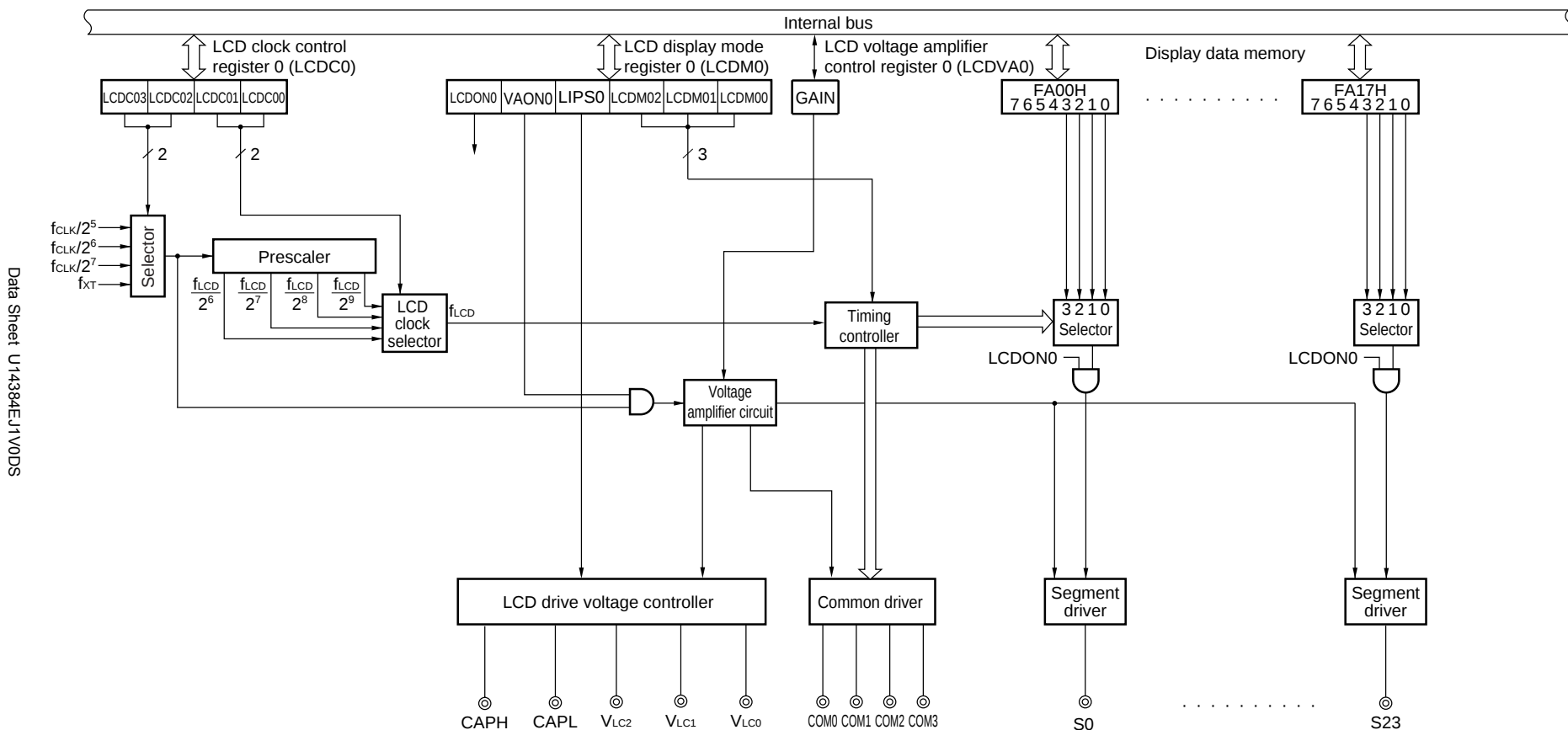


5.5 LCD Controller/Driver

The LCD controller/driver has the following functions.

- (1) Enables automatic output of segment signals and common signals by automatically reading from display data memory.
- (2) Two types of display modes can be selected:
 - 1/3 duty (1/3 bias)
 - 1/4 duty (1/3 bias)
- (3) Any of four frame frequency settings can be selected for each display mode.
- (4) There are up to 24 segment signal outputs (S0 to S23) and four common signal outputs (COM0 to COM3).
- (5) Operation using the subsystem clock is also supported.

Figure 5-11. Block Diagram of LCD Controller/Driver



Remark f_{CLK} : f_X or f_{CC}

6. INTERRUPT FUNCTIONS

A total of 15 interrupt sources divided into the following two types are provided.

- Non-maskable: 1
- Maskable: 14

Table 6-1. Interrupt Source List

Interrupt Type	Priority ^{Note 1}	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type ^{Note 2}
		Name	Trigger			
Non-maskable	–	INTWDT	Watchdog timer overflow (with watchdog timer mode 1 selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (with interval timer mode selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	
	3	INTP2			000AH	
	4	INTP3			000CH	
	5	INTSR20	End of serial interface 20 UART reception	Internal	000EH	(B)
		INTCSI20	End of serial interface 20 3-wire SIO transfer reception			
	6	INTCSI10	End of serial interface 10 3-wire SIO transfer reception		0010H	
	7	INTST20	End of serial interface 20 UART transmission		0012H	
	8	INTWTI	Watch timer interval timer interrupt		0014H	
	9	INTTM20	Generation of match signal of 16-bit timer 20		0016H	
	10	INTTM30	Generation of match signal of 8-bit timer 30		0018H	
	11	INTTM40	Generation of match signal of 8-bit timer/event counter 40		001AH	
	12	INTWT	Watch timer interrupt		001EH	
	13	INTKR00	Key return signal detection	External	0020H	(C)

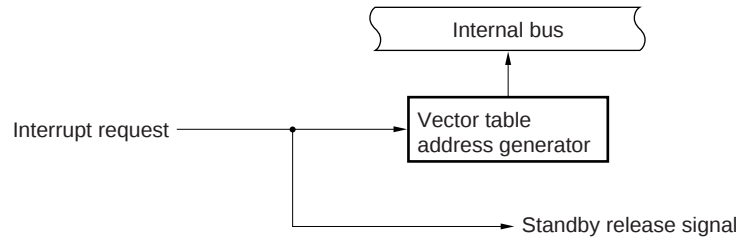
Notes 1. Default priority is the priority order when several maskable interrupt requests are generated at the same time. 0 is the highest order and 13 is the lowest order.

2. Basic configuration types (A) to (C) correspond to (A) to (C) in Figure 6-1.

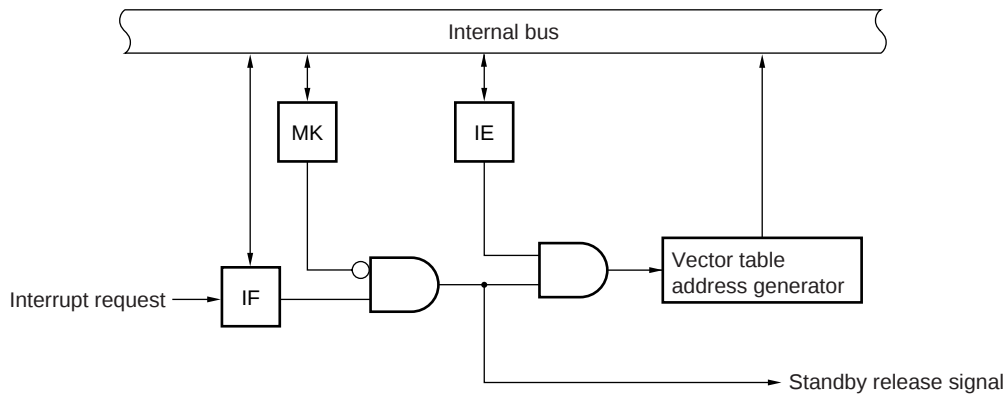
Remark Two watchdog timer interrupt sources (INTWDT): a non-maskable interrupt and a maskable interrupt (internal), are available, either of which can be selected.

Figure 6-1. Basic Configuration of Interrupt Function

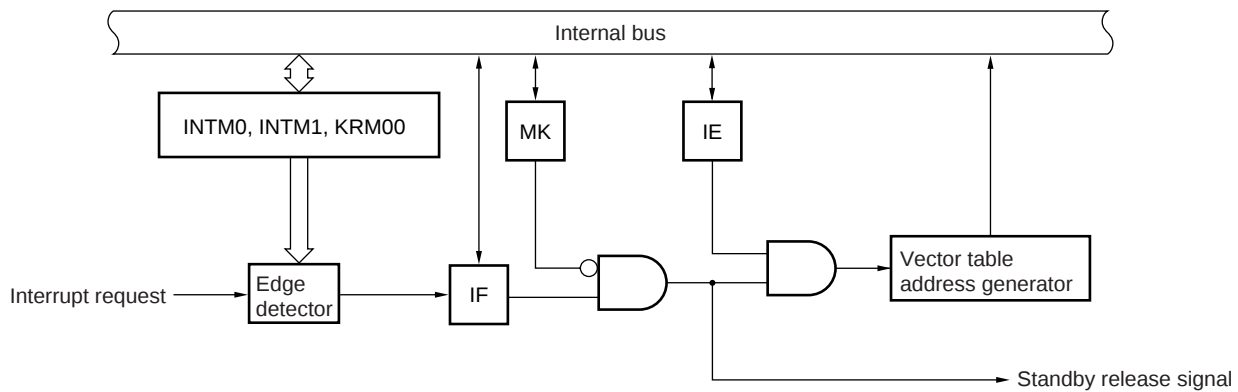
(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt



INTM0: External interrupt mode register 0

INTM1: External interrupt mode register 1

KRM00: Key return mode register 00

IF: Interrupt request flag

IE: Interrupt enable flag

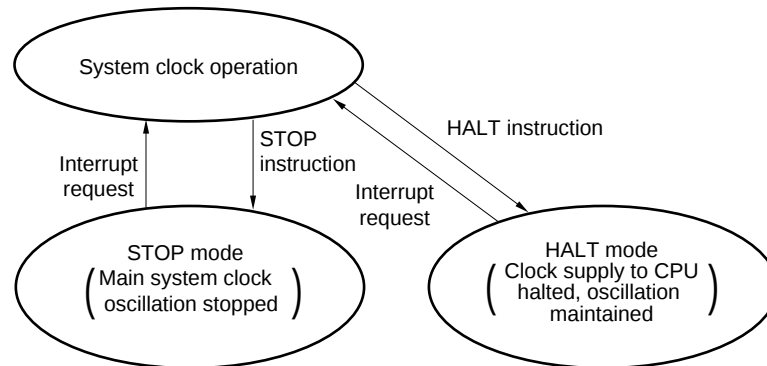
MK: Interrupt mask flag

7. STANDBY FUNCTION

The following two standby modes are available for further reduction of system current consumption.

- HALT mode: In this mode, the CPU operation clock is stopped. The average current consumption can be reduced by intermittent operation by combining this mode with the normal operation.
- STOP mode: In this mode, oscillation of the main system clock is stopped. All operations performed on the main system clock are suspended resulting in extremely small power consumption.

Figure 7-1. Standby Function



8. RESET FUNCTION

The following two reset methods are available.

- External reset by $\overline{\text{RESET}}$ pin
- Internal reset by watchdog timer program loop time detection

9. MASK OPTIONS

The μPD789304, 789306, 789314, and 789316 have the following mask options.

- Mask options for P50 to P53
An on-chip pull-up resistor can be selected.
<1> Specifies on-chip pull-up resistor in 1-bit units.
<2> Does not specify on-chip pull-up resistor.

10. OVERVIEW OF INSTRUCTION SET

This section lists the instruction set for the μPD789304, 789306, 789314, and 789316.

10.1 Conventions

10.1.1 Operand expressions and description methods

Operands are described in "Operand" column of each instruction in accordance with the description method of the instruction operand expression (see the assembler specifications for details). When there are two or more description methods, select one of them. Uppercase letters and symbols, #, !, \$, and [] are key words and are described as they are. The meaning of each symbol is described below.

- # : Immediate data specification
- ! : Absolute address specification
- \$: Relative address specification
- [] : Indirect address specification

For immediate data, enter an appropriate numeric value or a label. When using a label, be sure to enter the #, !, \$ and [] symbols.

For operand register expressions, r and rp, either function names (X, A, C, etc.) or absolute names (names in parenthesis in the table below, R0, R1, R2, etc.) can be used for the description.

Table 10-1. Operand Expressions and Description Methods

Expression	Description Method
r	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7)
rp	AX (RP0), BC (RP1), DE (RP2), HL (RP3)
sfr	Special function register symbol
saddr	FE20H to FF1FH: immediate data or label
saddrp	FE20H to FF1FH: immediate data or label (even addresses only)
addr16	0000H to FFFFH: immediate data or label (even addresses only for 16-bit data transfer instruction)
addr5	0040H to 007FH: immediate data or label (even addresses only)
word	16-bit immediate data or label
byte	8-bit immediate data or label
bit	3-bit immediate data or label

10.1.2 Description of “Operation” column

A:	A register; 8-bit accumulator
X:	X register
B:	B register
C:	C register
D:	D register
E:	E register
H:	H register
L:	L register
AX:	AX register pair; 16-bit accumulator
BC:	BC register pair
DE:	DE register pair
HL:	HL register pair
PC:	Program counter
SP:	Stack pointer
PSW:	Program status word
CY:	Carry flag
AC:	Auxiliary carry flag
Z:	Zero flag
IE:	Interrupt request enable flag
NMIS:	Flag indicating non-maskable interrupt servicing in progress
():	Memory contents indicated by address or register contents in parenthesis
X _H , X _L :	Higher 8 bits and lower 8 bits of 16-bit register
∧:	Logical product (AND)
∨:	Logical sum (OR)
⊕:	Exclusive logical sum (exclusive OR)
—:	Inverted data
addr16:	16-bit immediate data or label
jdsp8:	Signed 8-bit data (displacement value)

10.1.3 Description of “Flag” column

(Blank):	Unchanged
0:	Cleared to 0
1:	Set to 1
×	Set/cleared according to the result
R:	Previously saved value is restored

10.2 List of Operations

Mnemonic	Operand	Bytes	Clocks	Operation	Flags
					Z AC CY
MOV	r, #byte	3	6	$r \leftarrow \text{byte}$	
	saddr, #byte	3	6	$(\text{saddr}) \leftarrow \text{byte}$	
	sfr, #byte	3	6	$\text{sfr} \leftarrow \text{byte}$	
	A, r Note 1	2	4	$A \leftarrow r$	
	r, A Note 1	2	4	$r \leftarrow A$	
	A, saddr	2	4	$A \leftarrow (\text{saddr})$	
	saddr, A	2	4	$(\text{saddr}) \leftarrow A$	
	A, sfr	2	4	$A \leftarrow \text{sfr}$	
	sfr, A	2	4	$\text{sfr} \leftarrow A$	
	A, !addr16	3	8	$A \leftarrow (\text{addr16})$	
	!addr16, A	3	8	$(\text{addr16}) \leftarrow A$	
	PSW, #byte	3	6	$\text{PSW} \leftarrow \text{byte}$	× × ×
	A, PSW	2	4	$A \leftarrow \text{PSW}$	
	PSW, A	2	4	$\text{PSW} \leftarrow A$	× × ×
	A, [DE]	1	6	$A \leftarrow (\text{DE})$	
	[DE], A	1	6	$(\text{DE}) \leftarrow A$	
	A, [HL]	1	6	$A \leftarrow (\text{HL})$	
	[HL], A	1	6	$(\text{HL}) \leftarrow A$	
	A, [HL + byte]	2	6	$A \leftarrow (\text{HL} + \text{byte})$	
	[HL + byte], A	2	6	$(\text{HL} + \text{byte}) \leftarrow A$	
XCH	A, X	1	4	$A \leftrightarrow X$	
	A, r Note 2	2	6	$A \leftrightarrow r$	
	A, saddr	2	6	$A \leftrightarrow (\text{saddr})$	
	A, sfr	2	6	$A \leftrightarrow (\text{sfr})$	
	A, [DE]	1	8	$A \leftrightarrow (\text{DE})$	
	A, [HL]	1	8	$A \leftrightarrow (\text{HL})$	
	A, [HL + byte]	2	8	$A \leftrightarrow (\text{HL} + \text{byte})$	
MOVW	rp, #word	3	6	$\text{rp} \leftarrow \text{word}$	
	AX, saddrp	2	6	$\text{AX} \leftarrow (\text{saddrp})$	
	saddrp, AX	2	8	$(\text{saddrp}) \leftarrow \text{AX}$	
	AX, rp Note 3	1	4	$\text{AX} \leftarrow \text{rp}$	
	rp, AX Note 3	1	4	$\text{rp} \leftarrow \text{AX}$	
XCHW	AX, rp Note 3	1	8	$\text{AX} \leftrightarrow \text{rp}$	

- Notes**
1. Except r = A
 2. Except r = A, X
 3. rp = BC, DE and HL only

Remark One instruction clock cycle is one CPU clock cycle (f_{CPU}) selected via the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clocks	Operation	Flags		
					Z	AC	CY
ADD	A, #byte	2	4	$A, CY \leftarrow A + \text{byte}$	x	x	x
	saddr, #byte	3	6	$(saddr), CY \leftarrow (saddr) + \text{byte}$	x	x	x
	A, r	2	4	$A, CY \leftarrow A + r$	x	x	x
	A, saddr	2	4	$A, CY \leftarrow A + (saddr)$	x	x	x
	A, laddr16	3	8	$A, CY \leftarrow A + (addr16)$	x	x	x
	A, [HL]	1	6	$A, CY \leftarrow A + (HL)$	x	x	x
	A, [HL + byte]	2	6	$A, CY \leftarrow A + (HL + \text{byte})$	x	x	x
ADDC	A, #byte	2	4	$A, CY \leftarrow A + \text{byte} + CY$	x	x	x
	saddr, #byte	3	6	$(saddr), CY \leftarrow (saddr) + \text{byte} + CY$	x	x	x
	A, r	2	4	$A, CY \leftarrow A + r + CY$	x	x	x
	A, saddr	2	4	$A, CY \leftarrow A + (saddr) + CY$	x	x	x
	A, laddr16	3	8	$A, CY \leftarrow A + (addr16) + CY$	x	x	x
	A, [HL]	1	6	$A, CY \leftarrow A + (HL) + CY$	x	x	x
	A, [HL + byte]	2	6	$A, CY \leftarrow A + (HL + \text{byte}) + CY$	x	x	x
SUB	A, #byte	2	4	$A, CY \leftarrow A - \text{byte}$	x	x	x
	saddr, #byte	3	6	$(saddr), CY \leftarrow (saddr) - \text{byte}$	x	x	x
	A, r	2	4	$A, CY \leftarrow A - r$	x	x	x
	A, saddr	2	4	$A, CY \leftarrow A - (saddr)$	x	x	x
	A, laddr16	3	8	$A, CY \leftarrow A - (addr16)$	x	x	x
	A, [HL]	1	6	$A, CY \leftarrow A - (HL)$	x	x	x
	A, [HL + byte]	2	6	$A, CY \leftarrow A - (HL + \text{byte})$	x	x	x
SUBC	A, #byte	2	4	$A, CY \leftarrow A - \text{byte} - CY$	x	x	x
	saddr, #byte	3	6	$(saddr), CY \leftarrow (saddr) - \text{byte} - CY$	x	x	x
	A, r	2	4	$A, CY \leftarrow A - r - CY$	x	x	x
	A, saddr	2	4	$A, CY \leftarrow A - (saddr) - CY$	x	x	x
	A, laddr16	3	8	$A, CY \leftarrow A - (addr16) - CY$	x	x	x
	A, [HL]	1	6	$A, CY \leftarrow A - (HL) - CY$	x	x	x
	A, [HL + byte]	2	6	$A, CY \leftarrow A - (HL + \text{byte}) - CY$	x	x	x
AND	A, #byte	2	4	$A \leftarrow A \wedge \text{byte}$	x		
	saddr, #byte	3	6	$(saddr) \leftarrow (saddr) \wedge \text{byte}$	x		
	A, r	2	4	$A \leftarrow A \wedge r$	x		
	A, saddr	2	4	$A \leftarrow A \wedge (saddr)$	x		
	A, laddr16	3	8	$A \leftarrow A \wedge (addr16)$	x		
	A, [HL]	1	6	$A \leftarrow A \wedge (HL)$	x		
	A, [HL + byte]	2	6	$A \leftarrow A \wedge (HL + \text{byte})$	x		

Remark One instruction clock cycle is one CPU clock cycle (f_{CPU}) selected via the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clocks	Operation	Flags		
					Z	AC	CY
OR	A, #byte	2	4	$A \leftarrow A \vee \text{byte}$	×		
	saddr, #byte	3	6	$(\text{saddr}) \leftarrow (\text{saddr}) \vee \text{byte}$	×		
	A, r	2	4	$A \leftarrow A \vee r$	×		
	A, saddr	2	4	$A \leftarrow A \vee (\text{saddr})$	×		
	A, !addr16	3	8	$A \leftarrow A \vee (\text{addr16})$	×		
	A, [HL]	1	6	$A \leftarrow A \vee (\text{HL})$	×		
	A, [HL + byte]	2	6	$A \leftarrow A \vee (\text{HL} + \text{byte})$	×		
XOR	A, #byte	2	4	$A \leftarrow A \nabla \text{byte}$	×		
	saddr, #byte	3	6	$(\text{saddr}) \leftarrow (\text{saddr}) \nabla \text{byte}$	×		
	A, r	2	4	$A \leftarrow A \nabla r$	×		
	A, saddr	2	4	$A \leftarrow A \nabla (\text{saddr})$	×		
	A, !addr16	3	8	$A \leftarrow A \nabla (\text{addr16})$	×		
	A, [HL]	1	6	$A \leftarrow A \nabla (\text{HL})$	×		
	A, [HL + byte]	2	6	$A \leftarrow A \nabla (\text{HL} + \text{byte})$	×		
CMP	A, #byte	2	4	$A - \text{byte}$	×	×	×
	saddr, #byte	3	6	$(\text{saddr}) - \text{byte}$	×	×	×
	A, r	2	4	$A - r$	×	×	×
	A, saddr	2	4	$A - (\text{saddr})$	×	×	×
	A, !addr16	3	8	$A - (\text{addr16})$	×	×	×
	A, [HL]	1	6	$A - (\text{HL})$	×	×	×
	A, [HL + byte]	2	6	$A - (\text{HL} + \text{byte})$	×	×	×
ADDW	AX, #word	3	6	$\text{AX}, \text{CY} \leftarrow \text{AX} + \text{word}$	×	×	×
SUBW	AX, #word	3	6	$\text{AX}, \text{CY} \leftarrow \text{AX} - \text{word}$	×	×	×
CMPW	AX, #word	3	6	$\text{AX} - \text{word}$	×	×	×
INC	r	2	4	$r \leftarrow r + 1$	×	×	
	saddr	2	4	$(\text{saddr}) \leftarrow (\text{saddr}) + 1$	×	×	
DEC	r	2	4	$r \leftarrow r - 1$	×	×	
	saddr	2	4	$(\text{saddr}) \leftarrow (\text{saddr}) - 1$	×	×	
INCW	rp	1	4	$\text{rp} \leftarrow \text{rp} + 1$			
DECW	rp	1	4	$\text{rp} \leftarrow \text{rp} - 1$			
ROR	A, 1	1	2	$(\text{CY}, \text{A}_7 \leftarrow \text{A}_0, \text{A}_{m-1} \leftarrow \text{A}_m) \times 1 \text{ time}$			×
ROL	A, 1	1	2	$(\text{CY}, \text{A}_0 \leftarrow \text{A}_7, \text{A}_{m+1} \leftarrow \text{A}_m) \times 1 \text{ time}$			×
RORC	A, 1	1	2	$(\text{CY} \leftarrow \text{A}_0, \text{A}_7 \leftarrow \text{CY}, \text{A}_{m-1} \leftarrow \text{A}_m) \times 1 \text{ time}$			×
ROLC	A, 1	1	2	$(\text{CY} \leftarrow \text{A}_7, \text{A}_0 \leftarrow \text{CY}, \text{A}_{m+1} \leftarrow \text{A}_m) \times 1 \text{ time}$			×

Remark One instruction clock cycle is one CPU clock cycle (f_{CPU}) selected via the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clocks	Operation	Flags
					Z AC CY
SET1	saddr. bit	3	6	(saddr. bit) ← 1	
	sfr. bit	3	6	sfr. bit ← 1	
	A. bit	2	4	A. bit ← 1	
	PSW. bit	3	6	PSW. bit ← 1	× × ×
	[HL]. bit	2	10	(HL). bit ← 1	
CLR1	saddr. bit	3	6	(saddr. bit) ← 0	
	sfr. bit	3	6	sfr. bit ← 0	
	A. bit	2	4	A. bit ← 0	
	PSW. bit	3	6	PSW. bit ← 0	× × ×
	[HL]. bit	2	10	(HL). bit ← 0	
SET1	CY	1	2	CY ← 1	1
CLR1	CY	1	2	CY ← 0	0
NOT1	CY	1	2	CY ← $\overline{\text{CY}}$	×
CALL	!addr16	3	6	(SP - 1) ← (PC + 3) _H , (SP - 2) ← (PC + 3) _L , PC ← addr16, SP ← SP - 2	
CALLT	[addr5]	1	8	(SP - 1) ← (PC + 1) _H , (SP - 2) ← (PC + 1) _L , PC _H ← (00000000, addr5 + 1), PC _L ← (00000000, addr5), SP ← SP - 2	
RET		1	6	PC _H ← (SP + 1), PC _L ← (SP), SP ← SP + 2	
RETI		1	8	PC _H ← (SP + 1), PC _L ← (SP), PSW ← (SP + 2), SP ← SP + 3, NMIS ← 0	R R R
PUSH	PSW	1	2	(SP - 1) ← PSW, SP ← SP - 1	
	rp	1	4	(SP - 1) ← rp _H , (SP - 2) ← rp _L , SP ← SP - 2	
POP	PSW	1	4	PSW ← (SP), SP ← SP + 1	R R R
	rp	1	6	rp _H ← (SP + 1), rp _L ← (SP), SP ← SP + 2	
MOVW	SP, AX	2	8	SP ← AX	
	AX, SP	2	6	AX ← SP	
BR	!addr16	3	6	PC ← addr16	
	\$addr16	2	6	PC ← PC + 2 + jdisp8	
	AX	1	6	PC _H ← A, PC _L ← X	

Remark One instruction clock cycle is one CPU clock cycle (f_{CPU}) selected via the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clocks	Operation	Flags
					Z AC CY
BC	\$addr16	2	6	$PC \leftarrow PC + 2 + jdisp8$ if CY = 1	
BNC	\$addr16	2	6	$PC \leftarrow PC + 2 + jdisp8$ if CY = 0	
BZ	\$addr16	2	6	$PC \leftarrow PC + 2 + jdisp8$ if Z = 1	
BNZ	\$addr16	2	6	$PC \leftarrow PC + 2 + jdisp8$ if Z = 0	
BT	saddr. bit, \$addr16	4	10	$PC \leftarrow PC + 4 + jdisp8$ if (saddr. bit) = 1	
	sfr. bit, \$addr16	4	10	$PC \leftarrow PC + 4 + jdisp8$ if sfr. bit = 1	
	A. bit, \$addr16	3	8	$PC \leftarrow PC + 3 + jdisp8$ if A. bit = 1	
	PSW. bit, \$addr16	4	10	$PC \leftarrow PC + 4 + jdisp8$ if PSW. bit = 1	
BF	saddr. bit, \$addr16	4	10	$PC \leftarrow PC + 4 + jdisp8$ if (saddr. bit) = 0	
	sfr. bit, \$addr16	4	10	$PC \leftarrow PC + 4 + jdisp8$ if sfr. bit = 0	
	A. bit, \$addr16	3	8	$PC \leftarrow PC + 3 + jdisp8$ if A. bit = 0	
	PSW. bit, \$addr16	4	10	$PC \leftarrow PC + 4 + jdisp8$ if PSW. bit = 0	
DBNZ	B, \$addr16	2	6	$B \leftarrow B - 1$, then $PC \leftarrow PC + 2 + jdisp8$ if $B \neq 0$	
	C, \$addr16	2	6	$C \leftarrow C - 1$, then $PC \leftarrow PC + 2 + jdisp8$ if $C \neq 0$	
	saddr, \$addr16	3	8	$(saddr) \leftarrow (saddr) - 1$, then $PC \leftarrow PC + 3 + jdisp8$ if $(saddr) \neq 0$	
NOP		1	2	No Operation	
EI		3	6	$IE \leftarrow 1$ (Enable Interrupt)	
DI		3	6	$IE \leftarrow 0$ (Disable Interrupt)	
HALT		1	2	Set HALT Mode	
STOP		1	2	Set STOP Mode	

Remark One instruction clock cycle is one CPU clock cycle (f_{CPU}) selected via the processor clock control register (PCC).

11. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Power supply voltage	V _{DD}			−0.3 to +6.5	V
Input voltage	V _{I1}	P00 to P03, P10 to P13, P20 to P26, P30 to P33, X1 (CL1), X2 (CL2), XT1, XT2, RESET		−0.3 to V _{DD} + 0.3 ^{Note}	V
	V _{I2}	P50 to P53	N-ch open drain	−0.3 to +13	V
			On-chip pull-up resistor	−0.3 to V _{DD} + 0.3 ^{Note}	V
Output voltage	V _O			−0.3 to V _{DD} + 0.3 ^{Note}	V
Output current, high	I _{OH}	Per pin		−10	mA
		Total for all pins		−30	mA
Output current, low	I _{OL}	Per pin		30	mA
		Total for all pins		160	mA
Operating ambient temperature	T _A			−40 to +85	°C
Storage temperature	T _{stg}			−65 to +150	°C

Note 6.5 V or less

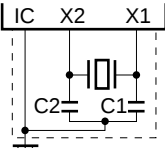
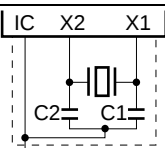
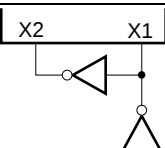
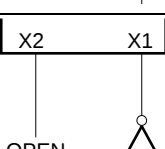
Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Pin names enclosed in parentheses are when using the μPD789304, 789306.
 2. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Main System Clock Oscillator Characteristics

Ceramic/crystal oscillation (μPD789304, 789306)

(T_A = −40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f _x) ^{Note 1}		1.0		5.0	MHz
		Oscillation stabilization time ^{Note 2}	After V _{DD} reaches oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillation frequency ^{Note 1}		1.0		5.0	MHz
		Oscillation stabilization time ^{Note 2}	V _{DD} = 4.5 to 5.5 V			10	ms
						30	ms
★ External clock		X1 input frequency (f _x) ^{Note 1}		1.0		5.0	MHz
		X1 input high-/low-level width (t _{xH} , t _{xL})		85		500	ns
		X1 input frequency (f _x) ^{Note 1}	V _{DD} = 2.7 to 5.5 V	1.0		5.0	MHz
		X1 input high-/low-level width (t _{xH} , t _{xL})	V _{DD} = 2.7 to 5.5 V	85		500	ns

Notes 1. Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

★ **2.** Time required to stabilize oscillation after reset or STOP mode release. Use a resonator whose oscillation stabilizes within the oscillation stabilization wait time.

Cautions 1. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
- Do not cross the wiring with the other signal lines.
- Do not route the wiring near a signal line through which a high fluctuating current flows.
- Always make the ground point of the oscillator capacitor the same potential as V_{ss}.
- Do not ground the capacitor to a ground pattern through which a high current flows.
- Do not fetch signals from the oscillator.

2. When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

RC oscillation (μPD789314, 789316)

(T_A = -40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
★		Oscillation frequency (f _{CC}) ^{Note 1}		2.0		4.0	MHz
		Oscillation stabilization time ^{Note 2}	V _{DD} = 2.7 to 5.5 V	32			μs
				128			μs
★		CL1 input frequency (f _{CC}) ^{Note 1}		1.0		4.0	MHz
		CL1 input high-/low-level width (t _{xH} , t _{xL})		100		500	ns
		CL1 input frequency (f _{CC}) ^{Note 1}	V _{DD} = 2.7 to 5.5 V	1.0		4.0	MHz
		CL1 input high-/low-level width (t _{xH} , t _{xL})	V _{DD} = 2.7 to 5.5 V	100		500	ns

Notes 1. Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

★ **2.** Time required to stabilize oscillation after reset or STOP mode release.

Cautions 1. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figure to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
- Do not cross the wiring with the other signal lines.
- Do not route the wiring near a signal line through which a high fluctuating current flows.
- Always make the ground point of the oscillator capacitor the same potential as V_{SS}.
- Do not ground the capacitor to a ground pattern through which a high current flows.
- Do not fetch signals from the oscillator.

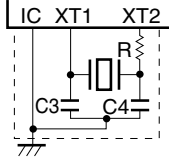
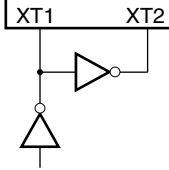
- 2.** When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

★ RC Oscillation Frequency Characteristics ($T_A = -40$ to $+85^\circ\text{C}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Oscillation frequency	f _{CC1}	R = 11.0 kΩ, C = 22 pF Target: 2 MHz	V _{DD} = 2.7 to 5.5 V	1.5	2.0	2.5	MHz
	f _{CC2}		V _{DD} = 1.8 to 3.6 V	0.5	2.0	2.5	MHz
	f _{CC3}		V _{DD} = 1.8 to 5.5 V	0.5	2.0	2.5	MHz
	f _{CC4}	R = 6.8 kΩ, C = 22 pF Target: 3 MHz	V _{DD} = 2.7 to 5.5 V	2.5	3.0	3.5	MHz
	f _{CC5}		V _{DD} = 1.8 to 3.6 V	0.75	3.0	3.5	MHz
	f _{CC6}		V _{DD} = 1.8 to 5.5 V	0.75	3.0	3.5	MHz
	f _{CC7}	R = 4.7 kΩ, C = 22 pF Target: 4 MHz	V _{DD} = 2.7 to 5.5 V	3.5	4.0	4.7	MHz
	f _{CC8}		V _{DD} = 1.8 to 3.6 V	1.0	4.0	4.7	MHz
	f _{CC9}		V _{DD} = 1.8 to 5.5 V	1.0	4.0	4.7	MHz

- Remarks**
1. Set the RC to one of the above nine values so that the typical value of the oscillation frequency is within 2.0 to 4.0 MHz.
 2. The resistor (R) and capacitor (C) error is not included.

Subsystem Clock Oscillator Characteristics ($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = 1.8$ to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT}) ^{Note 1}		32	32.768	35	kHz
		Oscillation stabilization time ^{Note 2}	$V_{DD} = 4.5$ to 5.5 V		1.2	2	s
External clock		XT1 input frequency (f_{XT}) ^{Note 1}		32		35	kHz
		XT1 input high-/low-level width (t_{XTH} , t_{XTL})		14.3		15.6	μs

- Notes**
1. Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.
 2. Time required to stabilize oscillation after V_{DD} reaches oscillation voltage range MIN.

Cautions

1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figure to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
- Do not cross the wiring with the other signal lines.
- Do not route the wiring near a signal line through which a high fluctuating current flows.
- Always make the ground point of the oscillator capacitor the same potential as V_{SS} .
- Do not ground the capacitor to a ground pattern through which a high current flows.
- Do not fetch signals from the oscillator.

2. The subsystem clock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

DC Characteristics (T_A = −40 to +85°C, V_{DD} = 1.8 to 5.5 V) (1/4)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low	I _{OL}	Per pin				10	mA
		All pins				80	mA
Output current, high	I _{OH}	Per pin				−1	mA
		All pins				−15	mA
Input voltage, high	V _{IH1}	P10 to P13	V _{DD} = 2.7 to 5.5 V	0.7V _{DD}		V _{DD}	V
				0.9V _{DD}		V _{DD}	V
	V _{IH2}	P50 to P53	N-ch open drain	V _{DD} = 2.7 to 5.5 V	0.7V _{DD}	12	V
					0.9V _{DD}	12	V
			On-chip pull-up resistor	V _{DD} = 2.7 to 5.5 V	0.7V _{DD}	V _{DD}	V
					0.9V _{DD}	V _{DD}	V
	V _{IH3}	RESET, P00 to P03, P20 to P26, P30 to P33	V _{DD} = 2.7 to 5.5 V	0.8V _{DD}		V _{DD}	V
				0.9V _{DD}		V _{DD}	V
	V _{IH4}	X1 (CL1), X2 (CL2), XT1, XT2	V _{DD} = 4.5 to 5.5 V	V _{DD} − 0.5		V _{DD}	V
				V _{DD} − 0.1		V _{DD}	V
Input voltage, low	V _{IL1}	P10 to P13	V _{DD} = 2.7 to 5.5 V	0		0.3V _{DD}	V
				0		0.1V _{DD}	V
	V _{IL2}	P50 to P53	V _{DD} = 2.7 to 5.5 V	0		0.3V _{DD}	V
				0		0.1V _{DD}	V
	V _{IL3}	RESET, P00 to P03, P20 to P26, P30 to P33	V _{DD} = 2.7 to 5.5 V	0		0.2V _{DD}	V
				0		0.1V _{DD}	V
	V _{IL4}	X1 (CL1), X2 (CL2), XT1, XT2	V _{DD} = 4.5 to 5.5 V	0		0.4	V
				0		0.1	V
Output voltage, high	V _{OH}	V _{DD} = 4.5 to 5.5 V, I _{OH} = −1 mA		V _{DD} − 1.0			V
		V _{DD} = 1.8 to 5.5 V, I _{OH} = −100 μA		V _{DD} − 0.5			V
Output voltage, low	V _{OL1}	P00 to P03, P10 to P13, P20 to P26, P30 to P33	4.5 ≤ V _{DD} ≤ 5.5 V, I _{OL} = 10 mA			1.0	V
			1.8 ≤ V _{DD} < 4.5 V, I _{OL} = 400 μA			0.5	V
	V _{OL2}	P50 to P53	4.5 ≤ V _{DD} < 5.5 V, I _{OL} = 10 mA			1.0	V
			1.8 ≤ V _{DD} < 4.5 V, I _{OL} = 1.6 mA			0.4	V

Remarks 1. Pin names enclosed in parentheses are when using the μPD789314, 789316.

2. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = −40 to +85°C, V_{DD} = 1.8 to 5.5 V) (2/4)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I _{LIH1}	V _{IN} = V _{DD}	P00 to P03, P10 to P13, P20 to P26, P30 to P33, RESET			3	μA
	I _{LIH2}		X1 (CL1), X2 (CL2), XT1, XT2			20	μA
	I _{LIH3}	V _{IN} = 12 V	P50 to P53 (N-ch open drain)			20	μA
Input leakage current, low	I _{LIL1}	V _{IN} = 0 V	P00 to P03, P10 to P13, P20 to P26, P30 to P33, RESET			−3	μA
	I _{LIL2}		X1 (CL1), X2 (CL2), XT1, XT2			−20	μA
	I _{LIL3}		P50 to P53 (N-ch open drain)			−3 ^{Note}	μA
Output leakage current, high	I _{LOH}	V _{OUT} = V _{DD}				3	μA
Output leakage current, low	I _{LOL}	V _{OUT} = 0 V				−3	μA
Software pull-up resistor	R ₁	V _{IN} = 0 V	P00 to P03, P10 to P13, P20 to P26, P30 to P33	50	100	200	kΩ
Mask option pull-up resistor	R ₂	V _{IN} = 0 V	P50 to P53	10	30	60	kΩ

Note If there is no on-chip pull-up resistor for P50 to P53 (specified by the mask option), if P50 to P53 have been set to input mode when a read instruction is executed to read from P50 to P53, a low-level input leakage current of up to −30 μA flows during only one cycle. At all other times, the maximum leakage current is −3 μA.

- Remarks**
1. Pin names enclosed in parentheses are when using the μPD789314, 789316.
 2. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

★ DC Characteristics (T_A = −40 to +85°C, V_{DD} = 1.8 to 5.5 V) (3/4)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
Power supply current ^{Note 1} (Ceramic/crystal oscillation)	I _{DD1}	5.0 MHz crystal oscillation operation mode (C1 = C2 = 22 pF)	V _{DD} = 5.0 V ±10% ^{Note 2}		1.8	2.9	mA	
			V _{DD} = 3.0 V ±10% ^{Note 3}		0.36	0.9	mA	
			V _{DD} = 2.0 V ±10% ^{Note 3}		0.16	0.45	mA	
	I _{DD2}	5.0 MHz crystal oscillation HALT mode (C1 = C2 = 22 pF)	V _{DD} = 5.0 V ±10% ^{Note 2}		0.96	1.92	mA	
			V _{DD} = 3.0 V ±10% ^{Note 3}		0.26	0.76	mA	
			V _{DD} = 2.0 V ±10% ^{Note 3}		0.1	0.34	mA	
	I _{DD3}	32.768 kHz crystal oscillation operation mode ^{Note 4} (C3 = C4 = 22 pF, R1 = 220 kΩ)	V _{DD} = 5.0 V ±10%		30	58	μA	
			V _{DD} = 3.0 V ±10%		9	26	μA	
			V _{DD} = 2.0 V ±10%		4	12	μA	
	I _{DD4}	32.768 kHz crystal oscillation HALT mode ^{Note 4} (C3 = C4 = 22 pF, R1 = 220 kΩ)	LCD not operating	V _{DD} = 5.0 V ±10%		25	48	μA
				V _{DD} = 3.0 V ±10%		7	20	μA
				V _{DD} = 2.0 V ±10%		4	10	μA
			LCD operating ^{Note 5}	V _{DD} = 5.0 V ±10%		28	57	μA
				V _{DD} = 3.0 V ±10%		9.6	27.8	μA
				V _{DD} = 2.0 V ±10%		6	16	μA
I _{DD5}	STOP mode ^{Note 6}	V _{DD} = 5.0 V ±10%		0.1	10	μA		
		V _{DD} = 3.0 V ±10%		0.05	5.0	μA		
		V _{DD} = 2.0 V ±10%		0.05	3.0	μA		

- Notes**
1. The port current (including the current that flows to the on-chip pull-up resistor) is not included.
 2. High-speed mode operation (when processor clock control register (PCC) is set to 00H)
 3. Low-speed mode operation (when PCC is set to 02H)
 4. When the main system clock is stopped
 5. This is the total current that flows when the LCD controller/driver is operating (LCDON0 = 1, VAON0 = 1, LIPS0 = 1). The power supply current when the LCD is not operating (LCDON0 = 0, VAON0 = 1, LIPS0 = 0) is included in I_{DD2}.
 6. This is the current when the LCD voltage booster circuit is stopped (LCDON0 = 0, VAON0 = 1).

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

★ DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (4/4)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
Power supply current ^{Note 1} (RC oscillation)	I _{DD1}	4.0 MHz RC oscillation operation mode (R = 4.7 kΩ, C = 22 pF)	V _{DD} = 5.0 V ±10% ^{Note 2}		1.65	3.0	mA	
			V _{DD} = 3.0 V ±10% ^{Note 3}		0.65	1.44	mA	
			V _{DD} = 2.0 V ±10% ^{Note 3}		0.38	1.05	mA	
	I _{DD2}	4.0 MHz RC oscillation HALT mode (R = 4.7 kΩ, C = 22 pF)	V _{DD} = 5.0 V ±10% ^{Note 2}		1.1	2.29	mA	
			V _{DD} = 3.0 V ±10% ^{Note 3}		0.6	1.28	mA	
			V _{DD} = 2.0 V ±10% ^{Note 3}		0.35	0.82	mA	
	I _{DD3}	32.768 kHz crystal oscillation operation mode ^{Note 4} (C3 = C4 = 22 pF, R1 = 220 kΩ)	V _{DD} = 5.0 V ±10%		30	58	μA	
			V _{DD} = 3.0 V ±10%		9	26	μA	
			V _{DD} = 2.0 V ±10%		4	12	μA	
	I _{DD4}	32.768 kHz crystal oscillation HALT mode ^{Note 4} (C3 = C4 = 22 pF, R1 = 220 kΩ)	LCD not operating	V _{DD} = 5.0 V ±10%		25	48	μA
				V _{DD} = 3.0 V ±10%		7	20	μA
				V _{DD} = 2.0 V ±10%		4	10	μA
			LCD operating ^{Note 5}	V _{DD} = 5.0 V ±10%		28	57	μA
				V _{DD} = 3.0 V ±10%		9.6	27.8	μA
				V _{DD} = 2.0 V ±10%		6	16	μA
I _{DD5}	STOP mode ^{Note 6}	V _{DD} = 5.0 V ±10%		0.1	10	μA		
		V _{DD} = 3.0 V ±10%		0.05	5.0	μA		
		V _{DD} = 2.0 V ±10%		0.05	3.0	μA		

Notes 1. The port current (including the current that flows to the on-chip pull-up resistor) is not included.

2. High-speed mode operation (when processor clock control register (PCC) is set to 00H)

3. Low-speed mode operation (when PCC is set to 02H)

4. When the main system clock is stopped

5. This is the total current that flows when the LCD controller/driver is operating (LCDON0 = 1, VAON0 = 1, LIPS0 = 1). The power supply current when the LCD is not operating (LCDON0 = 0, VAON0 = 1, LIPS0 = 0) is included in I_{DD2}.

6. This is the current when the LCD voltage booster circuit is stopped (LCDON0 = 0, VAON0 = 1).

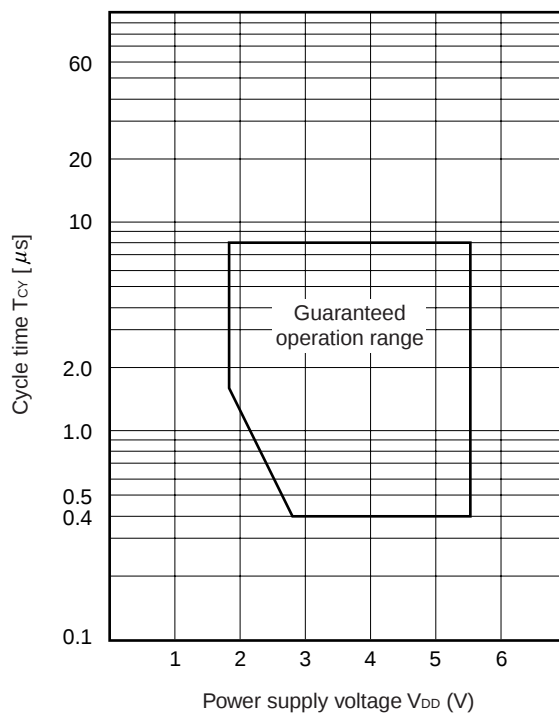
Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

AC Characteristics

(1) Basic operation ($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = 1.8$ to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY1}	Operating with main system clock	$V_{DD} = 2.7$ to 5.5 V	0.4		μs
				1.6	8.0	μs
		Operating with subsystem clock	114	122	125	μs
TMI40 input frequency	f_{TMI}	$V_{DD} = 2.7$ to 5.5 V	0		4	MHz
			0		275	kHz
★ TMI40 input high-/low-level width	t_{TIMH}	$V_{DD} = 2.7$ to 5.5 V	0.1			μs
	t_{TIML}		1.8			μs
Interrupt input high-/low-level width	t_{INTH} , t_{INTL}	INTP0 to INTP3	10			μs
Key return input low-level width	t_{KRL}	KR00 to KR03	10			μs
RESET low-level width	t_{RSL}		10			μs

T_{CY} vs. V_{DD} (main system clock)



(2) Serial interface 10, 20 (SIO10, SIO20) ($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = 1.8$ to 5.5 V)

(a) 3-wire serial I/O mode (internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCKn0 cycle time	t_{KCY1}	$V_{DD} = 2.7$ to 5.5 V	800			ns
			3200			ns
SCKn0 high-/low-level width	$t_{KH1},$ t_{KL1}	$V_{DD} = 2.7$ to 5.5 V	$t_{KCY1}/2-50$			ns
			$t_{KCY1}/2-150$			ns
SIn0 setup time (to SCKn0↑)	t_{SIK1}	$V_{DD} = 2.7$ to 5.5 V	150			ns
			500			ns
SIn0 hold time (from SCKn0↑)	t_{SI1}	$V_{DD} = 2.7$ to 5.5 V	400			ns
			600			ns
Delay time from SCKn0↓ to SOn0 output	t_{SO1}	$R = 1\text{ k}\Omega$, $C = 100\text{ pF}$ ^{Note} $V_{DD} = 2.7$ to 5.5 V	0		250	ns
			0		1000	ns

Note R and C are the load resistance and load capacitance of the SOn0 output lines.

Remark n = 1, 2

(b) 3-wire serial I/O mode (external clock input)

	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
★	SCKn0 cycle time	t_{KCY2}	$V_{DD} = 2.7$ to 5.5 V	800			ns
★				3200			ns
	SCKn0 high-/low-level width	$t_{KH2},$ t_{KL2}	$V_{DD} = 2.7$ to 5.5 V	400			ns
				1600			ns
	SIn0 setup time (to SCKn0↑)	t_{SIK2}	$V_{DD} = 2.7$ to 5.5 V	100			ns
				150			ns
	SIn0 hold time (from SCKn0↑)	t_{SI2}	$V_{DD} = 2.7$ to 5.5 V	400			ns
				600			ns
	Delay time from SCKn0↓ to SOn0 output	t_{SO2}	$R = 1\text{ k}\Omega$, $C = 100\text{ pF}$ ^{Note} $V_{DD} = 2.7$ to 5.5 V	0		300	ns
				0		1000	ns

Note R and C are the load resistance and load capacitance of the SOn0 output lines.

Remark n = 1, 2

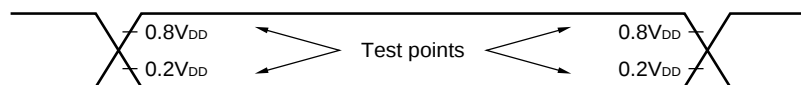
(c) UART mode (SIO20 only) (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		$V_{DD} = 2.7 \text{ to } 5.5 \text{ V}$			78125	bps
					19531	bps

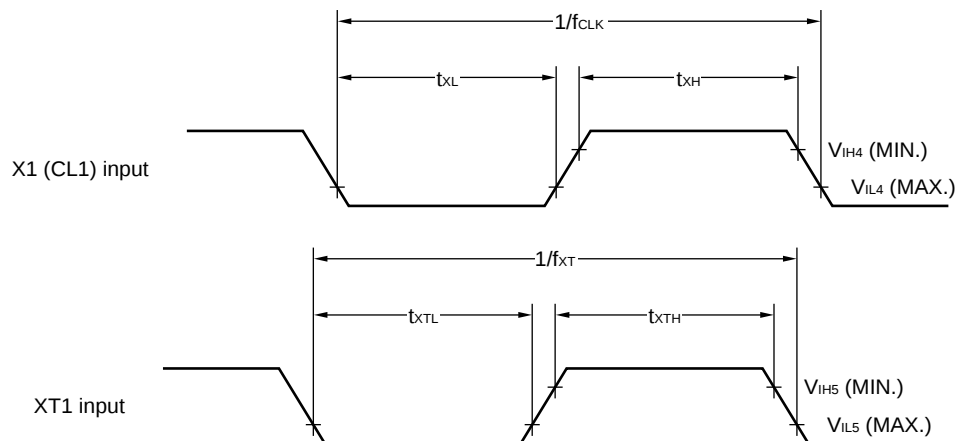
(d) UART mode (SIO20 only) (external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
★ ASCK20 cycle time	t_{KCY3}	$V_{DD} = 2.7 \text{ to } 5.5 \text{ V}$	800			ns
			3200			ns
★ ASCK20 high-/low-level width	t_{KH3}, t_{KL3}	$V_{DD} = 2.7 \text{ to } 5.5 \text{ V}$	400			ns
			1600			ns
Transfer rate		$V_{DD} = 2.7 \text{ to } 5.5 \text{ V}$			39063	bps
					9766	bps
ASCK20 rise/fall time	t_R, t_F				1	μs

AC Timing Test Points (excluding X1 (CL1) and XT1 inputs)

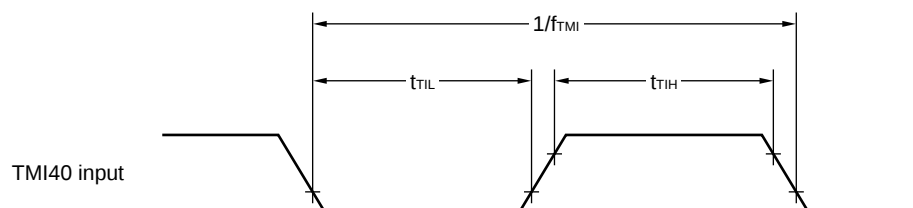


Clock Timing

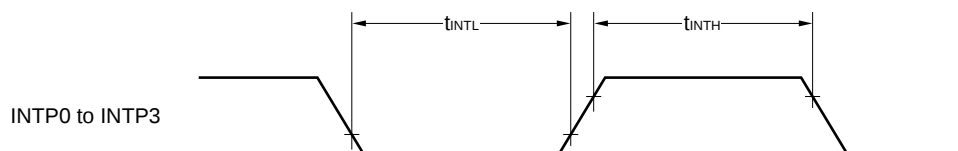


Remark f_{CLK}: f_x or f_{cc}

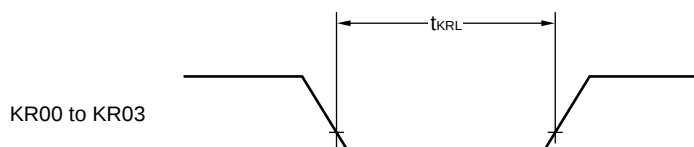
TMI Timing



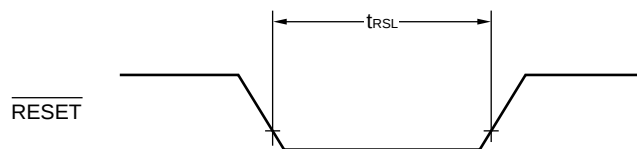
Interrupt Input Timing



Key Return Input Timing

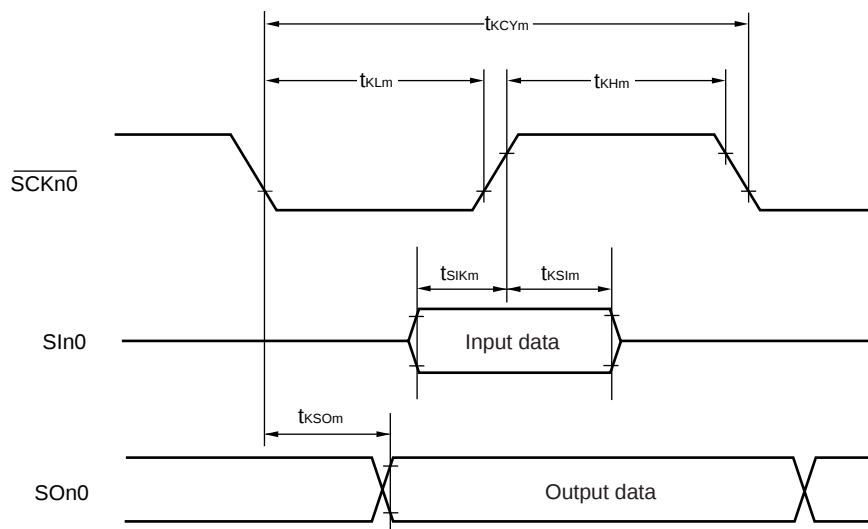


RESET Input Timing



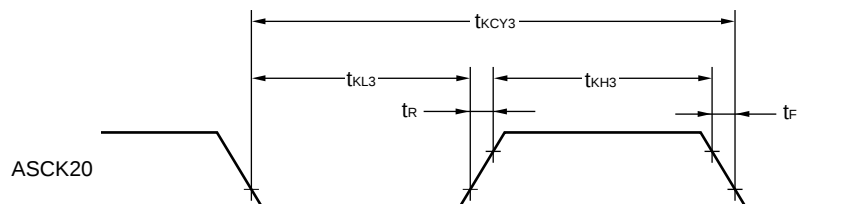
Serial Transfer Timing

3-wire serial I/O mode:



Remark $n, m = 1, 2$

UART mode (external clock input):



★ LCD Characteristics ($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = 1.8$ to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD output voltage variation range	V_{LCD2}	c1 to c4 = $0.47\ \mu\text{F}$ GAIN = 1	0.84	1.0	1.165	V
		GAIN = 0	1.26	1.5	1.74	V
Doubler output	V_{LCD1}	c1 to c4 = $0.47\ \mu\text{F}$	$2V_{LCD2} - 0.1$	$2.0V_{LCD2}$	$2.0V_{LCD2}$	V
Tripler output	V_{LCD0}	c1 to c4 = $0.47\ \mu\text{F}$	$3V_{LCD2} - 0.15$	$3.0V_{LCD2}$	$3.0V_{LCD2}$	V
Voltage boost wait time ^{Note 1}	t_{VWAIT}	GAIN = 0	0.5			s
		GAIN = 1	$5.0 \leq V_{DD} \leq 5.5\ \text{V}$	2.0		s
			$4.5 \leq V_{DD} < 5.0\ \text{V}$	1.0		s
			$1.8 \leq V_{DD} < 4.5\ \text{V}$	0.5		s
LCD output voltage differential ^{Note 2} (common)	V_{ODC}	$I_O = \pm 5\ \mu\text{A}$	0		± 0.2	V
LCD output voltage differential ^{Note 2} (segment)	V_{ODS}	$I_O = \pm 1\ \mu\text{A}$	0		± 0.2	V

Notes 1. This is the wait time from when voltage boosting is started ($VAON0 = 1$) until display is enabled ($LCDON0 = 0$).

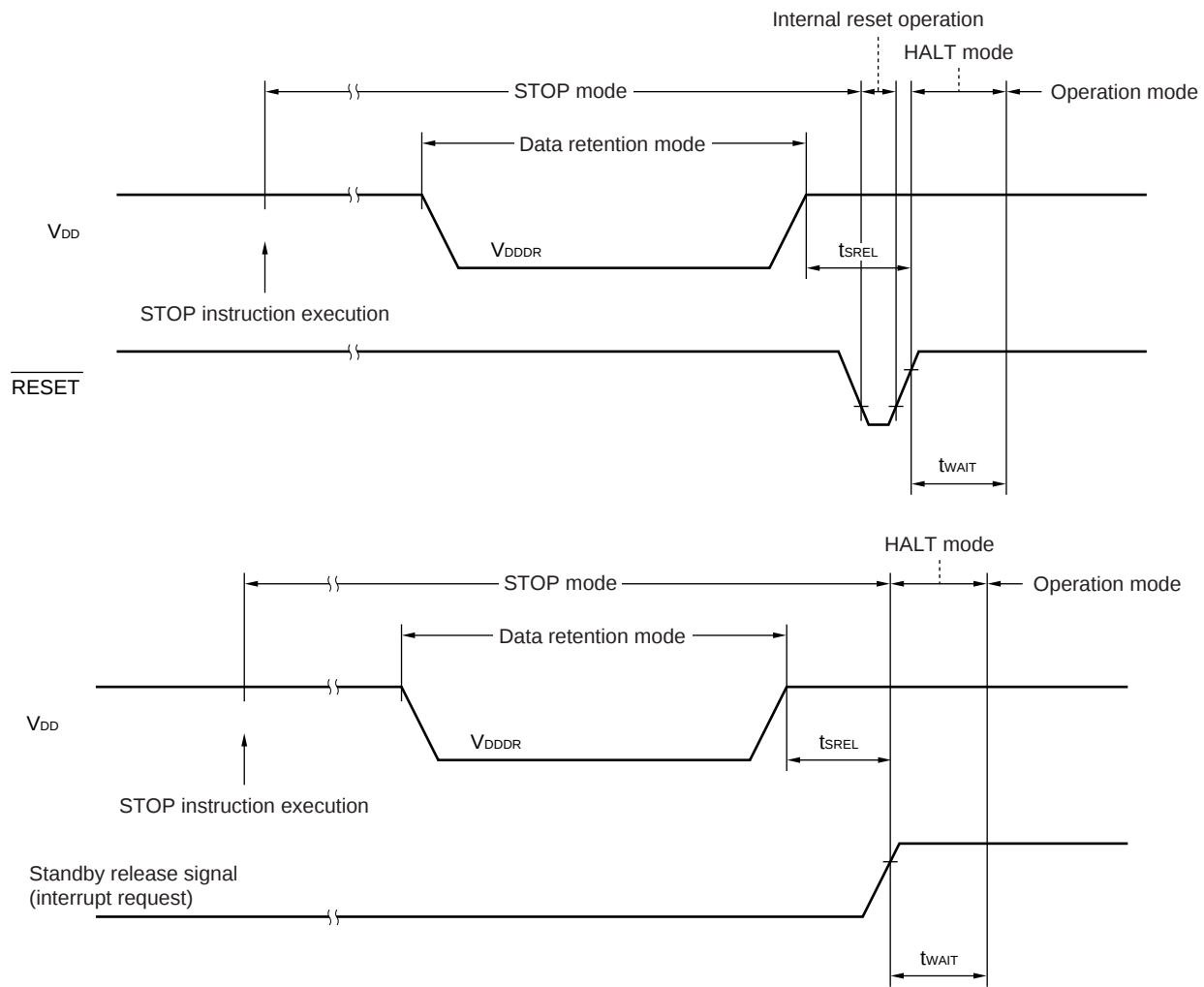
2. The voltage differential is the difference between the segment and common signal output's actual and ideal output voltages.

Remark c1: Capacitor connected between CAPH and CAPL
c2: Capacitor connected between V_{LC0} and ground
c3: Capacitor connected between V_{LC1} and ground
c4: Capacitor connected between V_{LC2} and ground

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics ($T_A = -40$ to $+85^\circ\text{C}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		1.8		5.5	V
Release signal set time	t_{SREL}		0			μs

Data Retention Timing



Oscillation Stabilization Wait Time ($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = 1.8$ to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Oscillation stabilization wait time ^{Note 1} (ceramic/crystal oscillation)	t_{WAIT}	Release by $\overline{\text{RESET}}$		$2^{15}/f_x$		s
		Release by interrupt		Note 2		s
Oscillation stabilization wait time (RC oscillation)	t_{WAIT}	Release by $\overline{\text{RESET}}$		$2^7/f_{cc}$		s
		Release by interrupt		$2^7/f_{cc}$		s

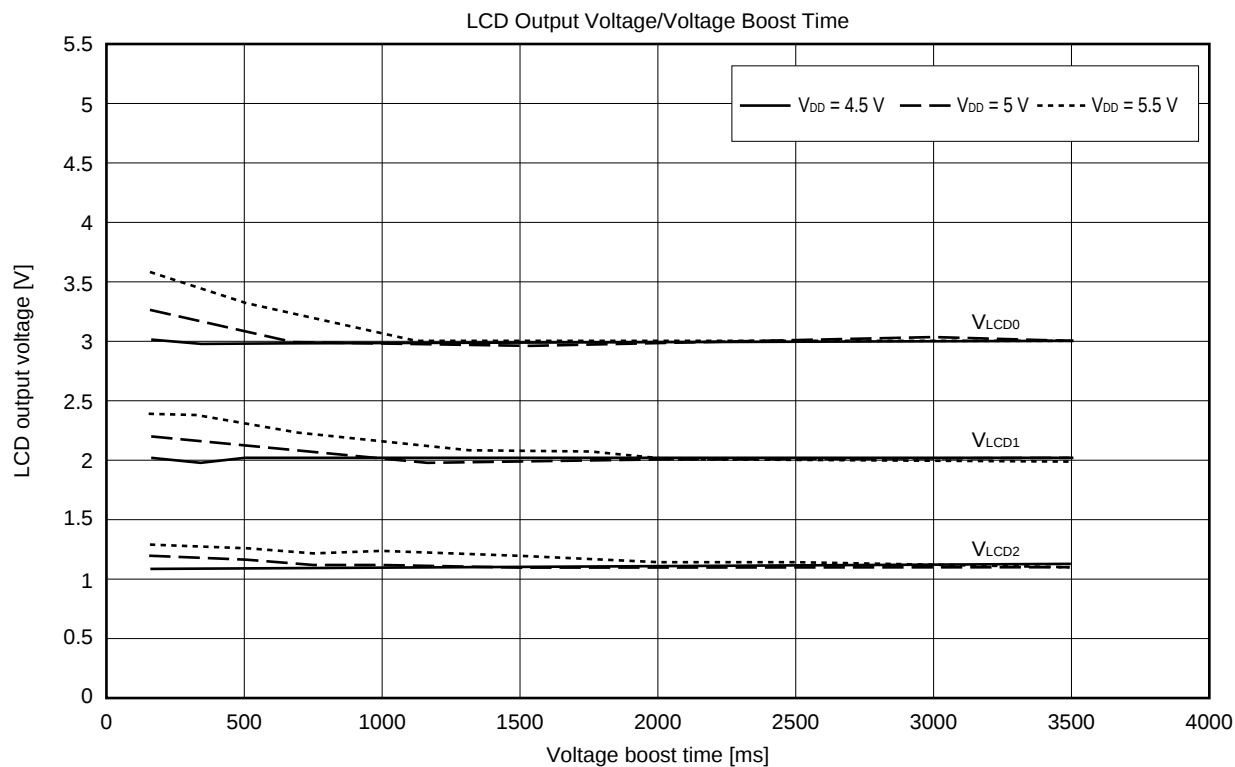
- Notes**
1. Use a resonator whose oscillation stabilizes within the oscillation stabilization wait time.
 2. Selection of $2^{12}/f_x$, $2^{15}/f_x$, or $2^{17}/f_x$ is possible with bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS).

- Remarks**
1. f_x : Main system clock oscillation frequency (ceramic/crystal oscillation)
 2. f_{cc} : Main system clock oscillation frequency (RC oscillation)

★ 12. CHARACTERISTICS CURVES OF LCD CONTROLLER/DRIVER (REFERENCE VALUES)

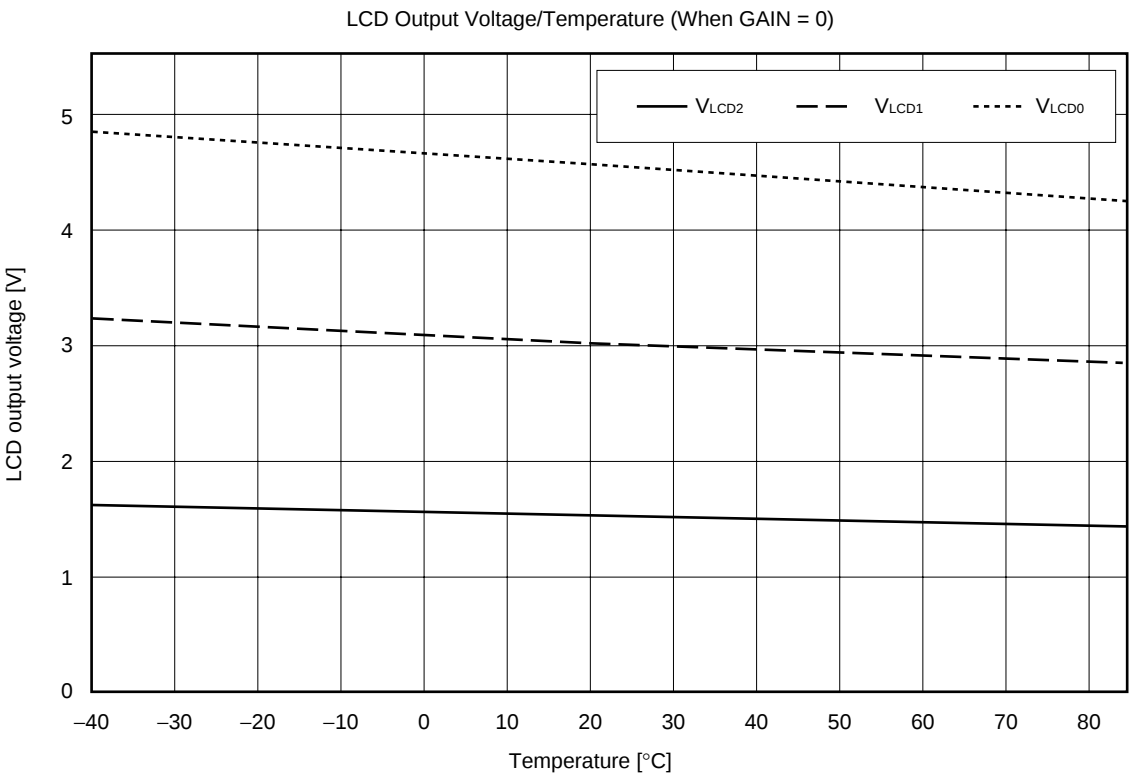
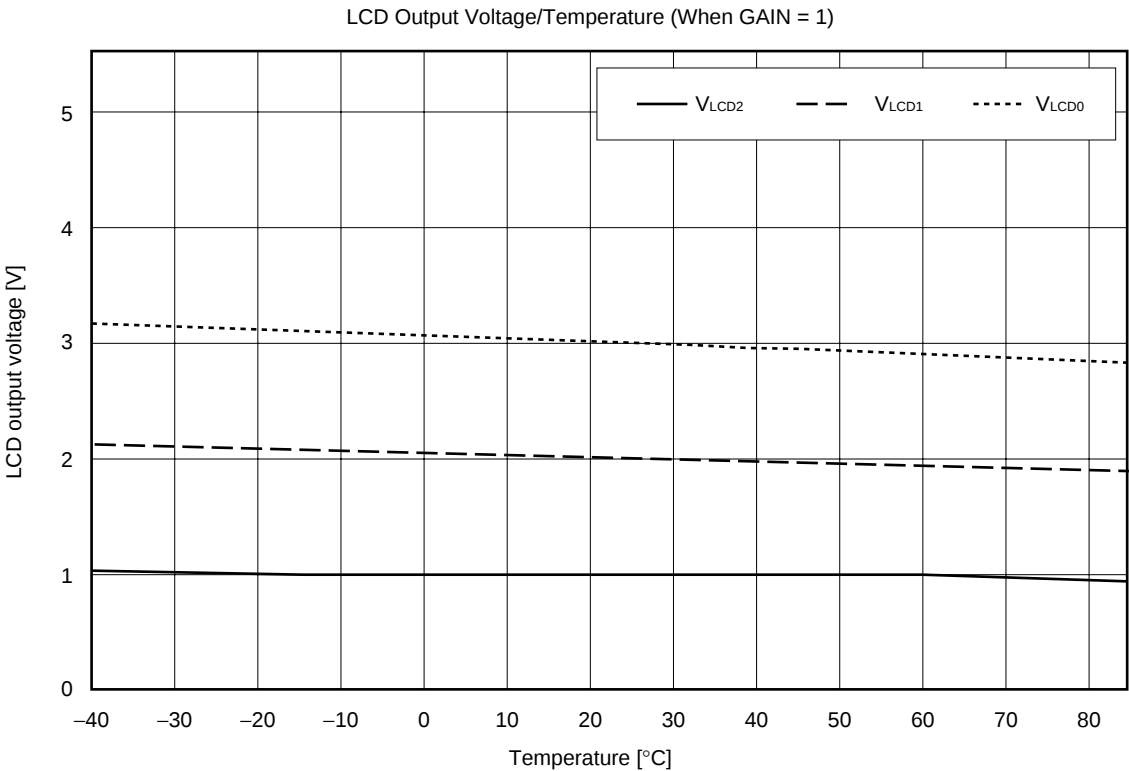
(1) Characteristics curves of voltage boost stabilization time

The following shows the characteristics curves of the time from the start of voltage boost (VAON0 = 1) and the changes in the LCD output voltage (when GAIN is set to 1 (using the 3 V display panel))



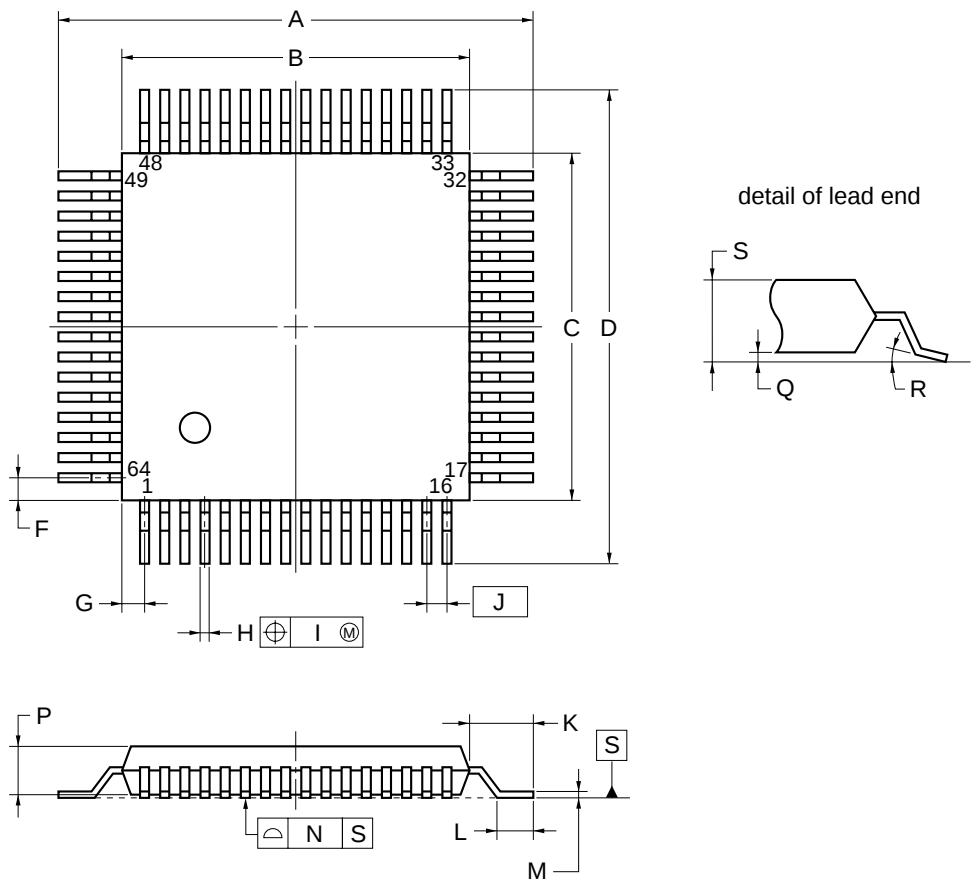
(2) Temperature characteristics of LCD output voltage

The following shows the temperature characteristics curves of LCD output voltage.



13. PACKAGE DRAWINGS

64-PIN PLASTIC QFP (14x14)

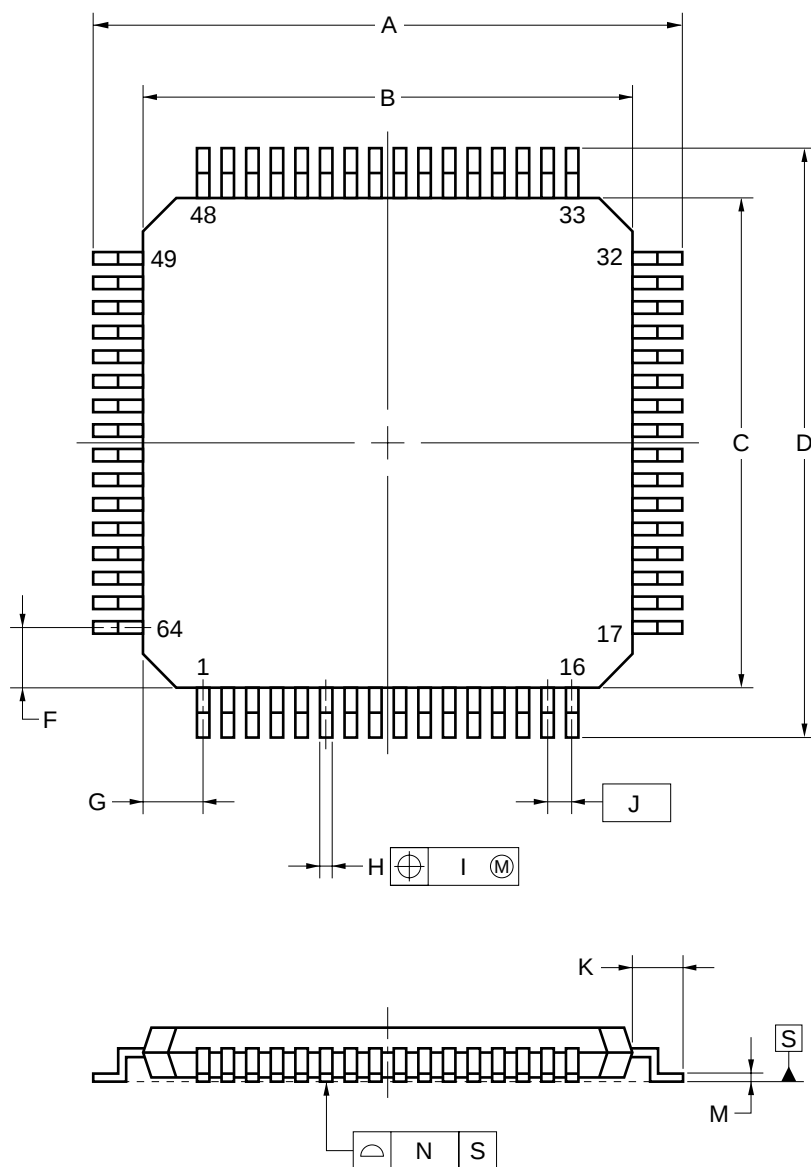


NOTE
Each lead centerline is located within 0.15 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	17.6±0.4
B	14.0±0.2
C	14.0±0.2
D	17.6±0.4
F	1.0
G	1.0
H	0.37 ^{+0.08} _{-0.07}
I	0.15
J	0.8 (T.P.)
K	1.8±0.2
L	0.8±0.2
M	0.17 ^{+0.08} _{-0.07}
N	0.10
P	2.55±0.1
Q	0.1±0.1
R	5°±5°
S	2.85 MAX.

P64GC-80-AB8-5

64-PIN PLASTIC TQFP (12x12)



detail of lead end

ITEM	MILLIMETERS
A	14.0±0.2
B	12.0±0.2
C	12.0±0.2
D	14.0±0.2
F	1.125
G	1.125
H	0.32 ^{+0.06} _{-0.10}
I	0.13
J	0.65 (T.P.)
K	1.0±0.2
L	0.5
M	0.17 ^{+0.03} _{-0.07}
N	0.10
P	1.0
Q	0.1±0.05
R	3° ^{+4°} _{-3°}
S	1.1±0.1
T	0.25
U	0.6±0.15

P64GK-65-9ET-2

NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

★ 14. RECOMMENDED SOLDERING CONDITIONS

The μPD789304, 789306, 789314, and μPD789316 should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

Table 14-1. Surface Mounting Type Soldering Conditions

μPD789304GC-xxx-AB8: 64-pin plastic QFP (14 × 14)

μPD789306GC-xxx-AB8: 64-pin plastic QFP (14 × 14)

μPD789314GC-xxx-AB8: 64-pin plastic QFP (14 × 14)

μPD789316GC-xxx-AB8: 64-pin plastic QFP (14 × 14)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: three times or less	IR35-00-3
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: three times or less	VP15-00-3
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once, Preheating temperature: 120°C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C max. Time: 3 seconds max. (per pin row)	—

Caution Do not use different soldering method together (except for partial heating).

μPD789304GK-xxx-9ET: 64-pin plastic TQFP (fine pitch) (12 × 12)

μPD789306GK-xxx-9ET: 64-pin plastic TQFP (fine pitch) (12 × 12)

μPD789314GK-xxx-9ET: 64-pin plastic TQFP (fine pitch) (12 × 12)

μPD789316GK-xxx-9ET: 64-pin plastic TQFP (fine pitch) (12 × 12)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: two times or less, Exposure limit: 7 days ^{Note} (after that, prebake at 125°C for 10 hours)	IR35-107-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: two times or less, Exposure limit: 7 days ^{Note} (after that, prebake at 125°C for 10 hours)	VP15-107-2
Partial heating	Pin temperature: 300°C max. Time: 3 seconds max. (per pin row)	—

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering method together (except for partial heating).

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD789304, 789306, 789314, and 789316.

Language Processing Software

RA78K0S ^{Notes 1, 2, 3}	Assembler package common to 78K/0S Series
CC78K0S ^{Notes 1, 2, 3}	C compiler package common to 78K/0S Series
★ DF789306 ^{Notes 1, 2, 3}	Device file for μPD789306, 789316 Subseries
CC78K0S-L ^{Notes 1, 2, 3}	C compiler library source file common to 78K/0S Series

Flash Memory Writing Tools

Flashpro III (Part No. FL-PR3 ^{Note 4} , PG-FP3)	Flash programmer dedicated to on-chip flash memory microcontroller
FA-64GC ^{Note 4}	Flash memory writing adapter for 64-pin plastic QFP (GC-AB8 type)
FA-64GK ^{Note 4}	Flash memory writing adapter for 64-pin plastic TQFP (fine pitch) (GK-9ET type)

Debugging Tools

IE-78K0S-NS In-circuit emulator	This is an in-circuit emulator for debugging hardware and software of application system using the 78K/0S Series. It supports the integrated debugger (ID78K0S-NS). It is used with an AC adapter, emulation probe, and interface adapter for connecting the host machine.
IE-70000-MC-PS-B AC adapter	This is the adapter for supplying power from an AC-100 to 240 V outlet.
IE-70000-98-IF-C Interface adapter	This adapter is needed when PC-9800 series PC (except notebook type) is used as the host machine for an IE-78K0S-NS (supports C bus).
IE-70000-CD-IF-A PC card interface	This PC card and interface cable are needed when a PC-9800 series notebook-type PC is used as the host machine for an IE-78K0S-NS (supports PCMCIA socket).
IE-70000-PC-IF-C Interface adapter	This adapter is needed when an IBM PC/AT™ or compatible PC is used as the host machine for an IE-78K0S-NS (supports ISA bus).
★ IE-70000-PCI-IF-A Interface adapter	This adapter is needed when a PC that includes a PCI bus is used as the host machine for an IE-78K0S-NS.
★ IE-789306-NS-EM1 Emulation board	This is an emulation board for emulating the peripheral hardware inherent to the device. It is used with an in-circuit emulator.
NP-64GC ^{Note 4}	This is a board that is used to connect an in-circuit emulator to the target system. It is for 64-pin plastic QFP (GC-AB8 type).
NP-64GK ^{Note 4}	This is a board that is used to connect an in-circuit emulator to the target system. It is for 64-pin plastic TQFP (GK-9ET type).
SM78K0S ^{Notes 1, 2}	System simulator common to 78K/0S Series
ID78K0S-NS ^{Notes 1, 2}	Integrated debugger common to 78K/0S Series
★ DF789306 ^{Notes 1, 2}	Device file for μPD789306, 789316 Subseries

Real-Time OS

MX78K0S ^{Notes 1, 2}	OS for 78K/0S Series
-------------------------------	----------------------

- Notes**
1. Based on PC-9800 series (Japanese Windows)
 2. Based on IBM PC/AT compatible (Japanese/English Windows)
 3. Based on HP9000 series 700™ (HP-UX™), SPARCstation™ (SunOS™, Solaris™), or NEWS™ (NEWS-OS™)
 4. This product is manufactured by Naito Densetsu Machida Mfg. Co., Ltd. (TEL +81-44-822-3813).

Remark The RA78K0S, CC78K0S, and SM78K0S are used in combination with the DF789306.

APPENDIX B. RELATED DOCUMENTS

Documents Related to Devices

Document Name	Document No.
μPD789304, 789306, 789314, 789316 Data Sheet	This manual
μPD78F9306, 78F9316 Data Sheet	To be prepared
μPD789306, 789316 Subseries User's Manual	U14800E
78K/0S Series User's Manual Instructions	U11047E

Documents Related to Development Tools (User's Manuals)

Document Name		Document No.
RA78K0S Assembler Package	Operation	U11622E
	Language	U11599E
	Structured Assembly Language	U11623E
CC78K0S C Compiler	Operation	U11816E
	Language	U11817E
SM78K0S, SM78K0 System Simulator Ver. 2.10 or Later Windows Based	Operation	U14611E
SM78K Series System Simulator Ver. 2.10 or Later	External Part User Open Interface Specifications	U15006E
ID-78K0-NS, ID78K0S-NS Integrated Debugger Ver. 2.20 or Later Windows Based	Operation	U14910E
IE-78K0S-NS In-Circuit Emulator		U13549E
IE-789306-NS-EM1 Emulation Board		To be prepared

Documents Related to Embedded Software (User's Manual)

Document Name		Document No.
78K/0S Series OS MX78K0S	Fundamental	U12938E

Other Related Documents

Document Name	Document No.
SEMICONDUCTOR SELECTION GUIDE Products & Packages (CD-ROM)	X13769X
Semiconductor Device Mounting Technology Manual	C10535E
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

EEPROM is a trademark of NEC Corporation.

Windows is either a registered trademark or a trademark of Microsoft Corporation in the United States and/or other countries.

PC/AT is a trademark of International Business Machines Corporation.

HP9000 series 700 and HP-UX are trademarks of Hewlett-Packard Company.

SPARCstation is a trademark of SPARC International, Inc.

Solaris and SunOS are trademarks of Sun Microsystems, Inc.

NEWS and NEWS-OS are trademarks of Sony Corporation.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

NEC Electronics Inc. (U.S.)

Santa Clara, California
Tel: 408-588-6000
800-366-9782
Fax: 408-588-6130
800-729-9288

NEC Electronics (Germany) GmbH

Duesseldorf, Germany
Tel: 0211-65 03 02
Fax: 0211-65 03 490

NEC Electronics (UK) Ltd.

Milton Keynes, UK
Tel: 01908-691-133
Fax: 01908-670-290

NEC Electronics Italiana s.r.l.

Milano, Italy
Tel: 02-66 75 41
Fax: 02-66 75 42 99

NEC Electronics (Germany) GmbH

Benelux Office
Eindhoven, The Netherlands
Tel: 040-2445845
Fax: 040-2444580

NEC Electronics (France) S.A.

Velizy-Villacoublay, France
Tel: 01-3067-5800
Fax: 01-3067-5899

NEC Electronics (France) S.A.

Madrid Office
Madrid, Spain
Tel: 091-504-2787
Fax: 091-504-2860

NEC Electronics (Germany) GmbH

Scandinavia Office
Taeby, Sweden
Tel: 08-63 80 820
Fax: 08-63 80 388

NEC Electronics Hong Kong Ltd.

Hong Kong
Tel: 2886-9318
Fax: 2886-9022/9044

NEC Electronics Hong Kong Ltd.

Seoul Branch
Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

NEC Electronics Singapore Pte. Ltd.

Novena Square, Singapore
Tel: 253-8311
Fax: 250-3583

NEC Electronics Taiwan Ltd.

Taipei, Taiwan
Tel: 02-2719-2377
Fax: 02-2719-5951

NEC do Brasil S.A.

Electron Devices Division
Guarulhos-SP, Brasil
Tel: 11-6462-6810
Fax: 11-6462-6829

The export of this product from Japan is regulated by the Japanese government. To export this product may be prohibited without governmental license, the need for which must be judged by the customer. The export or re-export of this product from a country other than Japan may also be prohibited without a license from that country. Please call an NEC sales representative.

• **The information in this document is current as of December, 2000. The information is subject to change without notice. For actual design-in, refer to the latest publications of NEC's data sheets or data books, etc., for the most up-to-date specifications of NEC semiconductor products. Not all products and/or types are available in every country. Please check with an NEC sales representative for availability and additional information.**

• No part of this document may be copied or reproduced in any form or by any means without prior written consent of NEC. NEC assumes no responsibility for any errors that may appear in this document.

• NEC does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from the use of NEC semiconductor products listed in this document or any other liability arising from the use of such products. No license, express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC or others.

• Descriptions of circuits, software and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software and information in the design of customer's equipment shall be done under the full responsibility of customer. NEC assumes no responsibility for any losses incurred by customers or third parties arising from the use of these circuits, software and information.

• While NEC endeavours to enhance the quality, reliability and safety of NEC semiconductor products, customers agree and acknowledge that the possibility of defects thereof cannot be eliminated entirely. To minimize risks of damage to property or injury (including death) to persons arising from defects in NEC semiconductor products, customers must incorporate sufficient safety measures in their design, such as redundancy, fire-containment, and anti-failure features.

• NEC semiconductor products are classified into the following three quality grades:
"Standard", "Special" and "Specific". The "Specific" quality grade applies only to semiconductor products developed based on a customer-designated "quality assurance program" for a specific application. The recommended applications of a semiconductor product depend on its quality grade, as indicated below. Customers must check the quality grade of each semiconductor product before using it in a particular application.

"Standard": Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

"Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

"Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.

The quality grade of NEC semiconductor products is "Standard" unless otherwise expressly specified in NEC's data sheets or data books, etc. If customers wish to use NEC semiconductor products in applications not intended by NEC, they must contact an NEC sales representative in advance to determine NEC's willingness to support a given application.

(Note)

(1) "NEC" as used in this statement means NEC Corporation and also includes its majority-owned subsidiaries.

(2) "NEC semiconductor products" means any semiconductor product developed or manufactured by or for NEC (as defined above).