M37204MC-XXXSP
M37204EC-XXXSP, M37204ECSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER and ON-SCREEN DISPLAY CONTROLLER

DESCRIPTION

The M37204MC-XXXSP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP.

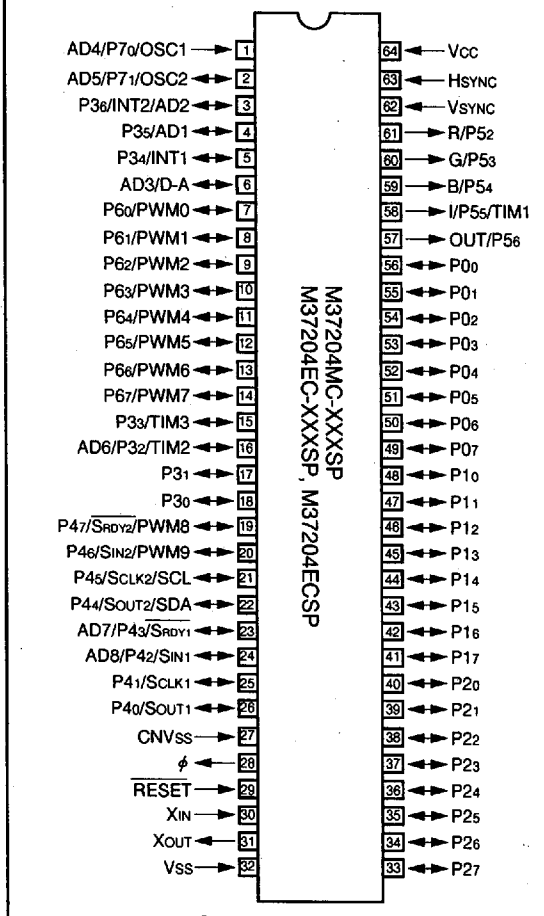
In addition to their simple instruction sets, the ROM, RAM and I/O addresses are placed on the same memory map to enable easy programming.

The M37204MC-XXXSP has a PWM function and an OSD function, so it is useful for a channel selection system for TV. The features of the M37204EC-XXXSP and the M37204ECSP are similar to those of the M37204MC-XXXSP except that these chips have a built-in PROM which can be written electrically. Accordingly, the following descriptions will be for the M37204MC-XXXSP unless otherwise noted.

FEATURES

- Number of basic instructions 69
- Memory size .....
  - ROM ..... 48 K bytes
  - RAM ..... 704 bytes
  - ROM for display ..... 8 K bytes
  - RAM for display ..... 144 bytes
- The minimum instruction execution time ..... 0.5 μs (at 8 MHz oscillation frequency)
- Power source voltage ..... 5 V ± 10 %
- Subroutine nesting ..... 128 levels (Max.)
- Interrupts ..... 13 types, 13 vectors
- 8-bit timers 4
- Programmable I/O ports (Ports P0, P1, P2, P30–P36, P4, P6) 47
- Output ports (Ports P52–P56) 5
- 12 V withstand ports 10
- LED drive ports 4
- Serial I/O ..... 8-bit × 2 channel (2 systems)
- Special serial I/O for master transmission and reception 1
- Power dissipation ..... 110 mW (at V_{CC} = 5.5 V, 4 MHz oscillation frequency, CRT on)
- A-D comparator (6-bit resolution) ..... 8 channels
- PWM output circuit ..... 14-bit × 1, 8-bit × 10
- Interrupt interval determination circuit 1
- CRT display function
  - Display characters ..... 24 characters × 3 lines (16 lines max.)
  - Character kinds ..... 256 kinds
  - Dot structure ..... 12 × 16 dots
  - Character size ..... 4 kinds
  - Character color kinds (It can be specified by the character) max. 15 kinds (R, G, B, I)
  - Character background color(It can be specified by the character) max. 7 kinds (R, G, B)
  - 1/2-character unit color specification is possible.
  - Raster color (max. 15 kinds)
  - Display layout
    - Horizontal ..... 64 levels
    - Vertical ..... 128 levels
  - Bordering (horizontal and vertical)
  - Wipe function
  - Scanning line double count mode display is possible.

PIN CONFIGURATION (TOP VIEW)



Outline 64P4B

APPLICATION

TV

M37204MC-XXXSP
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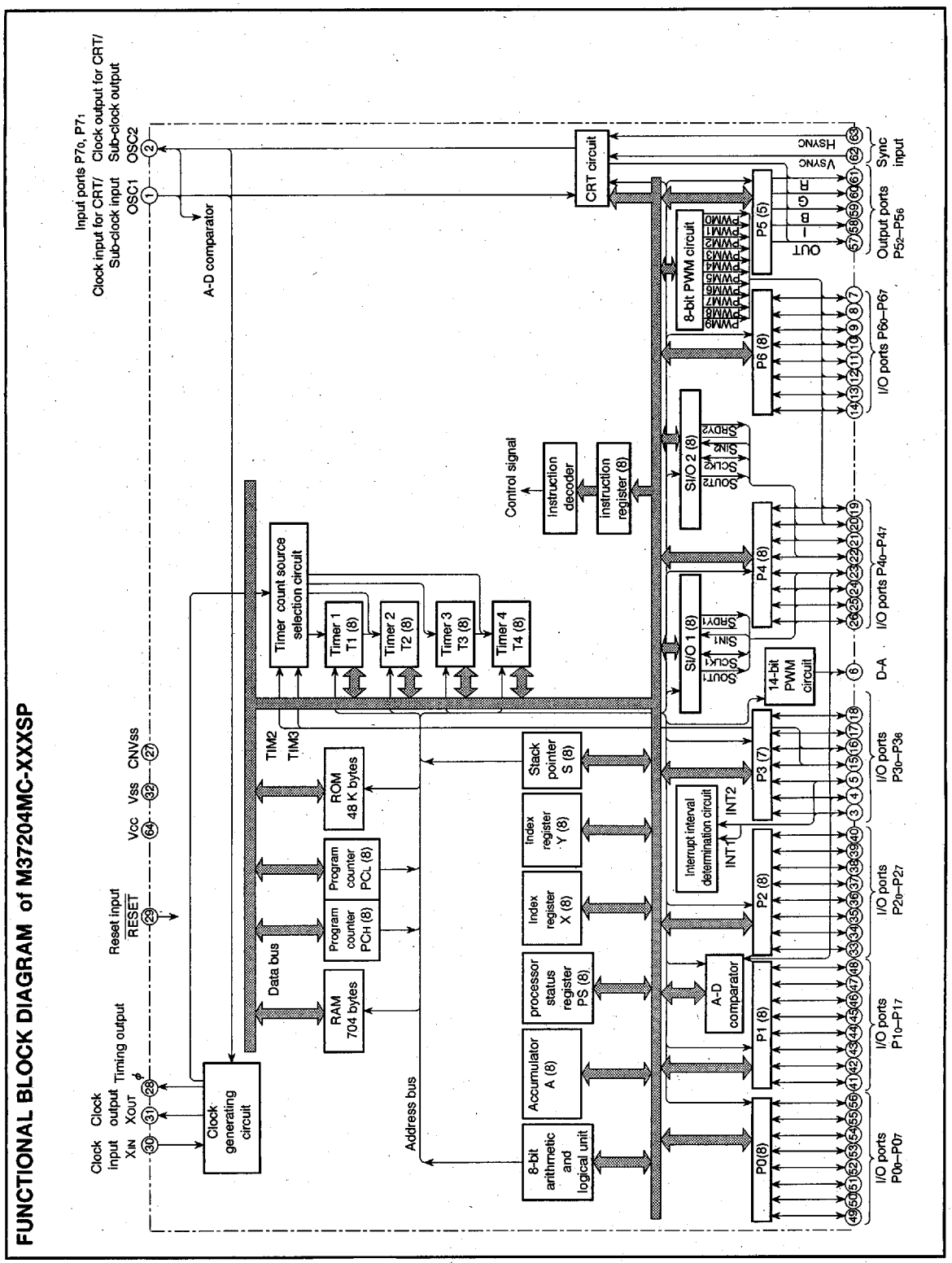
SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER and ON-SCREEN DISPLAY CONTROLLER

FUNCTIONAL BLOCK DIAGRAM of M37204MC-XXXSP



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SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER and ON-SCREEN DISPLAY CONTROLLER

FUNCTIONS

Parameter			Functions
Number of basic instructions			69
Instruction execution time			0.5 μs (the minimum instruction execution time, at 8 MHz oscillation frequency)
Clock frequency			8 MHz (maximum)
Memory size	ROM		48 K bytes
	RAM		704 bytes
	ROM for display		8 K bytes
	RAM for display		144 bytes
Input/Output ports	$P0_0$–$P0_7$	I/O	8-bit × 1 (CMOS input/output structure)
	$P1_0$–$P1_7$	I/O	8-bit × 1 (CMOS input/output structure)
	$P2_0$–$P2_7$	I/O	8-bit × 1 (CMOS input/output structure)
	$P3_0$, $P3_1$	I/O	2-bit × 1 (CMOS input/output structure)
	$P3_2$–$P3_6$	I/O	5-bit × 1 (N-channel open-drain output structure, can be used as external clock input pins, A-D input pins, INT input pins)
	$P4_0$–$P4_7$	I/O	8-bit × 1 (N-channel open-drain output structure, can be used as serial I/O pins, A-D input pins, PWM output pins)
	$P5_2$–$P5_6$	Output	5-bit × 1 (CMOS output structure, can be used as CRT output pins, an external clock output pin)
	$P6_0$–$P6_7$	I/O	8-bit × 1 (N-channel open-drain output structure, can be used as PWM outputs)
	$P7_0$		1-bit × 1 (can be used as a CRT display clock input pin, an A-D input pin)
	$P7_1$		1-bit × 1 (can be used as a CRT display clock output pin, an A-D input pin)
Serial I/O			8-bit × 2, special serial I/O (8-bit) × 1
A-D comparator			8 channels (6-bit resolution)
PWM output circuit			14-bit × 1, 8-bit × 10
Timers			8-bit timer × 4
Subroutine nesting			128 levels (maximum)
Interrupt interval determination circuit			1
Interrupt			External interrupt × 2, Internal timer interrupt × 4, Serial I/O interrupt × 1, CRT interrupt × 1, f(XIN)/4096 interrupt × 1, VSYNC interrupt × 1, BRK interrupt × 1
Clock generating circuit			2 built-in circuits (externally connected a ceramic resonator or a quartz-crystal oscillator)
Power source voltage			5 V ± 10 %
Power dissipation	CRT ON		110 mW typ. (at oscillation frequency f_{CPU} = 4 MHz, f_{CRT} = 8 MHz)
	CRT OFF		55 mW typ. (at oscillation frequency f_{CPU} = 4 MHz)
	In stop mode		1.65 mW (maximum)
Operating temperature range			−10 °C to 70 °C
Device structure			CMOS silicon gate process
Package			64-pin shrink plastic molded DIP
CRT display function	Number of character		24 characters × 3 lines (maximum 16 lines by software)
	Character dot construction		12 × 16 dots
	Kinds of characters		256 kinds
	Character size		4 kinds
	Kinds of color		Maximum 15 kinds (R, G, B, I)
	Display position (horizontal, vertical)		64 levels (horizontal) × 128 levels (vertical)

PIN DESCRIPTION

Pin	Name	Input/ Output	Name
V_{CC}, V_{SS}	Power source		Apply voltage of 5 V ± 10 % to V_{CC} and AV_{CC}, and 0 V to V_{SS}.
CNVss	CNVss		This is connected to V_{SS}.
RESET	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for 2 μs or more (under normal V_{CC} conditions). If more time is needed for the quartz-crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
XIN	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic resonator or a quartz-crystal oscillator is connected between pins XIN and XOUT. If an external clock is used, the clock source should be connected to the XIN pin and the XOUT pin should be left open.
XOUT	Clock output	Output	
$P0_0$–$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with direction register allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is CMOS output. The note of this Table gives a full of port P0 function.
$P1_0$–$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0. The output structure is CMOS output.
$P2_0$–$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0. The output structure is CMOS output.
$P3_0$, $P3_1$	I/O port P3	I/O	Ports $P3_0$, $P3_1$ are a 2-bit I/O port and have basically the same functions as port P0. The output structure is CMOS output.
AD6/$P3_2$/ TIM2,	I/O port P3	I/O	Ports $P3_2$–$P3_6$ are a 5-bit I/O port and basically the same functions as port P0. The output structure is N-channel open-drain output.
$P3_3$/TIM3,	Analog input	Input	Pins $P3_2$, $P3_5$, $P3_6$ are also used as analog input pins AD6, AD1 and AD2 respectively.
$P3_4$/INT1,	External clock input	Input	Pins $P3_2$, $P3_3$ are also used as external clock input pins TIM2, TIM3 respectively.
$P3_5$/AD1,	External interrupt input	Input	Pins $P3_4$, $P3_6$ are also used as external interrupt input pins INT1, INT2.
$P3_6$/INT2/ AD2			
$P4_0$/SOUT1,	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same functions as port P0. The output structure is N-channel open-drain output.
$P4_1$/SCLK1,	Serial I/O data input/output	I/O	Pins $P4_0$, $P4_2$, $P4_4$, $P4_6$ are also used as serial I/O data input/output pins SOUT1, SIN1, SOUT2, SIN2 respectively. The output structure is N-channel open-drain output.
AD8/$P4_2$/ SIN1,	Serial I/O synchronizing clock input/ output	I/O	Pins $P4_1$, $P4_5$ are also used as serial I/O synchronizing clock input/output pins SCLK1, SCLK2 respectively. The output structure is N-channel open-drain output.
AD7/$P4_3$/ $\overline{SRDY1}$,	Serial I/O receive enable signal output	Output	Pins $P4_3$, $P4_7$ are also used as serial I/O receive enable signal output pins $\overline{SRDY1}$, $\overline{SRDY2}$ respectively. The output structure is N-channel open-drain output.
$P4_4$/SOUT2/ SDA,	Special serial I/O input/output	I/O	Pins $P4_4$, $P4_5$ are also used as SDA, SCL respectively when special serial I/O is used. The output structure is N-channel open-drain output.
$P4_5$/SCLK2/ SCL,	Analog input	Input	Pins $P4_2$, $P4_3$ are also used as analog input pins AD8, AD7 respectively.
$P4_6$/SIN2/ PWM9,	PWM output	Output	Pins $P4_6$, $P4_7$ are also used as PWM output pins PWM9, PWM8 respectively. The output structure is N-channel open-drain output.
$P4_7$/$\overline{SRDY2}$/ PWM8			

PIN DESCRIPTION (continued)

R/P52, G/P53, B/P54, I/P55/TIM1, OUT/P56	Output port P5	Output	Ports P52–P56 are a 5-bit output port. The output structure is CMOS output.
	CRT output	Output	Pins P52–P56 are also used as CRT output pins R, G, B, I, OUT respectively. The output structure is CMOS output.
	Timer 1 overflow signal output	Output	Pin P55 is also used as timer 1 overflow signal output pin TIM1. The output structure is CMOS output.
P60/PWM0–P67/PWM7	I/O port P6	I/O	Port P6 is an 8-bit I/O port and has basically the same functions as port P0. The output structure is N-channel open-drain output.
	PWM output	Output	Pins P60–P67 are also used as PWM output pins PWM0–PWM7 respectively. The output structure is CMOS output.
AD4/P70/OSC1, AD5/P71/OSC2	Input port P7	Input	Ports P70, P71 are 2-bit input port.
	Clock input for CRT display	Input	Pin P70 is also used as CRT display clock input pin OSC1.
	Clock output for CRT display	Output	Pin P71 is also used as CRT display clock output pin OSC2. The output structure is CMOS output.
	Analog input	Input	Pins P70, P71 are also used as analog input pins AD4, AD5 respectively.
HSYNC	HSYNC input	Input	This is a horizontal synchronizing signal input for CRT display.
VSYNC	VSYNC input	Input	This is a vertical synchronizing signal input for CRT display.
ϕ	Timing output	Output	This is a timing output pin. This pin has reset-out output function. The output structure is CMOS output.
AD3/D-A	DA output	Output	This is an output pin for 14-bit PWM. The output structure is CMOS output.
	Analog input	Input	The D-A pin is also used as analog input pin AD3.

Note : As shown in the memory map (Figure 3), port P0 is accessed as a memory at address $00C0_{16}$ of zero page. Port P0 has the port P0 direction register (address $00C1_{16}$ of zero page) which can be used to program each bit as an input ("0") or an output ("1"). The pins programmed as "1" in the direction register are output pins. When pins are programmed as "0," they are input pins. When pins are programmed as output pins, the output data are written into the port latch and then output. When data is read from the output pins, the output pin level is not read but the data of the port latch is read. This allows a previously-output value to be read correctly even if the output "L" voltage has risen, for example, because a light emitting diode was directly driven. The input pins are in the floating state, so the values of the pins can be read. When data is written into the input pin, it is written only into the port latch, while the pin remains in the floating state.

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The M37204MC-XXXSP uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine instructions or the SERIES 740 <Software> User's Manual for details on the instruction set.

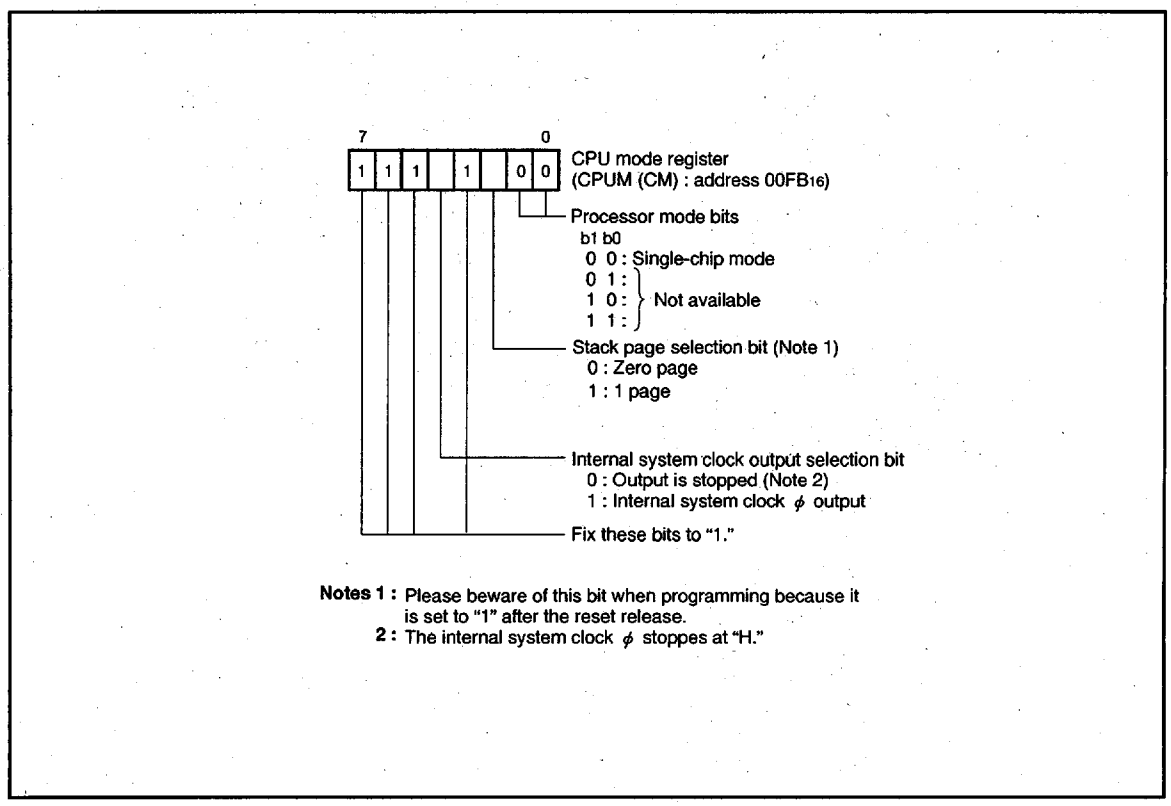
Machine-resident 740 family instructions are as follows:

The FST, SLW instruction cannot be used.

The MUL, DIV, WIT and STP instruction can be used.

CPU Mode Register

The CPU mode register contains the stack page selection bit and internal system clock output selection bit. The CPU mode register is allocated at address 00FB16.



Notes 1 : Please beware of this bit when programming because it is set to "1" after the reset release.
2 : The internal system clock φ stoppes at "H."

Fig. 1. Structure of CPU mode register

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MEMORY

Special Function Register (SFR) Area
The special function register (SFR) area in the zero page contains control registers such as I/O ports and timers.

RAM
RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM
ROM is used for storing user programs as well as the interrupt vector area.

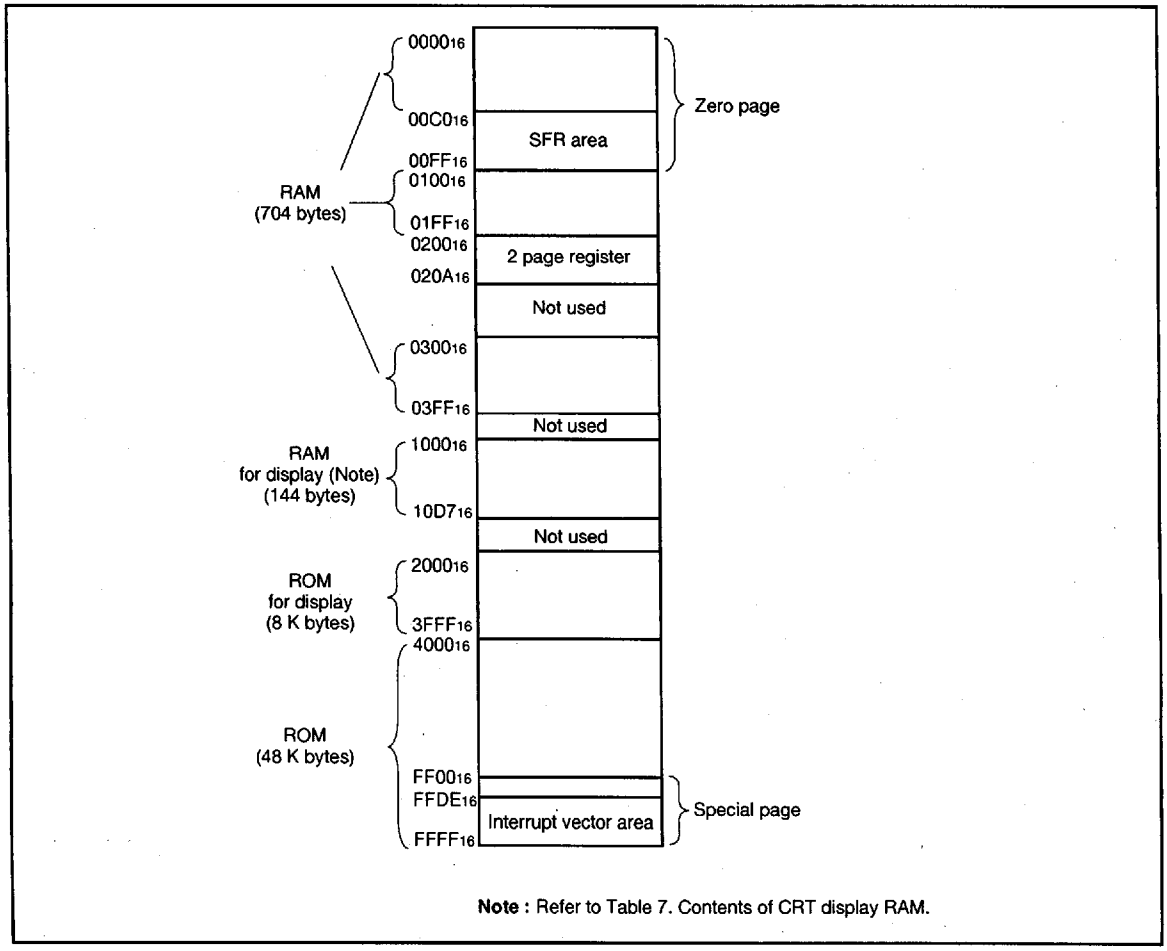
RAM for Display
RAM for display is used for specifying the character codes and colors to display.

ROM for Display
ROM for display is used for storing character data.

Interrupt Vector Area
The interrupt vector area contains reset and interrupt vectors.

Zero Page
The 256 bytes from addresses 000016 to $00FF16$ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.
The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special Page
The 256 bytes from addresses $FF0016$ to $FFFF16$ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.



Note : Refer to Table 7. Contents of CRT display RAM.

Fig. 2. Memory map

■SFR area (addresses $C0_{16}$ to DF_{16})

: Nothing is allocated

: Fix this bit to "0" (do not write "1")

0 : "0" immediately after reset

1 : "1" immediately after reset

? : undefined immediately after reset

Address	Register	Bit allocation (b7 ... b0)	State immediately after reset (b7 ... b0)
$C0_{16}$	Port P0 (P0)		?
$C1_{16}$	Port P0 direction register (D0)		00_{16}
$C2_{16}$	Port P1 (P1)		?
$C3_{16}$	Port P1 direction register (D1)		00_{16}
$C4_{16}$	Port P2 (P2)		?
$C5_{16}$	Port P2 direction register (D2)		00_{16}
$C6_{16}$	Port P3 (P3)		0 ? ? ? ? ? ? ?
$C7_{16}$	Port P3 direction register (D3)		0 0 0 0 0 0 0 0
$C8_{16}$	Port P4 (P4)		?
$C9_{16}$	Port P4 direction register (D4)		00_{16}
CA_{16}	Port P5 (P5)		0 ? ? ? ? ? ? ?
CB_{16}	Port P5 control register (C5)		0 0 0 0 0 0 0 0
CC_{16}	Port P6 (P6)		?
CD_{16}	Port P6 direction register (D6)		00_{16}
CE_{16}	DA-H register (DA-H)		?
CF_{16}	DA-L register (DA-L)		? 0 ? ? ? ? ? ?
$D0_{16}$	PWM0 register (PWM0)		?
$D1_{16}$	PWM1 register (PWM1)		?
$D2_{16}$	PWM2 register (PWM2)		?
$D3_{16}$	PWM3 register (PWM3)		?
$D4_{16}$	PWM4 register (PWM4)		?
$D5_{16}$	PWM output control register 1 (PW)	PW7 PW6 PW5 PW4 PW3 PW2 PW1 PW0	00_{16}
$D6_{16}$	PWM output control register 2 (PN)	PN4 PN3 PN2 PN1 PN0	0 0 0 0 0 0 0 0
$D7_{16}$	Interrupt interval determination register (RI)		?
$D8_{16}$	Interrupt interval determination conotrol register (RE)	RE4 RE3 RE2 RE1 RE0	0 0 0 0 0 0 0 0
$D9_{16}$	Special serial I/O register (SSIO)		?
DA_{16}	Special mode register 1 (SB)	SB7 SB6 SB5 SB4 SB3 SB2 SB1 SB0	00_{16}
DB_{16}	Special mode register 2 (SC)	SC7 SC6 SC5 SC4 SC3 SC2 SC1 SC0	00_{16}
DC_{16}	Serial I/O1 mode register (SM1)	SM15 SM14 SM13 SM12 SM11 SM10	0 0 0 0 0 0 0 0
DD_{16}	Serial I/O1 regsiter (SIO1)		?
DE_{16}	Serial I/O2 mode register (SM2)	SM25 SM24 SM23 SM22 SM21 SM20	0 0 0 0 0 0 0 0
DF_{16}	Serial I/O2 regsiter (SIO2)		?

Fig. 3. Memory map of special function register (SFR) (1)

■SFR area (addresses $E0_{16}$ to FF_{16})

▒ : Nothing is allocated

▨ : Fix this bit to "0" (do not write "1")

▨ : Fix this bit to "1" (do not write "0")

0 : "0" immediately after reset

1 : "1" immediately after reset

? : undefined immediately after reset

Address	Register	Bit allocation b7							b0	State immediately after reset b7							b0
$E0_{16}$	Horizontal position register (HR)			HR5	HR4	HR3	HR2	HR1	HR0	0	0	0	0	0	0	0	0
$E1_{16}$	Vertical position register 1 (CV1)		CV16	CV15	CV14	CV13	CV12	CV11	CV10	0	?	?	?	?	?	?	?
$E2_{16}$	Vertical position register 2 (CV2)		CV26	CV25	CV24	CV23	CV22	CV21	CV20	0	?	?	?	?	?	?	?
$E3_{16}$	Vertical position register 3 (CV3)		CV36	CV35	CV34	CV33	CV32	CV31	CV30	0	?	?	?	?	?	?	?
$E4_{16}$	Character size register (CS)	CS7		CS31	CS30	CS21	CS20	CS11	CS10	0	0	?	?	?	?	?	?
$E5_{16}$	Border selection register (MD)			MD31	MD30	MD21	MD20	MD11	MD10	0	0	0	0	0	0	0	0
$E6_{16}$	Color register 0 (CO0)			CO05	CO04	CO03	CO02	CO01	CO00	0	0	0	0	0	0	0	0
$E7_{16}$	Color register 1 (CO1)			CO15	CO04	CO13	CO12	CO11	CO10	0	0	0	0	0	0	0	0
$E8_{16}$	Color register 2 (CO2)			CO25	CO24	CO23	CO22	CO21	CO20	0	0	0	0	0	0	0	0
$E9_{16}$	Color register 3 (CO3)			CO35	CO34	CO33	CO32	CO31	CO30	0	0	0	0	0	0	0	0
EA_{16}	CRT control register (CC)		CC6	CC5	CC4	CC3	CC2	CC1	CC0	0	0	0	0	0	0	0	0
EB_{16}	Display block counter (CBC)					CBC3	CBC2	CBC1	CBC0	0	0	0	0	0	0	0	0
EC_{16}	CRT port control register (CC)	OP7	OP6	OP5	OUT	I	R/G/B	VSYC	HSYC	00_{16}							
ED_{16}	Wipe control register (SL)		SL6	SL5	SL4	SL3	SL2	SL1	SL0	0	0	0	0	0	0	0	0
EE_{16}	Wipe start register (SLS)									?							
EF_{16}	A-D control register 1 (ADM)				ADM4		ADM2	ADM1	ADM0	0	0	0	0	0	0	0	0
$F0_{16}$	Timer 1 (TM1)									FF_{16}							
$F1_{16}$	Timer 2 (TM2)									07_{16}							
$F2_{16}$	Timer 3 (TM3)									FF_{16}							
$F3_{16}$	Timer 4 (TM4)									07_{16}							
$F4_{16}$	Timer 12 mode register (T12M)				T12M4	T12M3	T12M2	T12M1	T12M0	0	0	0	0	0	0	0	0
$F5_{16}$	Timer 34 mode register (T34M)				T34M4	T34M3	T34M2	T34M1	T34M0	0	0	0	0	0	0	0	0
$F6_{16}$	PWM5 register (PWM5)									?							
$F7_{16}$	PWM6 register (PWM6)									?							
$F8_{16}$	PWM7 register (PWM7)									?							
$F9_{16}$	PWM8 register (PWM8)									?							
FA_{16}	PWM9 register (PWM9)									?							
FB_{16}	CPU mode register (CPUM)				CM4		CM2	CM1	CM0	1	1	1	1	1	1	0	0
FC_{16}	Interrupt request register 1 (IREQ1)			VSCR	CRTR	TM4R	TM3R	TM2R	TM1R	0	0	0	0	0	0	0	0
FD_{16}	Interrupt request register 2 (IREQ2)				MSR	S2R	S1R	1T2R	1T1R	0	0	0	0	0	0	0	0
FE_{16}	Interrupt control register 1 (ICON1)			VSCE	CRTE	TM4E	TM3E	TM2E	TM1E	0	0	0	0	0	0	0	0
FF_{16}	Interrupt control register 2 (ICON2)				MSE	S2E	S1E	1T2E	1T1E	0	0	0	0	0	0	0	0

Fig. 4. Memory map of special function register (SFR) (2)

■SFR area (addresses 200_{16} to $20A_{16}$)

▒ : Nothing is allocated

▨ : Fix this bit to "0" (do not write "1")

0 : "0" immediately after reset

Address	Register	Bit allocation b7							b0	State immediately after reset b7							b0
200_{16}										?	?	?	?	?	?	?	?
201_{16}										?	?	?	?	?	?	?	?
202_{16}										?	?	?	?	?	?	?	?
203_{16}										?	?	?	?	?	?	?	?
204_{16}										?	?	?	?	?	?	?	?
205_{16}										?	?	?	?	?	?	?	?
206_{16}	Port conotrol reigster (P7D)						DA	P71	P70	0	0	0	0	0	0	?	?
207_{16}	Shift register input switch register (SIC)							SIC1	SIC0	0	0	0	0	0	0	0	0
208_{16}	CRT control register 2 (CBR)				CBR4	CBR3	CBR2	CBR1	CBR0	0	0	0	0	0	0	0	0
209_{16}	CRT clock selection register (OP)							OP11	OP10	▨	0	0	0	0	0	0	0
$20A_{16}$	AD control register 2 (ADC)			ADC5	ADC4	ADC3	ADC2	ADC1	ADC0	0	▨	0	0	0	0	0	0

Fig. 5. Memory map of 2 page register

▒ : Nothing is allocated

1 : "1" immediately after reset

? : undefined immediately after reset

Register	Bit allocation b7							b0	State immediately after reset b7							b0
Processor status register (PS)	N	V	T	B	D	I	Z	C	?	?	?	?	?	1	?	?
Program counter (PCH)									Contents of address $FFFF_{16}$							
Program counter (PCL)									Contents of address $FFFE_{16}$							

Fig. 6. Internal state of processor status register and program counter at reset

INTERRUPTS

Interrupts can be caused by 13 different sources consisting of 3 external, 9 internal, 1 software, and reset. Interrupts are vectored interrupts with priorities shown in Table 1. Reset is also included in the table because its operation is similar to an interrupt.

When an interrupt is accepted,

(1) The contents of the program counter and processor status register are automatically stored into the stack.
(2) The interrupt disable flag I is set to "1" and the corresponding interrupt request bit is set to "0."
(3) The jump destination address is read from and the vector address enters the program counter.

Other interrupts are disabled when the interrupt disable flag is set to "1."

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit. The interrupt request bits are in interrupt request registers 1 and 2 and the interrupt enable bits are in interrupt control registers 1 and 2. Figure 7 shows the structure of the interrupt-related registers.

Interrupts other than the BRK instruction interrupt and reset are accepted when the interrupt enable bit is "1," interrupt request bit is "1," and the interrupt disable flag is "0." The interrupt request bit can be set to "0" by a program, but not set to "1." The interrupt enable bit can be set to "0" and "1" by a program.

Reset is treated as a non-maskable interrupt with the highest priority. Figure 8 shows interrupt control.

Interrupt Causes

(1) VSYNC and CRT interrupts
The VSYNC interrupt is an interrupt request synchronized with the vertical sync signal.
The CRT interrupt occurs after character block display to the CRT is completed.

(2) INT1, INT2 interrupts
With an external interrupt input, the system detects that the level of a pin changes from "L" to "H" or from "H" to "L," and generates an interrupt request. The input active edge can be selected by bits 3 and 4 of the interrupt interval determination control register (address $00D8_{16}$) : when this bit is "0," a change from "L" to "H" is detected; when it is "1," a change from "H" to "L" is detected. Note that all bits are cleared to "0" at reset.

(3) Timer 1, 2, 3 and 4 interrupts
An interrupt is generated by an overflow of timer 1, 2, 3 or 4.

(4) Serial I/O1, serial I/O2 interrupts
This is an interrupt request from the clock synchronous serial I/O function.

(5) f(XIN)/4096 interrupt
This interrupt occurs regularly with a f(XIN)/4096 period. Set bit 0 of the PWM output control register 1 to "0."

(6) BRK instruction interrupt
This software interrupt has the least significant priority. It does not have a corresponding interrupt enable bit, and it is not affected by the interrupt disable flag I (non-maskable).

Table 1. Interrupt vector addresses and priority

Interrupt source	Priority	Vector addresses	Remarks
Reset	1	$FFFF_{16}$, $FFFE_{16}$	Non-maskable
CRT interrupt	2	$FFFD_{16}$, $FFFC_{16}$	
INT2 interrupt	3	$FFFB_{16}$, $FFFA_{16}$	Active edge selectable
INT1 interrupt	4	$FFF9_{16}$, $FFF8_{16}$	Active edge selectable
Serial I/O2 interrupt	5	$FFF7_{16}$, $FFF6_{16}$	
Timer 4 interrupt	6	$FFF5_{16}$, $FFF4_{16}$	
f(XIN)/4096 interrupt	7	$FFF3_{16}$, $FFF2_{16}$	
VSYNC interrupt	8	$FFF1_{16}$, $FFF0_{16}$	Active edge selectable
Timer 3 interrupt	9	$FFEF_{16}$, $FFEE_{16}$	
Timer 2 interrupt	10	$FFED_{16}$, $FFEC_{16}$	
Timer 1 interrupt	11	$FFEB_{16}$, $FFEA_{16}$	
Serial I/O1 interrupt	12	$FFE9_{16}$, $FFE8_{16}$	
BRK instruction interrupt	13	$FFDF_{16}$, $FFDE_{16}$	Non-maskable (software interrupt)

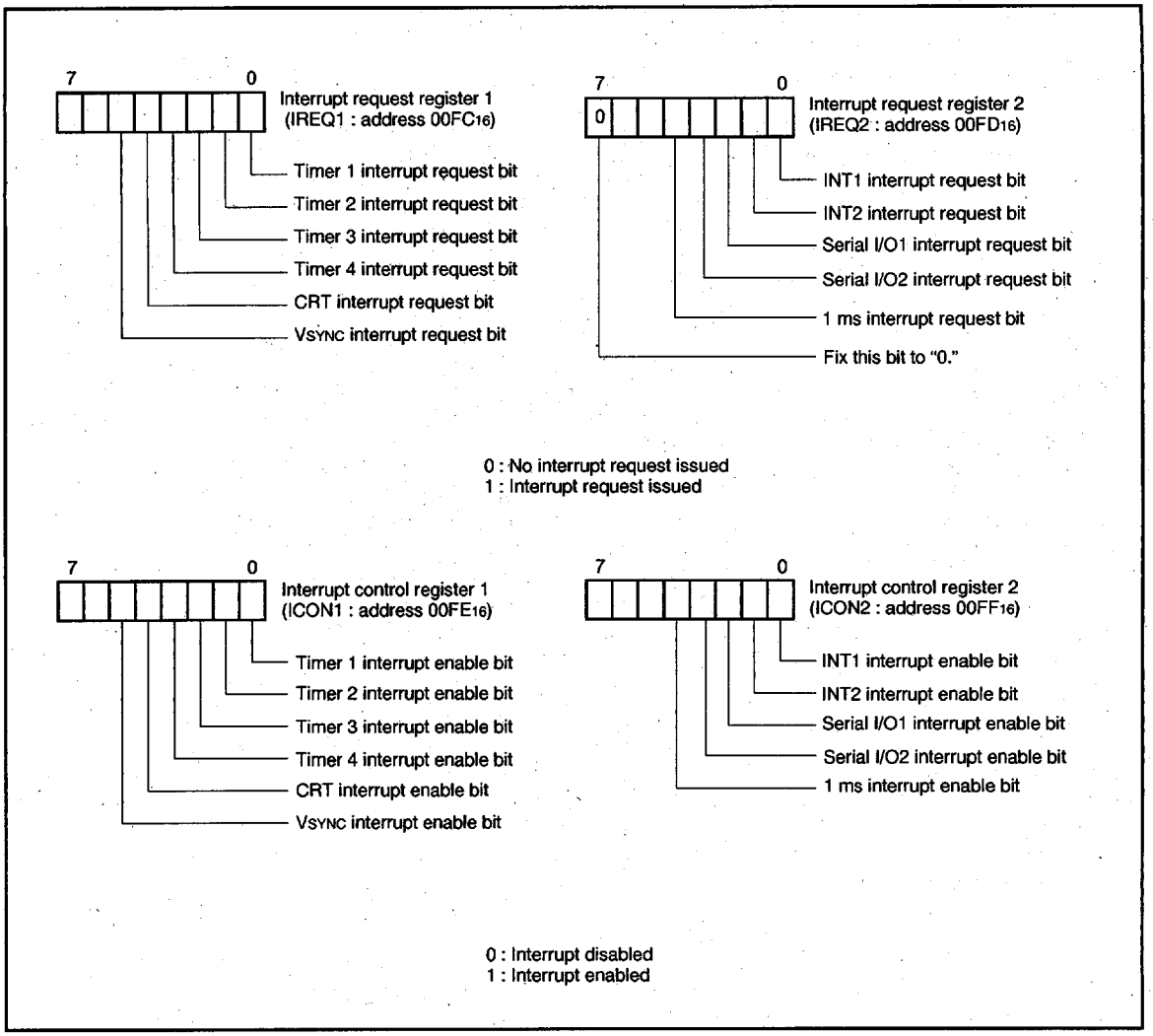


Fig. 7. Structure of interrupt-related registers

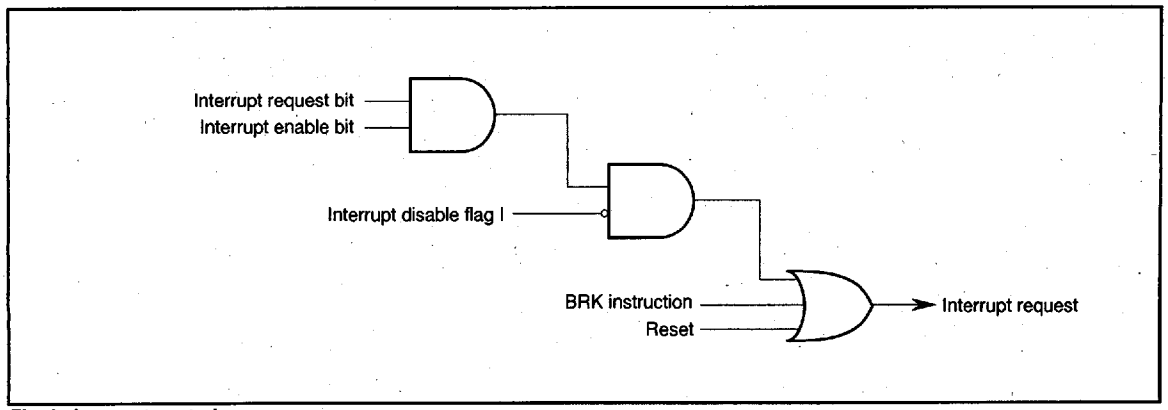


Fig. 8. Interrupt control

TIMERS

The M37204MC-XXXSP has 4 timers: timer 1, timer 2, timer 3, and timer 4. All timers are 8-bit timers with the 8-bit timer latch. The timer block diagram is shown in Figure 10.

All of the timers count down and their divide ratio is 1/(n+1), where n is the value of timer latch. The value is set to a timer at the same time by writing a count value to the corresponding timer latch (addresses $00F0_{16}$ to $00F3_{16}$: timers 1 to 4).

The count value is decremented by 1. The timer interrupt request bit is set to "1" by an timer overflow at the next count pulse after the count value reaches "00_{16}."

(1) Timer 1

Timer 1 can select one of the following count sources:

- f(XIN)/16
- f(XIN)/4096

The count source of timer 1 is selected by setting bit 0 of the timer 12 mode register (address $00F4_{16}$).

Timer 1 interrupt request occurs at timer 1 overflow. And besides, the timer 1 overflow signal divided by 2 (TIM1) is output from the I/P5$_5$/TIM1 pin.

(2) Timer 2

Timer 2 can select one of the following count sources:

- f(XIN)/16
- Timer 1 overflow signal
- External clock from the AD6/P3$_2$/TIM2 pin

The count source of timer 2 is selected by setting bits 4 and 1 of the timer 12 mode register (address $00F4_{16}$). When timer 1 overflow signal is a count source for the timer 2, the timer 1 functions as an 8-bit prescaler.

Timer 2 interrupt request occurs at timer 2 overflow.

(3) Timer 3

Timer 3 can select one of the following count sources:

- f(XIN)/16
- External clock from the P3$_3$/TIM3 pin

The count source of timer 3 is selected by setting bit 0 of the timer 34 mode register 2 (address $00F5_{16}$).

Timer 3 interrupt request occurs at timer 3 overflow.

(4) Timer 4

Timer 4 can select one of the following count sources:

- f(XIN)/16
- f(XIN)/2
- Timer 3 overflow signal

The count source of timer 3 is selected by setting bits 4 and 1 of the timer 34 mode register (address $00F5_{16}$). When timer 3 overflow signal is a count source for the timer 4, the timer 3 functions as an 8-bit prescaler.

Timer 4 interrupt request occurs at timer 4 overflow. And besides, the timer 4 overflow signal is also used as the clock source of special serial I/O.

At reset, timers 3 and 4 are connected by hardware and "FF_{16}" is automatically set in timer 3; "07_{16}" in timer 4. The f(XIN) /16 is selected as the timer 3 count source. The internal reset is released by timer 4 overflow at these state, the internal clock is connected .

At execution of the STP instruction, timers 3 and 4 are connected by hardware and "FF_{16}" is automatically set in timer 3; "07_{16}" in timer 4. However, the f(XIN) /16 is not selected as the timer 3 count source. So set bit 0 of the timer 34 mode register (address $00F5_{16}$) to "0" before the execution of the STP instruction (f(XIN) /16 is selected as the timer 3 count source). The internal STP state is released by timer 4 overflow at these state, the internal clock is connected .

Because of this, the program starts with stable clock.

The structure of timer-related registers is shown in Figure 9.

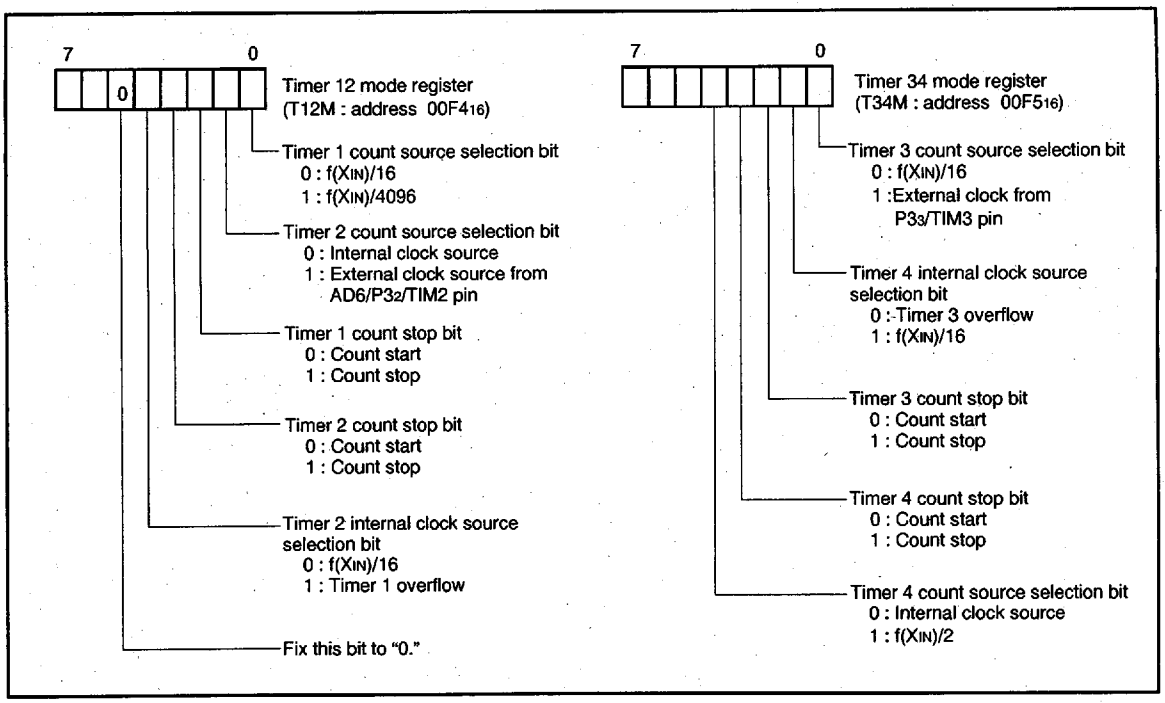
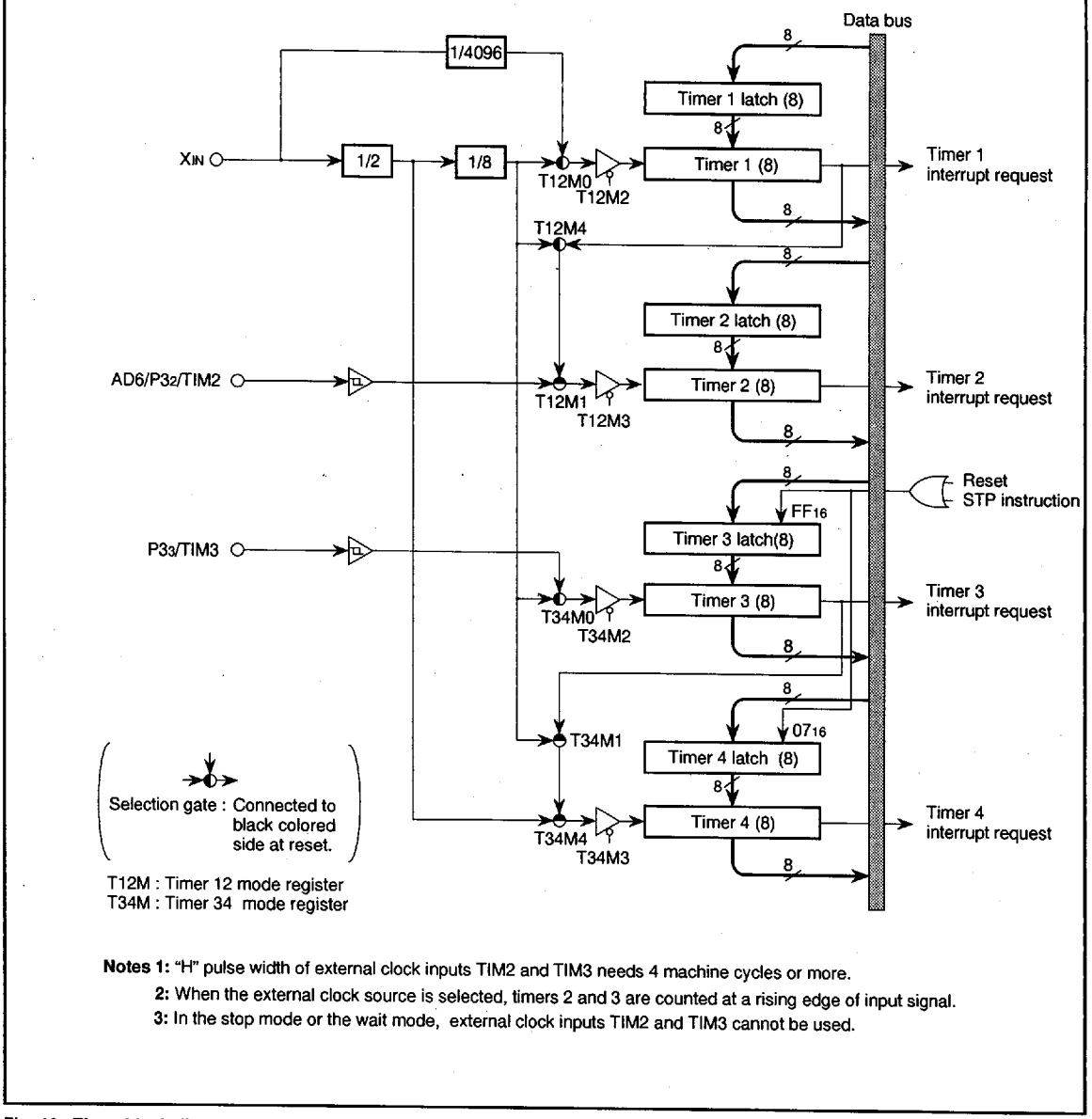


Fig. 9. Structure of timer-related registers



Notes 1: "H" pulse width of external clock inputs TIM2 and TIM3 needs 4 machine cycles or more.
2: When the external clock source is selected, timers 2 and 3 are counted at a rising edge of input signal.
3: In the stop mode or the wait mode, external clock inputs TIM2 and TIM3 cannot be used.

Fig. 10. Timer block diagram

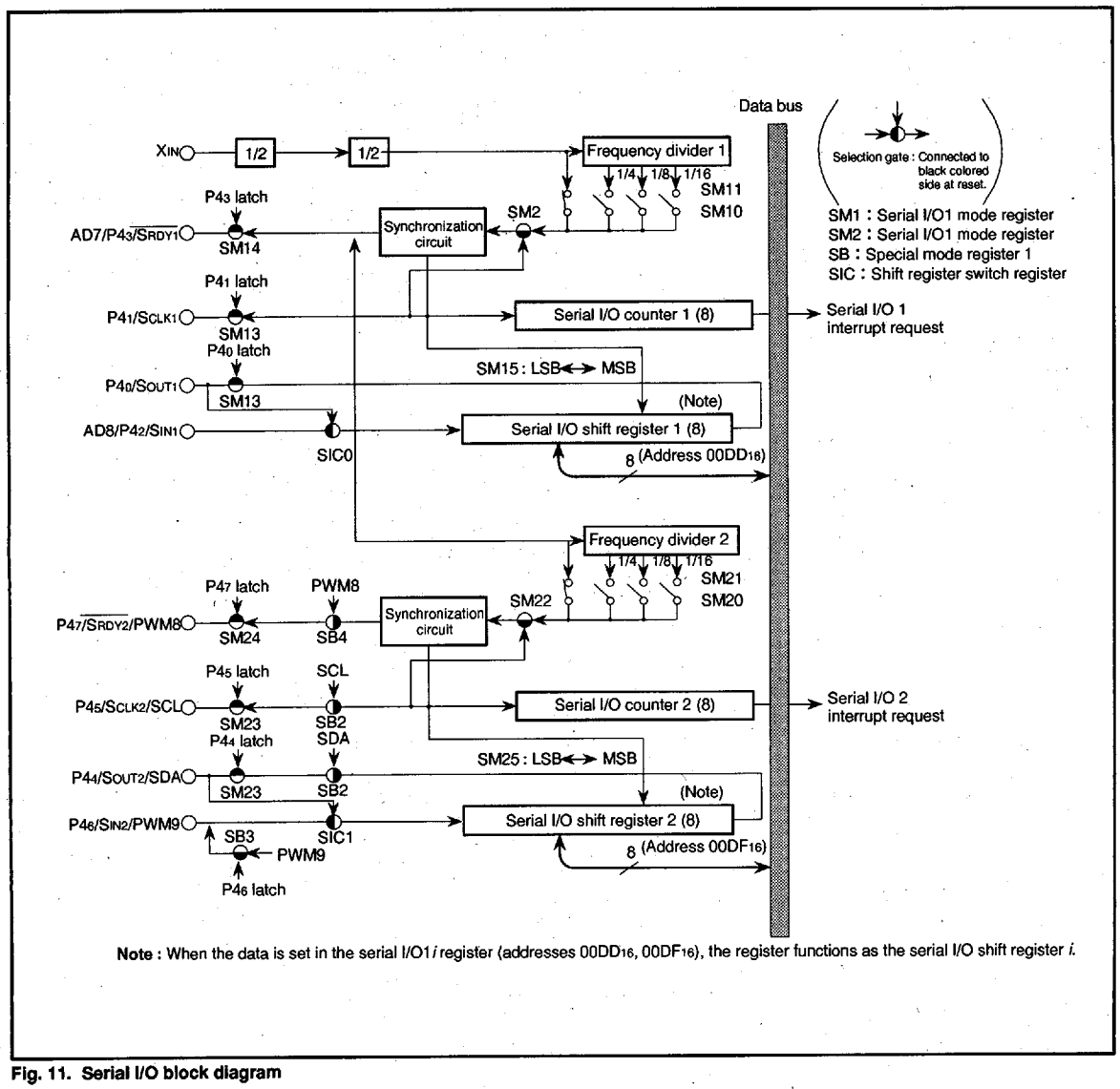
SERIAL I/O

The M37204MC-XXXSP has 2 built-in serial I/Os (serial I/O1, serial I/O2) which can either transmit or receive 8-bit data in the serial clock synchronous mode. Serial I/O1 has the same function as serial I/O2. Serial I/O1 and serial I/O2 are referred as "serial I/O*i*" hereafter.

The serial I/O block diagram is shown in Figure 11. The synchronizing clock I/O pin (SCLK*i*), and data I/O pins (SOUT*i*, SIN*i*), receive enable signal output pin ($\overline{\text{SRDY}i}$) also function as port P4.

Bit 2 of the serial I/O*i* mode register (addresses 00DC16, 00DE16) selects whether the synchronizing clock is supplied internally or externally (from the pins P45/SCLK2/SCL, P41/SCLK1). When an internal clock is selected, bits 1 and 0 select whether f(XIN) is divided by 4, 16, 32, or 64. To use pins for serial I/O, set the corresponding bits of the port P4 direction register (address 00C916) to "0." Also to use the serial I/O2 with internal clock, set bit 1 of the special mode register 1 (address 00DA16) to "1."

The operation of the serial I/O function is described below. The function of the serial I/O differs depending on the clock source; external clock or internal clock.



Note : When the data is set in the serial I/O1 *i* register (addresses 00DD16, 00DF16), the register functions as the serial I/O shift register *i*.

Fig. 11. Serial I/O block diagram

Internal clock—the $\overline{SRDY_i}$ signal goes to "H" during write cycle by writing data into the serial I/O*i* register (addresses 00DD16, 00DF16). After the write cycle, the $\overline{SRDY_i}$ signal goes to "L" (receive enable state). The $\overline{SRDY_i}$ signal goes to "H" at the next falling edge of the transfer clock for the serial I/O*i* register.

The serial I/O counter *i* is set to "7" during write cycle into the serial I/O*i* register (address 00DD16), and transfer clock goes "H" forcibly. At each falling edge of the transfer clock after the write cycle, serial data is output from the S_{OUTi} pin. Transfer direction can be selected by bit 5 of the serial I/O*i* mode register. At each rising edge of the transfer clock, data is input from the S_{INi} pin and data in the serial I/O*i* register is shifted 1 bit.

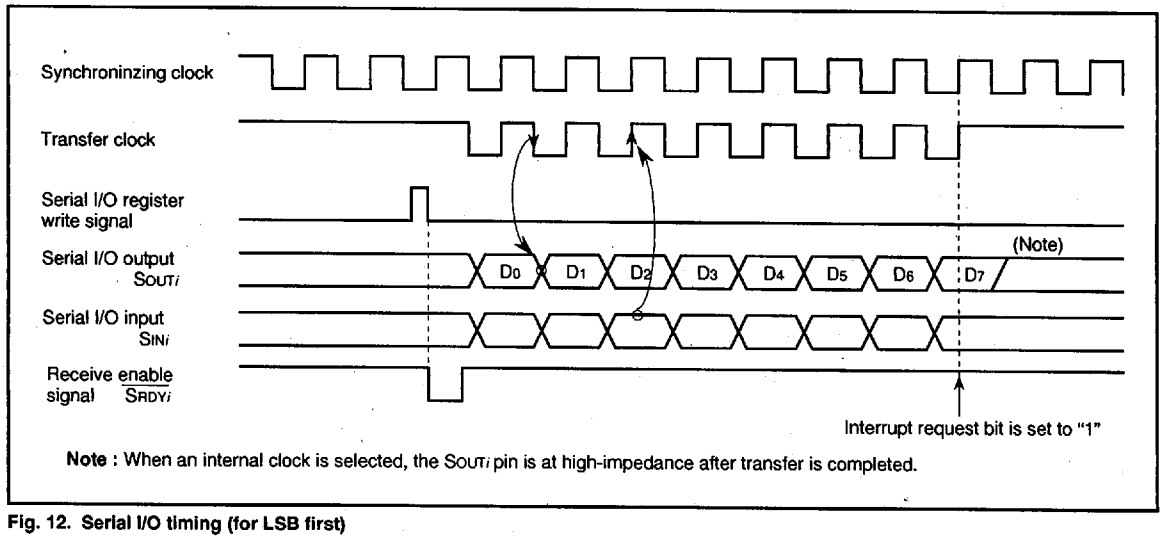
After the transfer clock has counted 8 times, the serial I/O counter becomes "0" and the transfer clock stops at "H." At this time the interrupt request bit is set to "1."

External clock—when an external clock is selected as the clock source, the interrupt request is set to "1" after the transfer clock has counted 8 times. However, transfer operation does not stop, so control the clock externally. Use the external clock of 1 MHz or less with a duty cycle of 50%.

The serial I/O timing is shown in Figure 12. When using an external clock for transfer, the external clock must be held at "H" for initializing the serial I/O counter *i*. When switching between an internal clock and an external clock, do not switch during transfer. Also, be sure to initialize the serial I/O*i* counter after switching.

Notes 1: On programming, note that the serial I/O counter*i* is set by writing to the serial I/O register with the bit managing instructions as SEB and CLB instructions.

2: When an external clock is used as the synchronizing clock, write transmit data to the serial I/O*i* register at "H" of the transfer clock input level.



Note : When an internal clock is selected, the S_{OUTi} pin is at high-impedance after transfer is completed.

Fig. 12. Serial I/O timing (for LSB first)

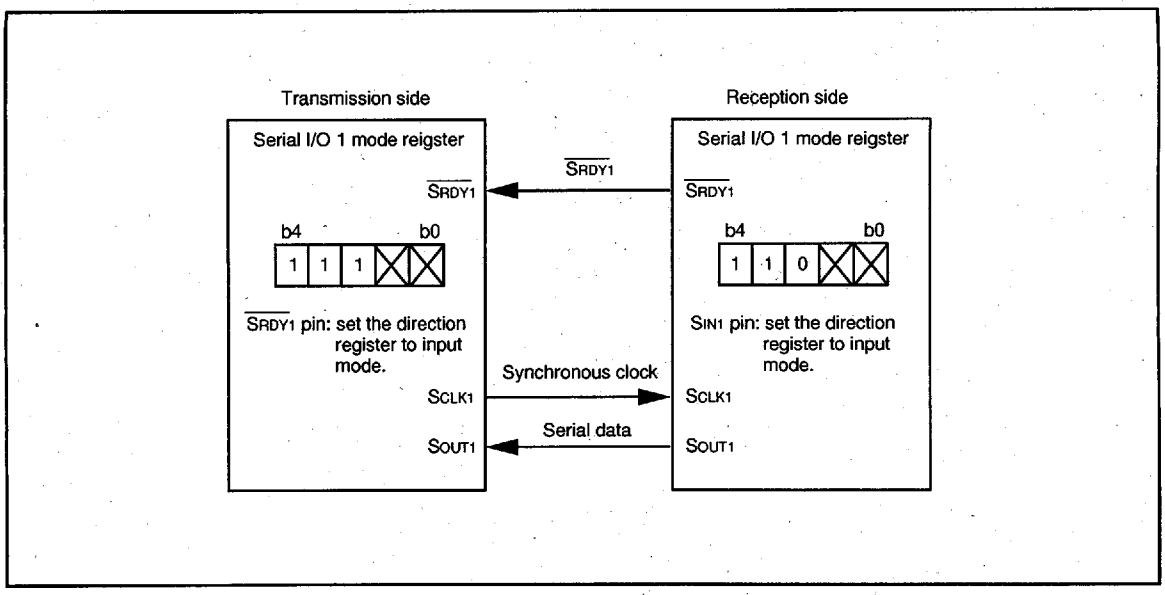


Fig. 13. Structure of serial I/O mode register

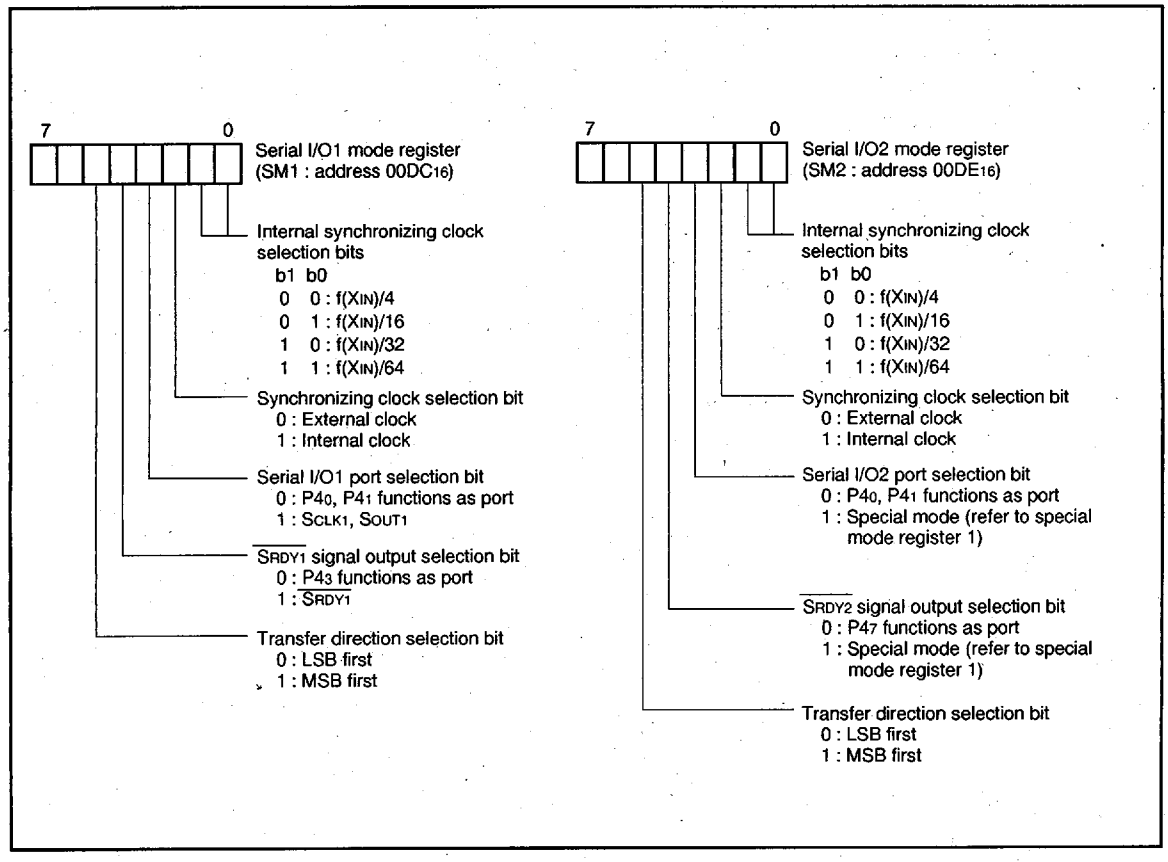


Fig. 14. Structure of serial I/O*i* mode registers

SPECIAL SERIAL I/O

The M37204MC-XXXSP has a special serial I/O circuit that can be reception or transmission of serial data in conformity with I^2C (Inter IC) bus format.

I^2C bus is a two line directional serial bus developed by Philips to transfer and control data among internal ICs of a machinery. Ports of special serial I/O are also used as those of serial I/O2. So special I/O cannnot be used when using serial I/O2.

The M37204MC-XXXSP's special serial I/O is not included the clock synchronization function and the arbitration detectable function at multi-master.

Figure 15 shows the special serial I/O block diagram. Operations of master transmission and master reception with special serial I/O are explained in the following:

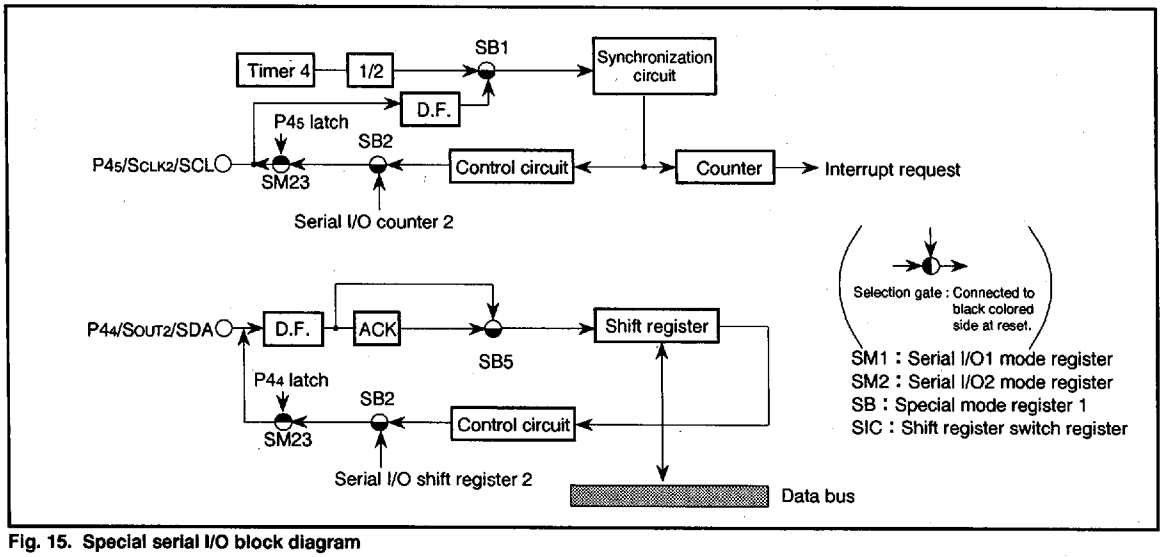


Fig. 15. Special serial I/O block diagram

(1) Master transmission example

① To generate an interrupt at the end of transmission, set bit 7 of the special mode register 2 (address $00DB_{16}$) to "1" (select the special serial I/O interrupt).

② Then set bit 3 of the interrupt control register 2 (address $00FF_{16}$) to "1" (enable the serial I/O2 interrupt). Also, set the interrupt disable flag I to "0" by the CLI instruction.

③ The output signals SDA and SCL at the master transmission are output form ports $P4_4$ and $P4_5$. Set all bits (bits 4 and 5) corresponding to $P4_4$ and $P4_5$ of the port P4 register (address $00C8_{16}$) and the port P4 direction register (address $00C9_{16}$) to "1."

④ Set the transmission clock. The transmission clock uses the overflow signal of timer 4. Set appropriate value in timer 4 and the timer mode register 2 (For instance, if f (X_{IN})/2 is selected as the clock source of timer 4 and 4_{16} is set in timer 4, the master transmission clock frequency is 25 kHz at f (X_{IN}) = 4 MHz).

⑤ Set contents value of the special mode register 2 (address $00DB_{16}$). (Ordinary, the value is "83_{16}")

⑥ Set bit 3 of the serial I/O2 mode register (address $00DE_{16}$). After that set the special mode register 1 (address $00DE_{16}$). Figure 17 shows the structure of special mode registers 1 and 2.

⑦ Write the next data to be transmitted in the special serial I/O register (address $00D9_{16}$). Immediately after this, set "0" to bits 0 and 1 of the serial mode register 2 to make both SDA and SCL output to "L." This is for arbitration. The start signal has been completed. The hardware automatically sends out data of 9-clock cycle. The 9th clock is for ACK reception and output level becomes "H" at this clock. If other master outputs the start signal to transmit data simultaneously with this 9th clock, it is not detected as an arbitration lost.

When the ACK bit has been transmitted , bit 3 of the interrupt request register 2 is set to "1" (occurrence of interrupt request), notifying the end of data transmission.

⑧ To transmit data successively, write data to be sent to the special serial I/O register, and enable an interrupt again. By repeating this procedure, unlimited number of bytes can be transmitted.

⑨ To terminate data transfer set bits 0 and 1 of the special mode register 2 to "0."

⑩ Set SCL (bit 1) to "1."

⑪ Then SDA (bit 0) to "1." This procedure transmits the stop signal.

Figure 16 shows master transmission timing explained above.

(2) Master reception example

Master reception is carried out in the interrupt processing routine after master transmission. For master transmission and interrupt occurrence thereafter, refer to the preceding section (1) Master transmission (the process until ⑦ in Figure 16).

⑫ In the interrupt routine, set master reception ACK provided (26_{16}) in the special mode register 1 (address $00DA_{16}$).

⑬ Set dummy data "FF_{16}" in the special serial I/O register (address $00D9_{16}$). This sets data line SDA to "H" to receive data for 8 clocks. Then, transmit "L" to data line SDA for receiving ACK. In the ACK provided mode, the above ACK is automatically sent out.

⑭ Repeat the above receiving operation for a necessary number of times. Then return to the master transmission mode and transmit the stop signal by the same procedure for the master transmission (the process from ⑨ to ⑪ in Figure 16).

Figure 17 shows the master reception timing.

(3) Wait function

The wait function 1 holds the SCL line at "L" after the 8th clock falls in special mode. The wait function 2 holds the SCL line at "L" after the 9th clock falls in the same way.

The wait functions can be released by setting the corresponding bits 5 and 6 of the special mode register 2 to "1."

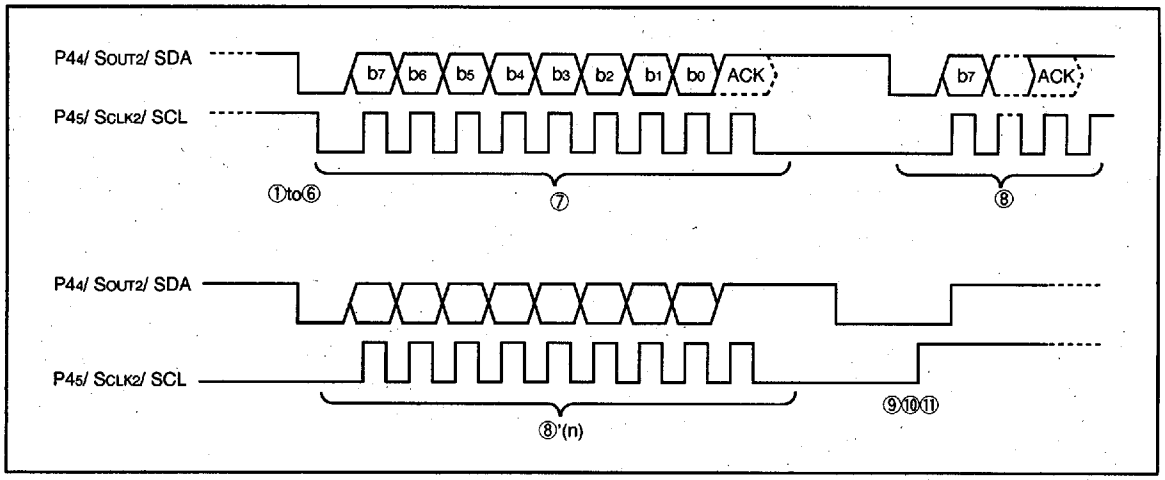


Fig. 16. Timing at master transmission

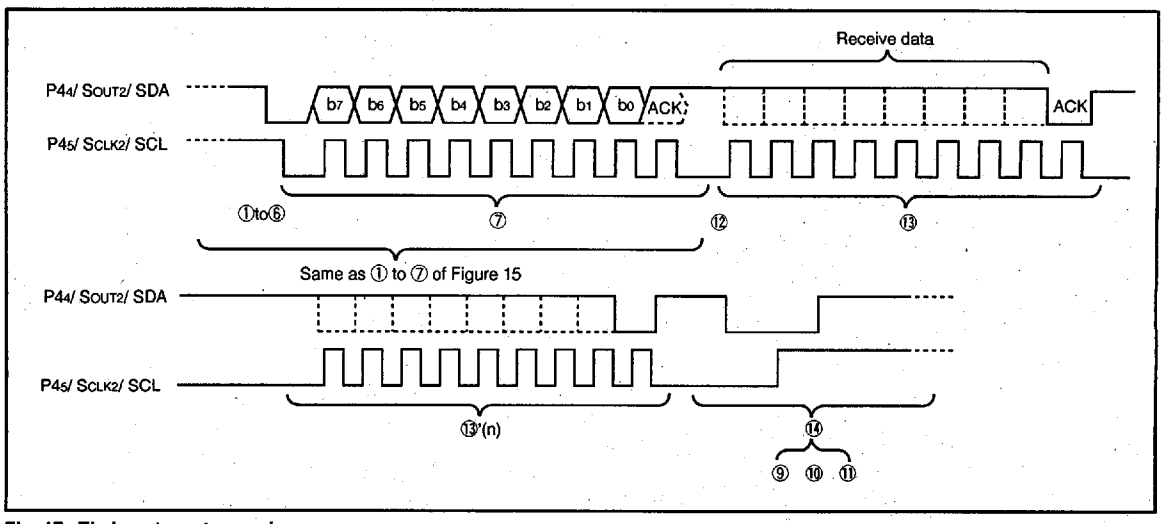


Fig. 17. Timing at master receive

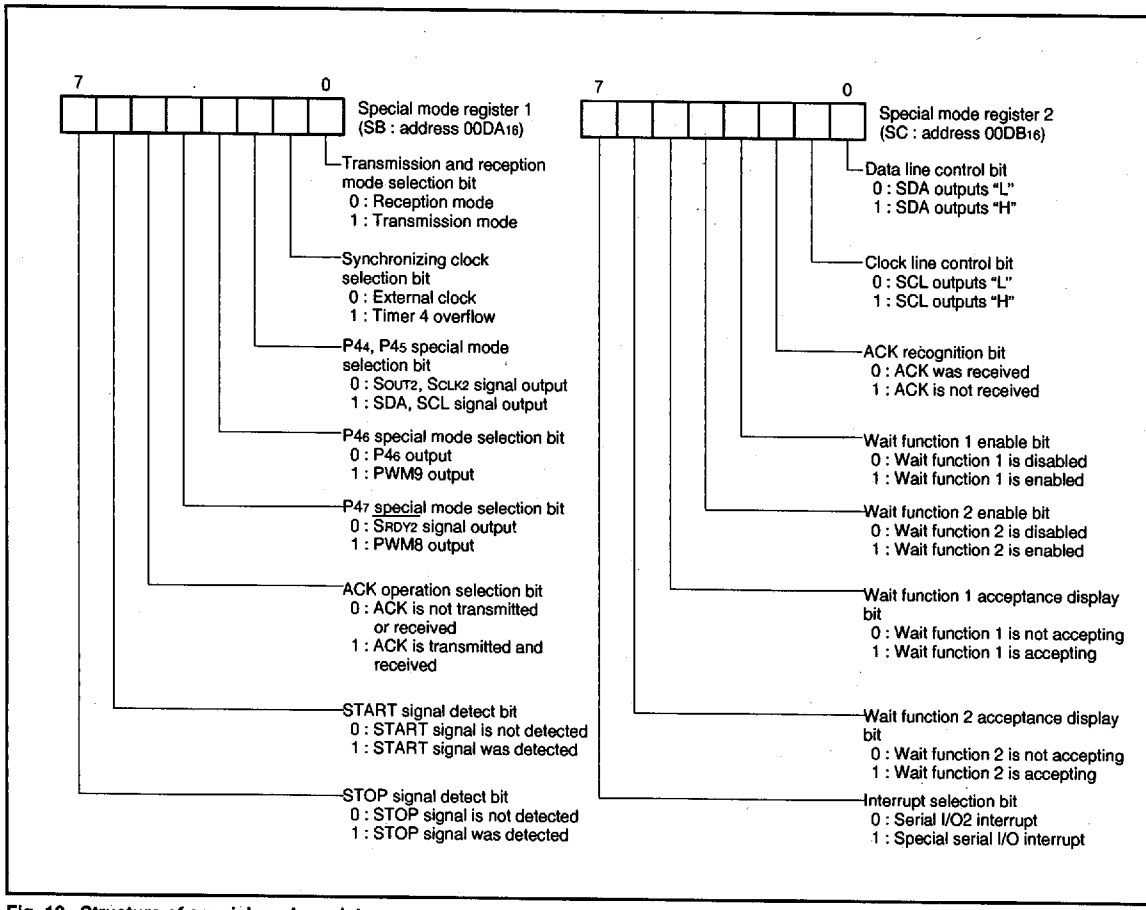


Fig. 18. Structure of special mode registers

(1) Serial I/O Common Transmission/Reception Mode

By writing "1" to bit 0 of the serial I/O control register, signals SIN and SOUT are switched internally to be able to transmit or receive the serial data.

Figure 20 shows signals on serial I/O common transmission/reception mode.

Note : When receiving the serial data after writing "FF16" to the serial I/O register.

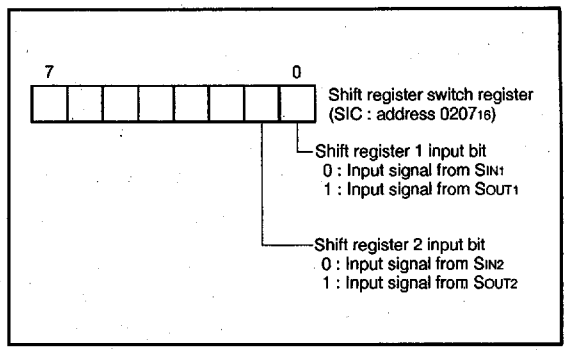


Fig. 19. Structure of shift register switch register

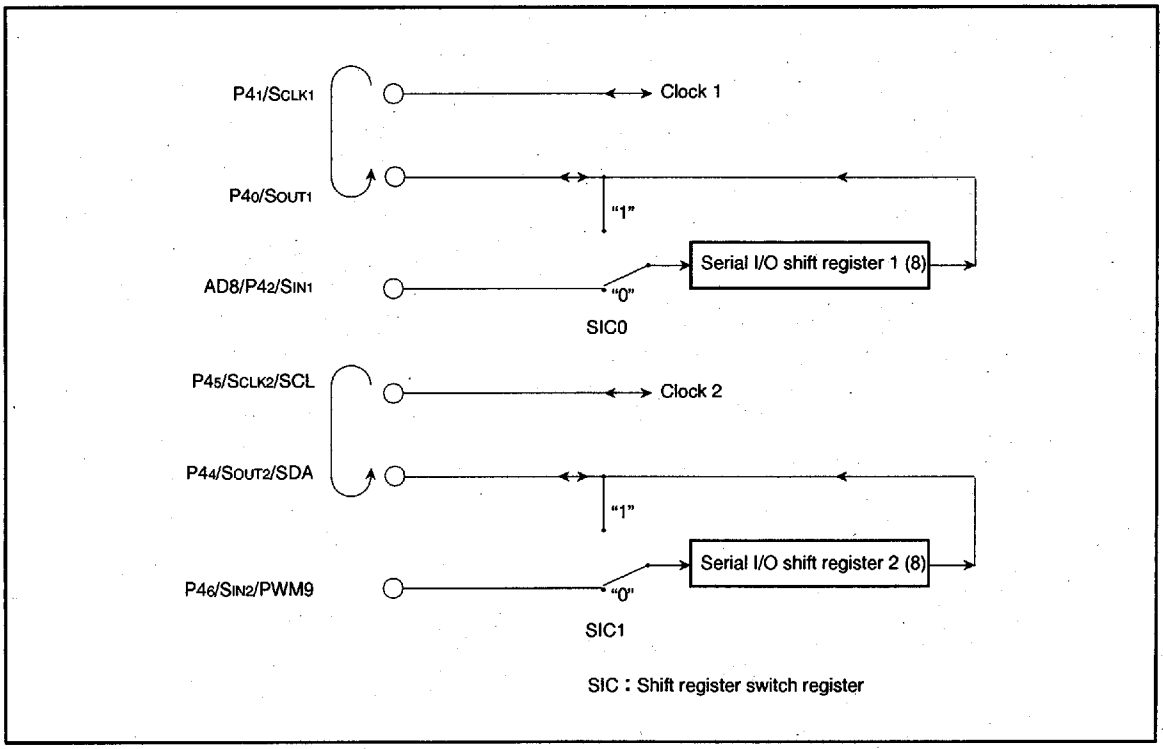


Fig. 20. Signals on serial I/O common transmission/reception mode

PWM OUTPUT FUNCTION

The M37204MC-XXXSP is equipped with a 14-bit PWM (DA) and ten 8-bit PWMs (PWM0–PWM9). DA has a 14-bit resolution with the minimum resolution bit width of 500 ns (for f(XIN) = 4 MHz) and a repeat period of 8192 μs. PWM0–PWM9 have the same circuit structure and an 8-bit resolution with minimum resolution bit width of 8 μs (for f(XIN) = 4 MHz) and repeat period of 2048 μs.

Figure 21 shows the PWM block diagram. The PWM timing generating circuit applies individual control signals to PWM0–PWM9 using f(XIN) divided by 2 as a reference signal.

(1) Data Setting

When outputting DA, first set the high-order 8 bits to the DA-H register (address 00CE16), then the low-order 6 bits to the DA-L register (address 00CF16). When outputting PWM0–PWM9, set 8-bit output data in the PWMi register (i means 0 to 9; addresses 00D016 to 00D416, 00F616 to 00FA16).

(2) Transmitting Data from Register to PWM circuit

The data written to the 8-bit PWM register is transferred to the PWM latch in each 8-bit PWM cycle period. For 14-bit PWM, the data transferred in the next high-order 8-bit period after the write. The signals output to the PWM pins correspond to the contents of these latches. When data in each PWM register is read, data in these latches has already been read allowing the data output by the PWM to be confirmed. However, bit 7 of the DA-L register indicated the completion of the data transfer from the DA register to the DA latch. When bit 7 if "0," the transfer has been completed. When bit 7 is "1," the transfer has not yet begun.

(3) Operating of 8-bit PWM

The following is the explanation about PWM operation.

At first, set the bit 0 of PWM output control register 1 (address 00D516) to "0" (at reset, bit 0 is already set to "0" automatically), so that the PWM count source is supplied.

PWM0–PWM7 are also used as pins P60–P67, PWM8, PWM9 are also used as ports pins P47, P46, respectively. For PWM0–PWM7, set the corresponding bits of the ports P4 or P6 direction register to "1" (output mode). And select each output polarity by bit 3 of the PWM output control register 2(address 00D616). Then, for PWM0–PWM5, set bits 2 to 7 of the PWM output control register 1 to "1" (PWM output). For PWM6 and PWM7, set bits 0 and 1 of the PWM output control register 2 to "1." For PWM8 and PWM9, set bits 3 and 4 of the special mode register 1 and bit 4 of the serial I/O2 mode register to "1."

The PWM waveform is output from the PWM output pins by setting these registers.

Figure 22 shows the 8-bit PWM timing. One cycle (T) is composed of 256 (2^8) segments. The 8 kinds of pulses relative to the weight of each bit (bits 0 to 7) are output inside the circuit during 1 cycle. Refer to Figure 22 (a). The 8-bit PWM outputs waveform which is the logical sum (OR) of pulses corresponding to the contents of bits 0 to 7 of the 8-bit PWM register. Several examples are shown in Figure 22 (b). 256 kinds of output ("H" level area: 0/256 to 255/256) are selected by changing the contents of the PWM register. A length of entirely "H" output cannot be output, i.e. 256/256.

(4) Operating of 14-bit PWM

As with 8-bit PWM, set the bit 0 of the PWM output control register 1 (address 00D516) to "0" (at reset, bit 0 is already set to "0" automatically), so that the PWM count source is supplied. Next, select the output polarity by bit 2 of the PWM output control register 2 (address 00D616). Then, the 14-bit PWM outputs from the D-A output pin by setting bit 1 of the PWM output control register 1 to "0" (at reset, this bit already set to "0" automatically) to select the DA output.

The output example of the 14-bit PWM is shown in Figure 23.

The 14-bit PWM divides the data of the DA latch into the low-order 6 bits and the high-order 8 bits.

The fundamental waveform is determined with the high-order 8-bit data "DH." A "H" level area with a length τ × DH("H" level area of fundamental waveform) is output every short area of "t" = 256τ = 128 μs (τ is the minimum resolution bit width of 0.5 μs). The "H" level area increase interval (tm) is determined with the low-order 6-bit data "DL." The "H" level are of smaller intervals "tm" shown in Table 2 is longer by τ than that of other smaller intervals in PWM repeat period "T" = 64t. Thus, a rectangular waveform with the different "H" width is output from the D-A pin. Accordingly, the PWM output changes by τ unit pulse width by changing the contents of the DA-H and DA-L registers. A length of entirely "H" output cannot be output, i. e. 256/256.

(5) Output after Reset

At reset, the output of ports P60–P67, P46 and P47 are in the high-impedance state, and the contents of the PWM register and the PWM circuit are undefined. Note that after reset, the PWM output is undefined until setting the PWM register.

Table 2. Relation between the low-order 6-bit data and high-level area increase interval

Low-order 6 bits of data	Area longer by τ than that of other tm (m = 0 to 63)
000000 (LSB)	Nothing
000001	m = 32
000010	m = 16, 48
000100	m = 8, 24, 40, 56
001000	m = 4, 12, 20, 28, 36, 44, 52, 60
010000	m = 2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62
100000	m = 1, 3, 5, 7, ... 57, 59, 61, 63

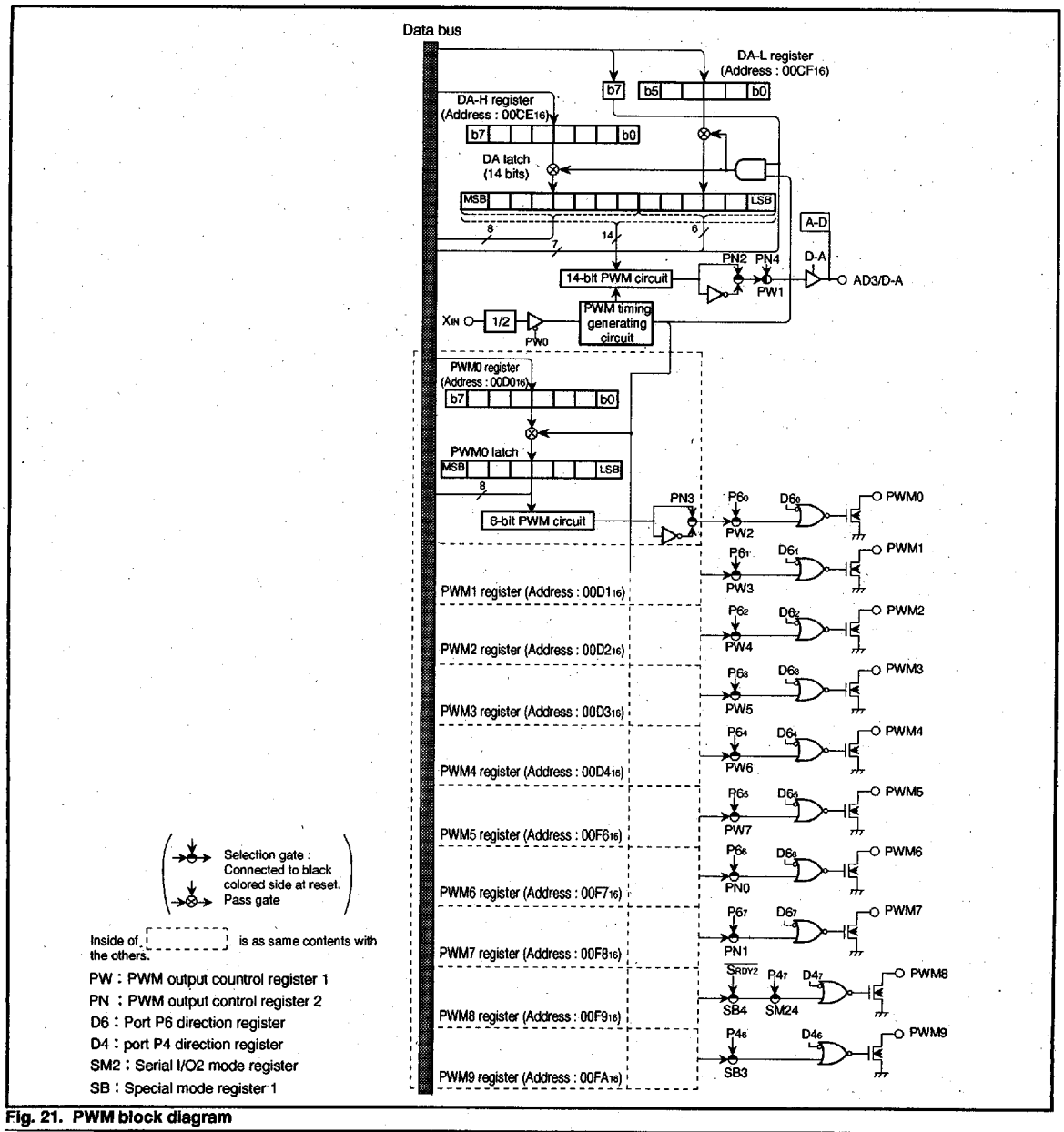


Fig. 21. PWM block diagram

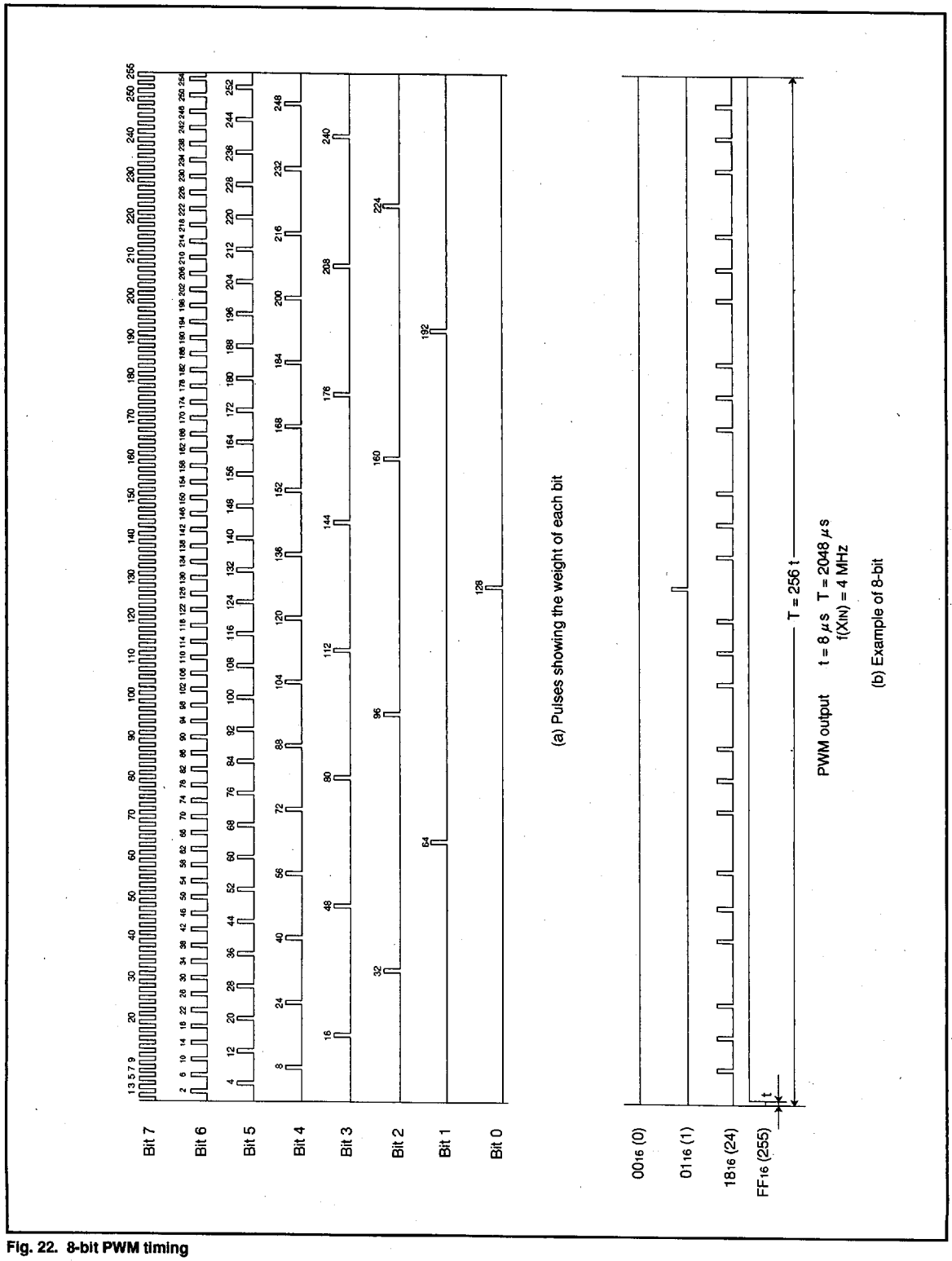


Fig. 22. 8-bit PWM timing

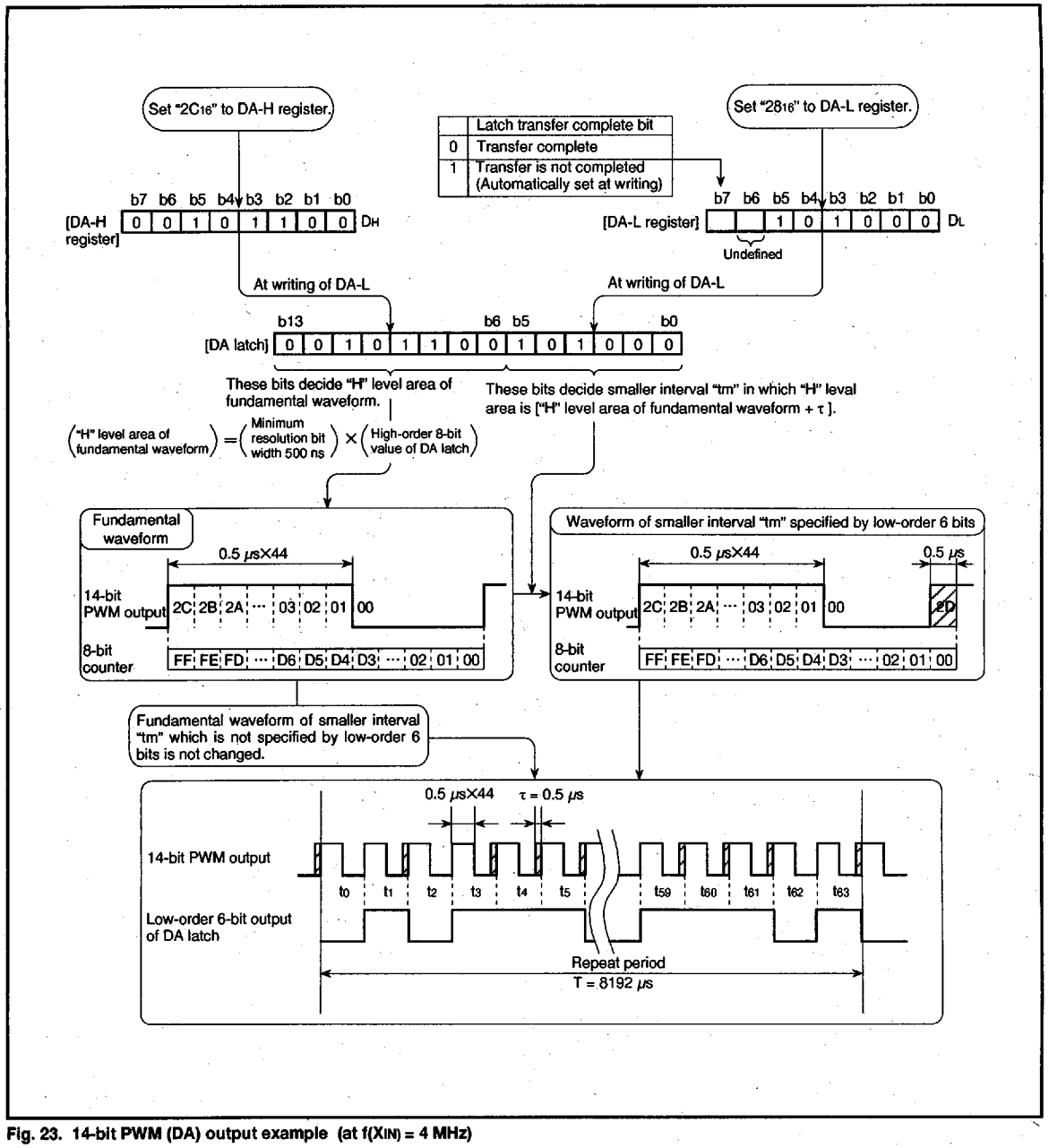


Fig. 23. 14-bit PWM (DA) output example (at f(XIN) = 4 MHz)

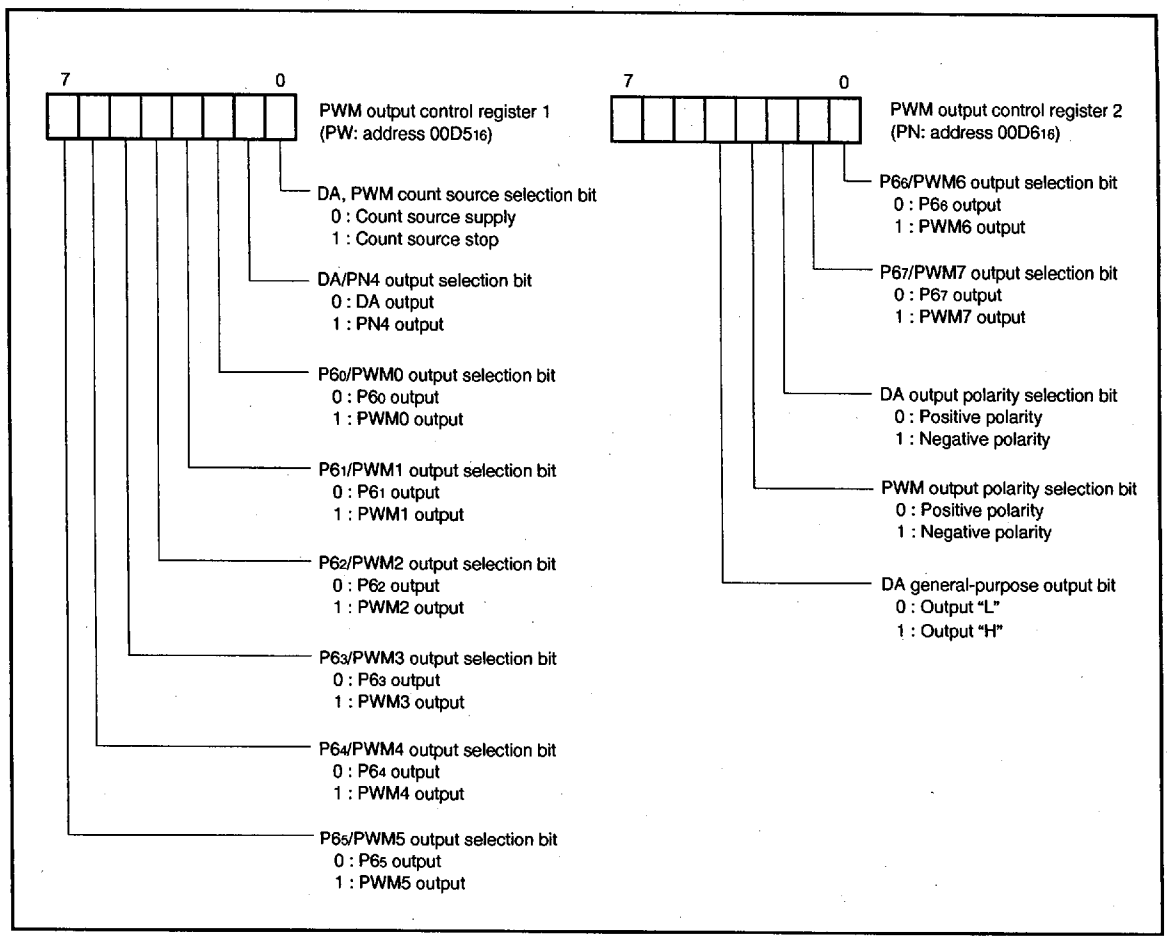


Fig. 24. Structure of PWM-related registers

A-D COMPARATOR

A-D comparator consists of 6-bit D-A converter and comparator. A-D comparator block diagram is shown in Figure 25.

The reference voltage "V_{ref}" for D-A conversion is set by bits 0 to 5 of the A-D control register 2 (address $020A_{16}$).

The comparison result of the analog input voltage and the reference voltage "V_{ref}" is stored in bit 4 of the A-D control register 1 (address $00EF_{16}$).

For A-D comparison, set "0" to corresponding bits of the direction register to use ports as analog input pins. Write the data for select of analog input pins to bits 0 to 2 of the A-D control register 1 and write the digital value corresponding to V_{ref} to be compared to the bits 0 to 5 of the A-D control register 2. The voltage comparison starts by writing to the A-D control register 2, and it is completed after 16 machine cycles (NOP instruction × 8).

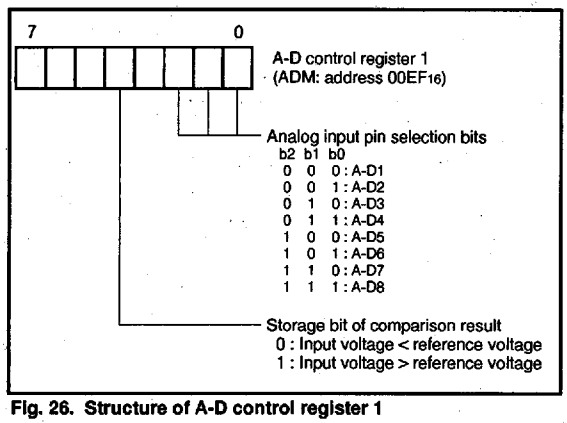


Fig. 26. Structure of A-D control register 1

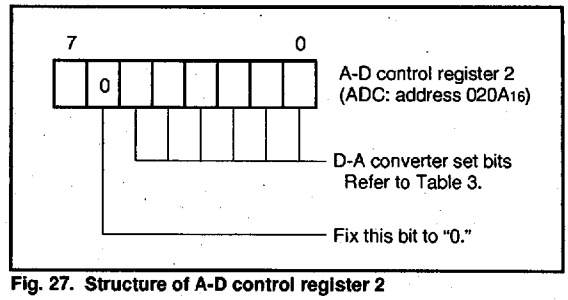


Fig. 27. Structure of A-D control register 2

Table 3. Relation between contents of A-D control register 2 and reference voltage "V_{ref}"

A-D control register 2						Reference voltage "V_{ref}"
Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0	0	0	0	0	0	1/128 Vcc
0	0	0	0	0	1	3/128 Vcc
0	0	0	0	1	0	5/128 Vcc
⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	0	1	123/128 Vcc
1	1	1	1	1	0	125/128 Vcc
1	1	1	1	1	1	127/128 Vcc

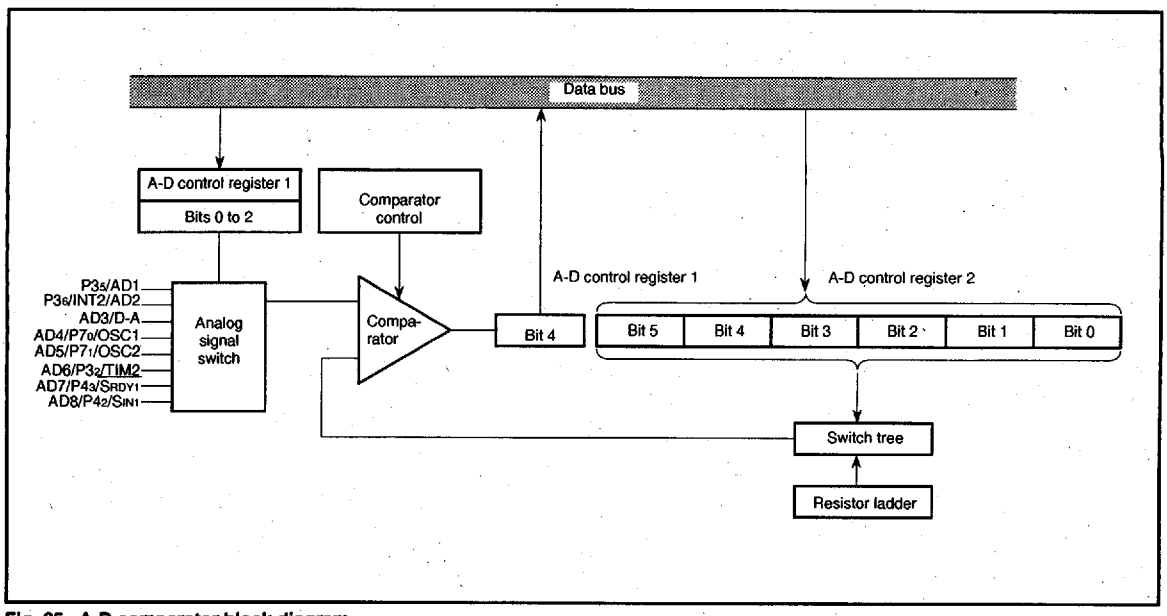


Fig. 25. A-D comparator block diagram

CRT DISPLAY FUNCTIONS

(1) Outline of CRT Display Functions

Table 4 outlines the CRT display functions of the M37204MC-XXXSP.The M37204MC-XXXSP incorporates a CRT display control circuit of 24 characters × 3 lines. CRT display is controlled by the CRT control register. Up to 256 kinds of characters can be displayed. The colors can be specified for each character and up to 4 kinds of colors can be displayed on one screen. A combination of up to 15 colors can be obtained by using each output signal (R, G, B and I). Characters are displayed in a 12 × 16 dots configuration to obtain smooth character patterns (refer to Figure 28).

The following shows the procedure how to display characters on the CRT screen.

① Write the display character code in the display RAM.
② Specify the display color by using the color register.
③ Write the color register in which the display color is set in the display RAM.
④ Specify the vertical position by using the vertical position register.
⑤ Specify the character size by using the character size register.
⑥ Specify the horizontal position by using the horizontal position register.
⑦ Write the display enable bit to the designated block display flag of the CRT control register. When this is done, the CRT display starts according to the input of the VSYNC signal.

The CRT display circuit has an extended display mode. This mode allows multiple lines (4 lines or more) to be displayed on the screen by interrupting the display each time one line is displayed and rewriting data in the block for which display is terminated by software.

Figure 29 shows the structure of the CRT display control register. Figure 30 shows the block diagram of the CRT display control circuit.

Table 4. Outline of CRT display functions

Parameter		Functions
Number of display characters		24 characters × 3 lines
Dot structure		12 × 16 dots (refer to Figure 27)
Kinds of characters		256 kinds
Kinds of character sizes		4 kinds
Color	Kinds of colors	1 screen : 4 kinds, maximum 15 kinds
	Coloring unit	A character
Display expansion		Possible (multiline display)
Raster coloring		Possible (maximum 15 kinds)
Character background coloring		Possible (A character unit, 1 screen : 1 kinds, maximum 7 kinds)

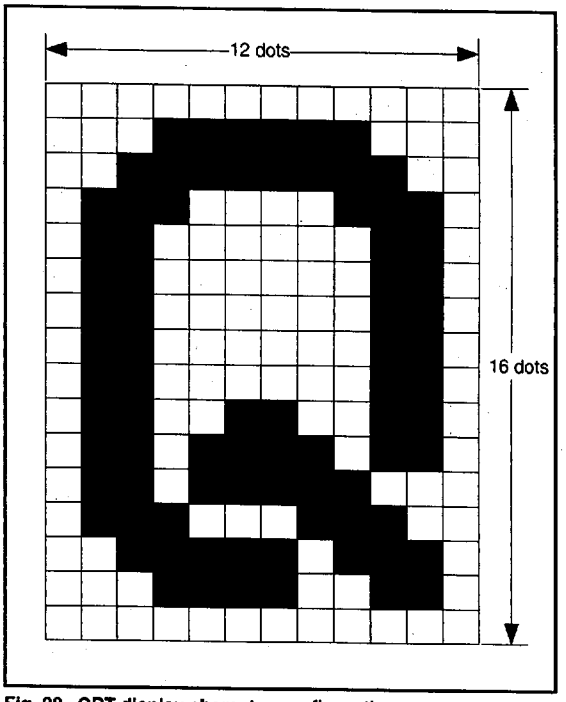


Fig. 28. CRT display character configuration

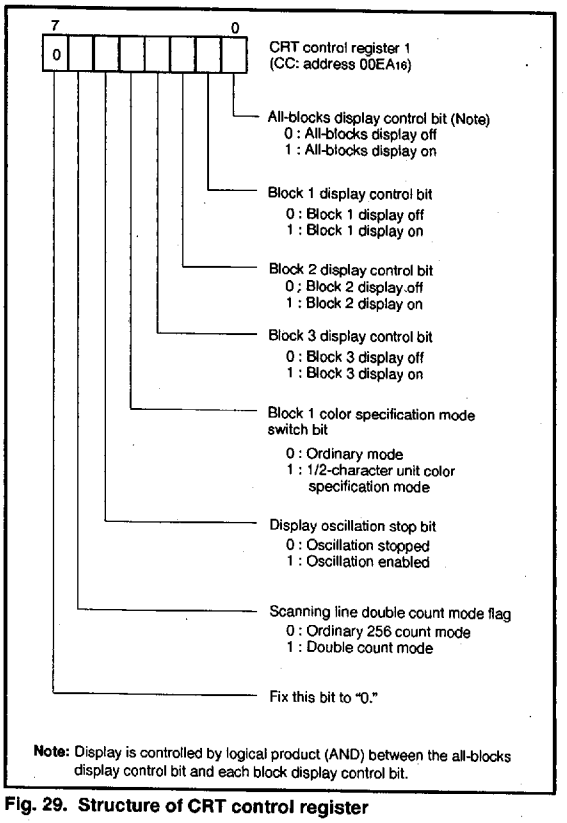


Fig. 29. Structure of CRT control register

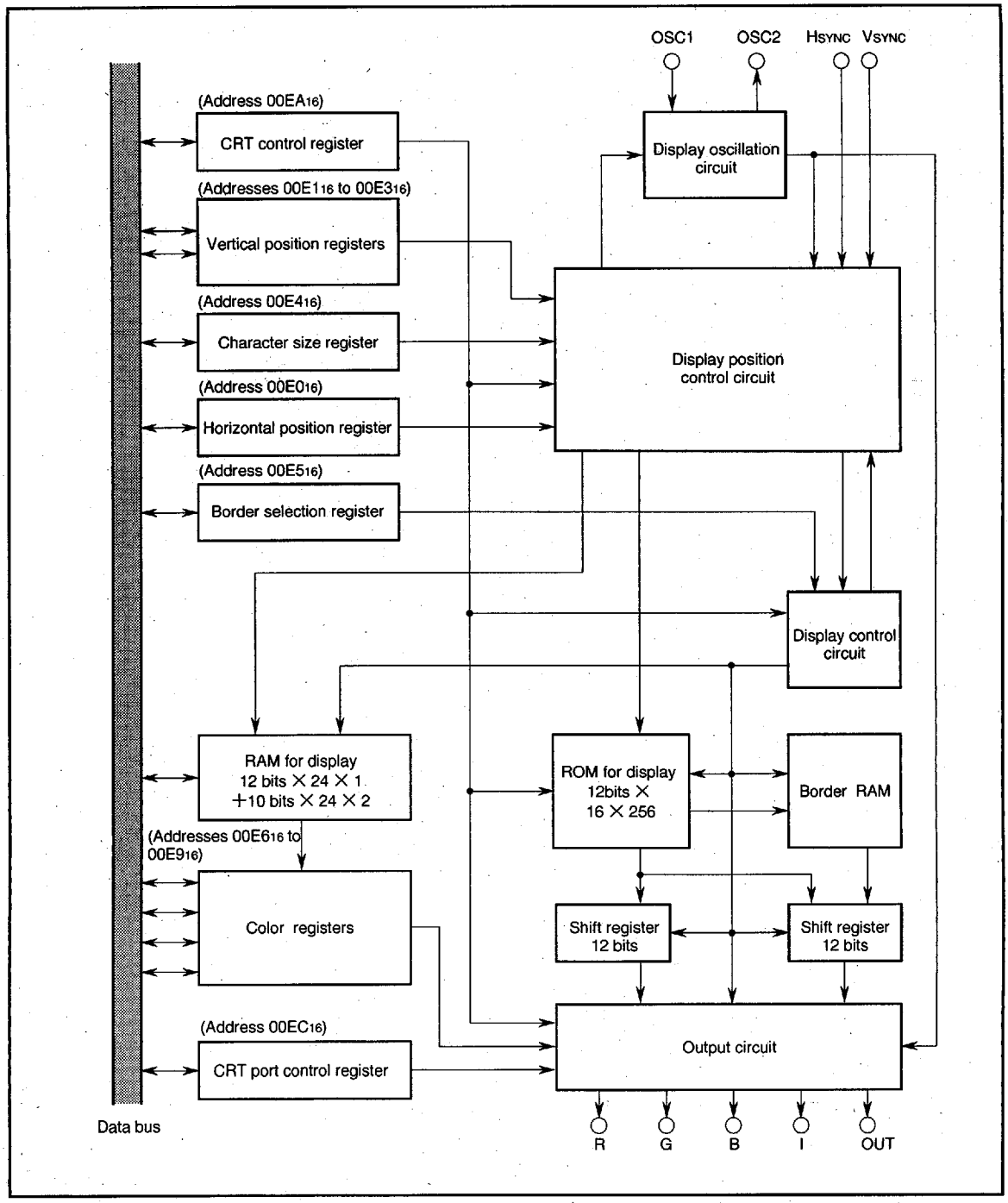


Fig. 30. Block diagram of CRT display control circuit

(2) Display Position

The display positions of characters are specified in units called a "block." There are 3 blocks, blocks 1 to 3. Up to 24 characters can be displayed in each block (refer to (4) Memory for Display).

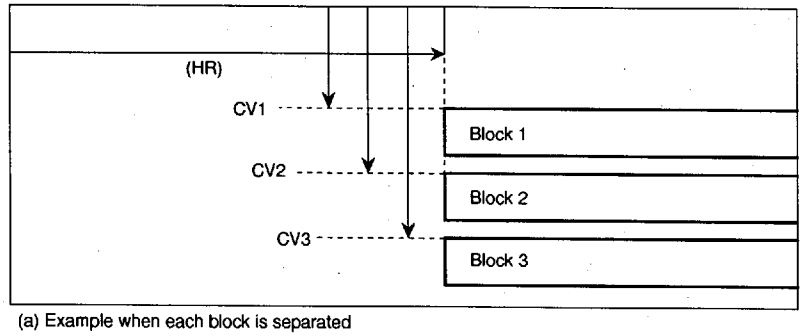
The display position of each block can be set in both horizontal and vertical directions by software.

The display position in the horizontal direction can be selected for all blocks in common from 64-step display positions in units of 4Tc (Tc = oscillating cycle for display).

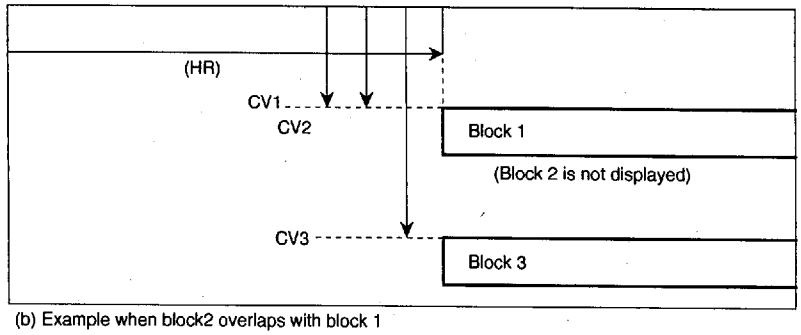
The display position in the vertical direction for each block can be selected from 128-step display positions in units of 4 scanning lines.

Block 2 is displayed after the display of block 1 is completed (refer to Figure 31 (a)). Accordingly, if the display of block 2 starts during the display of block 1, only block 1 is displayed. Similarly, when multiline display, block 1 is displayed after the display of block 2 is completed (refer to Figure 31 (b)).

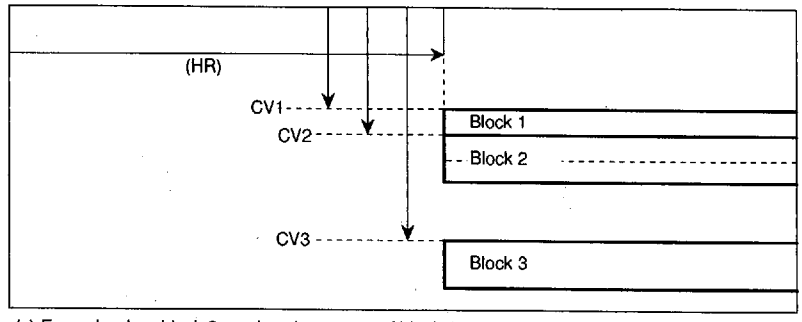
The vertical position can be specified from 128-step positions (4 scanning lines per a step) for each block by setting values "00$_{16}$" to "7F$_{16}$" to bits 0 to 6 in the vertical position register (addresses 00E1$_{16}$ to 00E3$_{16}$). Figure 33 shows the structure of the vertical position register.



(a) Example when each block is separated



(b) Example when block2 overlaps with block 1

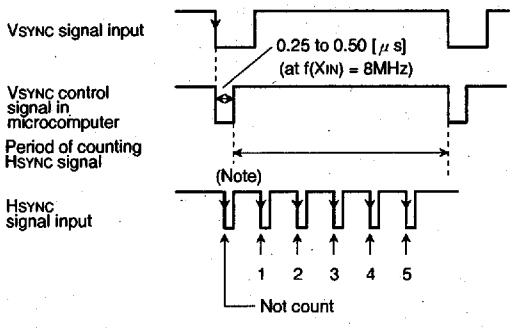


(c) Example when block 2 overlaps in process of block 1

Fig. 31. Display position

The display position in the vertical direction is determined by counting the horizontal sync signal (HSYNC). At this time, it starts to count the rising edge (falling edge) of HSYNC signal from after about 1 machine cycle of rising edge (falling edge) of VSYNC signal. So interval from rising edge (falling edge) of VSYNC signal to rising edge (falling edge) of HSYNC signal needs enough time (2 machine cycles or more) for avoiding jitter. The polarity of HSYNC and VSYNC signals can select with the CRT port control register (address 00EC16). For details. refer to (12) CRT Output Pin Control.

Note: When bits 0 and 1 of the CRT port control register (address 00EC16) are set to "1" (negative polarity), the vertical position is determined by counting falling edge of HSYNC signal after rising edge of VSYNC control signal in the microcomputer (refer to Figure 32).



When bits 0 and 1 of the CRT port control register (address 00EC16) are set to "1" (negative polarity)

Note: Do not generate falling edge of HSYNC signal near rising edge of VSYNC control signal in microcomputer to avoid jitter.

Fig. 32. Supplement explanation for display position

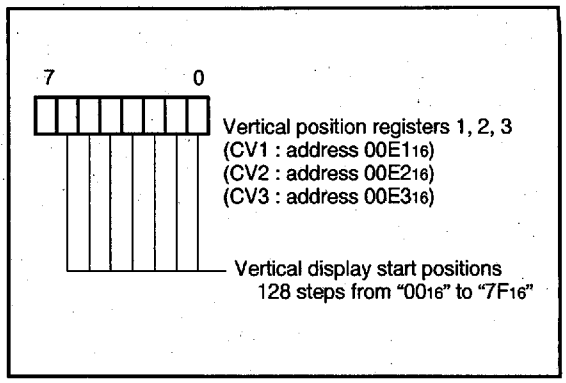


Fig. 33. Structure of vertical position register

The horizontal position is common to all blocks, and can be set in 64 steps (where 1 step is 4Tc, Tc being the display oscillation period) as values "0016" to "3F16" in bits 0 to 5 of the horizontal position register (address 00E016). The structure of the horizontal position register is shown in Figure 34.

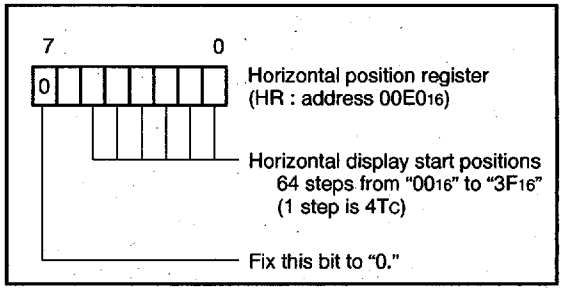
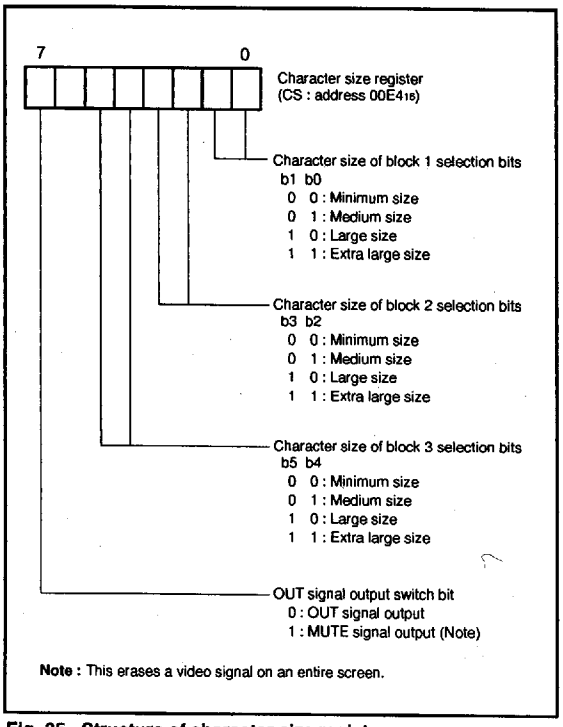


Fig. 34. Structure of horizontal position register

(3) Character Size

The size of characters to be displayed can be from 4 sizes for each block. Use the character size register (address 00E4₁₆) to set a character size. The character size of block 1 can be specified by using bits 0 and 1 of the character size register; the character size of block 2 can be specified by using bits 2 and 3; that in block 3 can be specified by using bits 4 and 5. Figure 35 shows the structure of the character size register.

The character size can be selected from 4 sizes: minimum size, medium size, large size and extra large size. Each character size is determined by the number of scanning lines in the height (vertical) direction and the oscillating cycle for display (Tc) in the width (horizontal) direction. The minimum size consists of [1 scanning line] × [1Tc]; the medium size consists of [2 scanning lines] × [2Tc]; the large size consists of [3 scanning lines] × [3Tc]; and the extra large size consists of [4 scanning lines] × [4Tc]. Table 5 shows the relation between the set values in the character size register and the character sizes.



Note : This erases a video signal on an entire screen.

Fig. 35. Structure of character size register

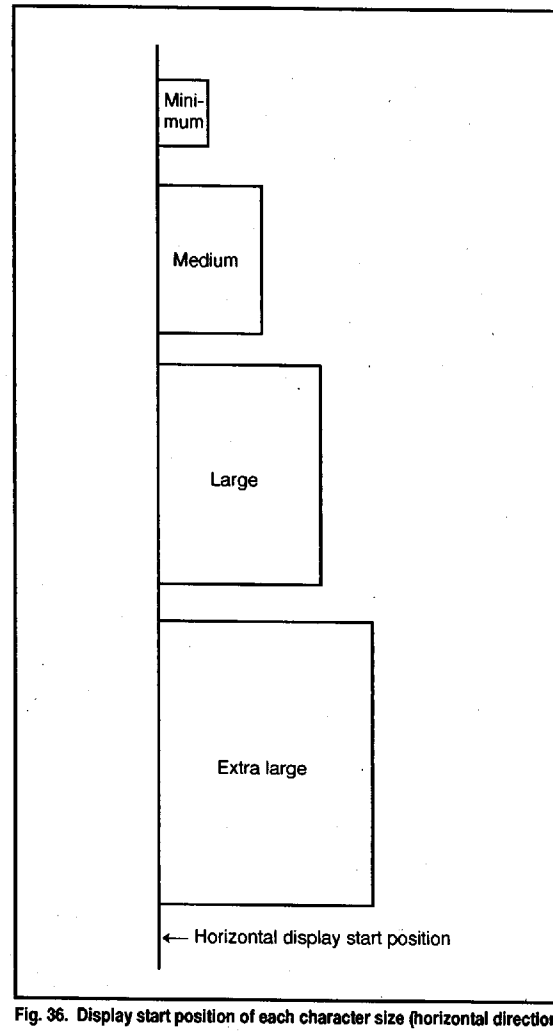


Fig. 36. Display start position of each character size (horizontal direction)

Table 5. Relation between set values in character size register and character sizes

Set values of character size register		Character size	Width (horizontal) direction Tc: oscillating cycle for display	Height (vertical) direction scanning lines
CSn1	CSn0			
0	0	Minimum	1Tc	1
0	1	Medium	2Tc	2
1	0	Large	3Tc	3
1	1	Extra large	4Tc	4

Note: The display start position in the horizontal direction is not affected by the character size. In other words, the horizontal display start position is common to all blocks even when the character size varies with each block (refer to Figure 35).

(4) Memory for Display

There are 2 types of memory for display : CRT display ROM (addresses 2000₁₆ to 3FFF₁₆) used to store character dot data (masked) and CRT display RAM (addresses 100₁₆ to 10D7₁₆) used to specify the colors and characters to be displayed. The following describes each type of display memory.

① ROM for display (addresses 2000₁₆ to 3FFF₁₆)

The CRT display ROM contains dot pattern data for characters to be displayed. For characters stored in this ROM to be actually displayed, it is necessary to specify them by writing the character code inherent to each character (code based on the addresses in the CRT display ROM) into the CRT display RAM. The character code list is shown in Table 6.

The CRT display ROM has a capacity of 8 K bytes. Since 32 bytes are required for 1 character data, the ROM can stores up to 256 kinds of characters.

The CRT display ROM space is broadly divided into 2 areas. The [vertical 16 dots] × [horizontal (left side) 8 dots] data of display characters are stored in addresses 2000₁₆ to 27FF₁₆ and 3000₁₆ to 37FFF₁₆; the [vertical 16 dots] × [horizontal (right side) 4 dots] data of display characters are stored in addresses 2800₁₆ to 2FFF₁₆ and 3800₁₆ to 3FFF₁₆ (refer to Figure 37). Note however that the high-order 4 bits in the data to be written to addresses 2800₁₆ to 2FFF₁₆ and 3800₁₆ to 3FFF₁₆ must be set to "1" (by writing data "FX₁₆").

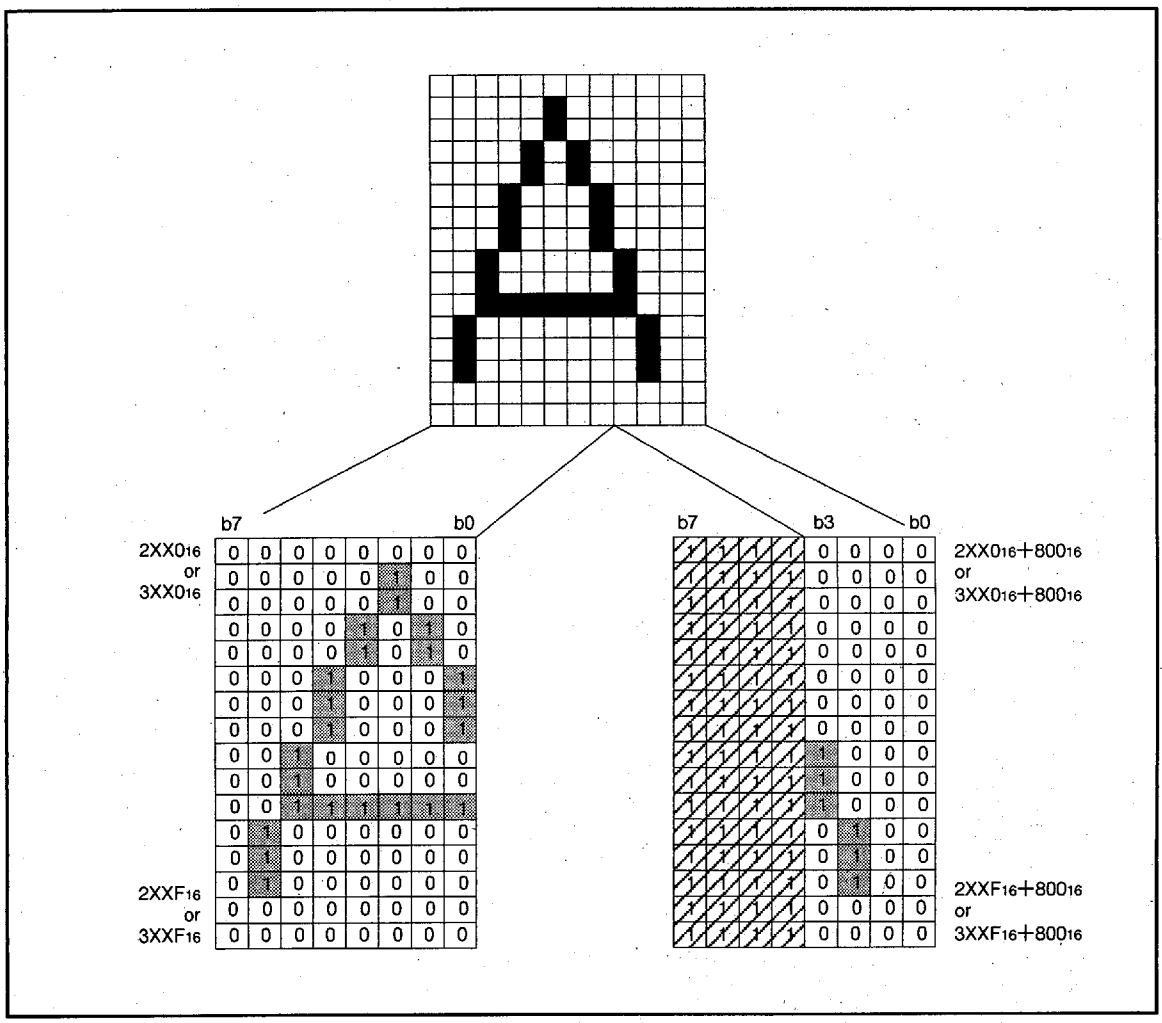


Fig. 37. Display character stored data

Table 6. Character code list (partially abbreviated)

Character code	Character data storage address	
	Left 8 dots lines	Right 4 dots lines
00_{16}	2000_{16} to $200F_{16}$	2800_{16} to $280F_{16}$
01_{16}	2010_{16} to $201F_{16}$	2810_{16} to $281F_{16}$
02_{16}	2020_{16} to $202F_{16}$	2820_{16} to $282F_{16}$
03_{16}	2030_{16} to $203F_{16}$	2830_{16} to $283F_{16}$
:	:	:
$7E_{16}$	$27E0_{16}$ to $27EF_{16}$	$2F00_{16}$ to $2F0F_{16}$
$7F_{16}$	$27F0_{16}$ to $27FF_{16}$	$2F10_{16}$ to $2F1F_{16}$
80_{16}	3000_{16} to $300F_{16}$	3800_{16} to $380F_{16}$
81_{16}	3010_{16} to $301F_{16}$	3810_{16} to $381F_{16}$
:	:	:
FD_{16}	$37D0_{16}$ to $37DF_{16}$	$3FD0_{16}$ to $3FDF_{16}$
FE_{16}	$37E0_{16}$ to $37EF_{16}$	$3FE0_{16}$ to $3FEF_{16}$
FF_{16}	$37F0_{16}$ to $37FF_{16}$	$3FF0_{16}$ to $3FFF_{16}$

② RAM for display (addresses 100_{16} to $10D_{16}$)

The CRT display RAM is allocated at addresses 100_{16} to $10D_{16}$, and is divided into a display character code specification part and display color specification part for each block. Table 7 shows the contents of the CRT display RAM.

For example, to display 1 character position (the left edge) in block 1, write the character code in address 100_{16} and write the color register No. to the low-order 2 bits (bits 0 and 1) in address 108_{16}. The color register No. to be written here is one of the 4 color registers in which the color to be displayed is set in advance. For details on color registers, refer to (5) Color Registers. The structure of the CRT display RAM is shown in Figure 37.

Table 7. Contents of CRT display RAM

Block	Display position (from left)	Character code specification	Color specification
Block 1	1st character	100_{16}	108_{16}
	2nd character	101_{16}	108_{16}
	3rd character : 22nd character	102_{16} : 101_{16}	108_{16} : 109_{16}
	23rd character	101_{16}	109_{16}
	24th character	101_{16}	109_{16}
Not used		101_{16} : 101_{16}	109_{16} : 109_{16}
Block 2	1st character	102_{16}	$10A_{16}$
	2nd character	102_{16}	$10A_{16}$
	3rd character : 22nd character	102_{16} : 103_{16}	$10A_{16}$: $10B_{16}$
	23rd character	103_{16}	$10B_{16}$
	24th character	103_{16}	$10B_{16}$
Not used		103_{16} : 103_{16}	$10B_{16}$: $10BF_{16}$
Block 2	1st character	104_{16}	$10C_{16}$
	2nd character	104_{16}	$10C_{16}$
	3rd character : 22nd character	104_{16} : 105_{16}	$10C_{16}$: $10D_{16}$
	23rd character	105_{16}	$10D_{16}$
	24th character	105_{16}	$10D_{16}$
Not used		105_{16} : 107_{16}	$10D_{16}$: $10FF_{16}$

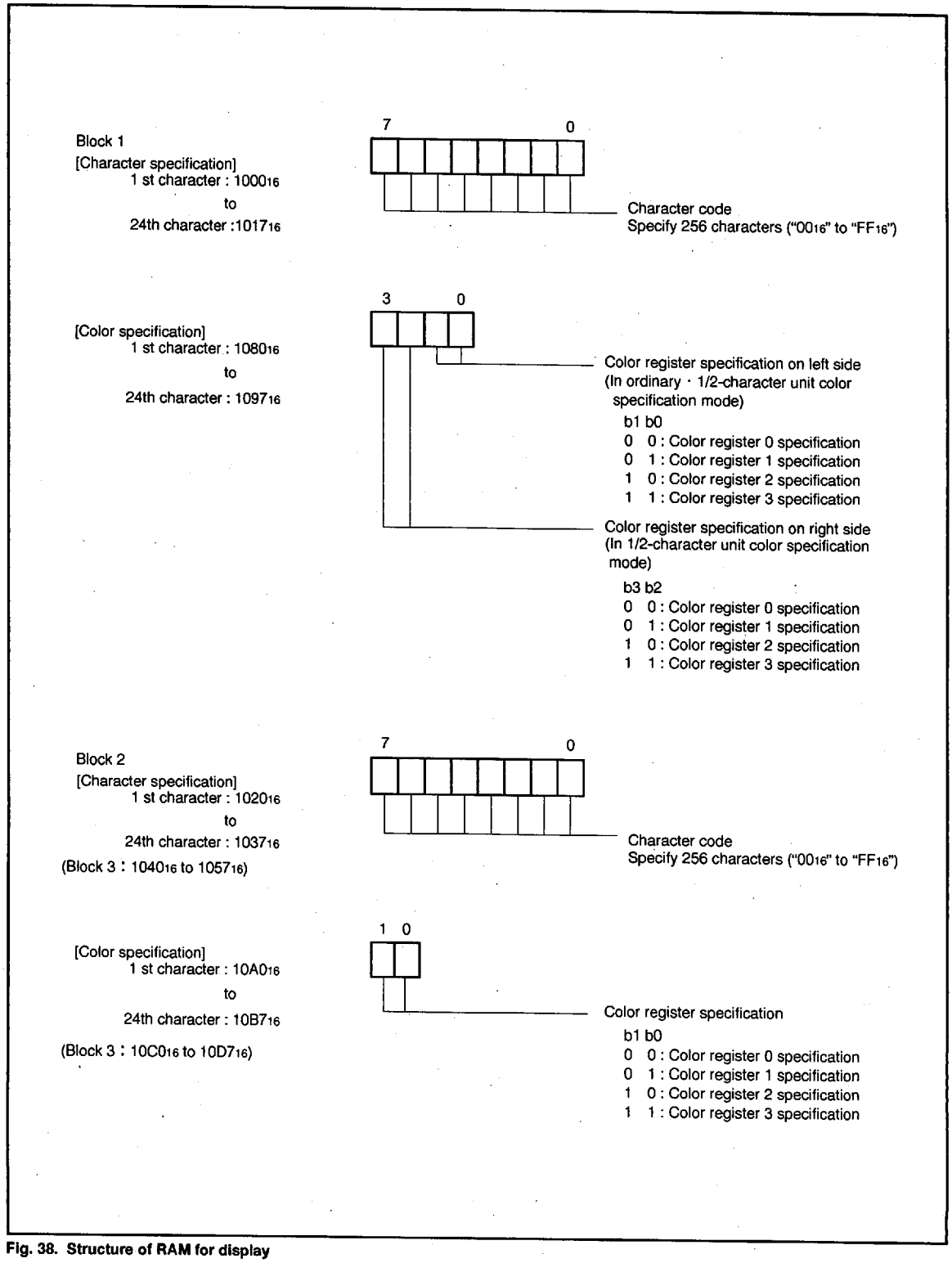


Fig. 38. Structure of RAM for display

(5) Color Registers

The color of a displayed character can be specified by setting the color to one of the 4 registers (CO0 to CO3: addresses 00E6$_{16}$ to 00E9$_{16}$) and then specifying that color register with the CRT display RAM. There are 4 color outputs; R, G, B and I. By using a combination of these outputs, it is possible to set 2^4-1 (when no output) = 15 colors. However, since only 4 color registers are available, up to 4 colors can be disabled at one time.

R, G, B and I outputs are set by using bits 0 to 3 in the color register. Bit 4 is used to set whether character output and blank output are enabled or not . Bit 5 is used to specify whether a character output or blank output.

Figure 39 shows the structure of the color register.

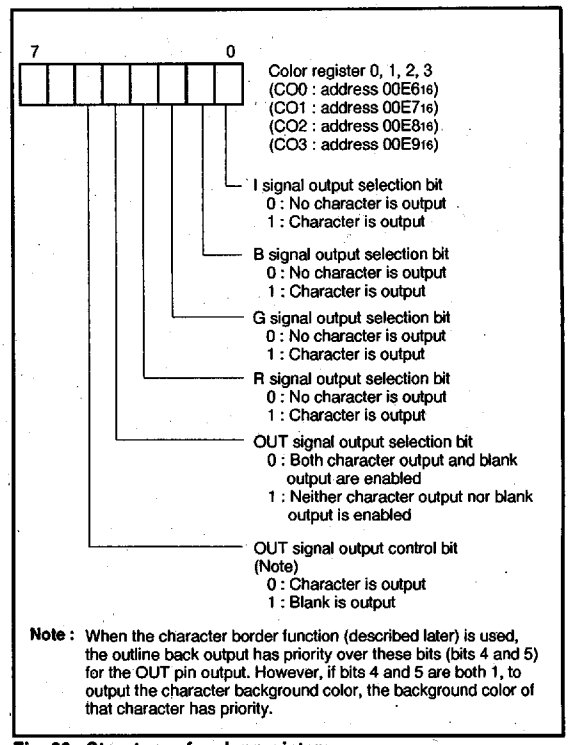


Fig. 39. Structure of color registers

(6) Character Background coloring

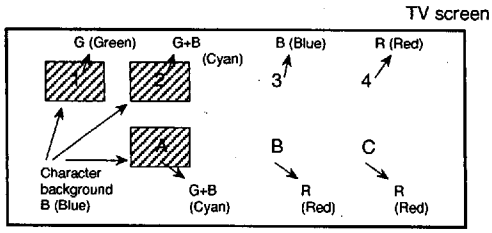
The background part of a character (its 12 × 16-dot area) can be colored as specified by bits 4 and 5 of the color registers (addresses 00E6$_{16}$ to 00E9$_{16}$) and bits 2, 3, and 4 of the CRT control register 2 (address 0208$_{16}$).

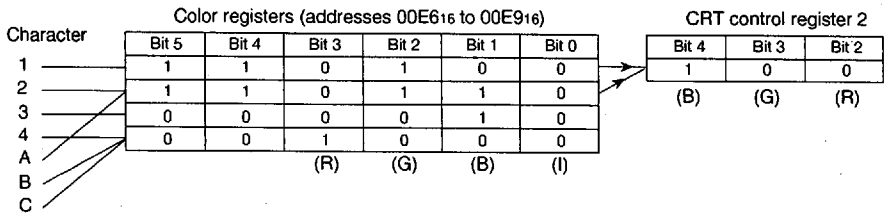
Set "1" in bits 4 and 5 of the color register of the character whose background is to be colored, and specify the background color with bits 2, 3, and 4 of the CRT control register 2. This means that the color of the character is paired with the background color of that character, so that up to 4 color pairs can be used in each screen (7 background colors are possible).

The structure of the CRT control register 2 is shown in Figure 52.

Table 8. Coloring to character background by R,G,B output signals

Color register			RGB output
Bit 4 (B)	Bit 3 (G)	Bit 2 (R)	Color
0	0	0	Black
0	0	1	Red
0	1	0	Green
0	1	1	Yellow
1	0	0	Blue
1	0	1	Magenta
1	1	0	Cyan
1	1	1	White





Note : If border and background color are applied to a character in contact with a 12 × 16 -dot frame in the same block, the border (1 dot) is protruded from the frame.

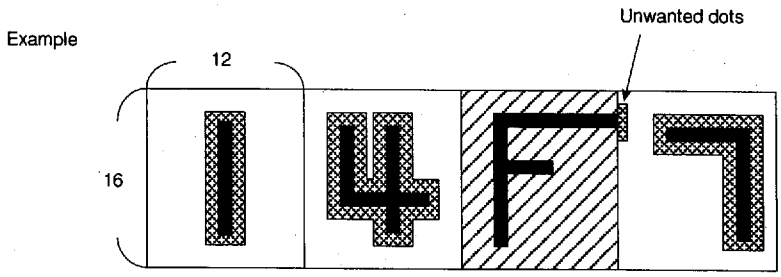


Fig. 40. Display example

(7) 1/2-character Unit Color Specification Mode

By setting "1" to bit 4 of the CRT control register 1 (address 00EA16) it is possible to specify colors, in units of a 1/2-character size (16 dots high × 6 dots wide), to characters in only block 1.
In the 1/2-character unit color specification mode, colors of display characters in block 1 are specified as follows:

- The color on the left side :
  this is set to the color of the color register which is specified by bits 0 and 1 at the color specification addresses (addresses 108016 to 109716) in the CRT display RAM.
- The color on the right side :
  this is set to the color of the color register which is specified by bits 2 and 3 at the color specification addresses (addresses 108016 to 109716) in the CRT display RAM.

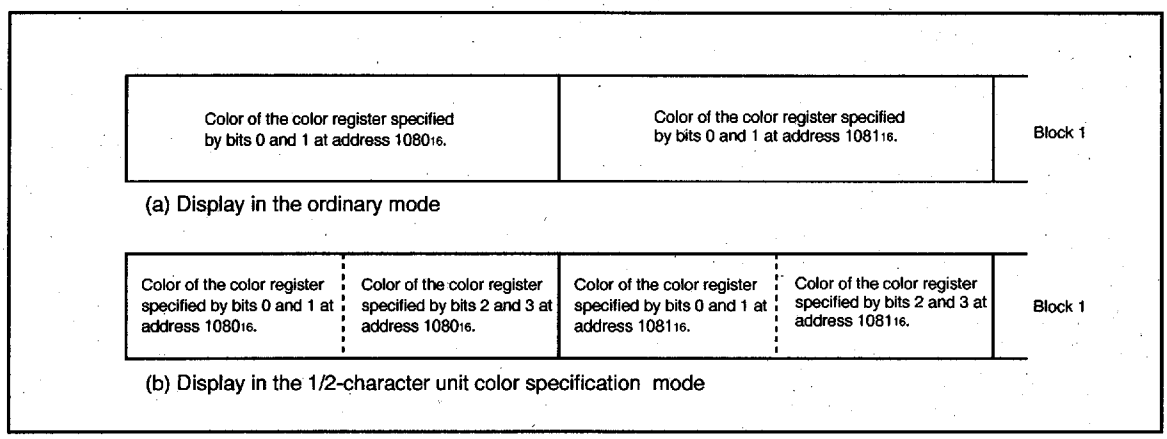


Fig. 41. Difference between ordinary color specification mode and 1/2-character unit color specification mode

(8) Character Border Function

An border of 1 clock (1 dot) equivalent size can be added to a character to be displayed in both horizontal and vertical directions. The border is output from the OUT pin. In this case, bits 4 and 5 in the color register (the OUT pin output contents) are ignored, and the border output is from the OUT pin.

Border can be specified in units of block by using the border selection register (address $00E5_{16}$). The setting of the border takes priority of the setting by bit 5 of the color register, however, the border of the character to which a background color has been set cannot be output. Figure 42 shows the structure of the border selection register. Table 9 shows the relationship between the values set in the border selection register and the character border function.

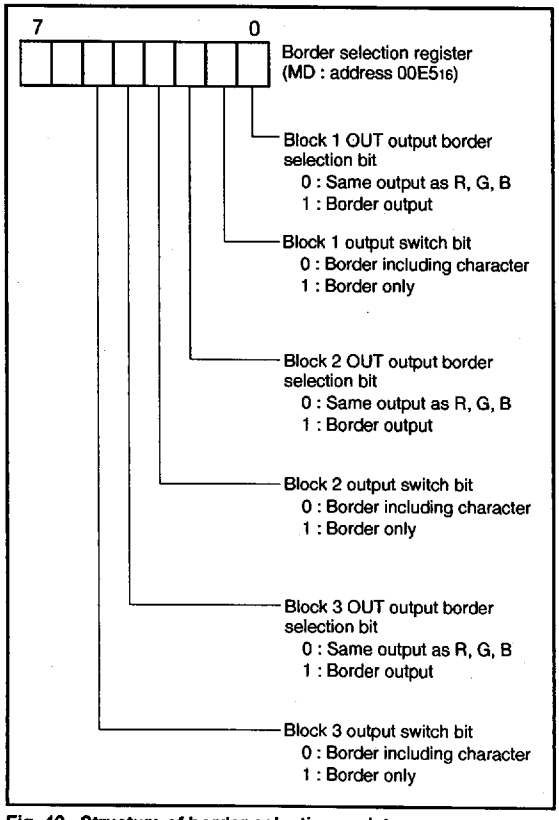


Fig. 42. Structure of border selection register

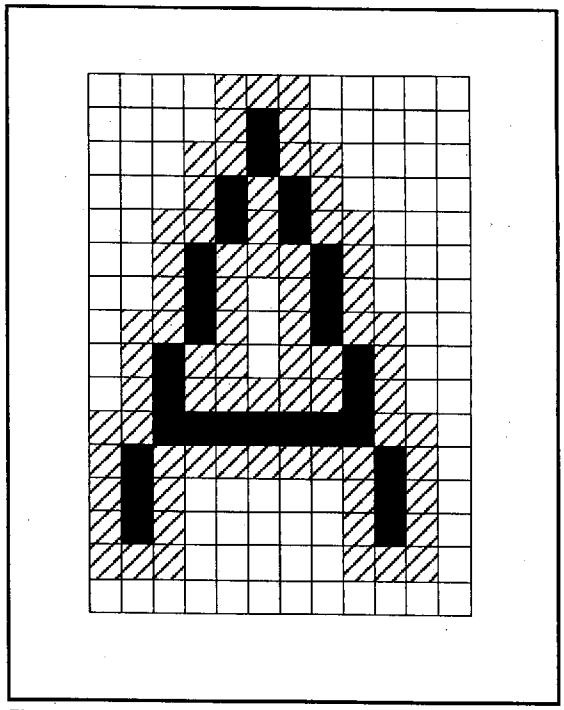


Fig. 43. Example of border

Table 9. Relationship between set value in border selection register and character border function

Border selection register		Functions	Example of output
MDn1	MDn0		
×	0	Ordinary	R, G, B, I output OUT output
0	1	Border including character	R, G, B, I output OUT output
1	1	Border only	R, G, B, I output OUT output

(9) Multiline Display

The M37204MC-XXXSP can ordinarily display 3 lines on the CRT screen by displaying 3 blocks at different vertical positions. In addition, it can display up to 16 lines by using CRT interrupts.

A CRT interrupt request occurs at the point at which display of each block has been completed. In other words, when a scanning line reaches the point of the display position (specified by the vertical position registers) of a certain block, the character display of that block starts, and an interrupt occurs at the point at which the scanning line exceeds the block.

The display block counter counts the number of times the display of a block has been completed, and its contents are incremented by 1 each time the display of one block is completed.

To provide multi-line display, enable CRT interrupts by clearing the interrupt disable flag to "0" and setting the CRT interrupt enable bit (bit 4 of address 00FE16) to "1." After that, process the following sequence within the CRT interrupt processing routine:

① Read the value of the display block counter.

② The block for which display is terminated (i.e., the cause of CRT interrupt generation) can be determined by the value read in ①.

③ Replace the display character data and vertical display position of that block with the character data (contents of CRT display RAM) and vertical display position (contents of vertical position register) to be displayed next.

Figure 44 shows the structure of the display block counter.

Note: A CRT interrupt does not occur at the end of display when the block is not displayed. In other words, if a block is set to off display with the display control bit of the CRT control register (address 00EA16), a CRT interrupt request does not occur (refer to Figure 45).

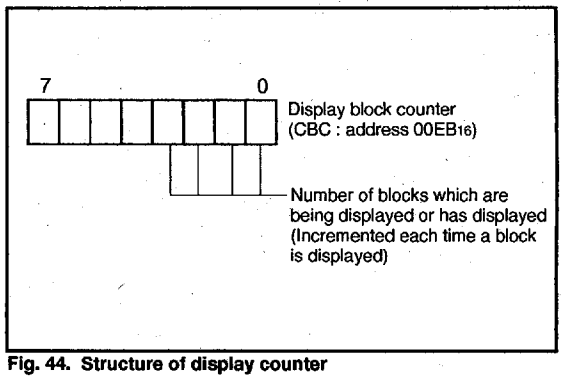


Fig. 44. Structure of display counter

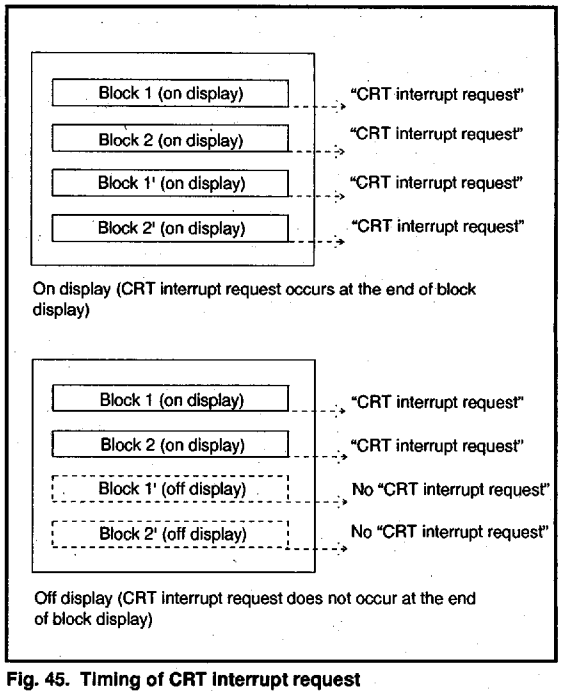


Fig. 45. Timing of CRT interrupt request

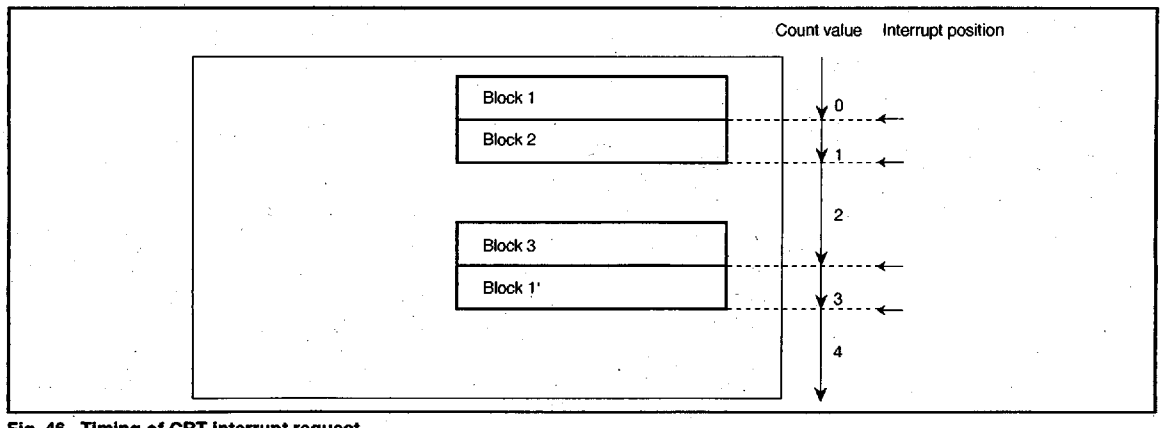


Fig. 46. Timing of CRT interrupt request

(10) Scanning Line Double Count Mode

1 dot in a displayed character is normally shown with 1 scanning line. In the scanning double count mode, 1 dot can be shown with 2 scanning lines. As a result, the displayed dot is extended 2 times the normal size in the vertical direction only (that is to say, the height of a character is extended twofold.)

In addition, because the scanning line count is doubled, the display start position of a character becomes also twofold position in the vertical direction.

In other words, the contents of the vertical position register is as follows:

- In ordinary mode
  256 steps as values "00$_{16}$" to "FF$_{16}$"
  (4 scanning lines per step)
- In scanning line double count mode
  128 steps as values "00$_{16}$" to "7F$_{16}$"
  (8 scanning lines per step)

If the contents of the vertical position register for a block are set in the range of "80$_{16}$" to "FF$_{16}$" in the scanning line double count mode, that block cannot be displayed (not output to the CRT screen). The scanning line double count mode is specified by setting bit 6 of the CRT control register 1 (address 00EA$_{16}$) to "1."

Since this function works in units of a screen, even if the mode is changed during display of 1 screen, the mode before the change remains until the display of the next screen.

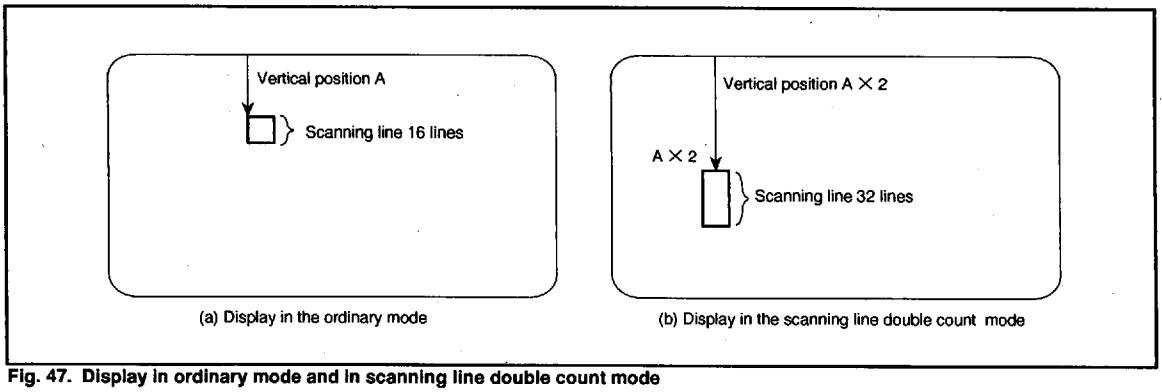


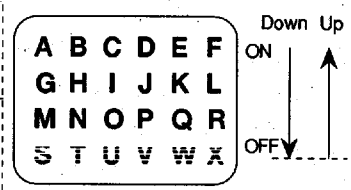
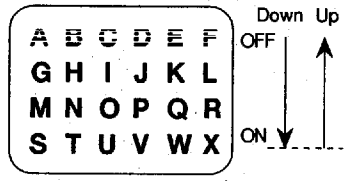
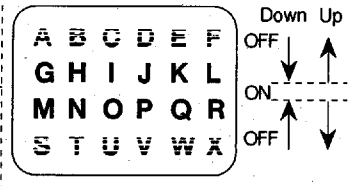
Fig. 47. Display in ordinary mode and in scanning line double count mode

(11) Wipe Function

① Wipe mode

The M37204MC-XXXSP allows the display area to be gradually expanded or shrunk in the vertically direction in units of 1H (H: HSYNC signal). There are 3 modes for this wipe method. Each mode has DOWN and UP modes, providing a total of 6 modes.
Table 10 shows the contents of each wipe mode.

Table 10. Wipe operation in each mode and values of wipe mode register

Mode		Wipe operation		Wipe mode register		
				Bit 2	Bit 1	Bit 0
1	DOWN	Appear from upper side		0	0	1
	UP	Erase from lower side		1	0	1
2	DOWN	Erase from upper side		0	1	0
	UP	Appear from lower side		1	1	0
3	DOWN	Erase from both upper and lower sides		0	1	1
	UP	Appear to both upper and lower sides		1	1	1

② Wipe speed

The wipe speed is determined by the vertical synchronization (VSYNC) signal. For the NTSC interlace method, assuming that VSYNC = 16.7 ms, 262.5 HSYNC signals (per field) we obtain the wipe speed as shown in Table 11.

Wipe resolution varies with each wipe mode. In mode 1 and mode 2, one of 3 resolutions (1H, 2H, 4H) can be selected. In mode 3, wipe is done in units of 4H only.

Table 11. Wipe speed
(NTSC interlace method, H = 262.5)

Wipe resolution	Wipe speed (entire screen)
1H Unit	16.7 (ms) × 262.5 ÷ 1 ≒ 4 (s)
2H Unit	16.7 (ms) × 262.5 ÷ 2 ≒ 2 (s)
4H Unit	16.7 (ms) × 262.5 ÷ 4 ≒ 1 (s)

Table 12. Wipe mode and wipe resolution

Mode	Wipe resolution	Wipespeed
Mode 1	1H Unit	about 4 (s)
Mode 2	2H Unit	about 2 (s)
	4H Unit	about 1 (s)
Mode 3	4H Unit	about 1 (s)

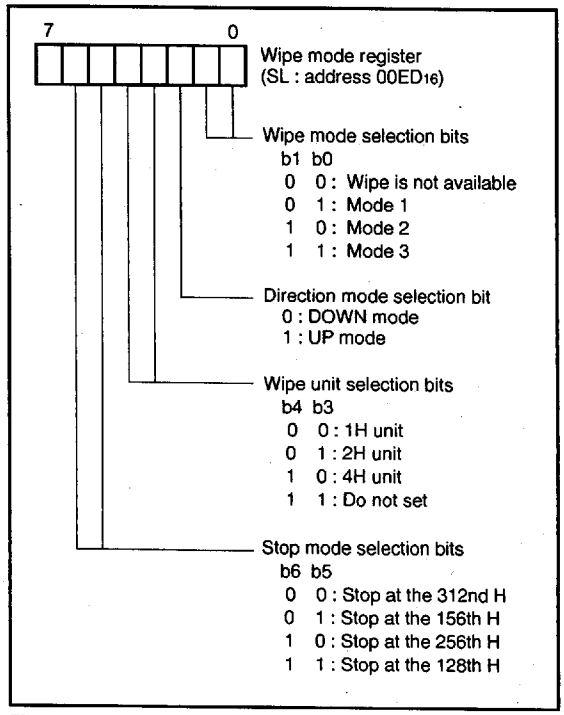


Fig. 48. Structure of scroll mode register

(12) CRT Output Pin Control

The CRT output pins R, G, B, I and OUT can also function as ports P52, P53, P54, P55 and P56. Set the corresponding bit of the port P5 control register (address 00CB16) to "0" to specify these pins as CRT output pins, or set it to "1" to specify it as a general-purpose port P5 pins.

The input polarity of signals HSYNC and VSYNC and output polarity of signals R, G, B, I and OUT can be specified with the bits of the CRT port control register (address 00EC16). Set a bit to "0" to specify positive polarity; set it to "1" to specify negative polarity.

The CRT clock I/O pins OSC1, OSC2 are controlled with the port control register (address 020616).

The structure of the CRT port control register is shown in Figure 49.

The structure of the port control register is shown in Figure 50.

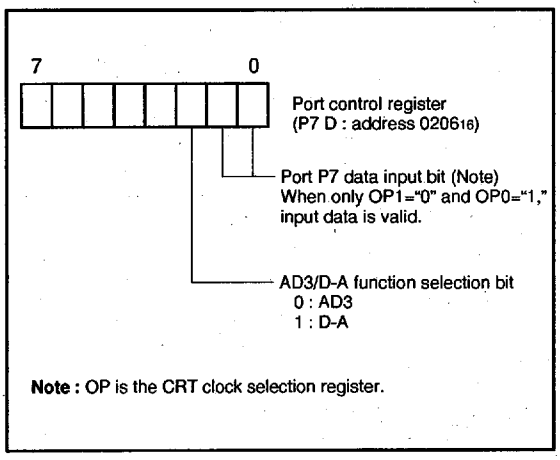


Fig. 50. Structure of port control register

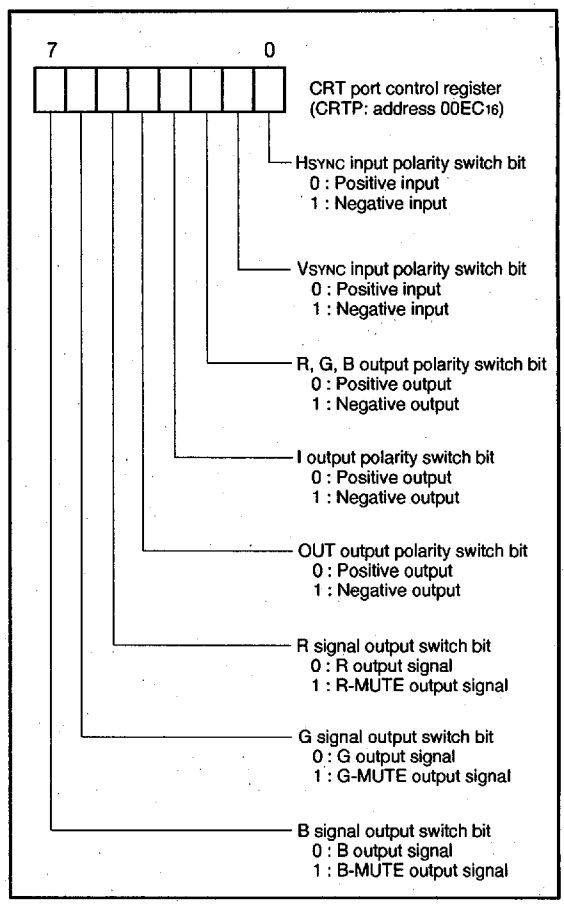


Fig. 49. Structure of CRT port control register

(13) Raster Coloring Function

An entire screen (raster) can be colored by switching each of the R, G, B, I and OUT pins to MUTE output. R, G, B are controlled with the CRT port control register; I is controlled with the CRT control register 2; OUT is controlled with the character size register. 15 raster colors can be obtained.

If the OUT pin has been set to raster coloring output, a raster coloring signal is always output during 1 horizontal scanning period. This setting is necessary for erasing a background TV image.

If the R, G, and B pins have been set to MUTE signal output, a raster coloring signal is output in the part except a no-raster colored character (in Figure 50, a character "O") during 1 horizontal scanning period. This ensures that character colors do not mix with the raster color. In this case, MUTE signal is output from the OUT pin.

An example in which a magenta character "I" and a red character "O" are displayed with blue raster coloring is shown in Figure 51.

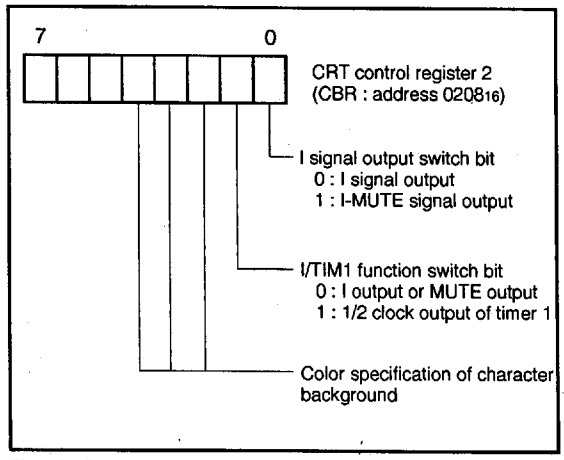


Fig. 52. Structure of CRT control register

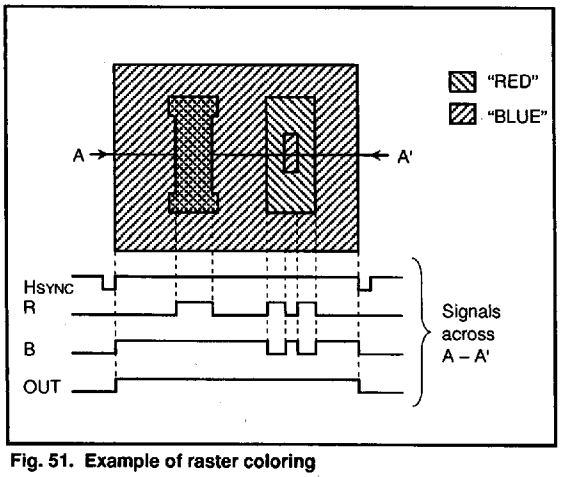


Fig. 51. Example of raster coloring

(14) Clock for Display

As a clock for display to be used for CRT display, it is possible to select one of the following 3 types.

- Main clock supplied from the XIN pin
- Clock from the LC or RC supplied from the pins OSC1 and OSC2.
- Clock from the ceramic resonator or quartz-crystal oscillator supplied from the pins OSC1 and OSC2.

This clock for display can be selected for each block by the CRT clock selection register (address 020916).

When selecting the main clock, set the oscillation frequency to 8 MHz.

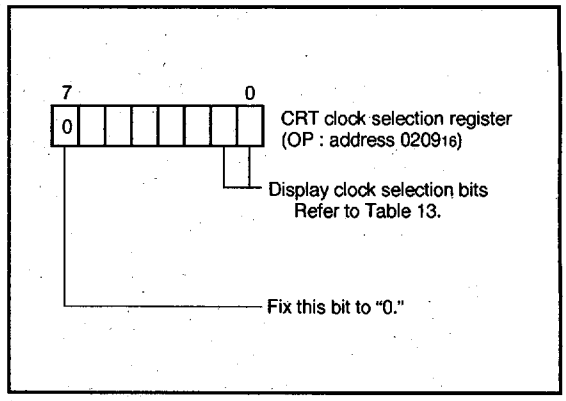


Fig. 53. Structure of CRT clock selection register

Table 13. Set value of CRT clock selection register and clock for display

b1	b0	Functions		Scanning line double count mode flag (CC6)
0	0	The clock for display is supplied by connecting RC or LC across the pins OSC1 and OSC2.		CC6 = "0" or "1"
0	1	Since the main clock is used as the clock for display, the oscillation frequency is limited. Because of this, the character size in width (horizontal) direction is also limited. In this case, pins OSC1 and OSC2 are also used as input ports P70 and P71 respectively.	CRT oscillation frequency = f(XIN)	CC6 = "0"
1	0	Do not set		—
1	1	The clock for display is supplied by connecting the following across the pins OSC1 and OSC2. • a ceramic resonator only for CRT display and a feedback resistor • a quartz-crystal oscillator only for CRT display and a feedback resistor (Note)		CC6 = "0"

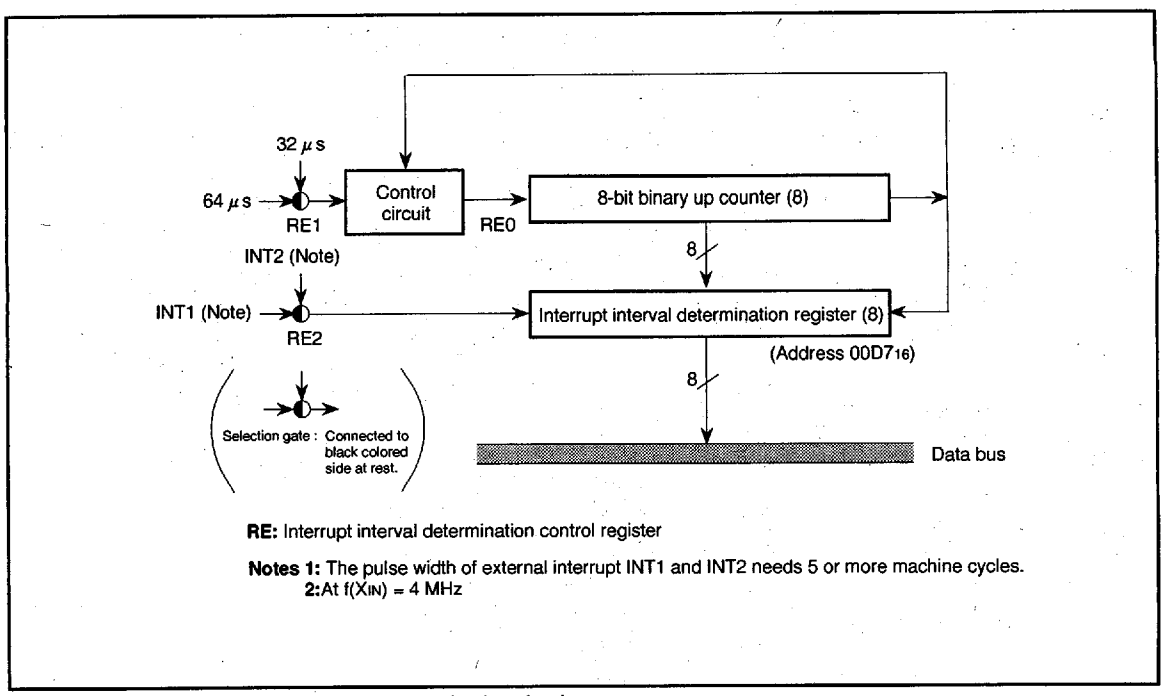
Note: It is necessary to connect other ceramic resonator or quartz-crystal oscillator across the pins XIN and XOUT.

INTERRUPT INTERVAL DETERMINATION FUNCTION

The M37204MC-XXXSP incorporates an interrupt interval determination circuit. This interrupt interval determination circuit has an 8-bit binary up counter as shown in Figure 53. Using this counter, it determines an interval on the INT1 or INT2 (refer to Figure 55).

The following describes how the interrupt interval is determined.

1. The interrupt input to be determined (INT1 input or INT2 input) is selected by using bit 2 in the interrupt interval determination control register (address 00D8$_{16}$). When this bit is cleared to "0," the INT1 input is selected ; when the bit is set to "1," the INT2 input is selected.
2. When the INT1 input is to be determined, the polarity is selected by using bit 3 of the interrupt interval determination control register ; when the INT2 input is to be determined, the polarity is selected by using bit 4 of the interrupt interval determination control register.
   When the relevant bit is cleared to "0," determination is made of the interval of a positive polarity (rising transition) ; when the bit is set to "1," determination is made of the interval of a negative polarity (falling transition).
3. The reference clock is selected by using bit 1 of the interrupt interval determination control register. When the bit is cleared to "0," a 64 μs clock is selected ; when the bit is set to "1," a 32 μs clock is selected (based on an oscillation frequency of 4MHz in either case).
4. Simultaneously when the input pulse of the specified polarity (rising or falling transition) occurs on the INT1 pin (or INT2 pin), the 8-bit binary up counter starts counting up with the selected reference clock (64 μs or 32 μs).
5. Simultaneously with the next input pulse, the value of the 8-bit binary up counter is loaded into the interrupt interval determination register (address 00D7$_{16}$) and the counter is immediately reset ("00$_{16}$"). The reference clock is input in succession even after the counter is reset, and the counter restarts counting up from "00$_{16}$."
6. When count value "FE$_{16}$" is reached, the 8-bit binary up counter stops counting. Then, simultaneously when the next reference clock is input, the counter sets value "FF$_{16}$" to the interrupt interval determination register. The reference clock is generated by setting bit 0 of the PWM output control register 1 to "0."



RE: Interrupt interval determination control register

Notes 1: The pulse width of external interrupt INT1 and INT2 needs 5 or more machine cycles.
2:At f(XIN) = 4 MHz

Fig. 54. Block diagram of interrupt interval determination circuit

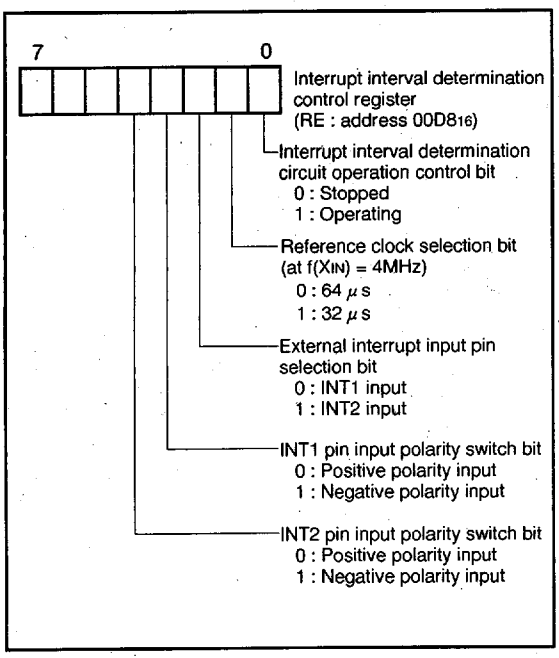


Fig. 55. Structure of interrupt interval determination control register

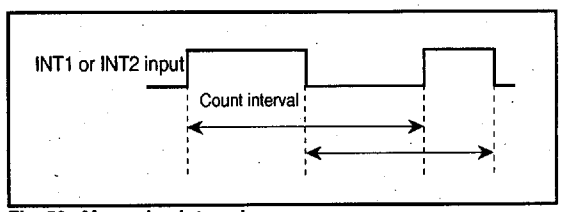


Fig. 56. Measuring interval

RESET CIRCUIT

The M37204MC-XXXSP is reset according to the sequence shown in Figure 57. It starts the program from the address formed by using the content of address FFFF16 as the high-order address and the content of the address FFFE16 as the low-order address, when the $\overline{\text{RESET}}$ pin is held at "L" level for 2 μs or more while the power source voltage is 5 V ± 10 % and the oscillation of a quartz-crystal oscillator or a ceramic resonator is stable and then returned to "H" level. The internal state of microcomputer at reset are shown in Figures 3 to 6. An example of the reset circuit is shown in Figure 58.

The reset input voltage must be kept 0.6 V or less until the power source voltage surpasses 4.5 V.

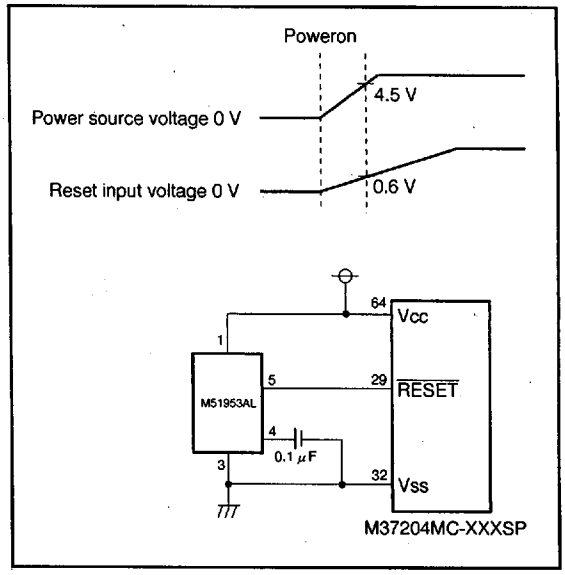


Fig. 58. Example of reset circuit

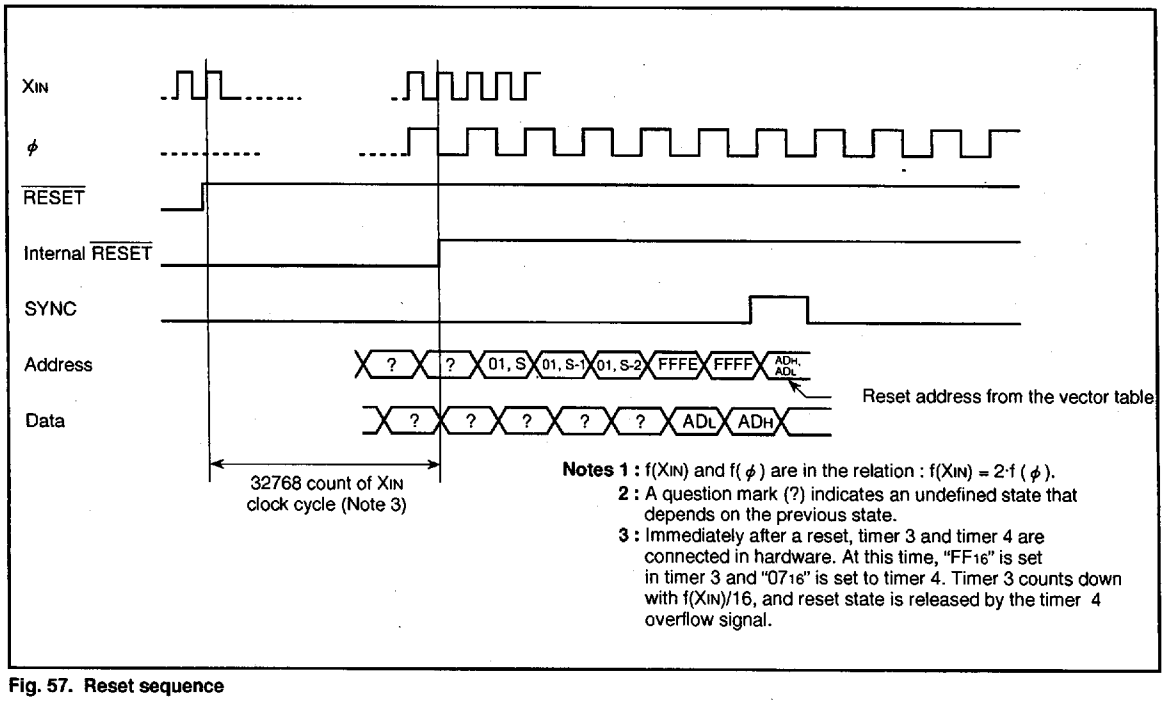
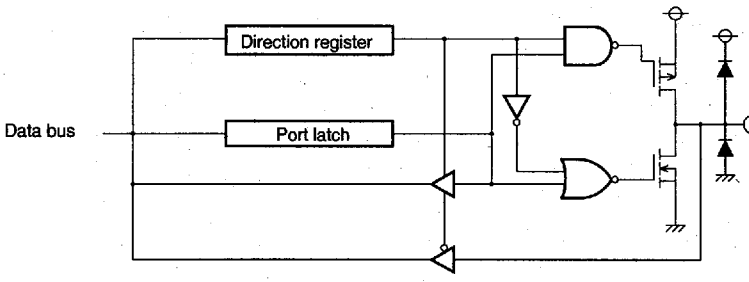


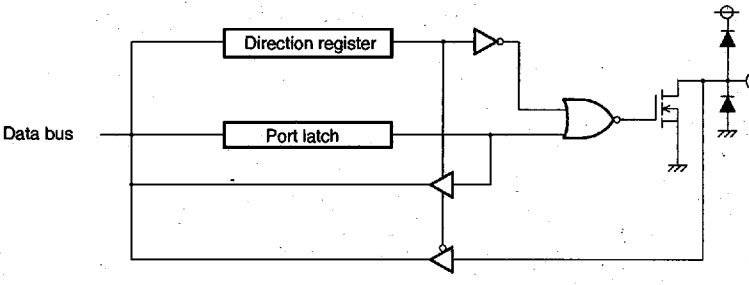
Fig. 57. Reset sequence

Ports P00–P07, P10–P17, P20–P27, P30, P31, D-A



Note: D-A pin does not have port input function. D-A pin is also used as AD3.

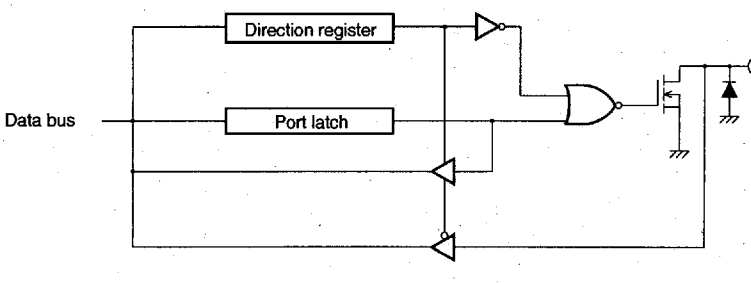
Ports P32–P36, P40–P45



Note: Each port is also used as below:

P32: AD6/TIM2	P40: SOUT1
P33: TIM3	P41: SCLK1
P34: INT1	P42: AD8/SIN1
P35: AD1	P43: AD7/$\overline{\text{SRDY1}}$
P36: INT2/AD2	P44: SOUT2/SDA
	P45: SCLK2/SCL

Ports P46, P47, P60–P67



Note: Each port is also used as below:

P46: SIN2/PWM9
P47: $\overline{\text{SRDY2}}$/PWM8
P60–P67: PWM0–PWM7

Fig. 59. I/O pin block diagram (1)

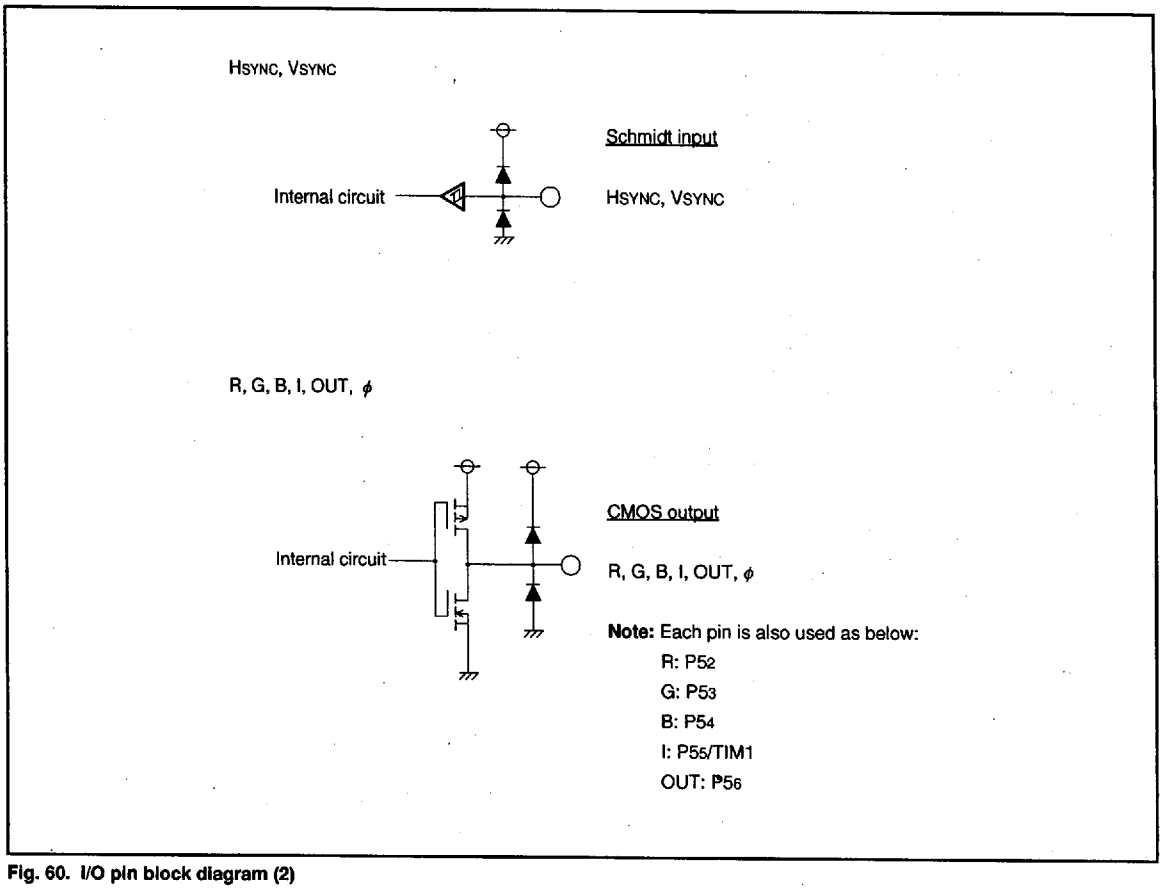


Fig. 60. I/O pin block diagram (2)

CLOCK GENERATING CIRCUIT

The built-in clock generating circuit is shown in Figure 63. When the STP instruction is executed, the internal clock ϕ stops at "H" level. At the same time, timers 3 and 4 are connected in hardware and "FF16" is set in the timer 3, "0716" is set in the timer 4. Select f(XIN)/16 as the timer 3 count source (set bit 0 of the timer 34 mode register to "0" before the execution of the STP instruction). And besides, set timer 3 and timer 4 interrupt enable bits to disabled ("0") before execution of the STP instruction. This connection is released when an external interrupt is accepted or at reset. The oscillator restarts when external interrupt is accepted, however, the internal clock ϕ keeps its "H" level until timer 4 overflows. Because this allows time for oscillation stabilizing when a ceramic resonator or a quartz-crystal oscillator is used.

When the WIT instruction is executed, the internal clock ϕ stops in the "H" level but the oscillator continues running. This wait state is released when an interrupt is accepted (Note). Since the oscillator does not stop, the next instruction can be executed at once.

When returning from the stop or the wait state, to accept an interrupt, set the corresponding interrupt enable bit to "1" before executing the STP or the WIT instructions.

The circuit example using a ceramic resonator (or a quartz-crystal oscillator) is shown in Figure 61. Use the circuit constants in accordance with the resonator manufacture's recommended values. The circuit example with external clock input is shown in Figure 62. Input the clock to the XIN pin, and open the XOUT pin.

Note: In the wait mode, the following interrupts are invalid.

(1) VSYNC interrupt
(2) CRT interrupt
(3) Timer 2 interrupt using AD6/P32/TIM2 pin input as count source
(4) Timer 3 interrupt using P33/TIM3 pin input as count source
(5) Timer 4 interrupt using f(XIN)/2 as count source

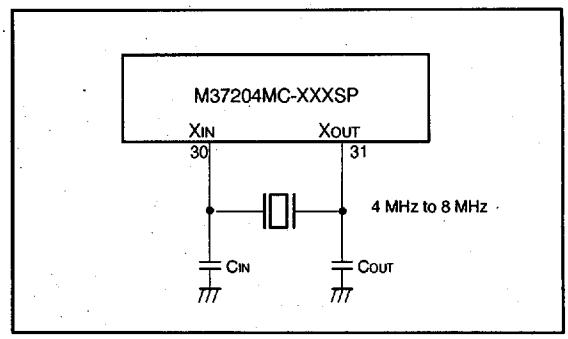


Fig. 61. Ceramic resonator circuit example

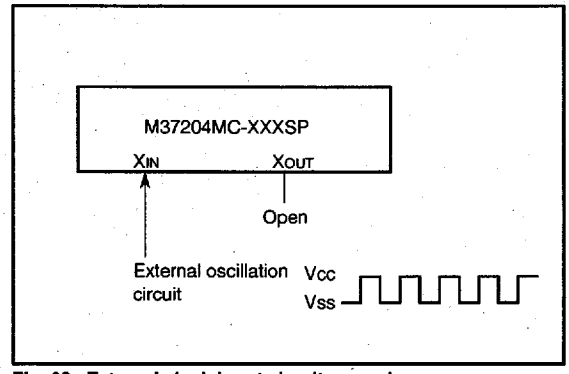


Fig. 62. External clock input circuit example

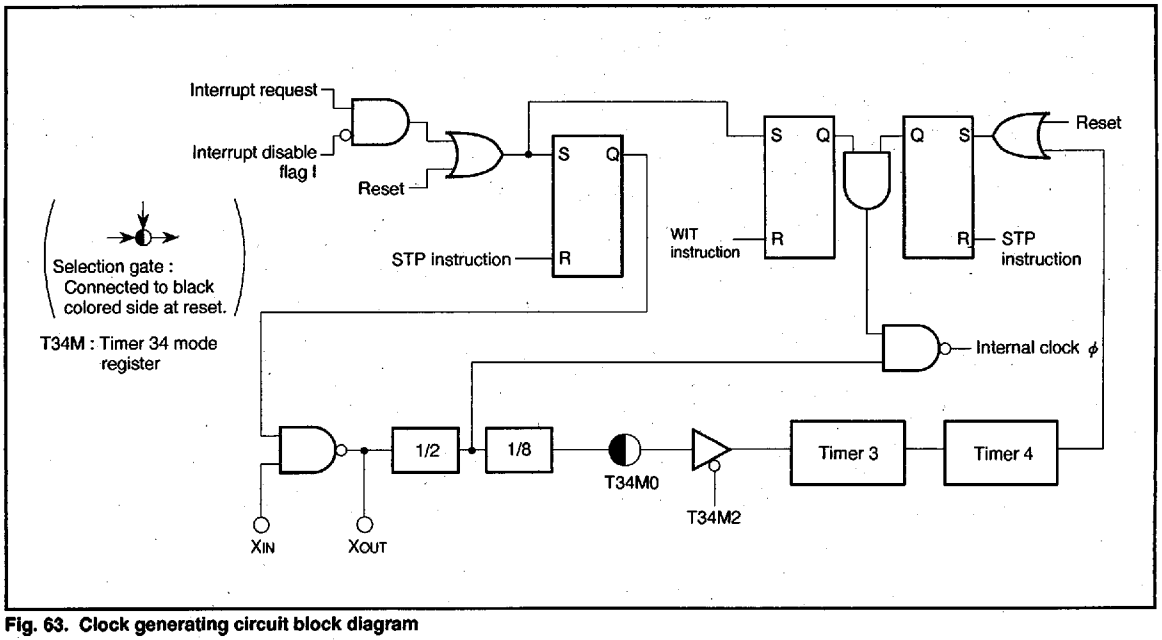


Fig. 63. Clock generating circuit block diagram

DISPLAY OSCILLATION CIRCUIT

The CRT display clock oscillation circuit has a built-in clock oscillation circuits, so that a clock for CRT display can be obtained simply by connecting an LC, an RC, a quartz-crystal oscillator or a ceramic resonator across the pins OSC1 and OSC2. Select the clock for display with bits 0 and 1 of the CRT clock selection register (address 0209_{16}).

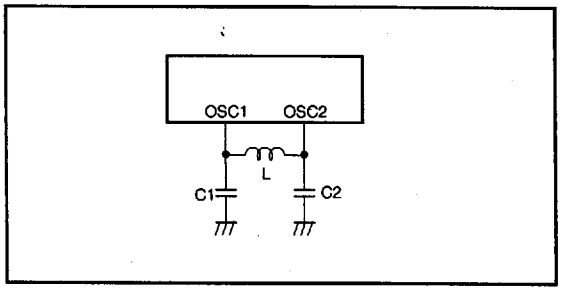
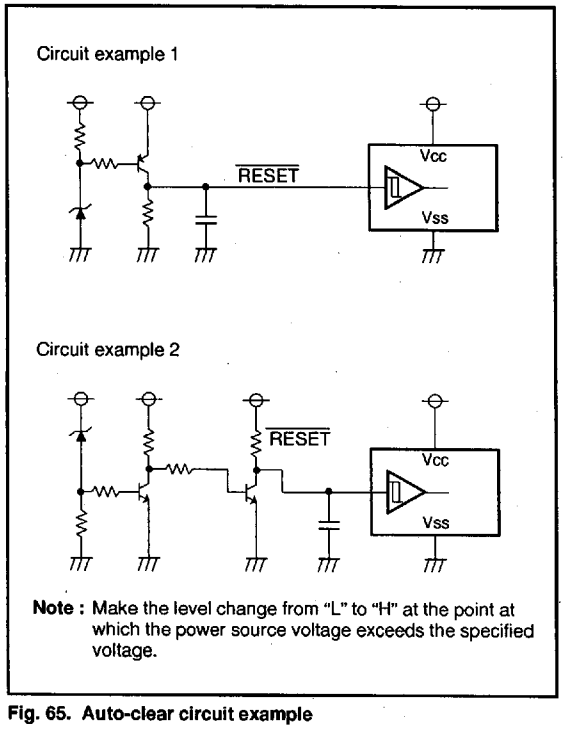


Fig. 64. Display oscillation circuit

AUTO-CLEAR CIRCUIT

When power source is supplied, the auto-clear function can be performed by connecting the following circuit to the $\overline{\text{RESET}}$ pin.



Note : Make the level change from "L" to "H" at the point at which the power source voltage exceeds the specified voltage.

Fig. 65. Auto-clear circuit example

ADDRESSING MODE

The memory access is reinforced with 17 kinds of addressing modes. Refer to the SERIES 740 <Software> User's Manual for details.

MACHINE INSTRUCTIONS

There are 71 machine instructions. Refer to the SERIES 740 <Software> User's Manual for details.

PROGRAMMING NOTES

(1) The divide ratio of the timer is 1/(n+1).

(2) Even though the BBC and BBS instructions are executed immediately after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. At least one instruction cycle is needed (such as an NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.

(3) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as an NOP) is needed before the SEC, CLC, or CLD instruction is executed.

(4) An NOP instruction is needed immediately after the execution of a PLP instruction.

(5) In order to avoid noise and latch-up, connect a bypass capacitor ($\approx 0.1\ \mu F$) directly between the V_{CC} pin–V_{SS} pin and the V_{CC} pin–CNV_{SS} pin using a thick wire.

(6) Note that the addresses of the M37204MC-XXXSP are different from the addresses of the M37204M8-XXXSP.

M37204MC-XXXSP
M37204EC-XXXSP, M37204ECSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER and ON-SCREEN DISPLAY CONTROLLER

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

(1) Mask ROM Order Confirmation Form
(2) Mark Specification Form
(3) Data to be written to ROM, in EPROM form (28-pin DIP type 27512, three identical copies)

PROM Programming Method

The built-in PROM of the One Time PROM version (blank) and built-in EPROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter.

Product	Name of Programming Adapter
M37204ECSP	PCA4762

The PROM of the One Time PROM version (blank) is not tested or screened in the assembly process and following processes. To ensure proper operation after programming, the procedure shown in Figure 66 is recommended to verify programming.

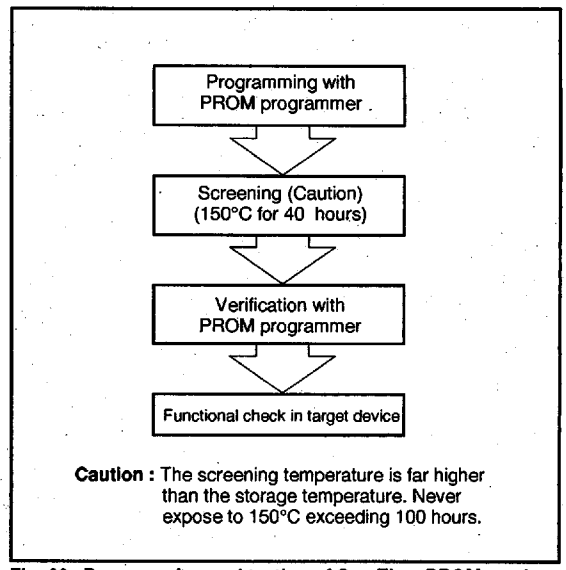


Fig. 66. Programming and testing of One Time PROM version

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Power source voltage	V_{CC}	All voltages are based on V_{SS}. Output transistors are cut off.	−0.3 to 6	V
V_I	Input voltage	CNVss		−0.3 to 6	V
V_I	Input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_6$, $P4_0$–$P4_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$, OSC1, XIN, HSYNC, VSYNC, RESET, AD1–AD8		−0.3 to V_{CC} + 0.3	V
V_O	Output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_6$, $P4_0$–$P4_5$, R, G, B, I, OUT, D-A, XOUT, OSC2		−0.3 to V_{CC} + 0.3	V
V_O	Output voltage	$P4_6$, $P4_7$, $P6_0$–$P6_7$		−0.3 to 13	V
I_{OH}	Circuit current	R, G, B, I, OUT, $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$, $P3_1$, D-A		0 to 1 (Note 1)	mA
I_{OL1}	Circuit current	R, G, B, I, OUT, $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P3_0$–$P3_6$, $P4_0$–$P4_3$, D-A		0 to 2 (Note 2)	mA
I_{OL2}	Circuit current	$P4_6$, $P4_7$, $P6_0$–$P6_7$		0 to 1 (Note 2)	mA
I_{OL3}	Circuit current	$P2_4$–$P2_7$		0 to 10 (Note 3)	mA
I_{OL4}	Circuit current	$P4_4$, $P4_5$		0 to 3 (Note 2)	mA
Pd	Power dissipation		Ta = 25 °C	550	mW
Topr	Operating temperature			−10 to 70	°C
Tstg	Storage temperature			−40 to 125	°C

RECOMMENDED OPERATING CONDITIONS (Ta = −10 °C to 70 °C, V_{CC} = 5 V ± 10 %, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Power source voltage (Note 4), During CPU, CRT operation		4.5	5.0	5.5	V
V_{SS}	Power source voltage		0	0	0	V
V_{IH1}	"H" input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_6$, $P4_0$–$P4_3$, $P4_6$, $P4_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$, HSYNC, VSYNC, RESET, XIN, OSC1	0.8V_{CC}		V_{CC}	V
V_{IH2}	"H" input voltage	$P4_4$, $P4_5$	0.7V_{CC}		V_{CC}	V
V_{IL1}	"L" input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_6$, $P4_0$–$P4_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$	0		0.4 V_{CC}	V
V_{IL2}	"L" input voltage	HSYNC, VSYNC, RESET, TIM2, TIM3, INT1, INT2, SOUT1, SCLK1, SIN1, SDA, SCL, XIN, OSC1	0		0.2 V_{CC}	V
I_{OH}	"H" average output current (Note 1)	R, G, B, I, OUT, D-A, $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$, $P3_1$			1	mA
I_{OL1}	"L" average output current (Note 2)	R, G, B, I, OUT, D-A, $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P3_0$–$P3_6$, $P4_0$–$P4_3$			2	mA
I_{OL2}	"L" average output current (Note 2)	$P4_6$, $P4_7$, $P6_0$–$P6_7$			1	mA
I_{OL3}	"L" average output current (Note 3)	$P2_4$–$P2_7$			10	mA
I_{OL4}	"L" average output current (Note 2)	$P4_4$, $P4_5$			3	mA
fCPU	Oscillation frequency (for CPU operation) (Note 5)	XIN	3.6	4.0	8.1	MHz
fCRT	Oscillation frequency (for CRT display) (Note 6)	In ordinary mode	6.0	7.0	8.0	kHz
		In double count mode	12.0	13.0	14.0	MHz
fhs1	Input frequency	TIM2, TIM3, INT1, INT2, SCL			100	kHz
fhs2	Input frequency	SCLK1, SCLK2			1	MHz

ELECTRIC CHARACTERISTICS (V_{CC} = 5 V ± 10 %, V_{SS} = 0 V, f(X_{IN}) = 4 MHz, Ta = −10 °C to 70 °C, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min.	Typ.	Max.	
I_{CC}	Power source current	System operation	V_{CC} = 5.5 V, f(X_{IN}) = 4 MHz	CRT OFF		10	20	mA
				CRT ON		20	50	
			V_{CC} = 5.5 V, f(X_{IN}) = 8 MHz	CRT OFF		20	40	
				CRT ON		30	60	
		Stop mode	V_{CC} = 5.5 V, f(X_{IN}) =0				300	μA
V_{OH}	"H" output voltage	R, G, B, I, OUT, P00–P07, P10–P17, P20–P27, D-A, P30, P31	V_{CC} = 4.5 V I_{OH} = −0.5 mA		2.4			V
V_{OL}	"L" output voltage	R, G, B, I, OUT, P00–P07, P10–P17, P20–P23, P30–P36, , P40–P43, D-A	V_{CC} = 4.5 V I_{OL} = 0.5 mA				0.4	V
	"L" output voltage	P46, P47, P60–P67	V_{CC} = 4.5 V I_{OL} = 0.5 mA				0.4	
	"L" output voltage	P24–P27	V_{CC} = 4.5 V I_{OL} = 10.0 mA				3.0	
	"L" output voltage	P44, P45	V_{CC} = 4.5 V I_{OL} = 3.0 mA				0.4	
V_{T+}–V_{T-}	Hysteresis	$\overline{RESET}$	V_{CC} = 5.0 V			0.5	0.7	V
	Hysteresis (Note 7)	HSYNC, VSYNC, P32–P34, P36, P40–P42, P44–P46	V_{CC} = 5.0 V			0.5	1.3	
I_{IZH}	"H" input leak current	$\overline{RESET}$, P00–P07, P10–P17, P20–P27, P30–P36, P40–P45, AD1–AD8	V_{CC} = 5.5 V V_I = 5.5 V				5	μA
I_{IZL}	"L" input leak current	$\overline{RESET}$, P00–P07, P10–P17, P20–P27, P30–P36, P40–P47, P60–P67, AD1–AD8	V_{CC} = 5.5 V V_I = 0 V				5	μA
I_{OZH}	"H" output leak current	P46, P47, P60–P67	V_{CC} = 5.5 V V_O = 12 V				10	μA

Notes 1: The total current that flows out of the IC must be 20 mA or less.
2: The total input current to IC (I_{OL1} + I_{OL2} + I_{OL4}) must be 30 mA or less.
3: The total average input current for ports P24–P27 to IC must be 20 mA or less.
4: Connect 0.022 μF or more capacitor externally across the power source pins V_{CC}–V_{SS} so as to reduce power source noise. Also connect 0.068 μF or more capacitor externally across the pins V_{CC}–CNV$_{SS}$.
5: Use a quartz-crystal oscillator or a ceramic resonator for the CPU oscillation circuit.
6: Use a RC or an LC for the CRT oscillation circuit.
7: P32–P34 ,P36 have the hysteresis when these pins are used as interrupt input pins or timer input pins. P40–P42, P44–P46 have the hysteresis when these pins are used as serial I/O pins.

Note 28. Self refresh sequence

Two refreshing ways should be used properly depending on the low pulse width (t_{RASS}) of $\overline{RAS}$ signal during self refresh period.

1. In case of $t_{RASS} < 300ms$

1.1 Distriduted refresh during Read/Write operation

(A) Timing Diagrams

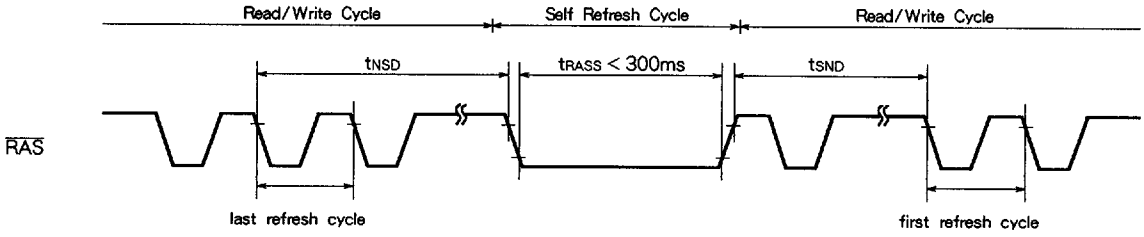


Table 2

Read/Write Cycle	Read/Write→ Self Refresh	Self Refresh→ Read/Write
CBR distributed refresh	$t_{NSD} + t_{SND} \leqq 16.4ms$	
$\overline{RAS}$ only distributed refresh	$t_{NSD} \leqq 16\ \mu s$	$t_{SND} \leqq 16\ \mu s$

(B) Definition of refresh

Definition of CBR distributed refresh

The CBR distributed refresh performs more then 1024 discrete CBR cycles within 16.4 ms.

Definition of $\overline{RAS}$ only distributed refresh

All combination of ten row address signals (A_0~A_9) are selected during 1024 discrete $\overline{RAS}$ only refresh cycles within 16.4 ms.

1.1.1 CBR distributed Refresh

- Switching from read/write operation to self refresh operation. The time interval from the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within t_{NSD} (shown in table 2).
- Switching from self refresh operation to read/write operation. The time interval from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within t_{SND} (shown in table 2).

1.1.2 $\overline{RAS}$ only distributed refresh

- Switching from read/write operation to self refresh operation. The time interval t_{NSD} from the falling edge of $\overline{RAS}$ signal in the last $\overline{RAS}$ only refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 16 μs.
- Switching from self refresh operation to read/write operation. The time interval t_{SND} from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within 16 μs.

1.2 Burst refresh during Read/Write operation

(A) Timing diagram

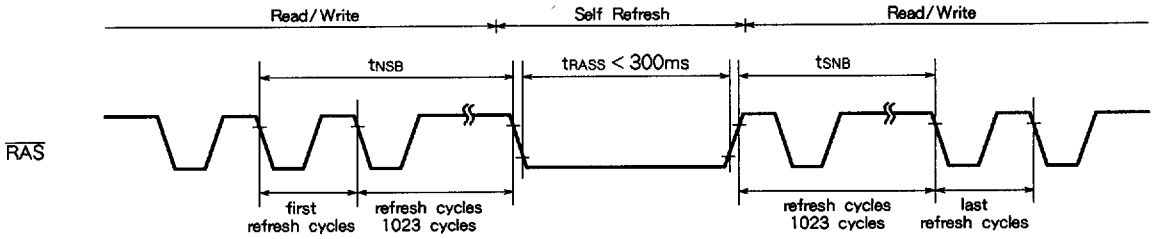


Table 3

Read/Write Cycle	Read/Write→ Self Refresh	Self Refresh→ Read/Write
CBR burst refresh	$t_{NSB} \leqq 16.4ms$	$t_{SNB} \leqq 16.4ms$
$\overline{RAS}$ only burst refresh	$t_{NSB} + t_{SNB} \leqq 16.4ms$	

(B) Definition of burst refresh

Definition of CBR burst refresh

The CBR burst refresh performs more then 1024 continuous CBR cycles within 16.4ms.

Definition of $\overline{RAS}$ only burst refresh

All combination of ten row address signals (A_0~A_9) are selected during 1024 continuous $\overline{RAS}$ only refresh cycles within 16.4 ms.

1.2.1 CBR distributed Refresh

- Switching from read/write operation to self refresh operation. The time interval t_{NSB} from the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 16.4 ms.
- Switching from self refresh operation to read/write operation. The time interval t_{SNB} from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read /write operation period should be set within 16.4 ms.

1.2.2 $\overline{RAS}$ only distributed refresh

- Switching from read/write operation to self refresh operation. The time interval from the falling edge of $\overline{RAS}$ signal in the first $\overline{RAS}$ only refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within t_{NSB} (shown in table 3).
- Switching from self refresh operation to read/write operation. The time interval from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the last $\overline{RAS}$ only refresh cycle during read/ write operation period should be set within t_{SNB} (shown in table 3).

2. In case of $t_{RASS} \geqq 300ms$
(A) Timing diagram

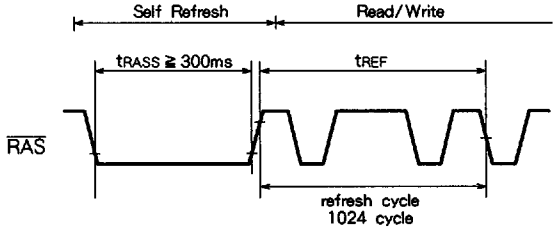


Table 4

Read/Write	Self Refresh→Read/Wirte
CBR distributed refresh $\overline{RAS}$ only distributed refresh CBR burst refresh $\overline{RAS}$ only burst refresh	$t_{REF} \leqq 16.4ms$

(B) Definition of refresh
The same as 1.1-(B) and 1.2-(B)

2.1
Regardless of the refresh (CBR distributed refresh, $\overline{RAS}$ only distributed refresh, CBR burst refresh, $\overline{RAS}$ only burst refresh) during Read/Write operation the minimum of 1024 cycles refresh should be preformed within 16.4 ms from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation.