



No.2057B

LA5316M

Variable Divided
Voltage Generator for LCD

Overview

The LA5316M is a variable divided voltage generator IC for multiple drive of LCD matrix.

Features

- Power supply for variable bias LCD drive (1/5 to 1/13 bias available by on-chip resistances).
- 5 OP amps to deliver 5 voltage outputs.
- Low current dissipation (1.5mA max).
- Miniflat package.
- On-chip variable voltage regulator for V_{REF} .

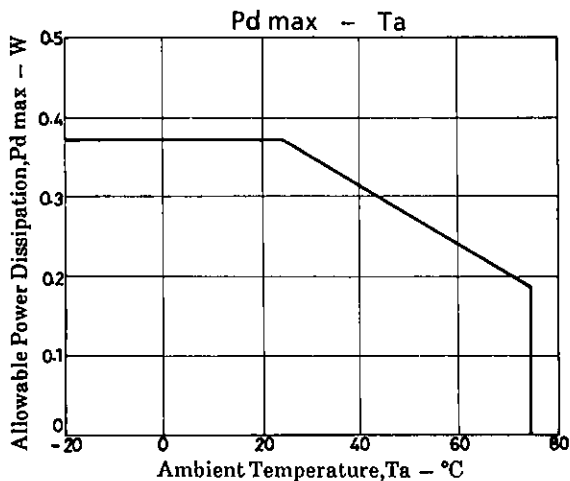
Maximum Ratings at $T_a = 25^\circ\text{C}$

				unit
Maximum Supply Voltage	V_{CC} max	GND- V_{CC}	-35 to 0	V
Maximum Output Current	I_{OUT} max	V1, V2, V3, V4, V5	15	mA
Allowable Power Dissipation	P_d max		370	mW
Operating Temperature	T_{opr}		-20 to +75	$^\circ\text{C}$
Storage Temperature	T_{stg}		-30 to +125	$^\circ\text{C}$

Operating Conditions at $T_a = 25^\circ\text{C}$

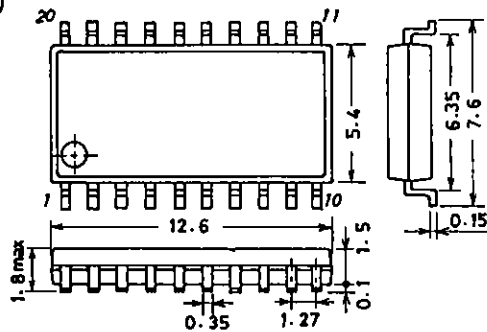
				unit
Supply Voltage	V_{CC} op	GND- V_{CC} : (When $V_1 > -1\text{V}$, I_{IN} is needed.) Note 1	-30 to -10	V
Recommended Input Voltage	V_{REF}	GND- V_{REF} : $V_{REF} \geq V_{CC}$ Note 1	-30 to -6	V
Recommended Input Current	I_{IN}	V_{IN} : $V_1 > -1\text{V}$, current source of I_{IN} : 1V or greater relative to GND	0.2 to 3	mA
Recommended Output Current	I_{OUT1}	V1	-0.1 to +5	mA
	$I_{OUT2,3}$	V2, V3	-5 to +5	mA
	$I_{OUT4,5}$	V4, V5	-10 to +0.1	mA

Note 1: Set V_{CC} , V_{REF} so that $|V_2|$, $|V_{CC}-V_5|$ become 1V or greater.



Package Dimensions 3036B

(unit: mm)



SANYO: MFP20

Operating Characteristics at Ta = 25°C, VCC = -16V				min	typ	max	unit
Current Dissipation	ICC	VIN, GND-VCC, VREF: VCC = VREF = -16V, VIN = GND, RX = 5R				1.5	mA
Output Voltage Ratio 1	Ra1	V2/V1	Vref = -12V VCC = -16V, 1/9 bias (RX = 5R)	1.96	2.00	2.04	
Output Voltage Ratio 2	Ra2	(V5-V3)/(V5-V4)		1.96	2.00	2.04	
Output Voltage Ratio 3	Rb1	V5/V1		8.73	9.00	9.27	
Output Voltage Ratio 4	Rb2	V5/V2		4.37	4.50	4.63	
Output Voltage Ratio 5	Rb3	V5/(V5-V3)		4.37	4.50	4.63	
Output Voltage Ratio 6	Rb4	V5/(V5-V4)		8.73	9.00	9.27	
Internal Resistance Ratio 1	4R	VIN3-RX1	Resistance ratio referenced to R across pins ⑤ and ⑥			4	
Internal Resistance Ratio 2	5R	VIN3-RX2				5	
Internal Resistance Ratio 3	6R	VIN3-RX3				6	
Internal Resistance Ratio 4	7R	VIN3-RX4				7	
Internal Resistance Ratio 5	8R	VIN3-RX5				8	
Internal Resistance Ratio 6	9R	VIN3-RX6				9	
Resistance	R	RX1-RX2: R value when 0.5V is applied across pins ⑤ and ⑥		20			kΩ
Load Regulation 1	ΔV1	V1: +100μA < IOU1 < +5mA				20	mV
Load Regulation 2	ΔV2	V2: +100μA < IOU2 < +5mA				20	mV
Load Regulation 3	ΔV3	V3: +100μA < IOU3 < +5mA				20	mV
Load Regulation 4	-ΔV2	V2: -5mA < IOU2 < -100μA				20	mV
Load Regulation 5	-ΔV3	V3: -5mA < IOU3 < -100μA				20	mV
Load Regulation 6	-ΔV4	V4: -10mA < IOU4 < -100μA				20	mV
Load Regulation 7	-ΔV5	V5: -10mA < IOU5 < -100μA				20	mV
Regulator Voltage	VReg	GND-VReg: Pins ⑦ and ⑧ shorted	-6.5	-6.2	-5.9		V
VReg Load Regulation	ΔVReg	VReg: -5mA < IO < +1mA				50	mV

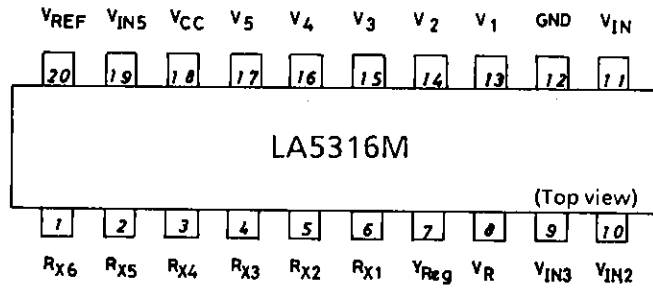
Pin Functions

Pin No.	Pin Name	Function	Remarks
1	RX6	RX pin	Pin ⑩ shorted RX = 9R
2	RX5	RX pin	Pin ⑩ shorted RX = 8R
3	RX4	RX pin	Pin ⑩ shorted RX = 7R
4	RX3	RX pin	Pin ⑩ shorted RX = 6R
5	RX2	RX pin	Pin ⑩ shorted RX = 5R
6	RX1	RX pin	Pin ⑩ shorted RX = 4R
7	VReg	VReg output	For supplying VREF
8	VR	VReg OP amp VIN-	
9	VIN3	V3 input	
10	VIN2	V2 input	
11	VIN	V1 supply (+ supply)	When V1 > -1.0V, VIN is applied. When V1 < -1.0V, this pin is shorted to GND.
12	GND	GND	
13	V1	V1 output	
14	V2	V2 output	
15	V3	V3 output	
16	V4	V4 output	
17	V5	V5 output	
18	VCC	VCC supply (- supply)	
19	VIN5	V5 input	
20	VREF	VREF supply (- supply)	

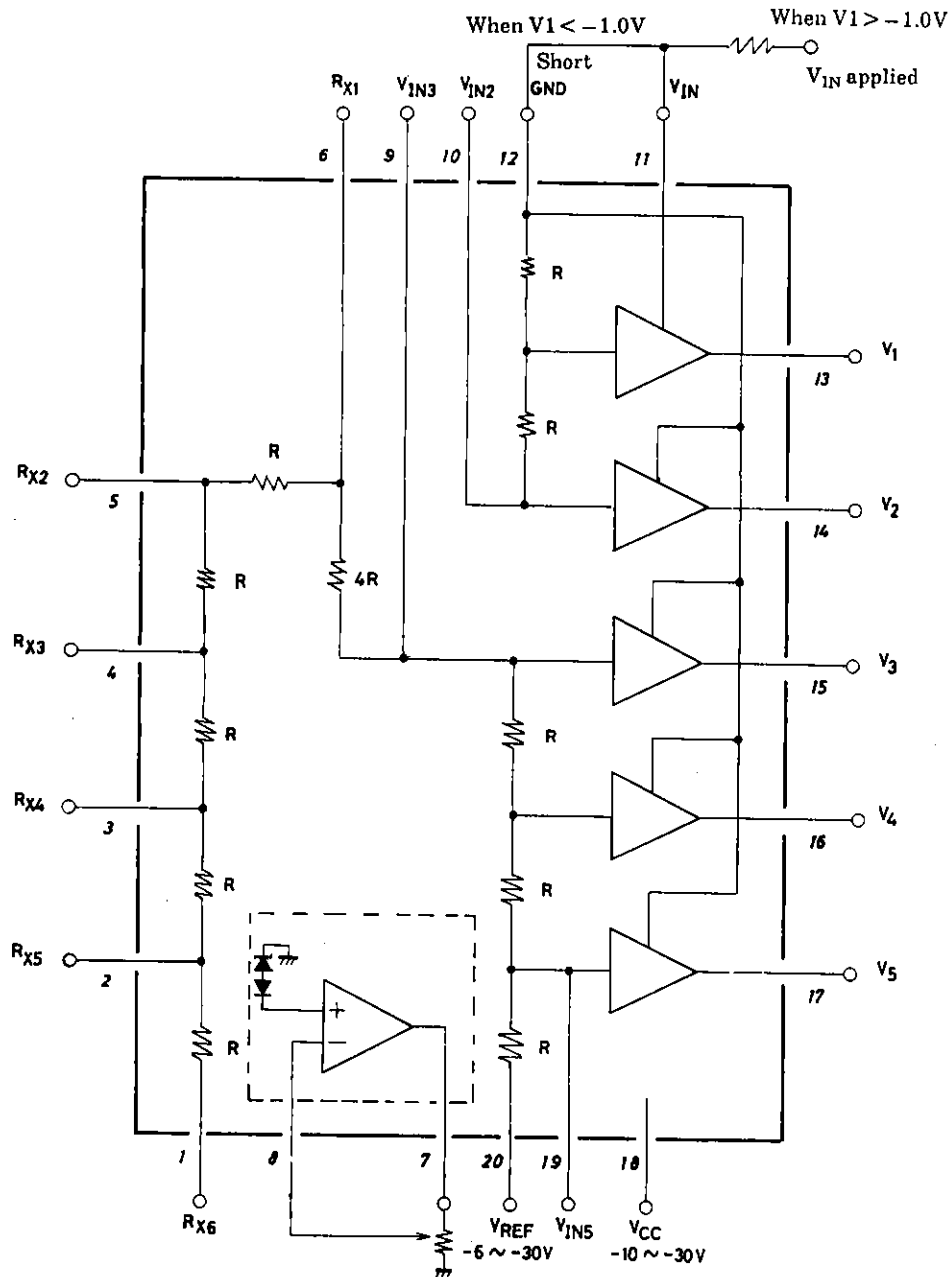
(Note) Do not use the NC pin.

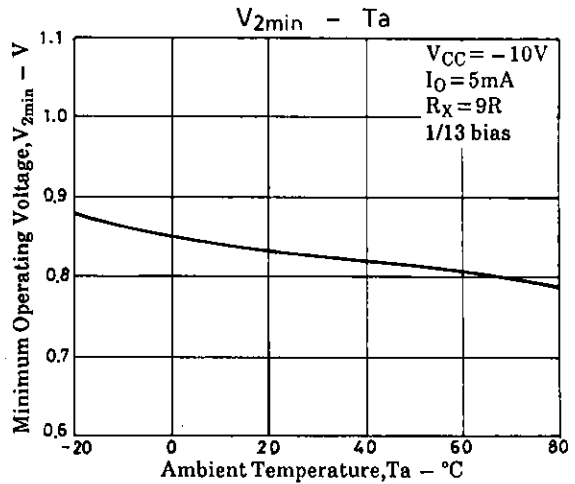
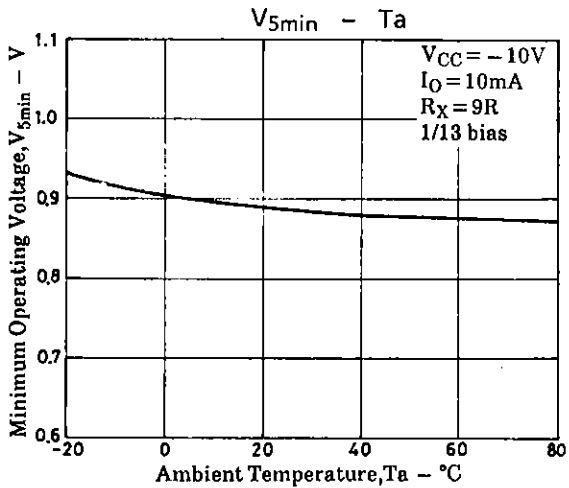
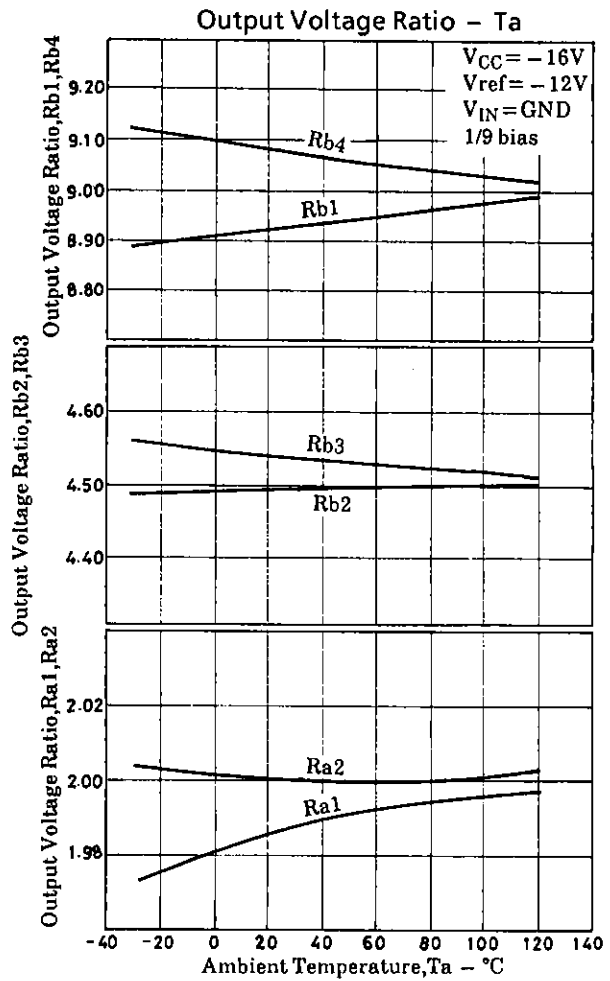
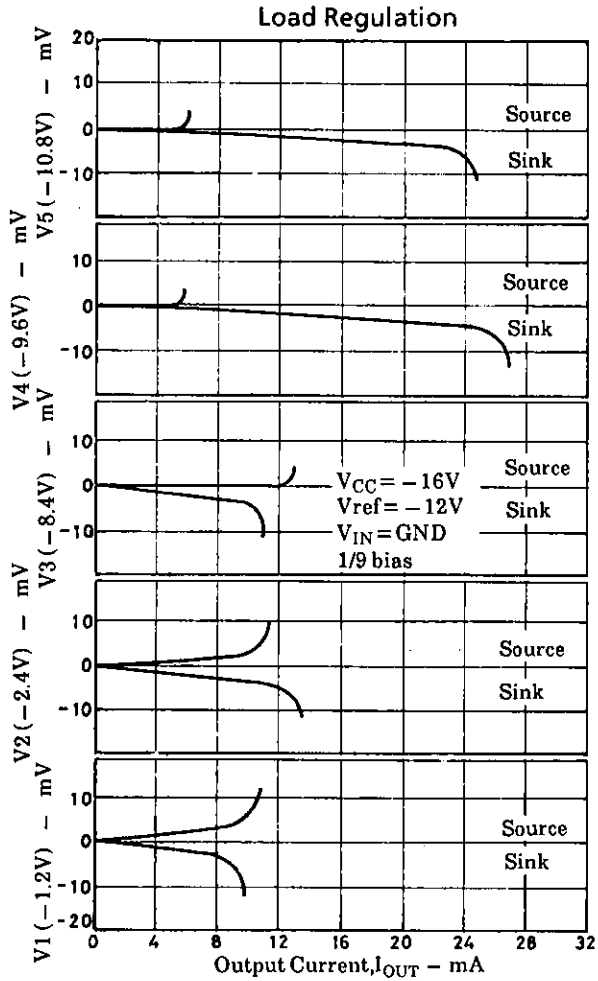
LA5316M

Pin Assignment



Equivalent Circuit Block Diagram





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