

# FAN8006D3

## 4-CH Motor Driver

### Features

- 4-Channel BTL (Balanced transformer-less) driver
- Built-in thermal shutdown circuit
- Built-in power save circuit
- Separated power supply
- Operating supply voltage: 4.5V ~ 13.2V
- Corresponds to 3.3V or 5V DSP

### Description

The FAN8006D3 is a monolithic integrated circuit, suitable for 4-CH motor driver which drives focus actuator, tracking actuator, sled motor and loading motor of a CD-media system.

28-SSOPH-375SG2



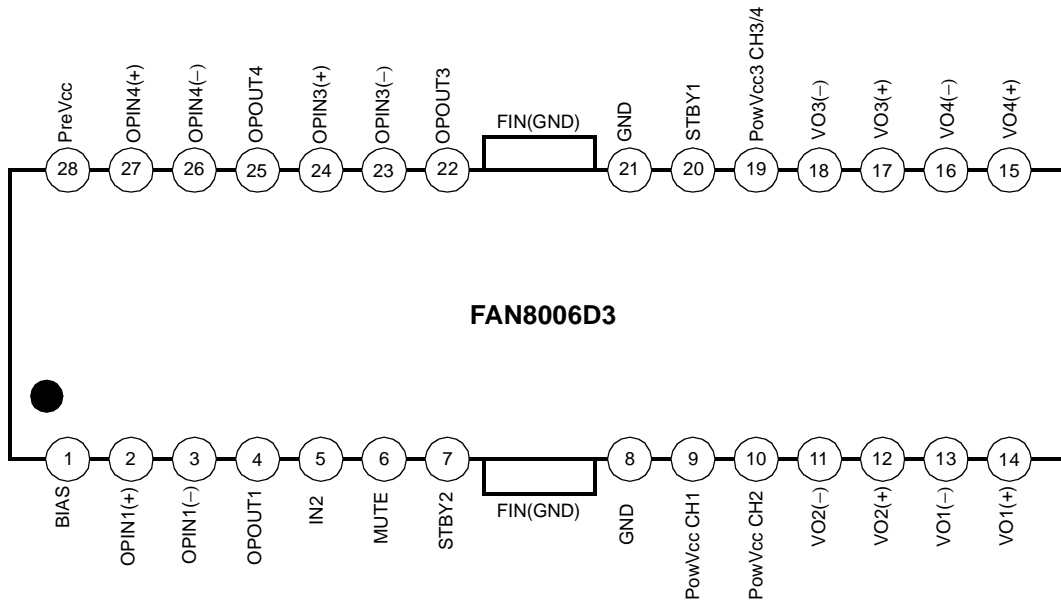
### Target Application

- Compact disk player
- Digital video disk player
- Compact disk ROM

### Ordering Information

Device	Package	Ope. Temp.
FAN8006D3	28-SSOPH-375SG2	-35°C ~ +85°C
FAN8006D3TF	28-SSOPH-375SG2	-35°C ~ +85°C

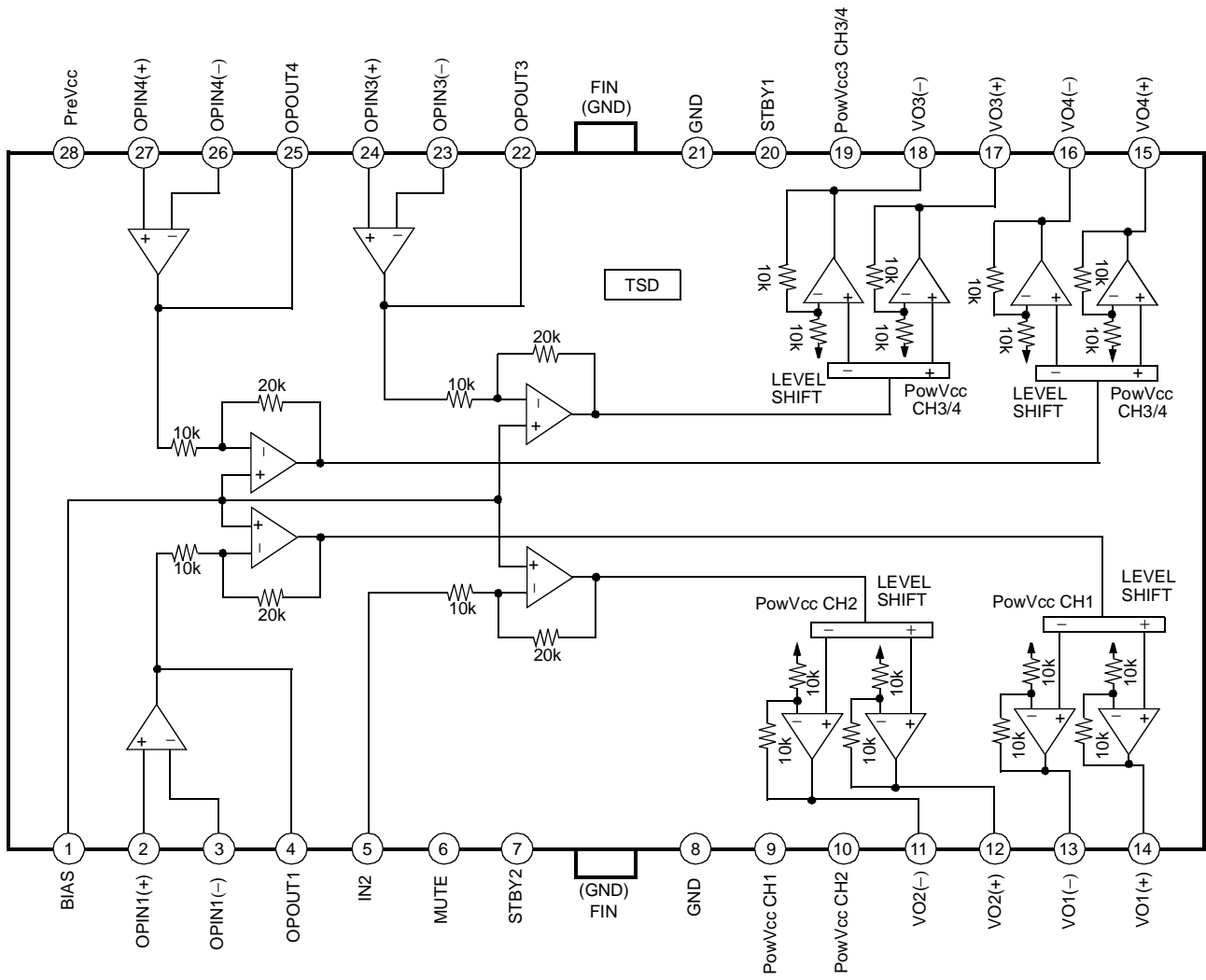
# FAN8006D3 Pin Assignments



## Pin Definitions

Pin Number	Pin Name	I/O	Pin Function Description
1	BIAS	I	Bias voltage input
2	OPIN1(+)	I	Op-amp CH1 input (+)
3	OPIN1(-)	I	Op-amp CH1 input (-)
4	OPOUT1	O	Op-amp CH1 output
5	IN2	I	CH2 input
6	MUTE	I	CH1 mute control when STBY1 is logic high
7	STBY2	I	CH2 standby control
8	GND	-	Signal ground
9	PowVcc1 CH1	-	BTL CH1 power supply
10	PowVcc2 CH2	-	BTL CH2 power supply
11	VO2(-)	O	Drive2 output (-)
12	VO2(+)	O	Drive2 output (+)
13	VO1(-)	O	Drive1 output (-)
14	VO1(+)	O	Drive1 output (+)
15	VO4(+)	O	Drive4 output (+)
16	VO4(-)	O	Drive4 output (-)
17	VO3(+)	O	Drive3 output (+)
18	VO3(-)	O	Drive3 output (-)
19	PowVcc3 CH3/4	-	BTL CH3/4 power supply
20	STBY1	I	Input for CH1/3/4 standby control
21	GND	-	Ground
22	OPOUT3	O	Op-amp CH3 output
23	OPIN3(-)	I	Op-amp CH3 input (-)
24	OPIN3(+)	I	Op-amp CH3 input (+)
25	OPOUT4	O	Op-amp CH4 output
26	OPIN4(-)	I	Op-amp CH4 input (-)
27	OPIN4(+)	I	Op-amp CH4 input (+)
28	PreVcc	-	Vcc for pre block

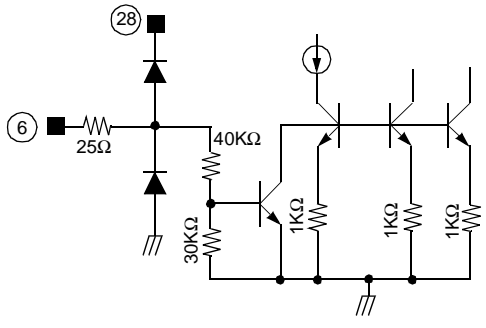
# Internal Block Diagram



## Equivalent Circuits (Continued)

POWER OUTPUT	CHANNEL OPAMP INPUT
CHANNEL OP-AMP OUTPUT	BIAS INPUT
CHANNEL 2 INPUT	STANDBY 1/2 INPUT

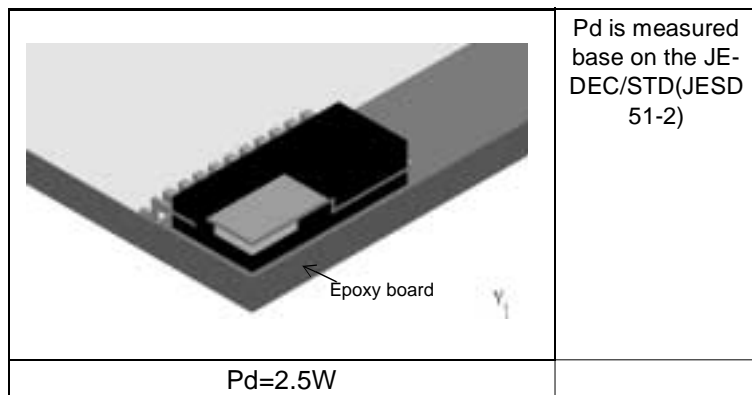
## Equivalent Circuits

MUTE INPUT	
 <p>The diagram shows the MUTE INPUT circuit. It features a 25Ω resistor connected to pin 6. Pin 28 is connected to a diode. The input signal is connected to a 40KΩ resistor. The circuit includes a 30KΩ resistor connected to ground, a 1KΩ resistor connected to the base of a transistor, and three 1KΩ resistors connected to the bases of three other transistors. The transistors are connected to ground and have their emitters grounded. The output of the transistors is connected to a common point, which is also connected to ground.</p>	

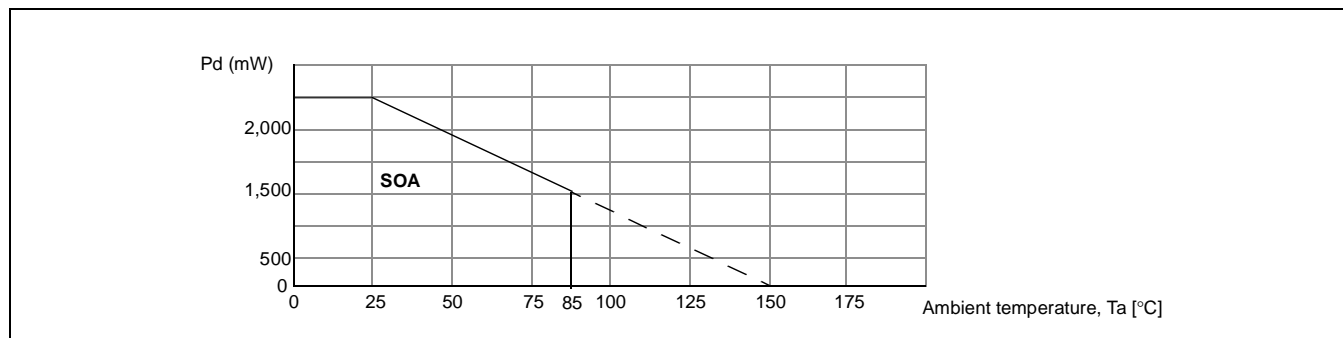
## Absolute Maximum Ratings ( Ta=25°C)

Parameter	Symbol	Value	Unit
Maximum supply voltage	PreV <sub>ccmax</sub>	15	V
Power dissipation	P <sub>D</sub>	2.5 <sup>note</sup>	W
Operating temperature range	T <sub>OPR</sub>	-35 ~ +85	°C
Storage temperature range	T <sub>STG</sub>	-55 ~ +150	°C

### NOTE:



1. Test PCB is single layer PCB which has only 1 signal plane. PCB size is 76mm × 114mm × 1.6mm.
2. Power dissipation is reduced for using above Ta=25°C. It's slope is -20.0mW/°C.
3. Do not exceed P<sub>D</sub> and SOA (Safe Operating Area).



## Recommended Operating Conditions ( Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	PreV <sub>cc</sub>	4.5	-	13.2	V
Supply voltage	PowV <sub>cc</sub> CH1	4.5	-	PreV <sub>cc</sub>	V
Supply voltage	PowV <sub>cc</sub> CH2	4.5	-	PreV <sub>cc</sub>	V
Supply voltage	PowV <sub>cc</sub> CH3/4	4.5	-	PreV <sub>cc</sub>	V

## Electrical Characteristics

(Unless otherwise specified,  $T_a=25^{\circ}\text{C}$ ,  $\text{PreV}_{\text{CC}}=12\text{V}$ ,  $\text{PowV}_{\text{CC}} \text{ CH1}=\text{PowV}_{\text{CC}} \text{ CH3/4}=5\text{V}$ ,  $\text{PowV}_{\text{CC}} \text{ CH2}=12\text{V}$ ,  $\text{RL}=8\Omega, 24\Omega$ )

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Quiescent current1	$I_{\text{CC1}}$	STBY1,2=0.5V,Mute=2V,RL=∞	-	0.1	1	mA
Quiescent current2	$I_{\text{CC2}}$	STBY1,2=2V,Mute=0.5V,RL=∞	-	22.0	31.0	mA
Quiescent current3	$I_{\text{CC3}}$	STBY2=2V, STBY1,Mute=0.5V	-	5.5	8.5	mA
Quiescent current4	$I_{\text{CC4}}$	STBY2=0.5V, STBY1,Mute=2V	-	12.0	17.0	mA
Quiescent current5	$I_{\text{CC5}}$	STBY2,Mute=0.5V,STBY1=2V,	-	17.5	24.5	mA
Mute on voltage	$V_{\text{MON}}$	-	2.0	-	-	V
Mute off voltage	$V_{\text{MOFF}}$	-	-	-	0.5	V
STBY1 on voltage	$V_{\text{STON1}}$	-	-	-	0.5	V
STBY1 off voltage	$V_{\text{STOFF1}}$	-	2.0	-	-	V
STBY2 on voltage	$V_{\text{STON2}}$	-	-	-	0.5	V
STBY2 off voltage	$V_{\text{STOFF2}}$	-	2.0	-	-	V
<b>BTL DRIVE CIRCUIT</b>						
<b>Channel 1,3,4(RL=8Ω)</b>						
Output offset voltage 1,3,4	$V_{\text{OF1,3,4}}$	-	-50	-	+50	mV
Maximum output voltage 1,3,4	$V_{\text{OM1,3,4}}$	-	3.6	4.0	-	V
Closed loop voltage gain 1,3,4	$G_{\text{VC1,3,4}}$	-	17	18	19	dB
Ripple rejection ratio 1,3,4	$\text{RR}_{1,3,4}$	-	-	60	-	dB
Slew rate 1,3,4	$\text{SR}_{1,3,4}$	-	-	1	-	V/μs
<b>Channel 2(RL=24Ω)</b>						
Output offset voltage 2	$V_{\text{OF2}}$	-	-50	-	+50	mV
Maximum output voltage 2	$V_{\text{OM2}}$	-	9.5	10.5	-	V
Closed loop voltage gain 2	$G_{\text{VC2}}$	-	17	18	19	dB
Ripple rejection ratio 2	$\text{RR}_2$	-	-	60	-	dB
Slew rate 2	$\text{SR}_2$	-	-	1	-	V/μs
<b>INPUT OP-AMP</b>						
Input offset voltage	$V_{\text{OFOP}}$	-	-10	-	+10	mV
Input bias current	$I_{\text{BOP}}$	-	-	-	400	nA
High level output voltage	$V_{\text{OHOP}}$	PreVcc=5V, RL=∞	4.5	-	-	V
Low level output voltage	$V_{\text{OLOP}}$	PreVcc=5V, RL=∞	-	-	0.5	V
Output sink current	$I_{\text{SINK}}$	PreVcc=5V, RL=50Ω	3	-	-	mA
Output source current	$I_{\text{SOURCE}}$	PreVcc=5V, RL=50Ω	2	-	-	mA
Open loop voltage gain	$G_{\text{VO}}$	$V_{\text{IN}}=-75\text{dB}$ , 1KHz	-	75	-	dB
Ripple rejection ratio	$\text{RR}_{\text{OP}}$	$V_{\text{IN}}=120\text{KHz}$ , 2VPP	-	60	-	dB
Slew rate	$\text{SR}_{\text{OP}}$	$V_{\text{IN}}=-20\text{dB}$ , 120Hz	-	1	-	V/μs
Common mode rejection ratio	$\text{CMRR}$	$V_{\text{IN}}=-20\text{dB}$ , 1KHz	-	80	-	dB
Common mode input range	$\text{CMIR}$	PreVcc=5V	-0.3	-	4	V



## Application Information

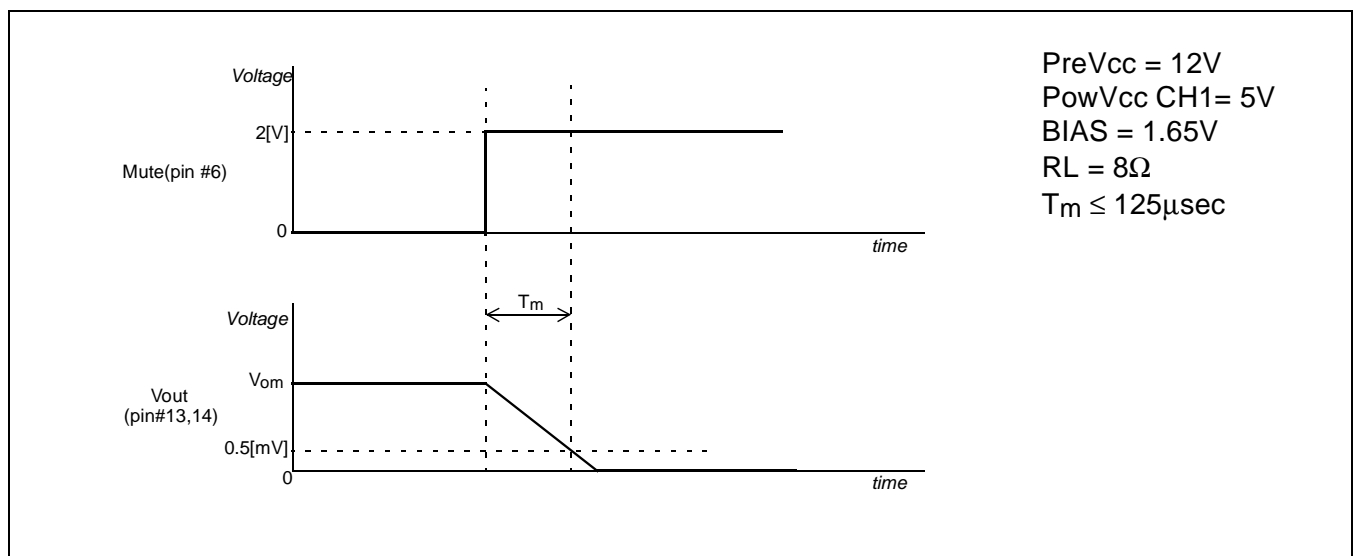
### 1. Standby/Mute Input

FAN8006D3 have 2 independent standby inputs that is , pin #7(STBY2) and pin #20(STBY1), and 1 independent mute input(pin #7). The digital logics of these functions are as below.

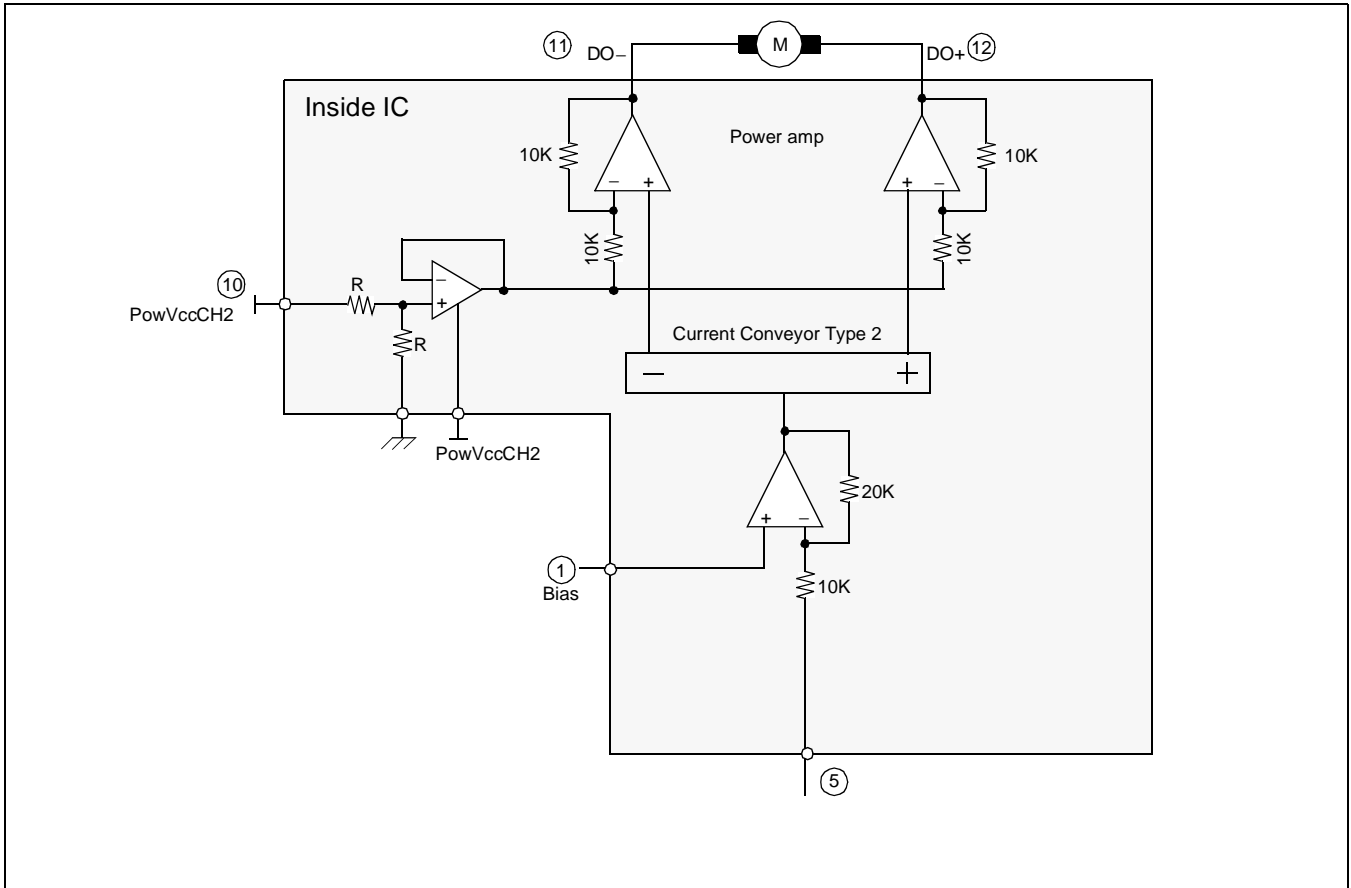
	STBY1=>Low		STBY1=>High		STBY2	
	Mute=>Low	Mute=>High	Mute=>Low	Mute=>High	High	Low
CH 1	standby		operate	high impedance	-	-
CH3/4				operate	-	-
CH2	-	-	-	-	operate	standby

### 2. Mute Timing Chart

If the mute input(pin #6) voltage rises above 2.0V, the output(CH1) current can be muted under normal operating conditions, make sure to open pin #7 or pull it down below 0.5V. Below figure is high impedance mute timing chart.

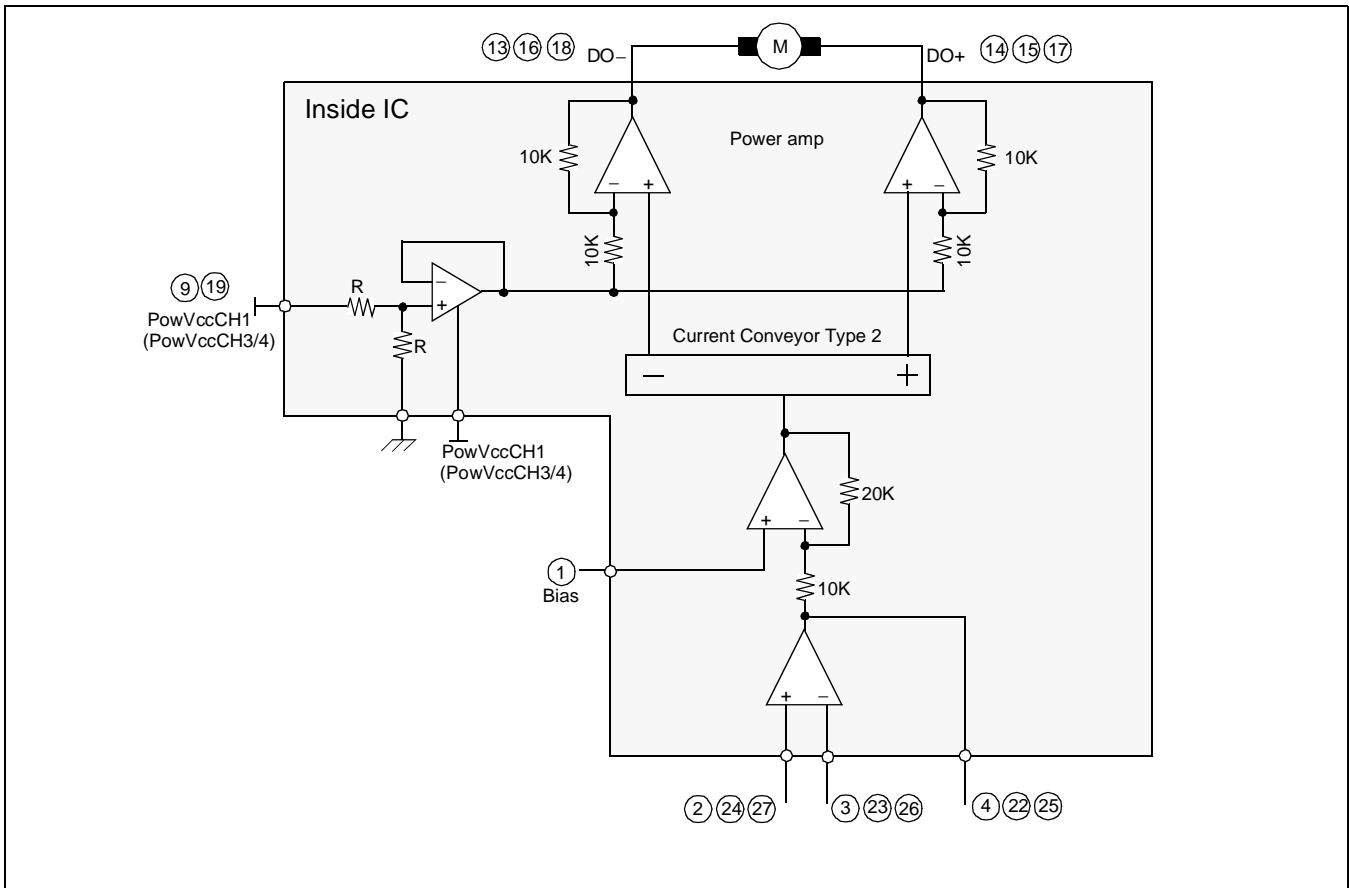


### 3. CH2 Drive Output Schematic



- The reference voltage BIAS is given externally through pin 1.
- The input signal is amplified by  $(20K/10K)$  times and then fed to the current conveyor type 2 circuit and the power amp circuit.
- The power amp circuit produces the differential output voltages and drives two output power amplifier circuits.
- Since the differential gain of the power amplifier is equal to  $2 \times (1 + 10K / 10K)$ , the output signal of the input OP-amp is amplified totally 8.
- If the total gain is insufficient or large, external resistor can be used to adjust the gain.

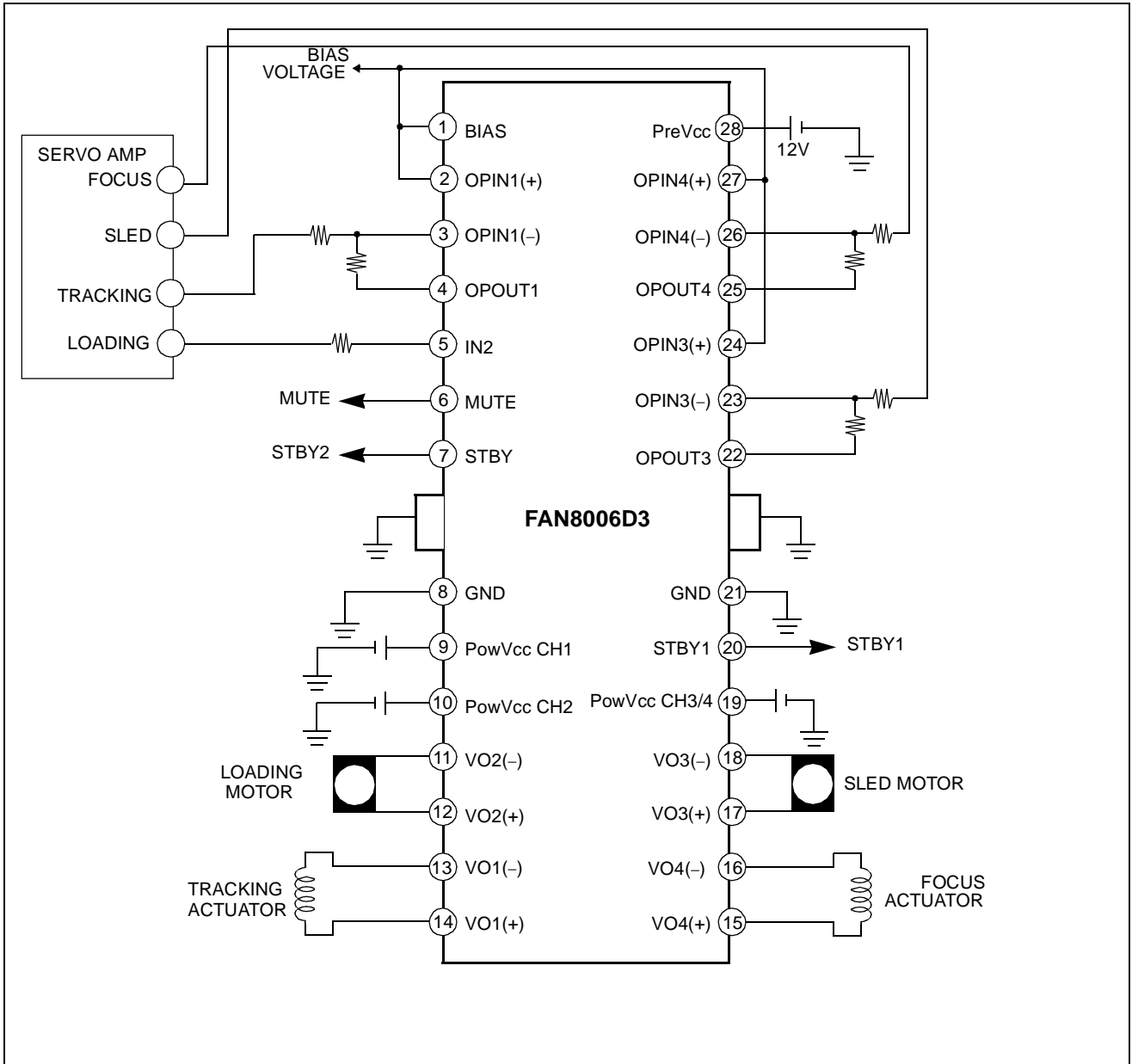
#### 4. CH1/3/4 Drive Output Schematic



- The reference voltage BIAS is given externally through pin 1.
- The input OP-amp output signal is amplified by  $(20K/10K)$  times and then fed to the current conveyor type 2 circuit and the power amp circuit.
- The power amp circuit produces the differential output voltages and drives two output power amplifier circuits.
- Since the differential gain of the power amplifier is equal to  $2 \times (1 + 10K / 10K)$ , the output signal of the input OP-amp is amplified totally 8.
- If the total gain is insufficient or large, the input OP-amp and the external resistors can be used to adjust the gain.

# Application Circuits

(Voltage control mode)





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