BTS 6142D

Smart High-Side Power Switch

PROFET

One Channel, 12 mΩ

Automotive Power

Never stop thinking.

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Smart High-Side Power Switch **BTS 6142D**
PROFET

Product Summary

The BTS 6142D is a one channel high-side power switch in P-TO-252-5-1 package providing embedded protective functions including ReverSave™.

The power transistor is built by a N-channel vertical power MOSFET with charge pump. The design is based on Smart SIPMOS chip on chip technology.

P-TO-252-5-1

Operating voltage	$V_{bb(on)}$	5.5 .. 24 V
Over-voltage protection	$V_{ON(CL)}$	39 V
On-State resistance	$R_{DS(ON)}$	12 mΩ
Nominal load current	$I_{L(nom)}$	7 A
Load current (ISO)	$I_{L(ISO)}$	27 A
Current limitation	$I_{L6(SC)}$	50 A
Stand-by current for whole device with load	$I_{bb(OFF)}$	6 µA

Basic Features

- Very low standby current
- Current controlled input pin
- Improved electromagnetic compatibility (EMC)
- Fast demagnetization of inductive loads
- Stable behavior at under-voltage

Type	Ordering Code	Package
BTS 6142D	SP000074866	P-TO-252-5-1

Protective Functions

- ReverSave™, channel switches on in case of reverse polarity
- Reverse battery protection without external components
- Short circuit protection with latch
- Over-load protection
- Multi-step current limitation
- Thermal shutdown with restart
- Over-voltage protection (including load dump)
- Loss of ground protection
- Loss of V_{bb} protection (with external diode for charged inductive loads)
- Electrostatic discharge protection (ESD)

Diagnostic Functions

- Proportional load current sense (with defined fault signal in case of overload operation, over temperature shutdown and/or short circuit shutdown)
- Open load detection in ON-state by load current sense

Applications

- µC compatible high-side power switch with diagnostic feedback for 12 V grounded loads
- All types of resistive, inductive and capacitive loads
- Most suitable for loads with high inrush currents, so as lamps
- Replaces electromechanical relays, fuses and discrete circuits

1 Overview

The BTS 6142D is a one channel high-side power switch (12 mΩ) in P-TO-252-5-1 power package providing embedded protective functions including ReverSave™.

ReverSave™ is a protection feature that causes the power transistors to switch on in case of reverse polarity. As a result, the power dissipation is reduced.

The BTS 6142D has a current controlled input and offers a diagnostic feedback with load current sense. The design is based on Smart SIPMOS chip on chip technology.

1.1 Block Diagram

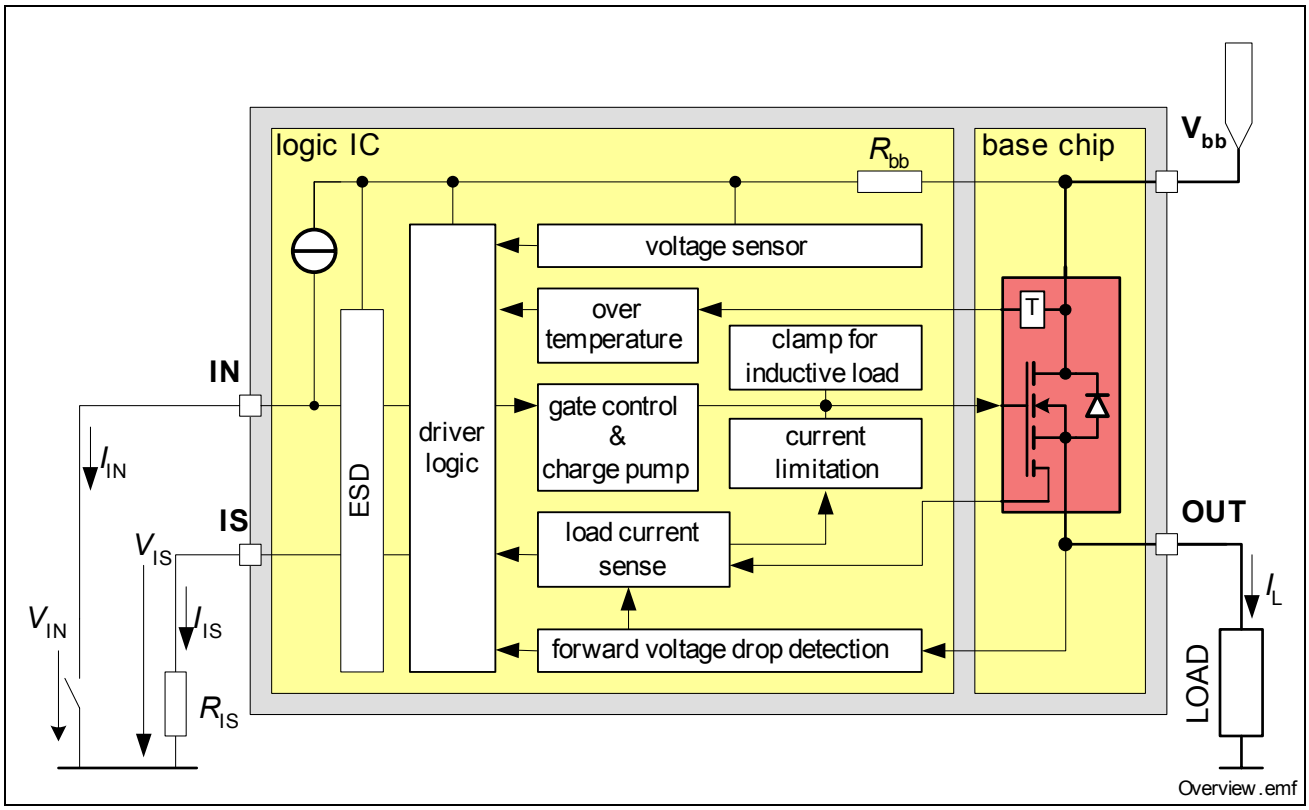


Figure 1 Block Diagram

1.2 Terms

Following figure shows all terms used in this data sheet.

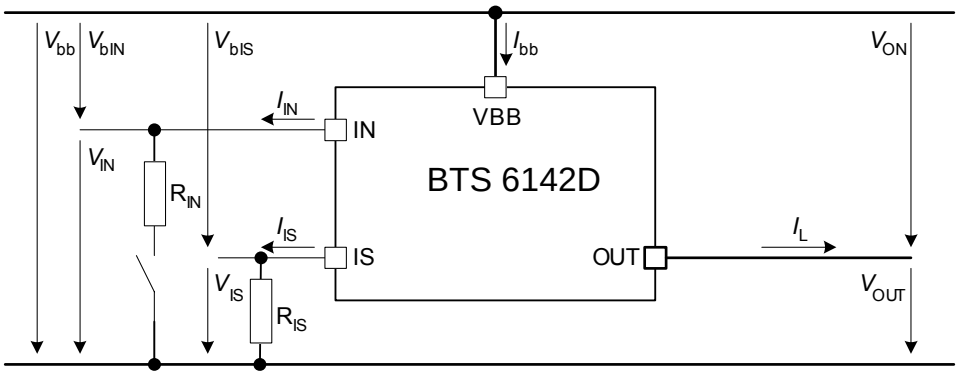


Figure 2 Terms

2 Pin Configuration

2.1 Pin Assignment BTS 6142D

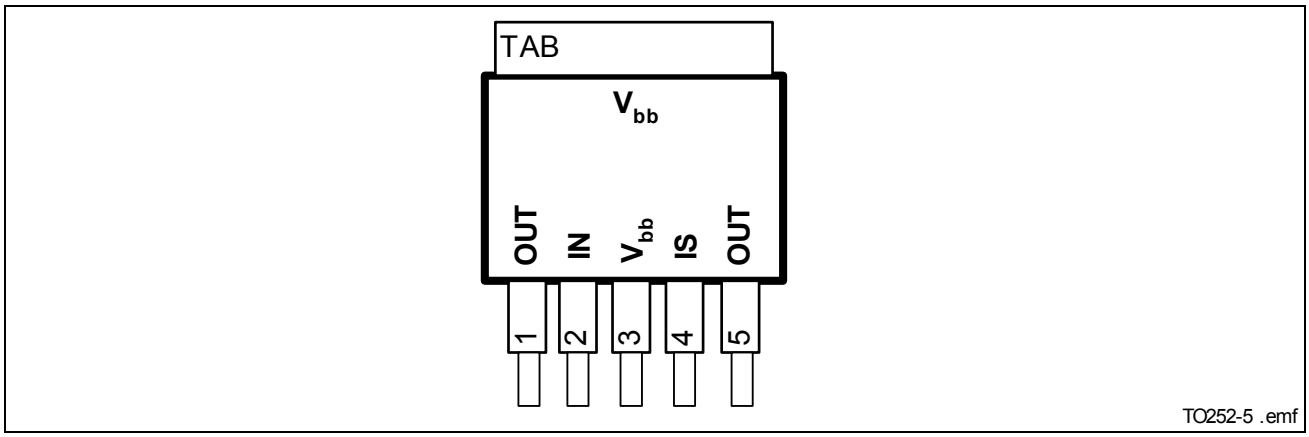


Figure 3 Pin Configuration P-TO-252-5-1

2.2 Pin Definitions and Functions

Pin	Symbol	I/O	Function
1	OUT	O	**Output;** output to the load; pin 1 and 5 must be externally shorted.[1)]
2	IN	I	**Input;** activates the power switch if shorted to ground.
3, Tab	V_{bb}	-	**Supply Voltage;** positive power supply voltage; tab and pin 3 are internally shorted.
4	IS	O	**Sense Output;** Diagnostic feedback; provides at normal operation a sense current proportional to the load current; in case of overload, over temperature and/or short circuit a defined current is provided (see **Table 1 "Truth Table" on Page 23**).
5	OUT	O	**Output;** output to the load; pin 1 and 5 must be externally shorted.[1)]

[1)] Not shorting all outputs will considerably increase the on-state resistance, reduce the peak current capability, the clamping capability and decrease the current sense accuracy.

3 Electrical Characteristics

3.1 Maximum Ratings

Stresses above the ones listed here may cause permanent damage to the device. Exposure to maximum rating conditions for extended periods may affect device reliability.

T_j = 25 °C (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Test Conditions
			min.	max.		
Supply Voltage						
3.1.1	Supply voltage	V_{bb}	-16	38	V	-
3.1.2	Supply voltage for full short circuit protection (single pulse) (T_j = -40°C .. 150°C) [1]	$V_{bb(SC)}$	0	24	V	–
3.1.3	Supply Voltage for Load Dump protection [2]	$V_{bb(LD)}$	-	45	V	R_I = 2 Ω R_L = 1.5 Ω
Logic Pins						
3.1.4	Voltage at input pin	$V_{b,IN}$	-16	63	V	-
3.1.5	Current through input pin	I_{IN}	-140	15	mA	-
3.1.6	Voltage at current sense pin	$V_{b,IS}$	-16	56	V	-
3.1.7	Current through sense pin	I_{IS}	-140	15	mA	-
3.1.8	Input voltage slew rate [3]	dV_{bIN}/dt	-20	20	V/µs	-
Power Stages						
3.1.9	Load current [4]	I_L	-	$I_{Lx(SC)}$	A	-
3.1.10	Maximum energy dissipation per channel (single pulse)	E_{AS}	-	0.25	J	$I_{L(0)}$ = 20 A $T_{j(0)}$ = 150°C
3.1.11	Total power dissipation (DC) for whole device	P_{tot}	-	50	W	T_C = 85 °C $T_j \leq$ 150 °C
Temperatures						
3.1.12	Junction temperature	T_j	-40	150	°C	-
3.1.13	Storage temperature	T_{stg}	-55	150	°C	-

T_j = 25 °C (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Test Conditions
			min.	max.		
ESD Susceptibility						
3.1.14	ESD susceptibility HBM	V_{ESD}	-3	3	kV	according to EIA/JESD 22-A 114B

1) Short circuit is defined as a combination of remaining resistances and inductances. See **Figure 13**.

2) Load Dump is specified in ISO 7637, R_I is the internal resistance of the Load Dump pulse generator

3) Slew rate limitation can be achieved by means of using a series resistor for the small signal driver or in series in the input path. A series resistor R_{IN} in the input path is also required for reverse operation at V_{bb}≤-16V. See also **Figure 14**.

4) Current limitation is a protection feature. Operation in current limitation is considered as “outside” normal operating range. Protection features are not designed for continuous repetitive operation.

4 Block Description and Electrical Characteristics

4.1 Power Stages

The power stage is built by a N-channel vertical power MOSFET (DMOS) with charge pump.

4.1.1 Input Circuit

Figure 4 shows the input circuit of the BTS 6142D. The current source to V_{bb} ensures that the device switches off in case of open input pin. The zener diode protects the input circuit against ESD pulses.

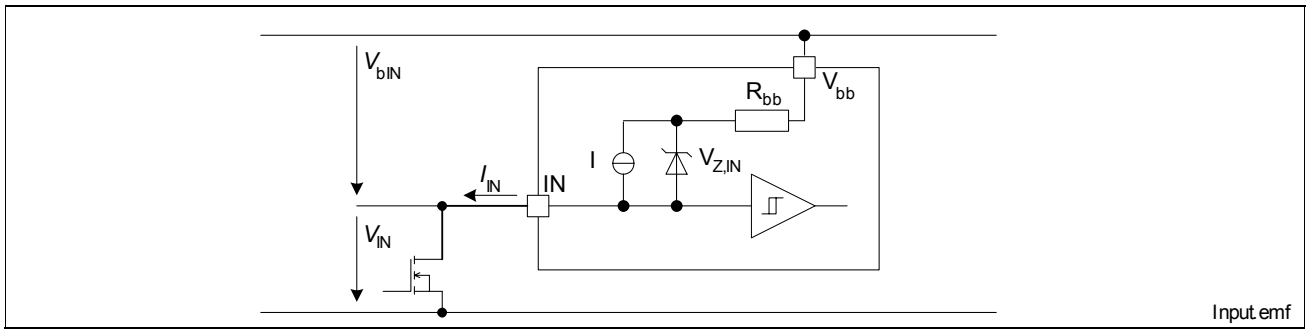


Figure 4 Input Circuit

A high signal at the required external small signal transistor pulls the input pin to ground. A logic supply current I_{IN} is flowing and the power DMOS switches on with a dedicated slope, which is optimized in terms of EMC emission.

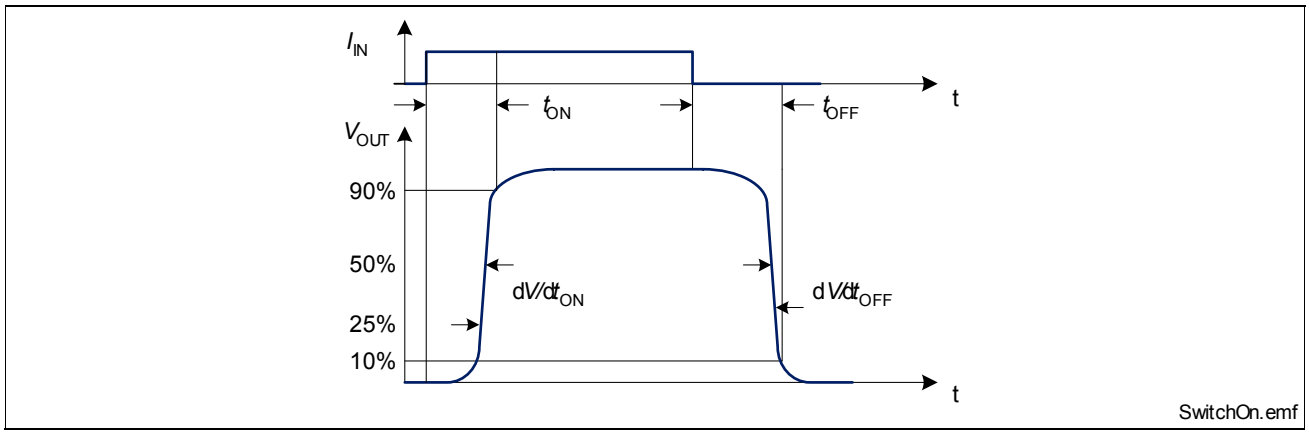


Figure 5 Switching a Load (resistive)

4.1.2 Output On-State Resistance

The on-state resistance $R_{DS(ON)}$ depends on the supply voltage as well as the junction temperature T_j. **Figure 6** shows these dependencies for the typical on-state resistance. The on-state resistance in reverse polarity mode is described in **Section 4.2.3**.

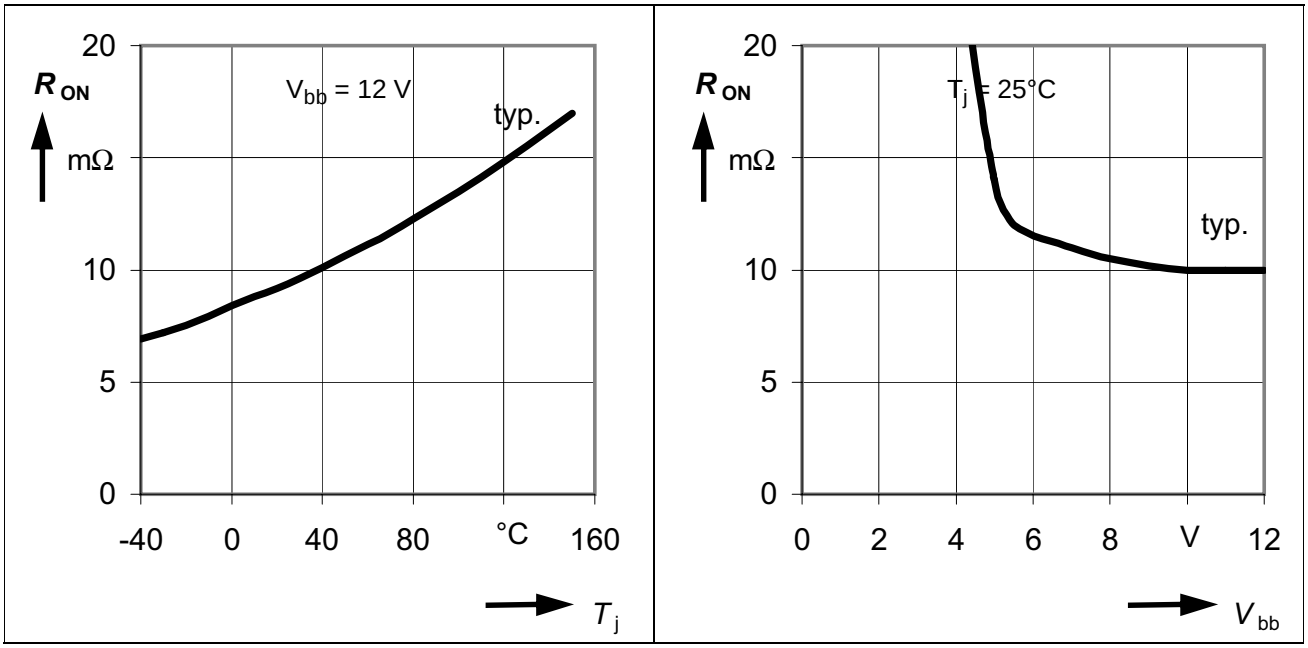


Figure 6 Typical On-State Resistance

At small load currents the resistance is artificially increased to improve current sense accuracy. Therefore the forward voltage drop V_{ON} at small load currents is no more proportional to the load current I_L , but is controlled by an internal “two level controller” to remain clamped to a defined value $V_{ON(NL)}$. **Figure 7** shows the dependency for a typical device.

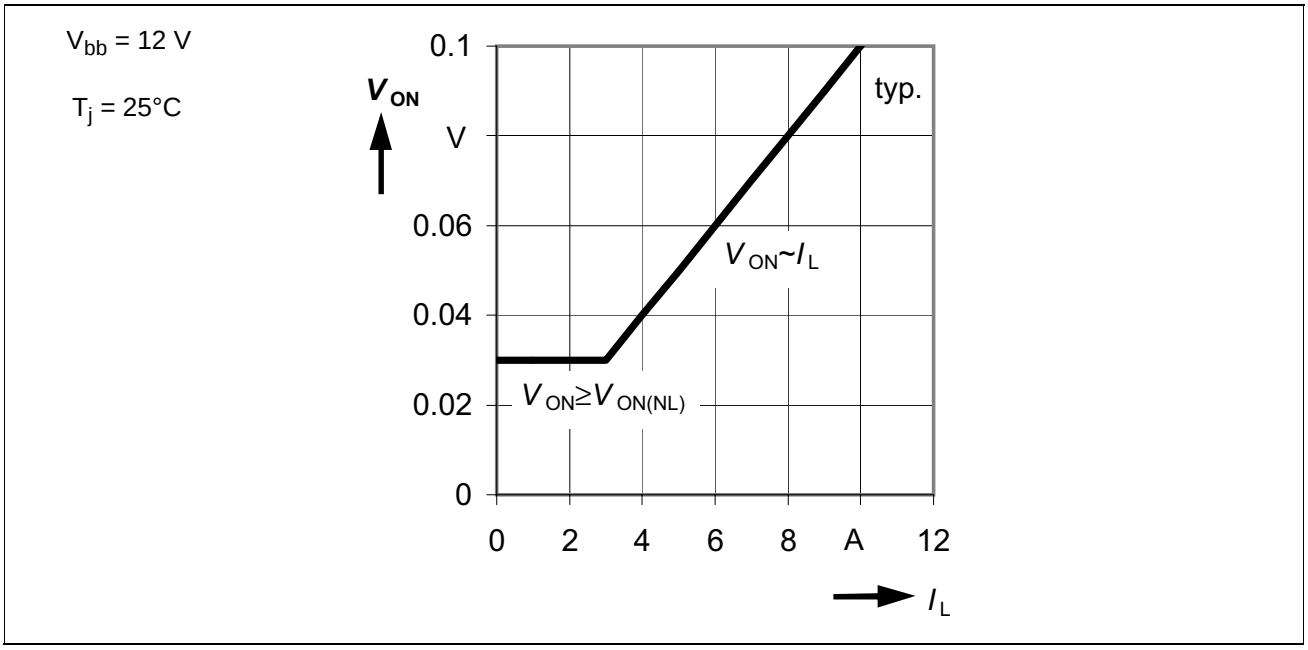


Figure 7 Typical Output Voltage Drop Limitation

4.1.3 Output Inductive Clamp

When switching off inductive loads, the output voltage V_{OUT} drops below ground potential due to the involved inductance ($-di_L/dt = -v_L/L$; $-V_{OUT} \cong -V_L$).

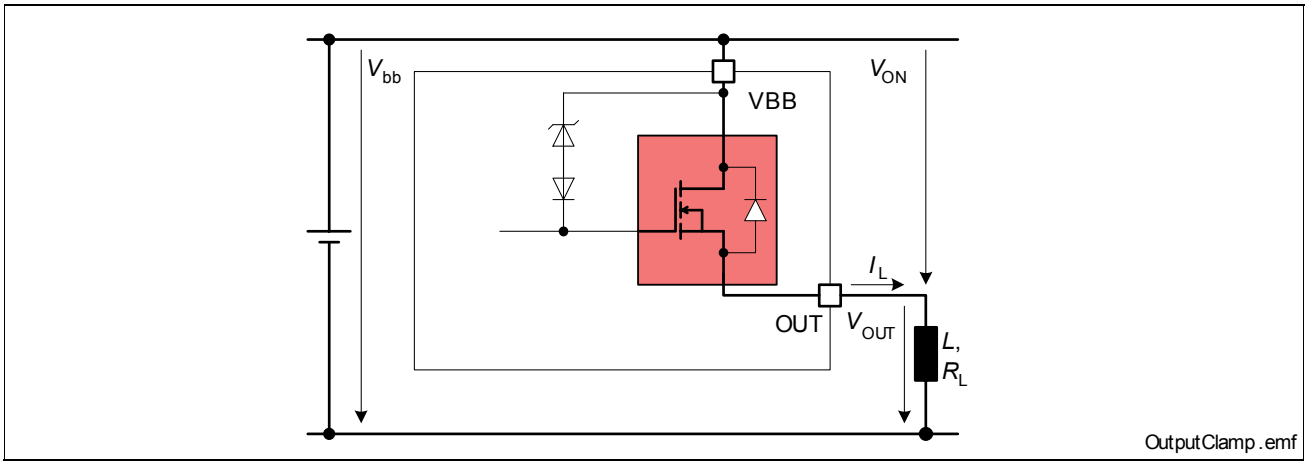


Figure 8 Output Clamp

To prevent destruction of the device, there is a voltage clamp mechanism implemented that keeps the voltage drop across the device at a certain level ($V_{ON(CL)}$). See **Figure 8** and **Figure 9** for details. The maximum allowed load inductance is limited.

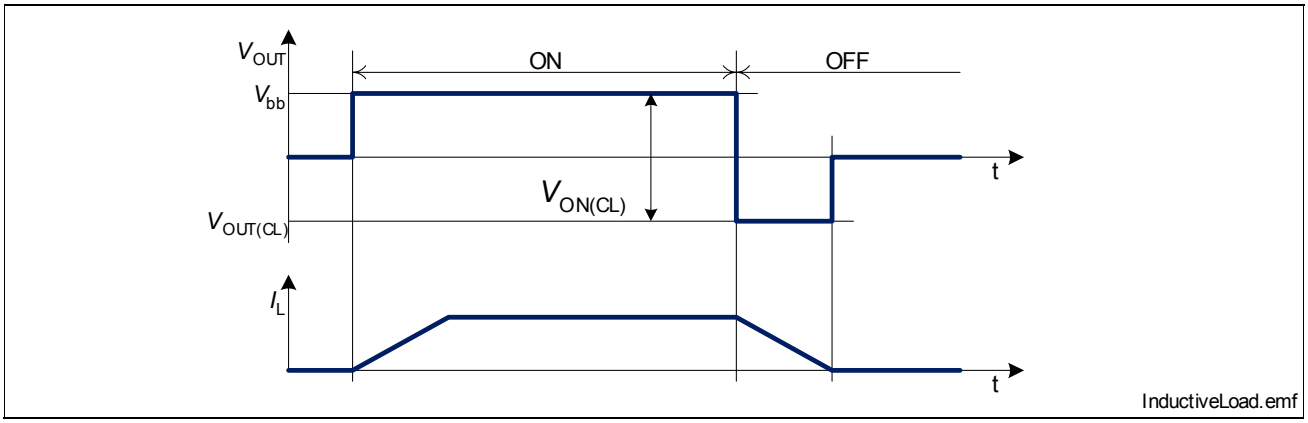


Figure 9 Switching an Inductance

Maximum Load Inductance

While de energizing inductive loads, energy has to be dissipated in the BTS 6142D. This energy can be calculated via the following equation:

$$E = V_{ON(CL)} \cdot \left[\frac{V_{bb} - |V_{ON(CL)}|}{R_L} \cdot \ln\left(1 + \frac{R_L \cdot I_L}{|V_{ON(CL)}| - V_{bb}}\right) + I_L \right] \cdot \frac{L}{R_L}$$

In the event of de-energizing very low ohmic inductances ($R_L \approx 0$) the following, simplified equation can be used:

$$E = \frac{1}{2} L I_L^{\,2} \cdot \frac{|V_{ON(CL)}|}{|V_{ON(CL)}| - V_{bb}}$$

The energy, which is converted into heat, is limited by the thermal design of the component. For given starting currents the maximum allowed inductance is therefore limited. See **Figure 10** for the maximum allowed inductance at V_{bb}=12V.

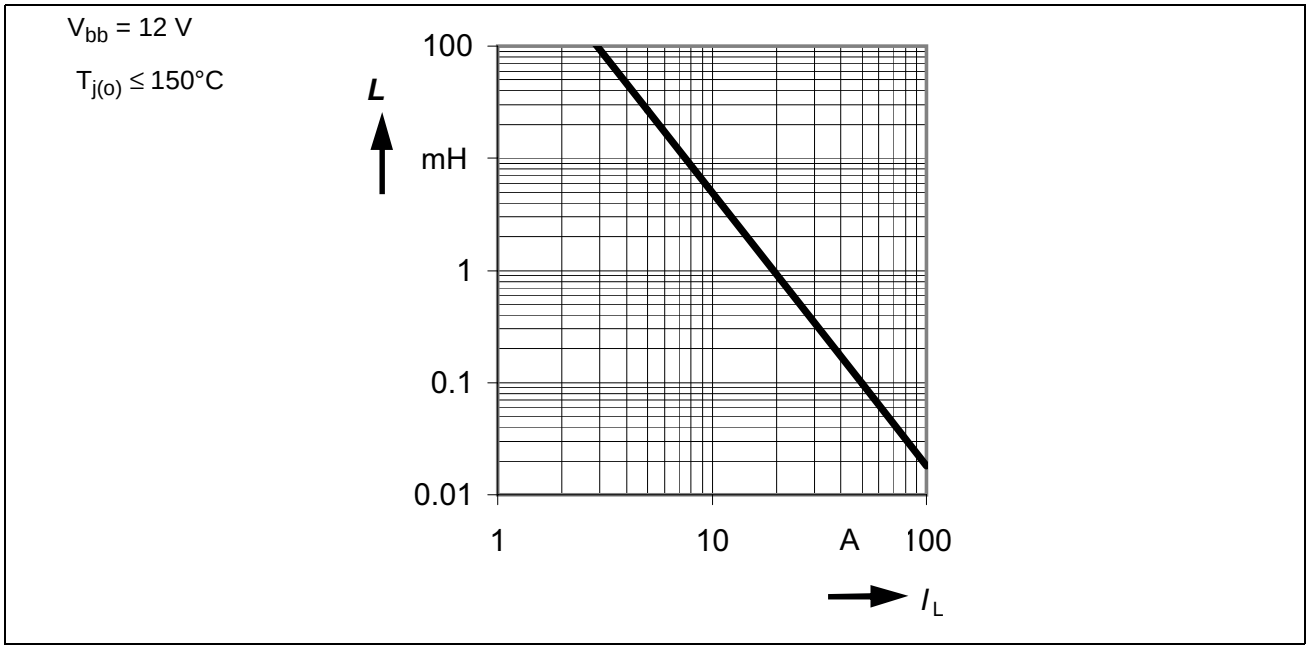


Figure 10 Maximum load inductance for single pulse, $T_{j,Start}$ = 150°C

4.1.4 Electrical Characteristics

V_{bb} = 12 V, T_j = 25 °C (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
General							
4.1.1	Operating voltage	V_{bb}	5.5	-	38	V	V_{IN} = 0 V T_j = -40..150 °C
4.1.2	Undervoltage shutdown [1]	$V_{bIN(u)}$	-	2.5	3.5	V	-
4.1.3	Undervoltage restart of charge pump	$V_{bb(ucp)}$	-	4	5.5	V	-
4.1.4	Operating current	I_{IN}	-	1.4	2.2	mA	T_j = -40..150 °C
4.1.5	Stand-by current T_j = -40 °C, T_j = 25 °C $T_j \leq$ 120 °C [1] T_j = 150 °C	$I_{bb(OFF)}$	 - - -	 3 3 9	 6 6 16	µA	I_{IN} = 0 A
Input characteristics							
4.1.6	Input current for turn-on	$I_{IN(on)}$	-	1.4	2.2	mA	$V_{bIN} \geq V_{bb(ucp)} - V_{IN}$, T_j = -40 … 150 °C
4.1.7	Input current for turn-off	$I_{IN(off)}$	-	-	30	µA	T_j = -40 … 150 °C
Output characteristics							
4.1.8	On-state resistance T_j=25°C T_j=150°C V_{bb}=5.5V, T_j=25°C V_{bb}=5.5V, T_j=150°C	$R_{DS(ON)}$	 - - - -	 10 17 12 22	 12 22 17 29	mΩ	V_{IN}=0V, I_L=7.5A, (Tab to pin 1 and 5)
4.1.9	Output voltage drop limitation at small load currents	$V_{ON(NL)}$	-	30	65	mV	T_j = -40..150 °C
4.1.10	Nominal load current (Tab to pin1 & 5) [2] [3]	$I_{L(nom)}$	7	8.5	-	A	T_a = 85 °C $V_{ON} \leq$ 0.5 V, $T_j \leq$ 150 °C
	ISO load current (Tab to pin 1 & 5) [3]	$I_{L(ISO)}$	27	33	-	A	T_c = 85 °C $V_{ON} \leq$ 0.5 V, $T_j \leq$ 150 °C

V_{bb} = 12 V, T_j = 25 °C (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
4.1.11	Output clamp	$V_{ON(CL)}$	39	42	-	V	I_L = 40 mA
4.1.12	Inverse current output voltage drop [1) 4)] (Tab to pin 1 and 5) T_j = 25 °C T_j = 150 °C	$-V_{ON(inv)}$	 - -	 800 600	 - -	mV	I_L = -7.5 A, R_{IS} = 1 kΩ
Timings							
4.1.13	Turn-on time to 90% V_{bb}	t_{ON}	-	250	600	µs	R_L = 2.2 Ω, T_j = -40 … 150 °C
4.1.14	Turn-off time to 10% V_{bb}	t_{OFF}	-	250	600	µs	R_L = 2.2 Ω, T_j = -40 … 150 °C
4.1.15	Turn-on delay after inverse operation [1)] $V_{IN(inv)} = V_{IN(fwd)} = 0$ V	$t_{d(inv)}$	-	1	-	ms	$V_{bb} > V_{OUT}$
4.1.16	Slew rate On 25% to 50% V_{bb}	dV/dt_{ON}	-	0.3	0.7	V/µs	R_L = 2.2 Ω, T_j = -40 … 150 °C
4.1.17	Slew rate Off 50% to 25% V_{bb}	$-dV/dt_{OFF}$	-	0.3	0.7	V/µs	R_L = 2.2 Ω, T_j = -40 … 150 °C
Thermal Resistance							
4.1.18	Junction to case [1)]	R_{thjc}	-	-	1.3	K/W	-
4.1.19	Junction to ambient [1)] free air device on PCB [2)]	R_{thja}	 - -	 80 45	 - 55	K/W	-

1) Not subject to production test, specified by design

2) Device mounted on PCB (50 mm x 50 mm x 1.5mm epoxy, FR4) with 6 cm^2 copper heatsinking area (one layer, 70 µm thick) for V_{bb} connection. PCB is vertical without blown air.

3) Not subject to production test, parameters are calculated from $R_{DS(ON)}$ and R_{th}

4) Permanent Inverse operation results eventually in a current flow via the intrinsic diode of the power DMOS. In this case the device switches on with a time delay $t_{d(inv)}$ after the transition from inverse to forward mode. A sense current $I_{IS(fault)}$ can be provided by the pin IS until standard forward operation is reached.

Note: Characteristics show the deviation of parameter at the given supply voltage and junction temperature. Typical values show the typical parameters expected from manufacturing.

4.2 Protection Functions

The device provides embedded protective functions. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are neither designed for continuous nor repetitive operation.

4.2.1 Over-Load Protection

The load current I_L is limited by the device itself in case of over-load or short circuit to ground. There are multiple steps of current limitation $I_{Lx(SC)}$ which are selected automatically depending on the voltage drop V_{ON} across the power DMOS. Please note that the voltage at the OUT pin is V_{bb} - V_{ON}. **Figure 11** shows the dependency for a typical device.

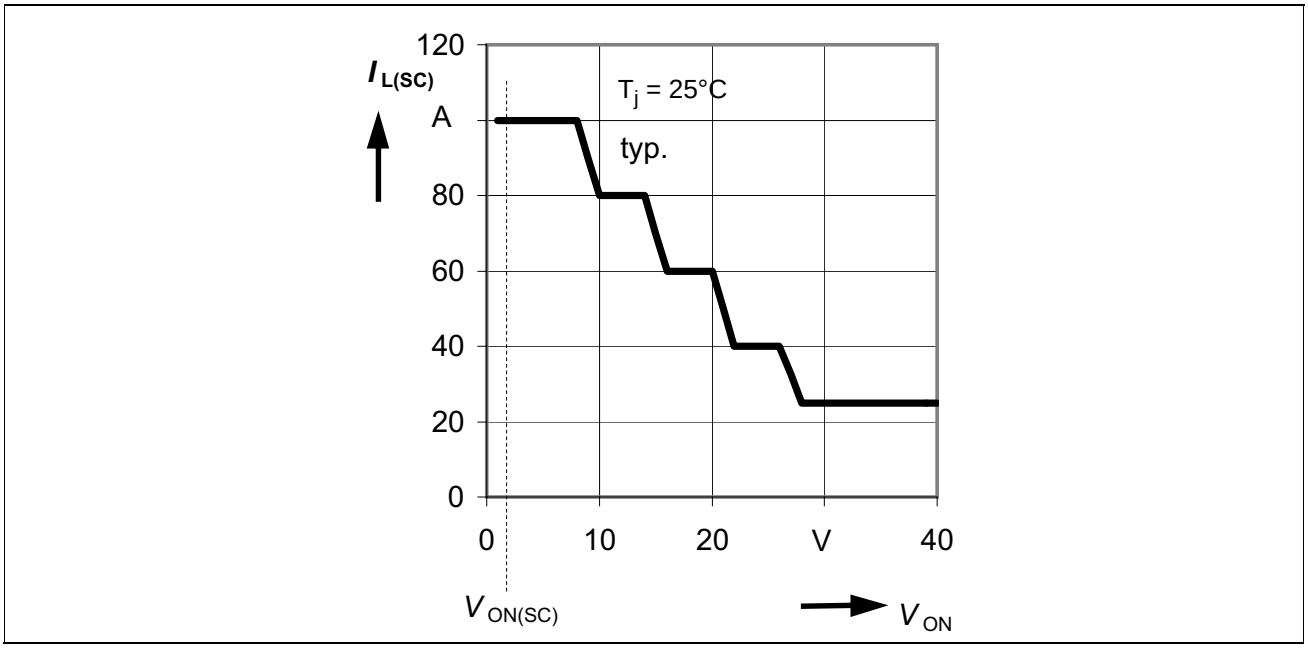


Figure 11 Typical Current Limitation

Depending on the severity of the short condition as well as on the battery voltage the resulting voltage drop across the device varies.

Whenever the resulting voltage drop V_{ON} exceeds the short circuit detection threshold $V_{ON(SC)}$, the device will switch off immediately and latch until being reset via the input. The $V_{ON(SC)}$ detection functionality is activated, when V_{bIN}>10V typ. and the blanking time $t_{d(SC1)}$ expired after switch on.

In the event that either the short circuit detection via $V_{ON(SC)}$ is not activated or that the on chip temperature sensor senses over-temperature before the blanking time $t_{d(SC1)}$ expired, the device switches off resulting from over-temperature detection. After cooling down with thermal hysteresis, the devices switches on again. Please refer to **Figure 12** for details.

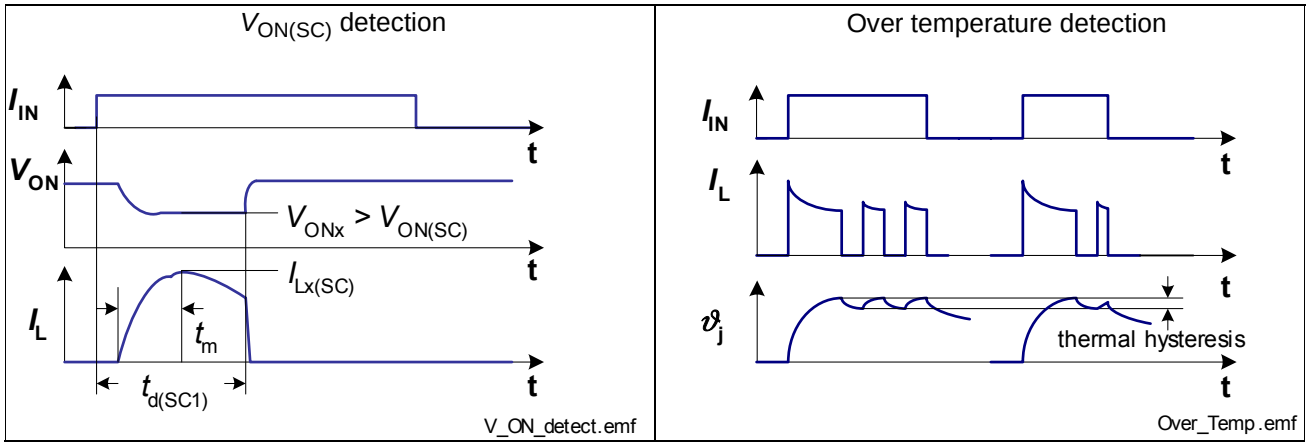


Figure 12 Overload Behavior

4.2.2 Short circuit impedance

The capability to handle single short circuit events depends on the battery voltage as well as on the primary and secondary short impedance. **Figure 13** outlines allowable combinations for a single short circuit event of maximum, secondary inductance for given secondary resistance.

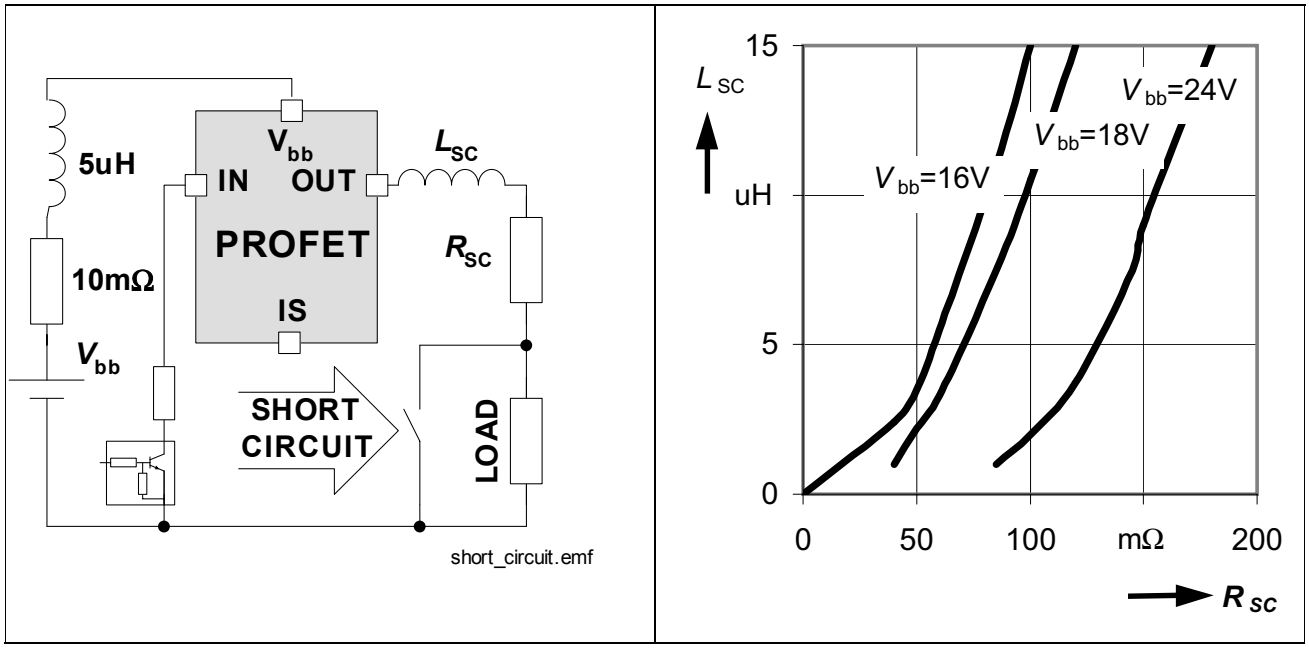


Figure 13 Short circuit

4.2.3 Reverse Polarity Protection - Reversave™

The device can not block a current flow in reverse battery condition. In order to minimize power dissipation, the device offers Reversave™ functionality. In reverse polarity condition the channel will be switched on provided a sufficient gate to source voltage is generated $V_{GS} \approx V_{Rbb}$. Please refer to **Figure 14** for details.

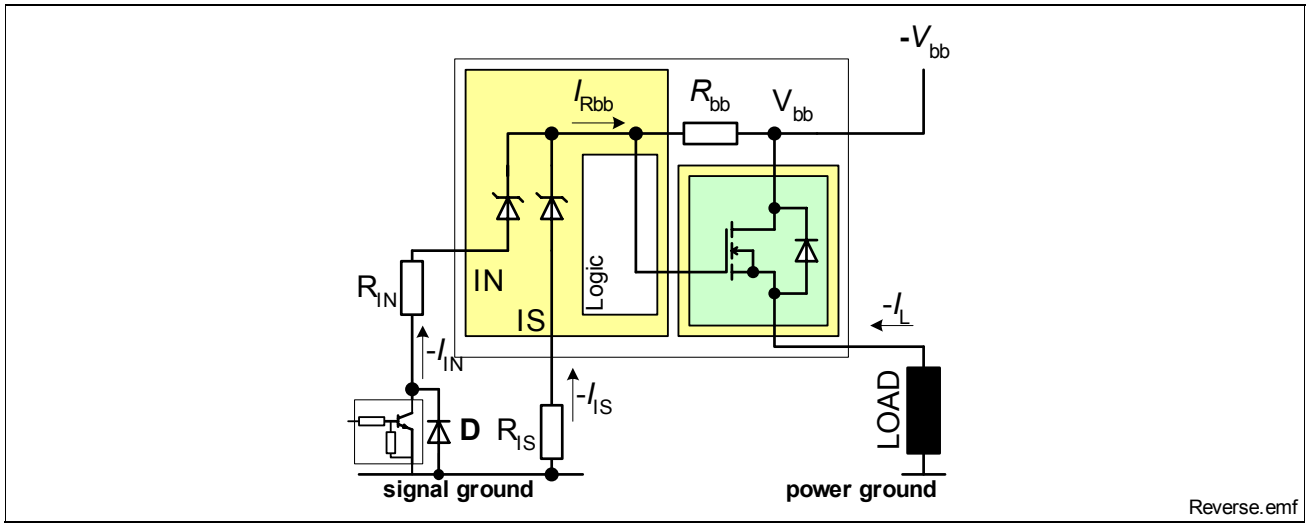


Figure 14 Reverse battery protection

Additional power is dissipated by the integrated R_{bb} resistor. Use following formula for estimation of overall power dissipation $P_{diss(rev)}$ in reverse polarity mode.

$$P_{diss(rev)} \approx R_{ON(rev)} \cdot I_L^2 + R_{bb} \cdot I_{Rbb}^2$$

For reverse battery voltages up to V_{bb} <16V the pin IN or the pin IS should be low ohmic connected to signal ground. This can be achieved e.g. by using a small signal diode D in parallel to the input switch or by using a small signal MOSFET driver. For reverse battery voltages higher then V_{bb} >16V an additional resistor R_{IN} is recommended. For reverse battery voltages higher then V_{bb} >16 the overall current through R_{bb} should be about 80mA.

$$\frac{1}{R_{IN}} + \frac{1}{R_{bb}} = \frac{0{,}08\text{A}}{|V_{bb}| - 12\text{V}}$$

Note: No protection mechanism is active during reverse polarity. The IC logic is not functional.

4.2.4 Over-Voltage Protection

Beside the output clamp for the power stage as described in **Section 4.1.3** there is a clamp mechanism implemented for all logic pins. See **Figure 15** for details.

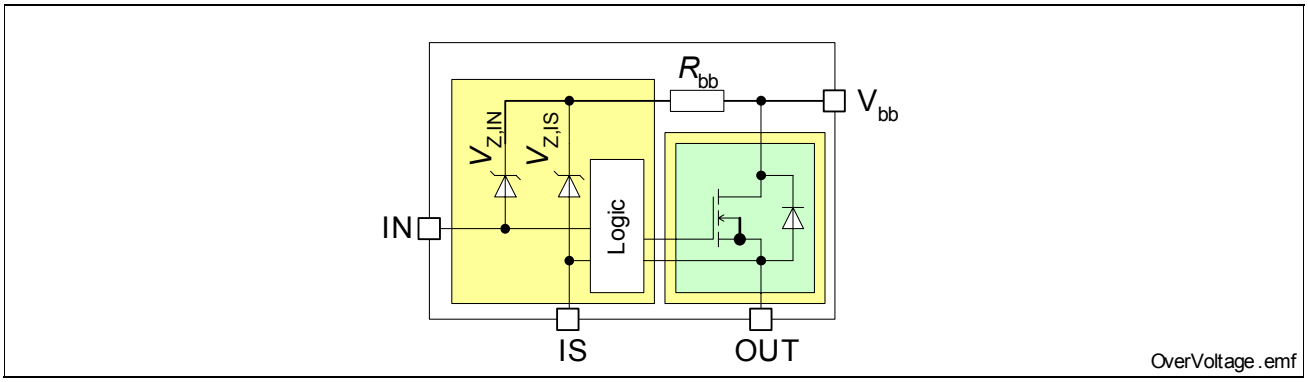


Figure 15 Over-Voltage Protection

4.2.5 Loss of Ground Protection

In case of complete loss of the device ground connections the BTS 6142D securely changes to or remains in off state.

4.2.6 Loss of V_{bb} Protection

In case of complete loss of V_{bb} the BTS 6142D remains in off state.

In case of loss of V_{bb} connection with charged inductive loads a current path with load current capability has to be provided, to demagnetize the charged inductances. It is recommended to use a diode, a Z-diode, or a varistor (V_{ZL}+V_D < 39 V or V_{Zb}+V_D < 16 V if R_{IN} = 0). For higher clamp voltages currents through IN and IS have to be limited to 120 mA. Please refer to **Figure 16** for details.

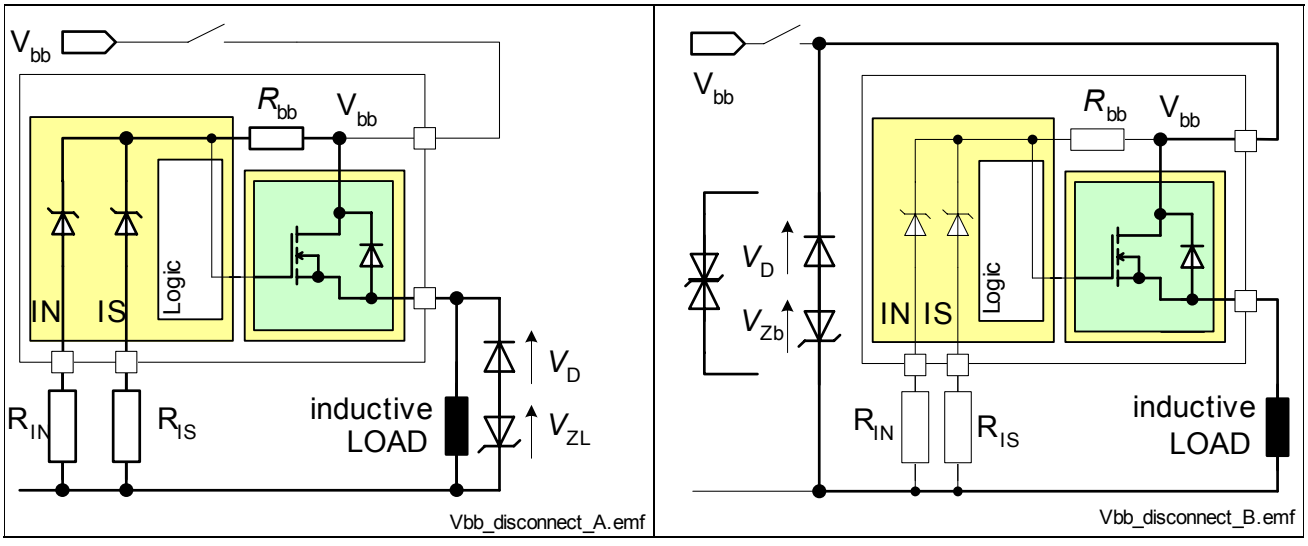


Figure 16 Loss of V_{bb}

4.2.7 Electrical Characteristics

V_{bb} = 12 V, T_j = +25 °C (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Over-Load Protection							
4.2.1	Load current limitation[1) 2)] T_j = -40 °C T_j = +25 °C T_j = +150 °C	$I_{L6(SC)}$	 - - 50	 110 100 75	 160 - -	A	V_{ON} = 6 V, (Tab to pin 1 and 5)
4.2.2	Load current limitation [2)] T_j = -40 °C T_j = +25 °C T_j = +150 °C	$I_{L12(SC)}$	 - - 45	 90 80 70	 120 - -	A	V_{ON} = 12 V, t_m = 170 µs, (Tab to pin 1 and 5)
4.2.3	Load current limitation[1) 2)] T_j = -40 °C T_j = +25 °C T_j = +150 °C	$I_{L18(SC)}$	 - - 30	 60 60 50	 90 - -	A	V_{ON} = 18 V, (Tab to pin 1 and 5)
4.2.4	Load current limitation [2)] T_j = -40 °C T_j = +25 °C T_j = +150 °C	$I_{L24(SC)}$	 - - -	 40 40 35	 - - -	A	V_{ON} = 24 V, t_m = 170 µs, (Tab to pin 1 and 5)
4.2.5	Load current limitation[1) 2)] T_j = -40 °C T_j = +25 °C T_j = +150 °C	$I_{L30(SC)}$	 - - -	 25 25 25	 - - -	A	V_{ON} = 30 V, (Tab to pin 1 and 5)
4.2.6	Short circuit shutdown detection voltage [1)]	$V_{ON(SC)}$	2.5	3.5	4.5	V	V_{bIN} > 10 V typ.
4.2.7	Short circuit shutdown delay after input current pos. slope[3)]	$t_{d(SC1)}$	200	650	1200	µs	V_{ON} > $V_{ON(SC)}$, T_j = -40 … 150 °C
4.2.8	Thermal shut down temperature	$T_{j(SC)}$	150	165 [1)]	-	°C	-
4.2.9	Thermal hysteresis [1)]	ΔT_j	-	10	-	K	-

V_{bb} = 12 V, T_j = +25 °C (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Reverse Battery							
4.2.10	On-State resistance in case of reverse polarity V_{bb}=-8V, T_j=25°C 1) V_{bb}=-8V, T_j=150°C 1) V_{bb}=-12V, T_j=25°C V_{bb}=-12V, T_j=150°C	$R_{ON(rev)}$	 - - - -	 12 20 12 18	 16 27 15 24	mΩ	V_{IN} = 0, I_L = -7.5A, R_{IS} = 1 kΩ, (pin 1 and 5 to TAB)
4.2.11	Integrated resistor in V_{bb} line	R_{bb}	-	100	150	Ω	-
Over-Voltage							
4.2.12	Over-voltage protection	V_Z				V	I_{bb} = 15 mA, T_j = -40 … 150 °C
	Input pin	$V_{Z,IN}$	63	67	-	V	
	Sense pin	$V_{Z,IS}$	56	61	-	V	

1) Not subject to production test, specified by design

2) Short circuit current limit for max. duration of $t_{d(SC1)}$, prior to shutdown, see also **Figure 12**.

3) min. value valid only if input “off-signal” time exceeds 30 µs

4.3 Diagnosis

For diagnosis purpose, the BTS 6142D provides an IntelliSense signal at the pin IS.

The pin IS provides during normal operation a sense current, which is proportional to the load current as long as $V_{b,IS}$>5V. The ratio of the output current is defined as $k_{ILIS}=I_L/I_{IS}$. During switch-on no current is provided, until the forward voltage drops below V_{ON}<1V typ. The output sense current is limited to $I_{IS,lim}$.

The pin IS provides in case of any fault conditions a defined fault current $I_{IS(fault)}$. Fault conditions are over-current (V_{ON}>1V typ.), current limit or over-temperature switch off.

The pin IS provides no current during open load in ON, de-energisation of inductive loads and inverse current mode.

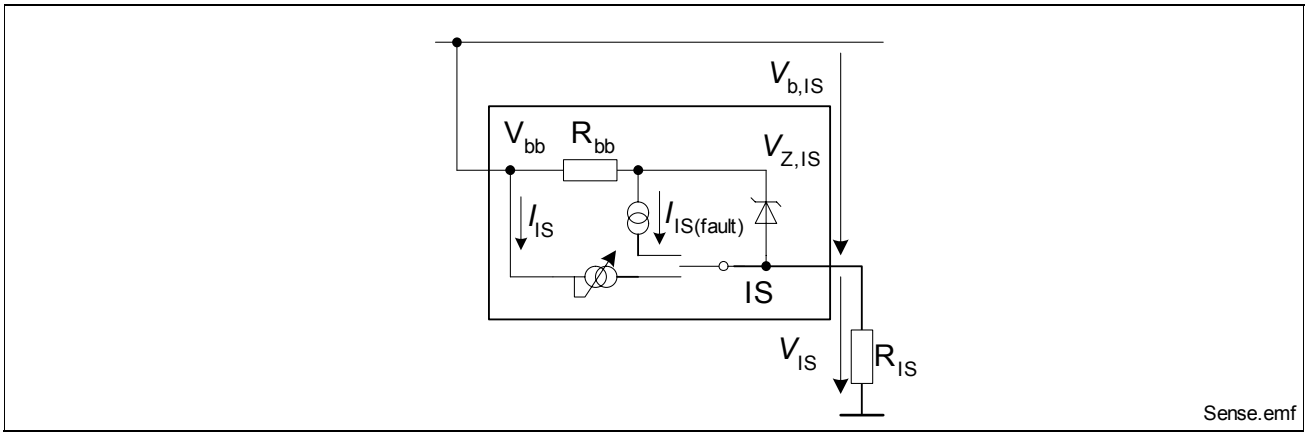


Figure 17 Block Diagram: Diagnosis

Table 1 Truth Table

Parameter	Input Current Level	Output Level	Current Sense I_{IS}
Normal operation	L[1)] H[1)]	L H	≈ 0 ($I_{IS(LL)}$) nominal
Overload	L H	L H	≈ 0 ($I_{IS(LL)}$) $I_{IS,fault}$
Short circuit to GND	L H	L L	≈ 0 ($I_{IS(LL)}$) $I_{IS,fault}$
Overtemperature	L H	L L	≈ 0 ($I_{IS(LL)}$) $I_{IS,fault}$
Short circuit to V_{bb}	L H	H H	≈ 0 ($I_{IS(LL)}$) < nominal[2)]
Open load	L H	Z[1)] H	≈ 0 ($I_{IS(LL)}$) ≈ 0 ($I_{IS(LH)}$)

1) H = “High” Level, L = “Low” Level, Z = high impedance, potential depends on external circuit

2) Low ohmic short to V_{bb} may reduce the output current I_L and therefore also the sense current I_{IS}.

The accuracy of the provided current sense ratio ($k_{ILIS} = I_L / I_{IS}$) depends on the load current. Please refer to **Figure 18** for details. A typical resistor R_{IS} of 1 kΩ is recommended.

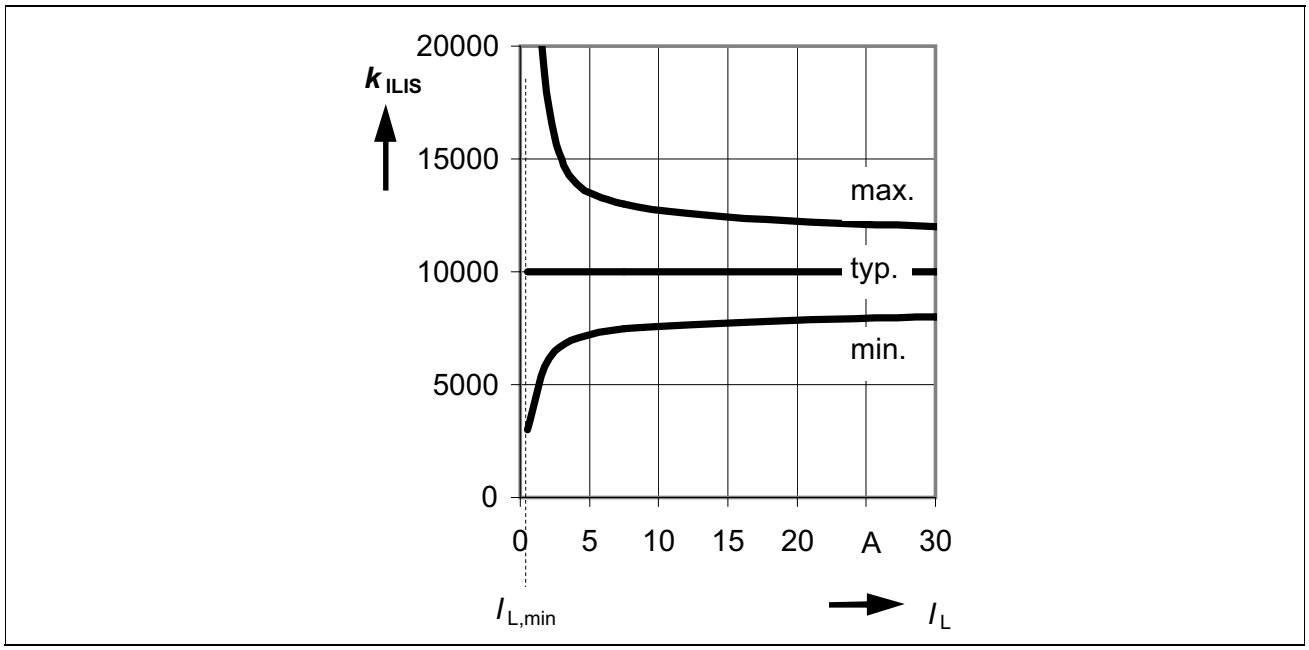


Figure 18 Current sense ratio k_{ILIS}[1)]

Details about timings between the diagnosis signal I_{IS}, the forward voltage drop V_{ON} and the load current I_L in ON-state can be found in **Figure 19**.

Note: During operation at low load current and at activated forward voltage drop limitation the “two level control” of $V_{ON(NL)}$ can cause a sense current ripple synchronous to the “two level control” of $V_{ON(NL)}$. The ripple frequency increases at reduced load currents.

1) The curves show the behavior based on characterization data. The marked points are guaranteed in this Data Sheet in **Section 4.3.1** (Position **4.3.1**).

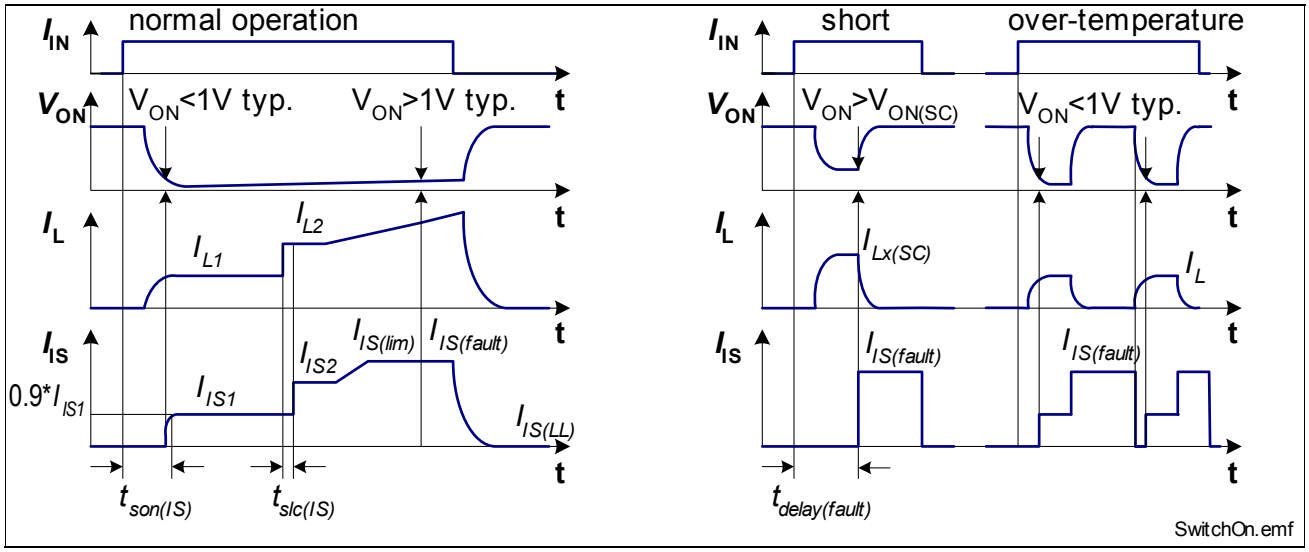


Figure 19 Timing of Diagnosis Signal in ON-state

4.3.1 Electrical Characteristics

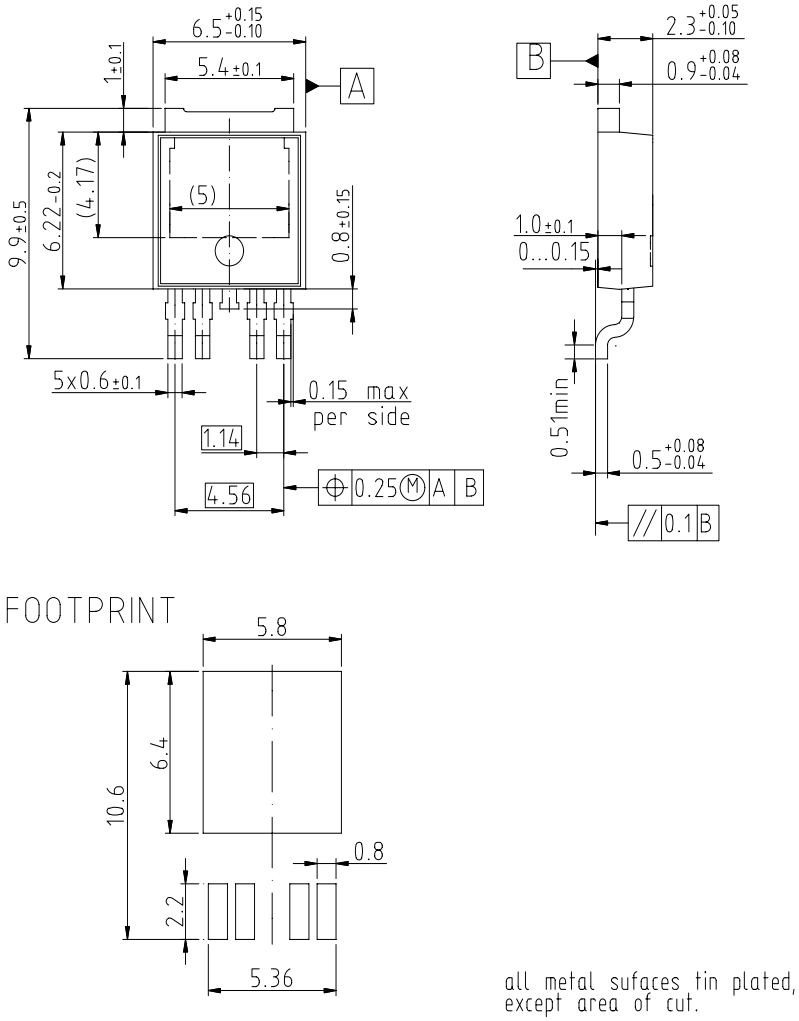
V_{bb} = 12 V, T_j = 25 °C (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Load Current Sense							
4.3.1	Current sense ratio, static on-condition	k_{ILIS}	-	10	-	k	V_{IN} = 0 V, $I_{IS} < I_{IS,lim}$
	I_L=30A		8	10	12		T_j = -40..150 °C
	I_L=7.5A		7.5	10	13		
	I_L=2.5A		6.5	10	16		
	I_L=0.5A		3	10	30		
	I_{IN} = 0 (e.g. during de energizing of inductive loads) [1]		disabled			-	-
4.3.2	Sense saturation current [1]	$I_{IS(lim)}$	2.5	6	10	mA	V_{ON} < 1 V, typ. T_j = -40 … 150 °C
4.3.3	Sense current under fault conditions	$I_{IS(fault)}$	2.5	6	10	mA	V_{ON} > 1 V, typ. T_j = -40 … 150 °C
4.3.4	Current sense leakage current	$I_{IS(LL)}$	–	0.1	0.5	µA	I_{IN} = 0
4.3.5	Current sense offset current	$I_{IS(LH)}$	–	0.1	1	µA	V_{IN} = 0, $I_L \leq 0$
4.3.6	Minimum load current for sense functionality	$I_{L(MIN)}$	0.5	–	–	A	V_{IN} = 0, T_j = -40 … 150 °C
4.3.7	Current sense settling time to 90% $I_{IS\_stat.}$ [1]	$t_{son(IS)}$	–	350	700	µs	I_L = 0 ⎍ 20 A T_j = -40 … 150 °C
4.3.8	Current sense settling time to 90% $I_{IS\_stat.}$ [1]	$t_{slc(IS)}$	–	50	100	µs	I_L = 10 ⎍ 20 A T_j = -40 … 150 °C
4.3.9	Fault-Sense signal delay after input current positive slope	$t_{delay(fault)}$	200	650	1200	µs	V_{ON} > 1 V, typ. T_j = -40 … 150 °C

[1] Not subject to production test, specified by design

5 Package Outlines BTS 6142D

P-TO-252-5-1
(Plastic Dual Small Outline Package)



You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: http://www.infineon.com/products.

SMD = Surface Mounted Device

Dimensions in mm

6 Revision History

Version	Date	Changes
V1.0	04-10-25	initial version of Final Data Sheet

Edition 2005-10-25

**Published by Infineon Technologies AG,
St.-Martin-Strasse 53,
D-81541 München, Germany**

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