AS1120
46-Segment LCD Driver

Data Sheet

1 General Description

The AS1120 is an LCD direct-driver capable of driving up to 46 LCD segments with one non-multiplexed backplane.

The device contains an integrated serial-to-parallel interface and generates the necessary signals to drive LCD panels.

Internal synchronous backplane signal regeneration allows the device to mix different drivers with different LCDs for superior brightness stability over a wide temperature range. The device also supports external backplane signals.

The AS1120 was specifically designed to easily interface with a variety of microprocessors and a wide range of LCD panel types.

The AS1120 is available in a 64-pin PQFP package.

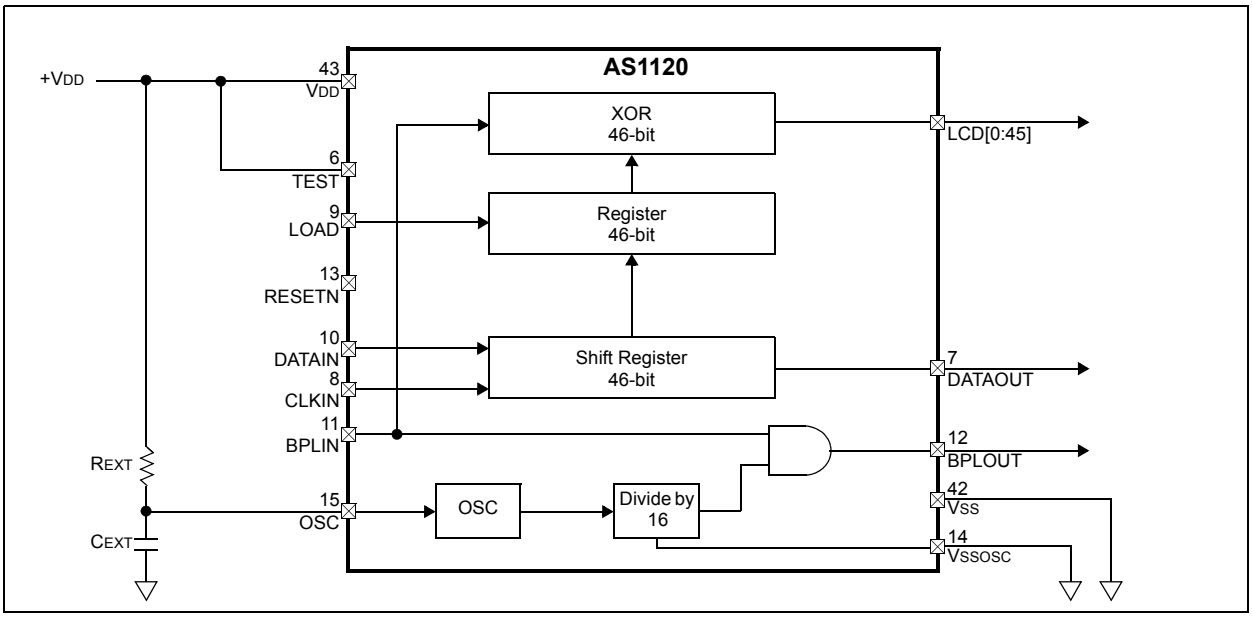
2 Key Features

- 46-Segment LCD Driver
- Serial-to-Parallel Interface
- Integrated Oscillator w/ External R/C and Backplane Input
- Supports Alphanumeric and Bar-Graph Devices
- Two Data Transfer Configurations:
  - Cascade
  - Parallel
- Non-Multiplexed Backplane
- Very-Low Current Consumption
- Power Supply Range: 3.0 to +5.5V
- Operating Temperature Range: -40 to +85ºC
- 64-pin PQFP Package

3 Applications

The device is ideal for industrial LCD systems, portable-system displays, panel meters with wide temperature ranges, high-performance optical displays, or for any other space-limited A/D application with low power-consumption and single-supply requirements.

Figure 1. Application Diagram



4 Absolute Maximum Ratings

Stresses beyond those listed in Table 1 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Section 5 Electrical Characteristics on page 3 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 1. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Comments
V_{DD}	Positive Supply Voltage to Ground	-0.3	+7.0	V	
V_{IN}, V_{OUT}	Digital Input and Output Voltage to Ground	0	V_{DD}	V	
I_{SCR}	Input Current (Latchup Immunity)	-200	+200	mA	Norm: *JEDEC 17*
T_{JMAX}	Maximum Junction Temperature		+150	ºC	
T_{STRG}	Storage Temperature	-65	+150	ºC	
Pt	Package Power Dissipation (T_{JMAX} - T_{AMB})/R_{TH}		760	mW	Package related
ESD	Electrostatic Discharge		1000	V	*HBM Mil-Std883E 3015.7* methods
	Humidity (Non-Condensing)	5	85	%	
	Package Body Temperature		+250	ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020C "Moisture/Reflow Sensitivity Classification for non-hermetic Solid State Surface Mount Devices"*

5 Electrical Characteristics

Table 2. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Positive Supply Voltage		+3.0	+5.5	V
T_{AMB}	Ambient Temperature	Verify that the LCD is compatible with the desired temperature range	-40	85	ºC
I_{DD}	Supply Current	f_{BPL} =50Hz, output not connected, T_{AMB} = *25*ºC	5		µA
f_{OSC}	Oscillator Frequency	Bpfreq = f_{OSC}/16	0.5	100	kHz
C_{SEG}	Segment Capacitance			300	pF
C_{BP}	Backplane Capacitance			50	nF
CMOS Input Pin: TEST (V_{DD} = 5V, T_{AMB} = -40 to +85 ºC unless otherwise noted).					
V_{IH}	High Level Input Voltage		0.7 x V_{DD}		V
V_{IL}	Low Level Input Voltage			0.2 x V_{DD}	V
I_{LEAK}	Input Leakage Current			±1	µA
t_T	Input Transition Time			10	ns
CMOS Input with Schmitt Trigger, **Pin**: CLKIN, LOAD, DATAIN, BPLIN, RESETN (V_{DD} = 5V, T_{AMB} = -40 to +85 ºC unless otherwise noted).					
V_{TH+}	Positive-Going Threshold	V_{DD} = 4.5V	2.8	3.2	V
		V_{DD} = 5.5V	3.4	3.9	
V_{TL-}	Negative-Going Threshold	V_{DD} = 4.5V	1.1	1.6	V
		V_{DD} = 5.5V	1.4	1.9	
I_{LEAK}	Input Leakage Current			±1	µA
CMOS Output Pins: BPLOUT, DATAOUT (V_{DD} = 5V, T_{AMB} = -40 to +85 ºC unless otherwise noted).					
V_{OH}	High Level Input Voltage	V_{DD} = 5V, I_{OH} = -4mA	4.0		V
		V_{DD} = 3.3V, I_{OH} = -2.8mA	2.5		
V_{OL}	Low Level Input Voltage	V_{DD} = 5V, I_{OL} = 4mA		0.4	V
		V_{DD} = 3.3V, I_{OL} = 3.2mA		0.4	
CMOS Output Pin: LCDxx (V_{DD} = 5V, T_{AMB} = -40 to +85 ºC unless otherwise noted).					
V_{OH}	High Level Input Voltage	V_{DD} = 5V, I_{OH} = -25µA	4.0		V
		V_{DD} = 3.3V, I_{OH} = -16µA	2.5		
V_{OL}	Low Level Input Voltage	V_{DD} = 5V, I_{OL} = 22µA		0.4	V
		V_{DD} = 3.3V, I_{OL} = 17µA		0.4	
Oscillator Pin: OSC (V_{DD} = 5V, T_{AMB} = -40 to +85 ºC unless otherwise noted).					
V_{OL}	Low Level Output Voltage (open collector)	V_{DD} = 5V, I_{OL} = 4mA		0.4	V
R_{EXT}	External Resistance		47		kΩ
C_{EXT}	External Capacitance		0.3	1	nF
f_{OSC}	Frequency	1/f_{OSC} = 0.69 x R_{EXT} x C_{EXT}	0.5	100	kHz

Table 3. Timing Characteristics

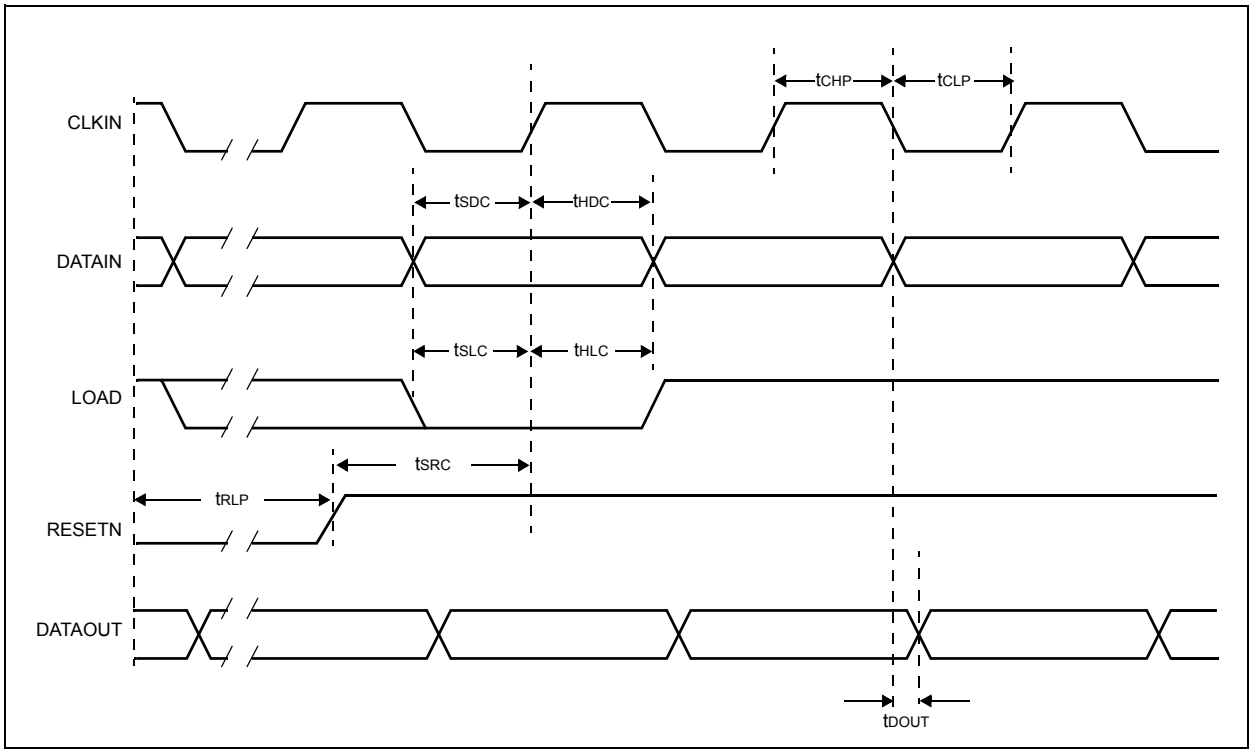
Symbol	Parameter	Min	Max	Unit
t_{CHP}	Time CLKIN high pulse	50		ns
t_{CLP}	Time CLKIN low pulse	50		ns

Table 3. Timing Characteristics

Symbol	Parameter	Min	Max	Unit
t_{SDC}	Time setup DATAIN to CLKIN rising edge	30		ns
t_{HDC}	Time hold DATAIN from CLKIN rising edge	30		ns
t_{SLC}	Time setup LOAD to CLKIN rising edge (active low) [1, 2]	30		ns
t_{HLC}	Time hold LOAD to CLKIN rising edge (active low) [1, 2]	30		ns
t_{RLP}	Time RESETN low pulse (active low)	20000		ns
t_{SRC}	Time setup RESETN to CLKIN rising edge	30		ns
t_{DOUT}	Time from CLKIN falling edge to DATAOUT		10	ns

1. LOAD must be high while RESETN is active (low).
2. LOAD can stay low for more than one CLKIN cycle.

Figure 2. Signal Waveform Timing



6 Detailed Description

The AS1120 can drive up to 46 LCD segments and multiple AS1120 devices can be cascaded (see Figure 7 on page 8) to increase the number of LCD segments.

Note: Due to the accurate delay balance between the backplane input, backplane output, and the LCD segments, it is possible to mix segments of different display crystal types.

Shift Register

Data accesses are made serially via pins DATAIN and CLKIN. At each CLKIN rising edge the signal present at DATAIN pin is shifted in the first bit of the internal shift register and the other bits are shifted ahead of the first bit.

To cascade multiple AS1120 devices (see Figure 7 on page 8), the last bit of the internal shift register is presented at pin DATAOUT at the falling edge of the same CLKIN pulse. The LSB is entered first while MSB is the last bit to be shifted into the shift register.

Note: The shift register is cleared at when the AS1120 is reset.

Latch Register and Error

When a signal is applied at pin LOAD, data present in the shift register is latched into the internal latch register and presented to the LCD output segments (LCD[0:45]), also passing through an XOR gate with the backplane signal (BPLIN). The XOR function is necessary to generate the appropriate signals to drive the LCD segments.

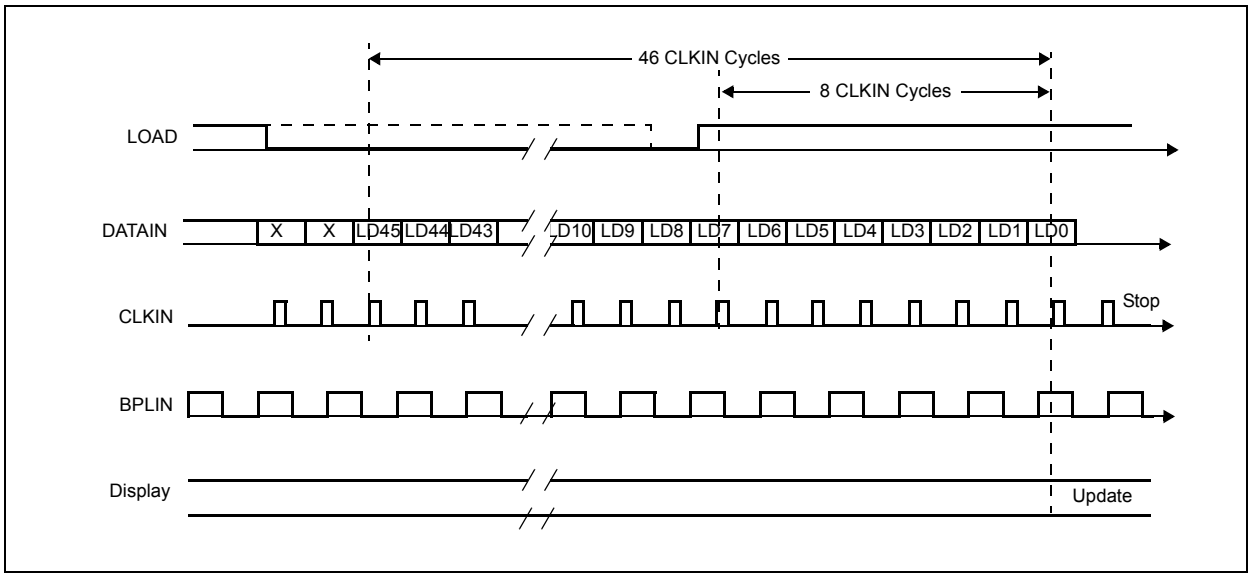
Note: At reset the latch register is cleared, thus no LCD segment will be active at power-on.

Synchronous Mode

Data is shifted into the internal shift register at the rising edge of the CLKIN signal. To load the shift register all 46 data bits are clocked into the register at the rising edge of CLKIN (see Figure 3). The LOAD signal has to be set high for 8 CLKIN periods before the end of the 46 bits. The display will be updated at the 8th CLKIN rising edge after LOAD goes high as is shown in Figure 3.

Note: During synchronous mode, a clock on BPLIN must be applied to avoid the risk of damaging the LCD crystal.

Figure 3. Synchronous Mode Timing Diagram

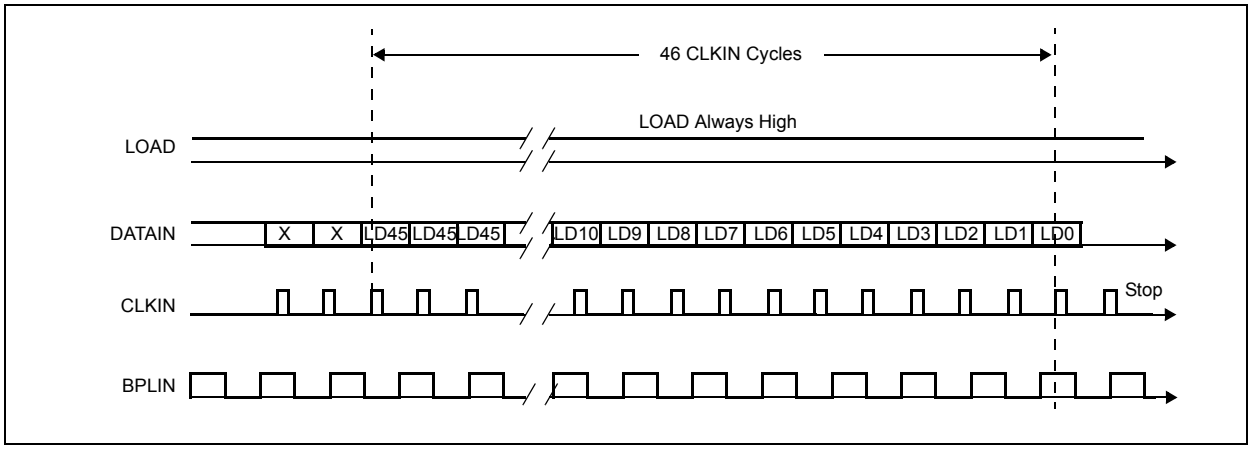


Asynchronous Mode

Data can be preloaded into the AS1120 shift register and then activated via a LOAD pulse. To preload the shift register the LOAD signal must stay high as all 46 data bits are clocked into the internal shift register at the rising edge of CLKIN (see Figure 4).

Note: In asynchronous mode, a clock signal must be applied on pin BPLIN. Asynchronous mode does not support the use of the AS1120 internal clock.

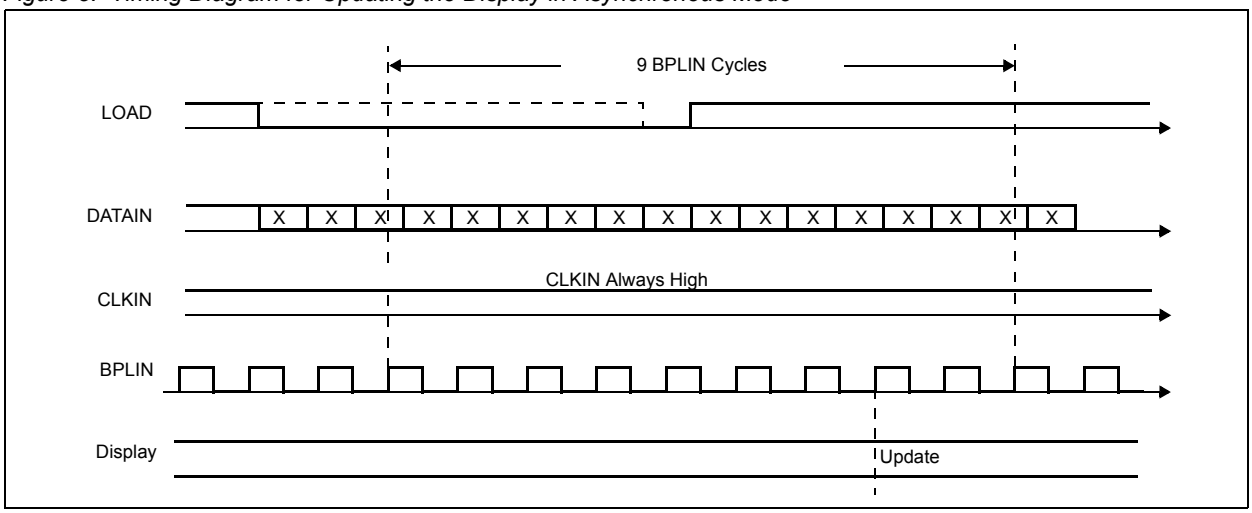
Figure 4. Timing Diagram for Preloading the Shift Register



To update the LCD display the LOAD signal must be held low for at least 8 periods of the clock applied at BPLIN, and CLKIN must be set to low. Note that since BPLIN is normally asynchronous in respect to LOAD, it is advisable to keep LOAD low for 8+1 BPLIN cycles. The display will be updated at the 8th BPLIN rising edge while LOAD is Low.

In case of internal BPLIN generation through the internal oscillator BPLIN = $f_{OSC}/16$.

Figure 5. Timing Diagram for Updating the Display in Asynchronous Mode



R/C Oscillator and Backplane Generation

The AS1120 can generate the backplane signal using an internal R/C oscillator, or an externally generated backplane signal can be supplied.

When cascading multiple AS1120 devices (see Figure 7 on page 8), only the first device should have the oscillator running; the other devices must use pin BPLIN to regenerate the backplane signal and to synchronize their LCD output segments with the common backplane.

The selection of internal or external backplane signal (see Table 4) is initiated after RESETN is disabled – the first rising edge at pin OSC after RESETN is disabled will force pin BPLOUT to deliver the internally generated backplane signal. If there is no rising edge at pin OSC, BPLOUT will simply buffer the signal at pin BPLIN.

Table 4. Backplane Source Generation Selection

Mode	OSC Pin	BPLOUT
Internal	Running	fOSC/16
External	Tied Low	BPLIN

Note: The LCD should never be supplied with static signals. Verify that signals at pins BPLIN and BPLOUT are always running while VDD is supplied; note that pin BPLOUT is stopped during a reset.

Internal Mode – R/C Oscillator Running (Generating the Backplane)

Connect external R/C components to pin OSC as shown in Figure 1 on page 1. When an external REXT and CEXT are connected to pin OSC, a clock signal whose frequency is equal to fOSC divided by 16 will be present at pin BPLOUT.

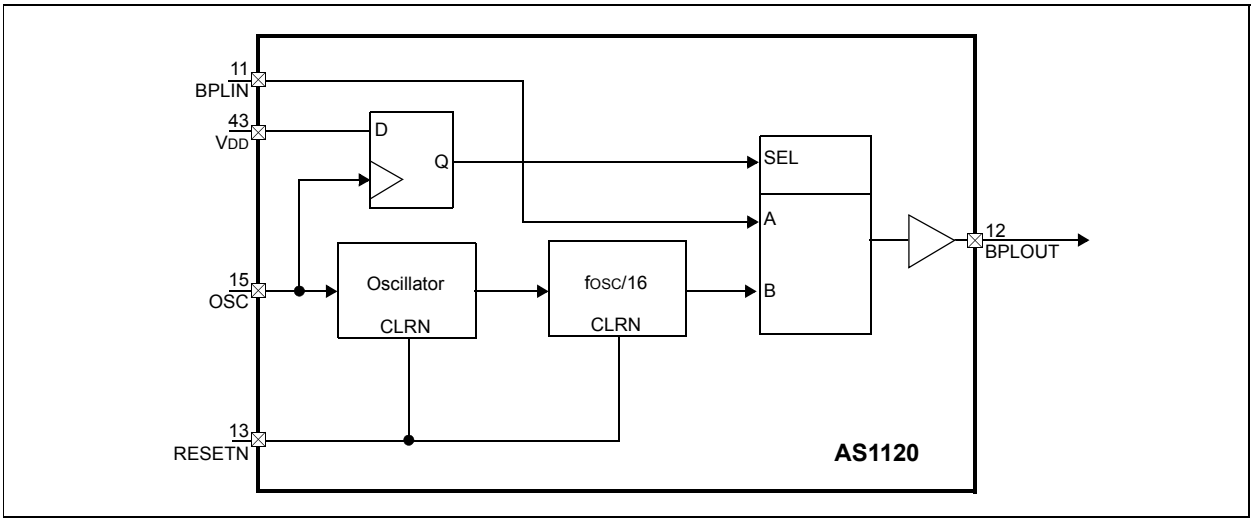
Note: Internal mode requires that pin BPLIN be connected to pin BPLOUT.

The oscillation period is approximately tOSC = 1/fOSC = 0.69 x REXT x CEXT, and the error between the expected frequency and the generated frequency increases as indicated in Table 5.

Table 5. Oscillator Error Rate

Expected Oscillator Frequency	Error
1 kHz	1%
10 kHz	5%
50 kHz	20%
100 kHz	40%

Figure 6. AS1120 Clock Circuit



External Mode: R/C Oscillator Stopped (External Backplane)

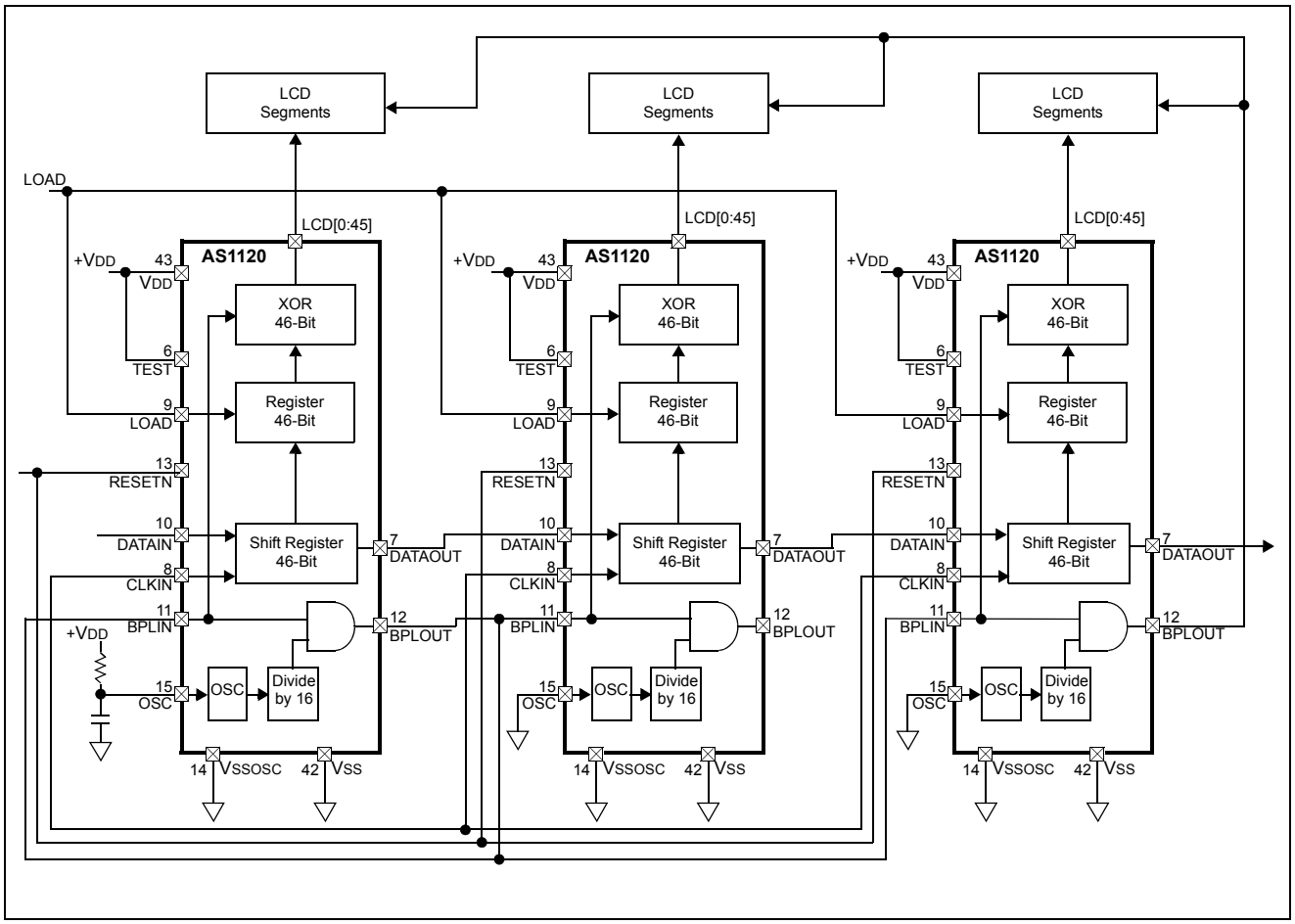
Connect pin OSC to VSS in order to block the internal oscillator. In this external mode, an external backplane signal should be presented at pin BPLIN, which will be regenerated and presented at pin BPLOUT.

7 Application Information

The AS1120 can support all types of static LCD displays.

Note: For proper display operation, ensure that the LCD can safely operate within the full temperature range of the AS1120 (see page 1).

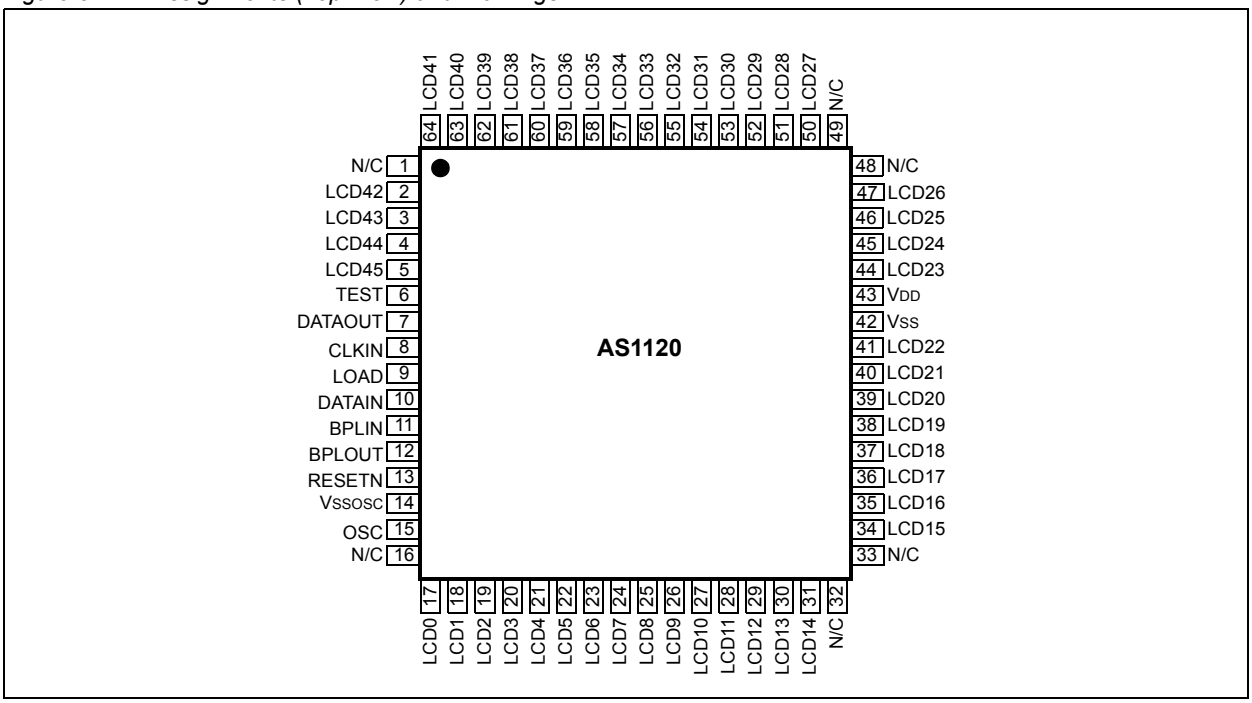
Figure 7. Cascaded Configuration



8 Pinout and Packaging

Pin Assignments and Markings

Figure 8. Pin Assignments (Top View) and Markings



Pin Descriptions

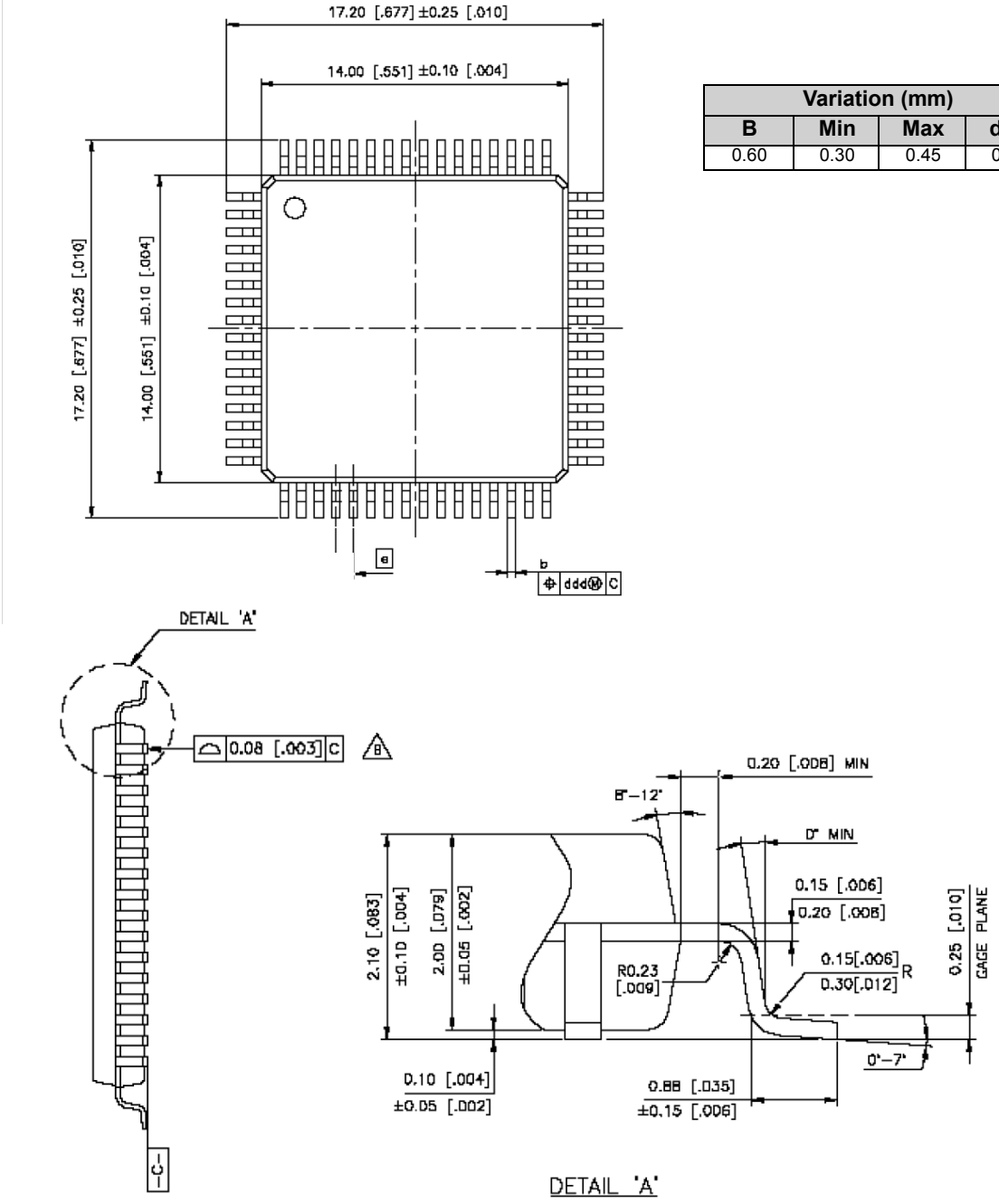
Table 6. Pin Descriptions

Pin Number	Pin Name	Description
1, 16, 32, 33, 48, 49	N/C	Not Connected
2:5	LCD42:LCD45	LCD Output Segments 42:45
6	TEST	Test pin. This pin must be tied to pin VDD.
7	DATAOUT	Serial Data Output
8	CLKIN	Shift Register Clock
9	LOAD	Load Strobe from Shift Register to Latch
10	DATAIN	Serial Data Input
11	BPLIN	Backplane Input
12	BPLOUT	Backplane Output
13	RESETN	Active-Low Asynchronous Reset
14	VSSOSC	Internal Oscillator Power Ground
15	OSC	Oscillator Pad. a). Internal clock (see page 7) b) External clock; tied to VSSOSC
17:31	LCD0:LCD14	LCD Output Segments 0:14
34:41	LCD15:LCD22	LCD Output Segments 15:22
42	VSS	Power Ground
43	VDD	Positive Power Supply
44:47	LCD23:LCD26	LCD Output Segments 23:26
50:64	LCD27:LCD41	LCD Output Segments 27:41

Package Drawings and Markings

The devices are available in an 64-pin PQFP package.

Figure 9. 64-pin PQFP Package



Variation (mm)			
B	**Min**	**Max**	**ddd**
0.60	0.30	0.45	0.20

Notes:

1. Controlling dimension is millimeters.
2. Pin 1 indicator may be chamfer, dot, or both.
3. Center line reference is defined by the mid-point of the center lead or the center space between leads at the package.

9 Ordering Information

The device is available as the standard product shown in Table 7.

Table 7. Ordering Information

Type	Description	Delivery Form	Package
AS1120	46-Segment LCD Driver	Tape and Reel	PQFP44

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