

36- 40GHz Integrated Down Converter

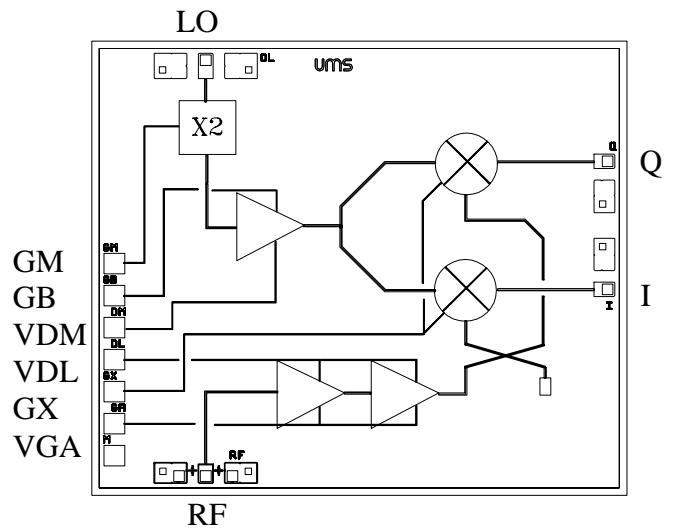
GaAs Monolithic Microwave IC

preliminary

Description

The CHR2296 is a multifunction chip which integrates a LO time two multiplier, a balanced cold FET mixer, and a RF LNA. It is designed for a wide range of applications, typically commercial communication systems. The backside of the chip is both RF and DC grounds. This helps simplify the assembly process.

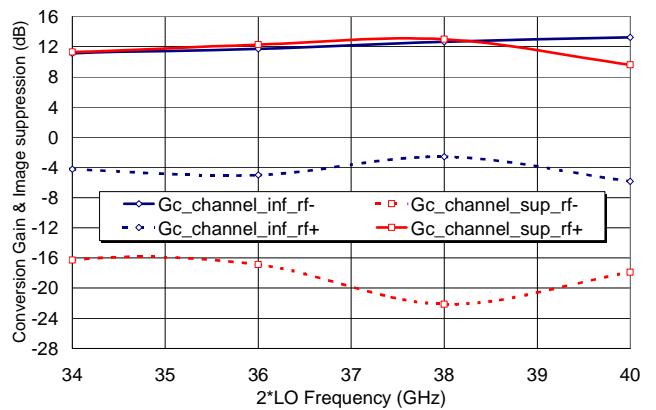
The circuit is manufactured with a PM-HEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography. It is available in chip form.



Main Features

- Broadband performances : 36-40GHz
- 11 dB conversion gain
- 5dB noise figure
- 10dBm LO input power
- -10dBm RF input power (1dB gain comp.)
- Low DC power consumption, 110mA@3.5V
- Chip size : 2.49 X 1.97 X 0.10 mm

Typical on wafer measurement:



Conversion Gain & Image suppression @ IF=1GHz

Main Characteristics

Tamb. = 25°C

| | Parameter | Min | Typ | Max | Unit |
|-----------------|--------------------|------|-----|-----|------|
| F _{RF} | RF frequency range | 36 | | 40 | GHz |
| F _{LO} | LO frequency range | 17 | | 20 | GHz |
| F _{IF} | IF frequency range | 0.25 | | 1.5 | GHz |
| G _c | Conversion gain | | 11 | | dB |

ESD Protection : Electrostatic discharge sensitive device. Observe handling precautions !

Ref. : DSCHR22962147 25-May-02

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Specifications subject to change without notice

Electrical Characteristics for Broadband Operation

T_{amb} = +25°C, V_d = 3.5V*preliminary*

| Symbol | Parameter | Min | Typ | Max | Unit |
|-----------------|-------------------------------------|------|-------|-----|------|
| F _{RF} | RF frequency range | 36 | | 40 | GHz |
| F _{LO} | LO frequency range | 17 | | 20 | GHz |
| F _{IF} | IF frequency range | 0.25 | | 1.5 | GHz |
| G _c | Conversion gain (1) | | 11 | | dB |
| NF | Noise Figure (1) | | 5 | | dB |
| P _{LO} | LO Input power | | +10 | | dBm |
| Img Sup | Image Suppression | | 15 | | dBc |
| P1dB | Input power at 1dB gain compression | | -10 | | dBm |
| LO VSWR | Input LO VSWR (1) | | 2.0:1 | | |
| RF VSWR | Input RF VSWR (1) | | 3.0:1 | | |
| I _d | Bias current (2) | | 110 | | mA |

(1) On Wafer measurements

(2) Current source biasing network is recommended. Optimum performances for I_{dm}= 50mA and I_{dl}= 60mA

Absolute Maximum Ratings

T_{amb.} = 25°C (1)

| Symbol | Parameter | Values | Unit |
|------------------|---|--------------|------|
| V _d | Maximum drain bias voltage | 4.0 | V |
| I _d | Maximum drain bias current | 200 | mA |
| V _g | Gate bias voltage | -2.0 to +0.4 | V |
| V _{gd} | Minimum negative gate drain voltage (V _g – V _d) | -5 | V |
| P _{in} | Maximum peak input power overdrive (2) | +15 | dBm |
| T _{ch} | Maximum channel temperature | 175 | °C |
| T _a | Operating temperature range | -40 to +85 | °C |
| T _{stg} | Storage temperature range | -55 to +125 | °C |

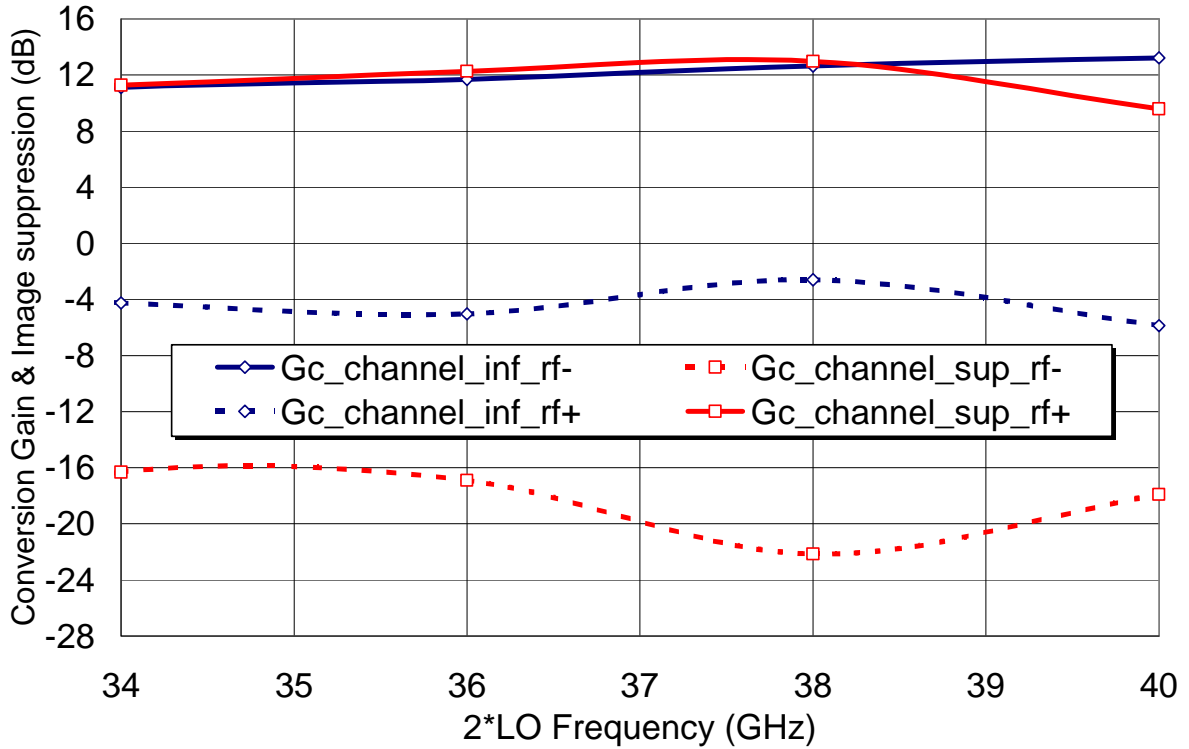
(1) Operation of this device above anyone of these parameters may cause permanent damage.

(2) Duration < 1s.

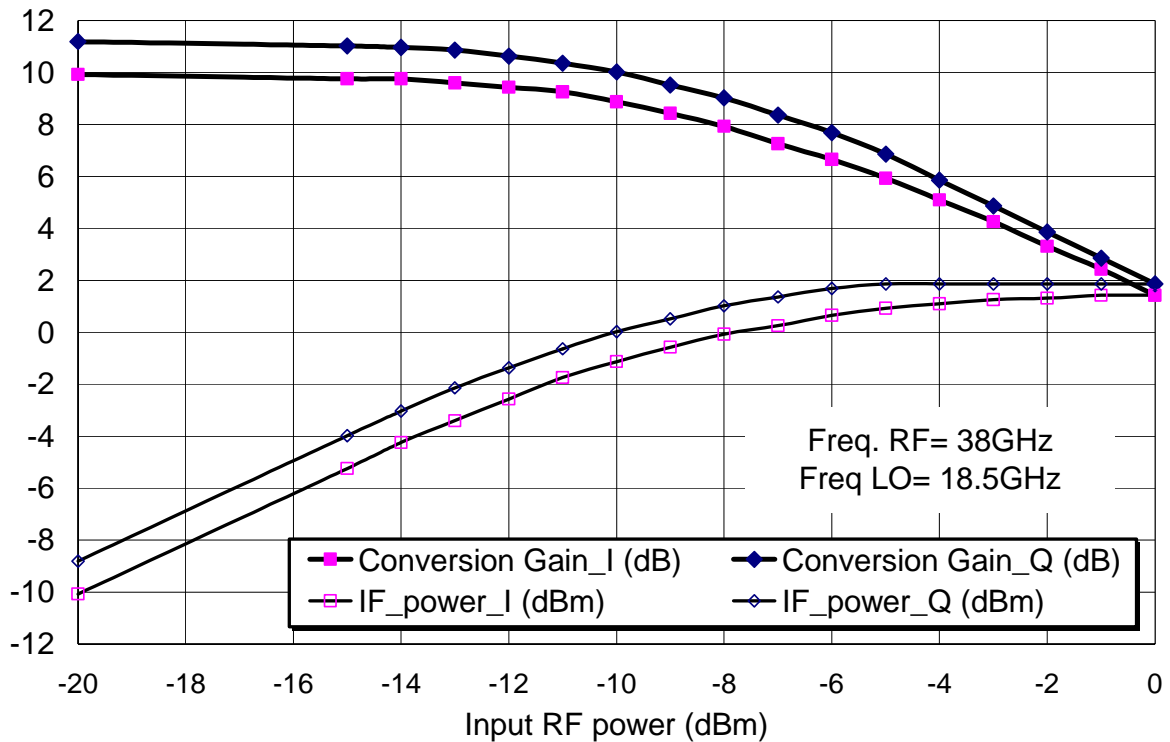
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Typical On-wafer Measurements

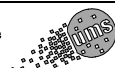
Bias Conditions : $V_{dm} = V_{dl} = 3.5\text{ V}$, $V_{gm} = -0.9\text{ V}$, $V_{gb} = -0.4\text{ V}$, $V_{gx} = -0.8\text{ V}$, $V_{ga} = -0.5\text{ V}$



Conversion gain & Image suppression with a 90° IQ combiner @ IF=1GHz

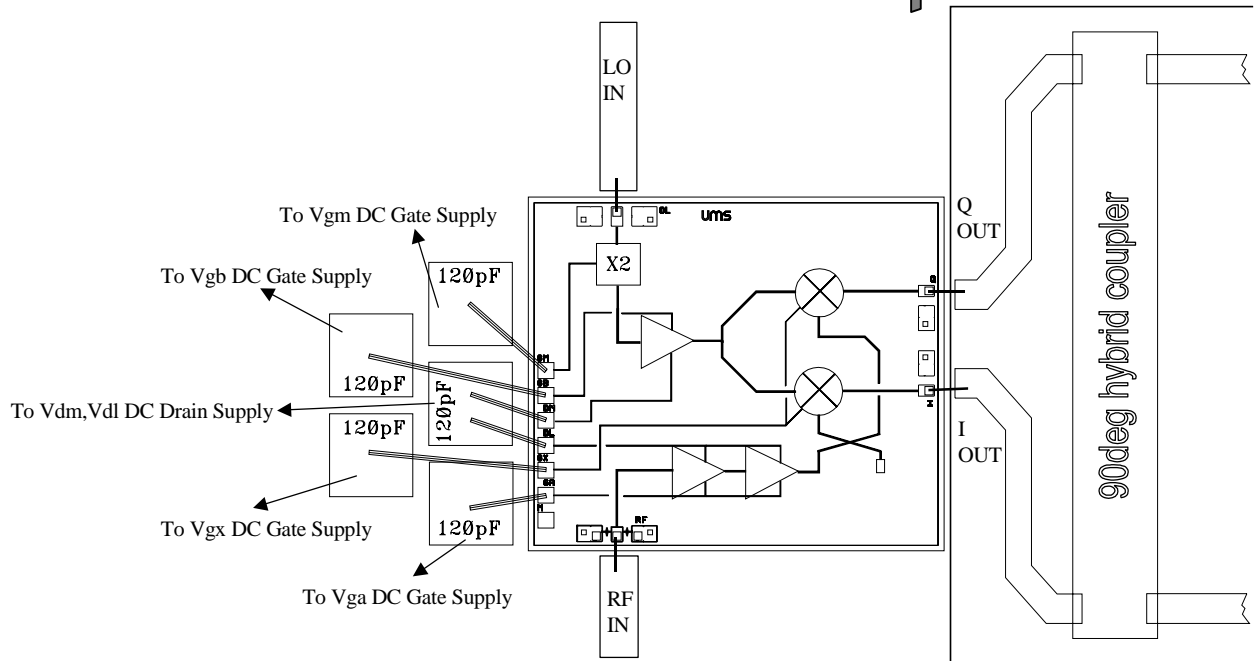


Input RF compression by channel

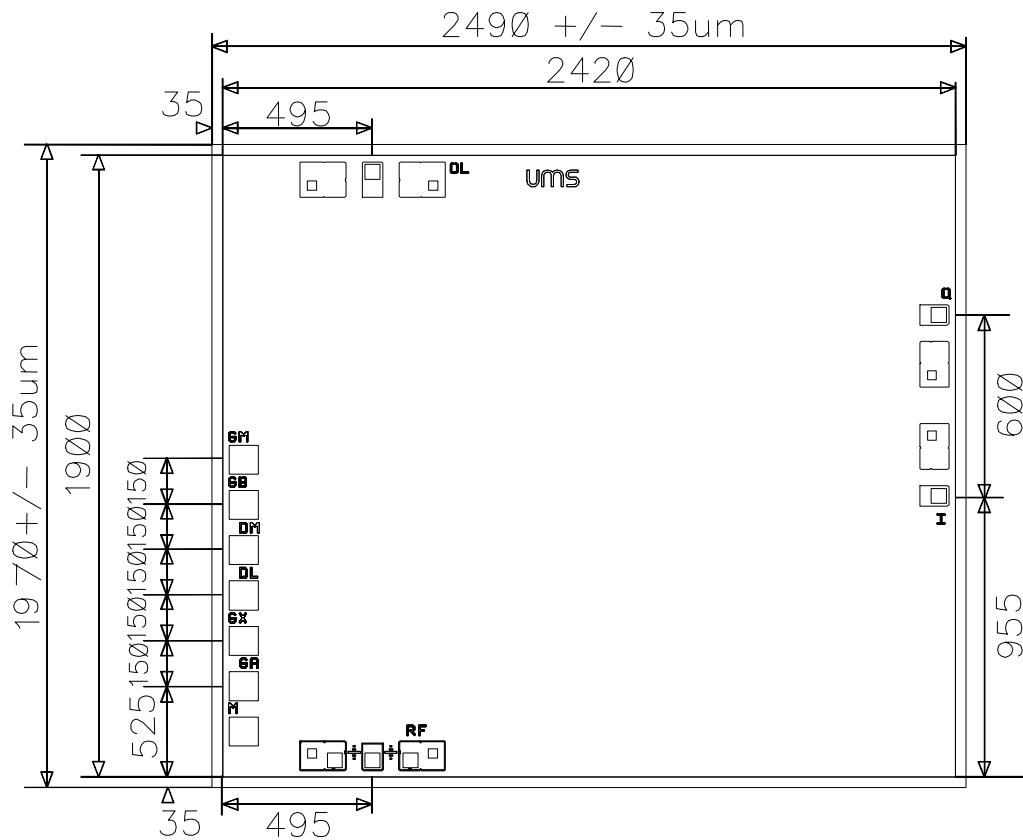


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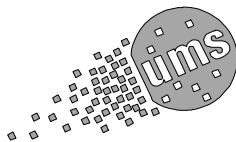
Chip Assembly and Mechanical Data



Note : Supply feed should be capacitively bypassed. 25µm diameter gold wire is recommended



Bonding pad positions
(Chip thickness : 100µm. All dimensions are in micrometers)



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Ordering Information

Chip form : CHR2296-99F/00

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