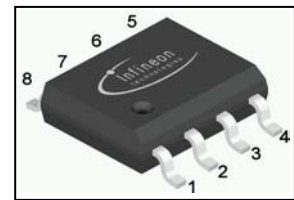


**OptiMOS<sup>®</sup> 2 Power-Transistor**
**Features**

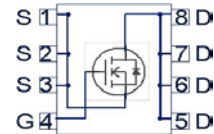
- Fast switching MOSFET for SMPS
- Optimized technology for notebook DC/DC
- Qualified according to JEDEC<sup>1</sup> for target applications
- N-channel
- Logic level
- Excellent gate charge x  $R_{DS(on)}$  product (FOM)
- Very low on-resistance  $R_{DS(on)}$
- Avalanche rated
- $dv/dt$  rated

**Product Summary**

$V_{DS}$	30	V
$R_{DS(on),max}$	11.9	m $\Omega$
$I_D$	11	A

**P-DSO-8**


Type	Package	Ordering Code	Marking
BSO119N03S	P-DSO-8	Q67042-S4211	119N3S


**Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified**

Parameter	Symbol	Conditions	Value		Unit
			10 secs	steady state	
Continuous drain current	$I_D$	$T_A=25\text{ °C}^{(2)}$	11	9.0	A
		$T_A=70\text{ °C}^{(2)}$	9.1	7.2	
Pulsed drain current	$I_{D,pulse}$	$T_A=25\text{ °C}^{(3)}$	44		
Avalanche energy, single pulse	$E_{AS}$	$I_D=11\text{ A}$ , $R_{GS}=25\ \Omega$	58		mJ
Reverse diode $dv/dt$	$dv/dt$	$I_D=11\text{ A}$ , $V_{DS}=20\text{ V}$ , $di/dt=200\text{ A}/\mu\text{s}$ , $T_{j,max}=150\text{ °C}$	6		kV/ $\mu\text{s}$
Gate source voltage	$V_{GS}$		$\pm 20$		V
Power dissipation	$P_{tot}$	$T_A=25\text{ °C}^{(2)}$	2.5	1.56	W
Operating and storage temperature	$T_j$ , $T_{stg}$		-55 ... 150		$^{\circ}\text{C}$
IEC climatic category; DIN IEC 68-1			55/150/56		

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Thermal characteristics**

Thermal resistance, junction - soldering point	$R_{thJS}$		-	-	35	K/W
Thermal resistance, junction - ambient	$R_{thJA}$	minimal footprint, $t_p \leq 10$ s	-	-	110	
		minimal footprint, steady state	-	-	150	
		6 cm <sup>2</sup> cooling area <sup>2)</sup> , $t_p \leq 10$ s	-	-	50	
		6 cm <sup>2</sup> cooling area <sup>2)</sup> , steady state	-	-	80	

**Electrical characteristics, at  $T_j=25$  °C, unless otherwise specified**
**Static characteristics**

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0$ V, $I_D=1$ mA	30	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$ , $I_D=25$ $\mu$ A	1.2	1.6	2	
Zero gate voltage drain current	$I_{DSS}$	$V_{DS}=30$ V, $V_{GS}=0$ V, $T_j=25$ °C	-	0.1	1	$\mu$ A
		$V_{DS}=30$ V, $V_{GS}=0$ V, $T_j=125$ °C	-	10	100	
Gate-source leakage current	$I_{GSS}$	$V_{GS}=20$ V, $V_{DS}=0$ V	-	10	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=4.5$ V, $I_D=10$ A	-	13	16.3	m $\Omega$
		$V_{GS}=10$ V, $I_D=11$ A	-	9.9	11.9	
Gate resistance	$R_G$		-	0.9	-	$\Omega$
Transconductance	$g_{fs}$	$ V_{DS}  > 2 I_D R_{DS(on)max}$ , $I_D=11$ A	15	30	-	S

<sup>1)</sup>J-STD20 and JESD22

<sup>2)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70  $\mu$ m thick) copper area for drain connection. PCB is vertical in still air.

<sup>3)</sup> See figure 3

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic characteristics**

Input capacitance	$C_{iss}$	$V_{GS}=0\text{ V}, V_{DS}=15\text{ V}, f=1\text{ MHz}$	-	1300	1730	pF
Output capacitance	$C_{oss}$		-	470	630	
Reverse transfer capacitance	$C_{rss}$		-	62	93	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=15\text{ V}, V_{GS}=10\text{ V}, I_D=5.5\text{ A}, R_G=2.7\ \Omega$	-	4.3	6.5	ns
Rise time	$t_r$		-	3.8	5.7	
Turn-off delay time	$t_{d(off)}$		-	18	27	
Fall time	$t_f$		-	2.8	4.2	

**Gate Charge Characteristics<sup>4)</sup>**

Gate to source charge	$Q_{gs}$	$V_{DD}=15\text{ V}, I_D=5.5\text{ A}, V_{GS}=0\text{ to }5\text{ V}$	-	3.7	4.9	nC
Gate charge at threshold	$Q_{g(th)}$		-	2.1	2.8	
Gate to drain charge	$Q_{gd}$		-	2.5	3.7	
Switching charge	$Q_{sw}$		-	4.1	5.8	
Gate charge total	$Q_g$		-	10	13	
Gate plateau voltage	$V_{plateau}$		-	2.8	-	V
Gate charge total, sync. FET	$Q_{g(sync)}$	$V_{DS}=0.1\text{ V}, V_{GS}=0\text{ to }5\text{ V}$	-	8.8	12	nC
Output charge	$Q_{oss}$	$V_{DD}=15\text{ V}, V_{GS}=0\text{ V}$	-	11	15	

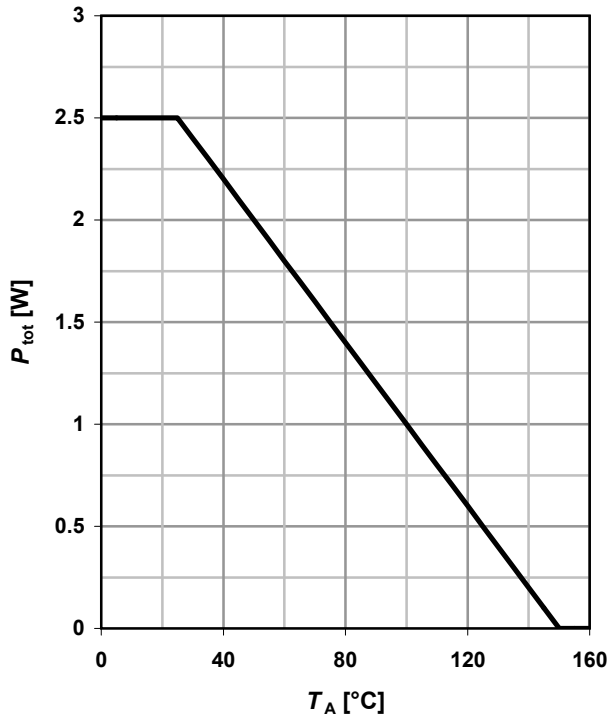
**Reverse Diode**

Diode continuous forward current	$I_S$	$T_A=25\text{ }^\circ\text{C}$	-	-	2.5	A
Diode pulse current	$I_{S,pulse}$		-	-	44	
Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_F=2.5\text{ A}, T_j=25\text{ }^\circ\text{C}$	-	0.75	1	V
Reverse recovery charge	$Q_{rr}$	$V_R=12\text{ V}, I_F=I_S, di_F/dt=400\text{ A}/\mu\text{s}$	-	-	10	nC

<sup>4)</sup> See figure 16 for gate charge parameter definition

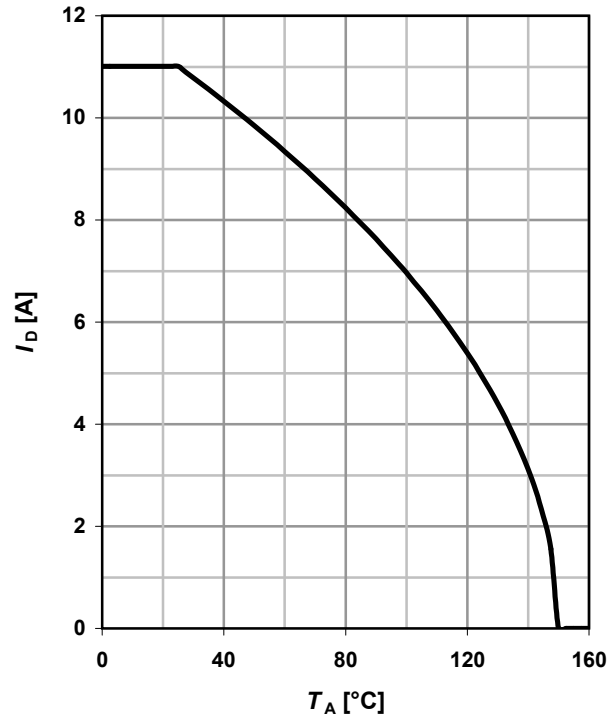
**1 Power dissipation**

$P_{tot}=f(T_A); t_p \leq 10 \text{ s}$



**2 Drain current**

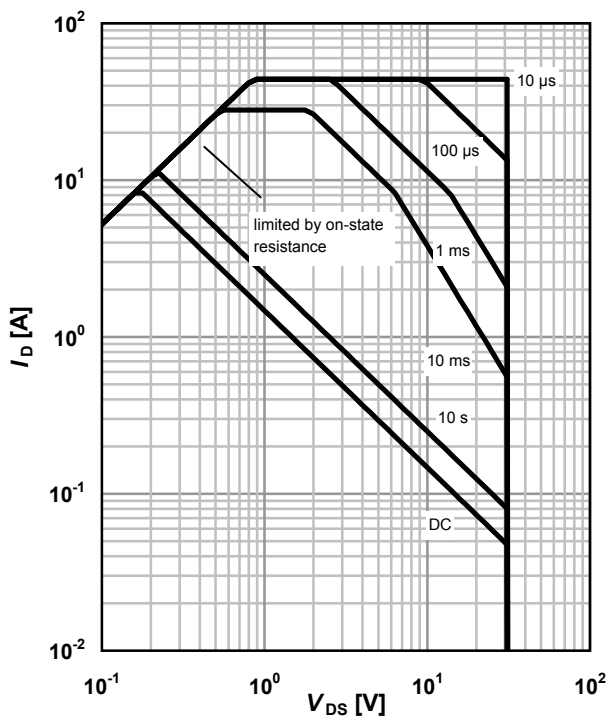
$I_D=f(T_A); V_{GS} \geq 10 \text{ V}; t_p \leq 10 \text{ s}$



**3 Safe operation area**

$I_D=f(V_{DS}); T_A=25 \text{ °C}^1; D=0$

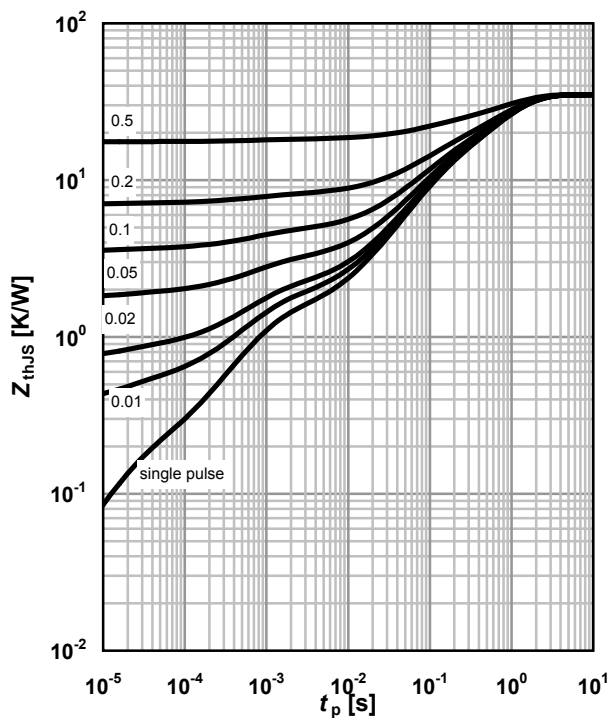
parameter:  $t_p$



**4 Max. transient thermal impedance**

$Z_{thJS}=f(t_p)$

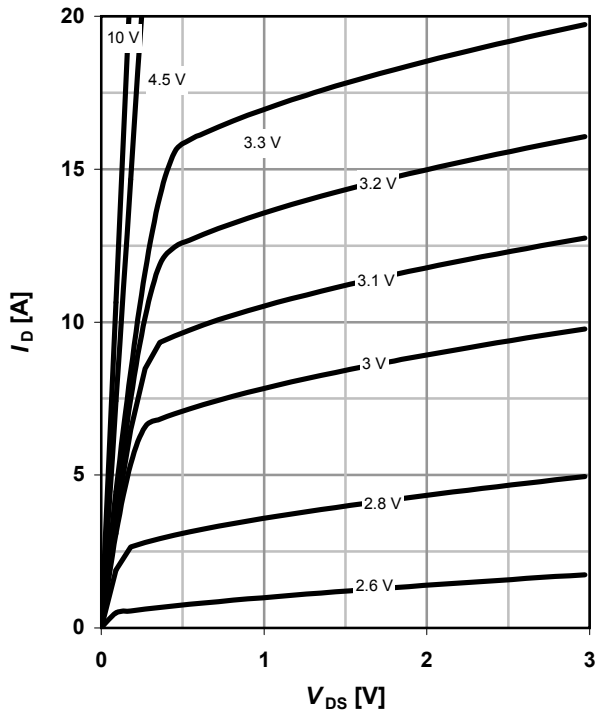
parameter:  $D=t_p/T$



**5 Typ. output characteristics**

$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$

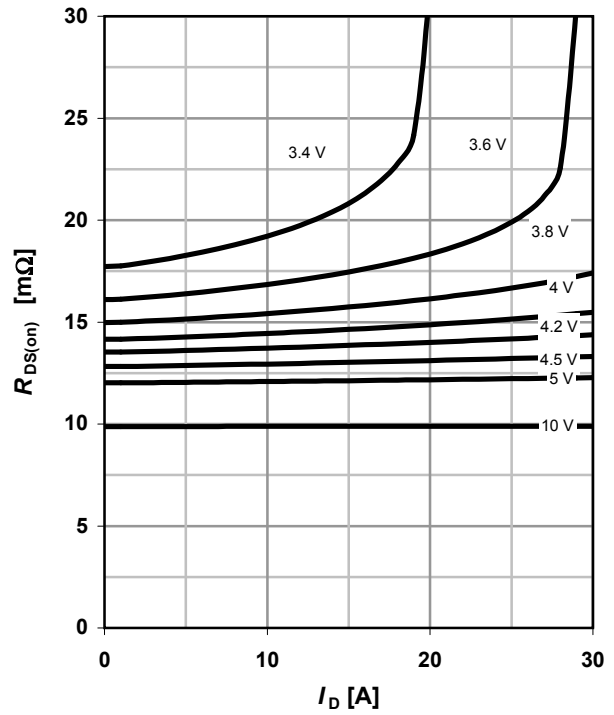
parameter:  $V_{GS}$



**6 Typ. drain-source on resistance**

$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

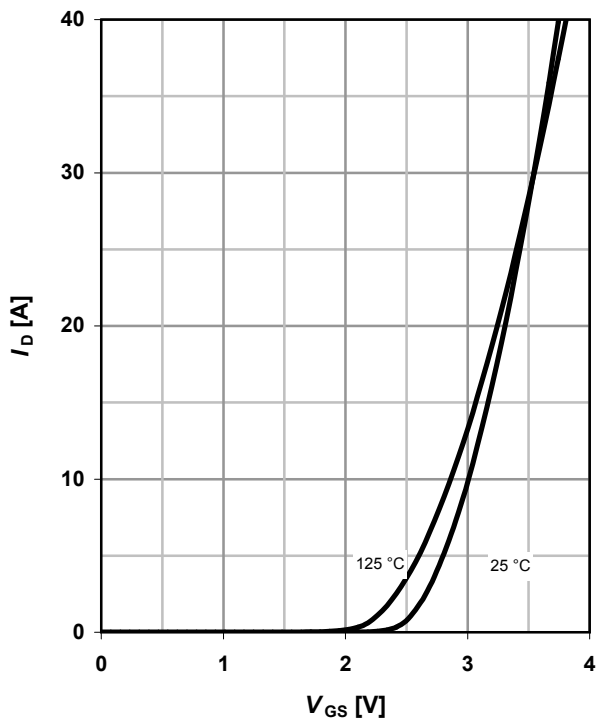
parameter:  $V_{GS}$



**7 Typ. transfer characteristics**

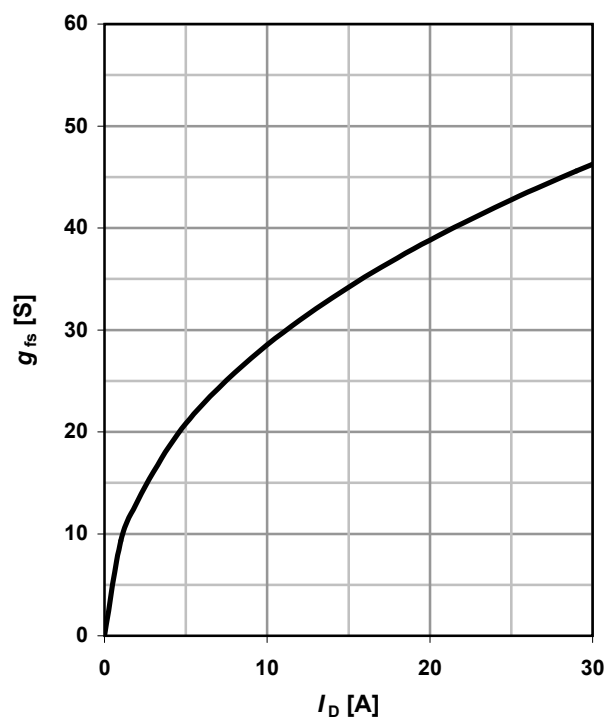
$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$

parameter:  $T_j$



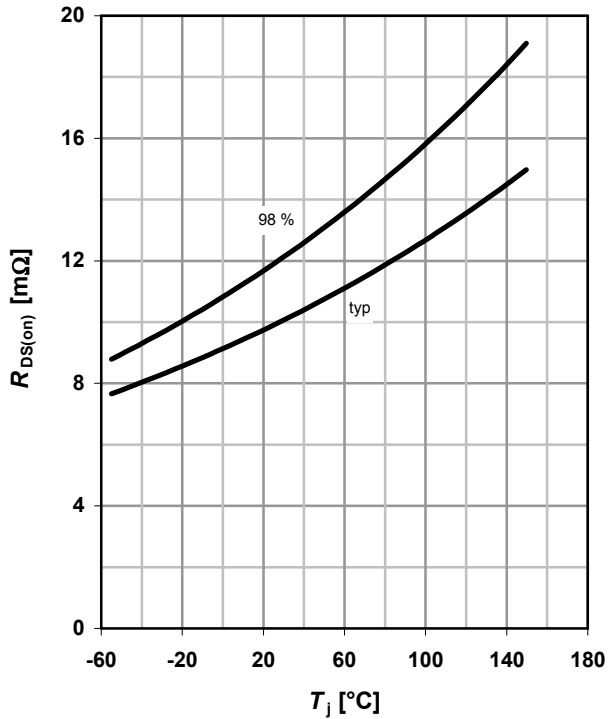
**8 Typ. forward transconductance**

$g_{fs} = f(I_D); T_j = 25\text{ }^\circ\text{C}$



**9 Drain-source on-state resistance**

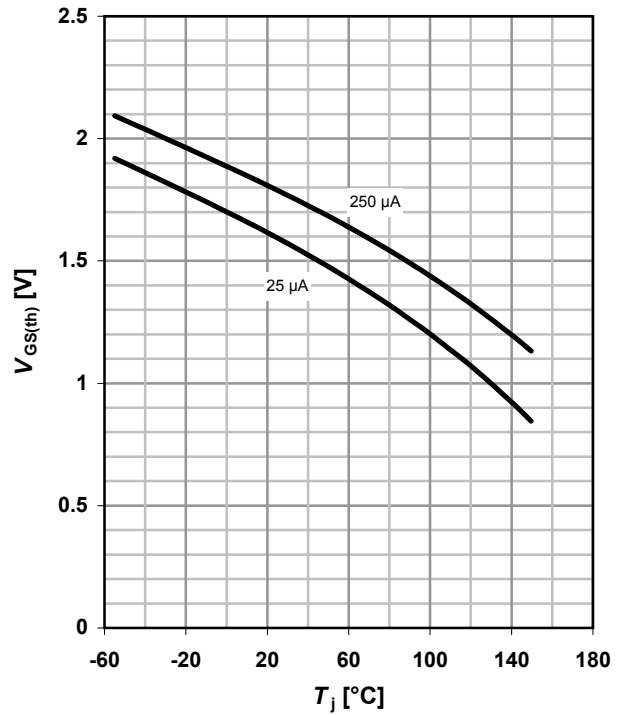
$R_{DS(on)}=f(T_j); I_D=11\text{ A}; V_{GS}=10\text{ V}$



**10 Typ. gate threshold voltage**

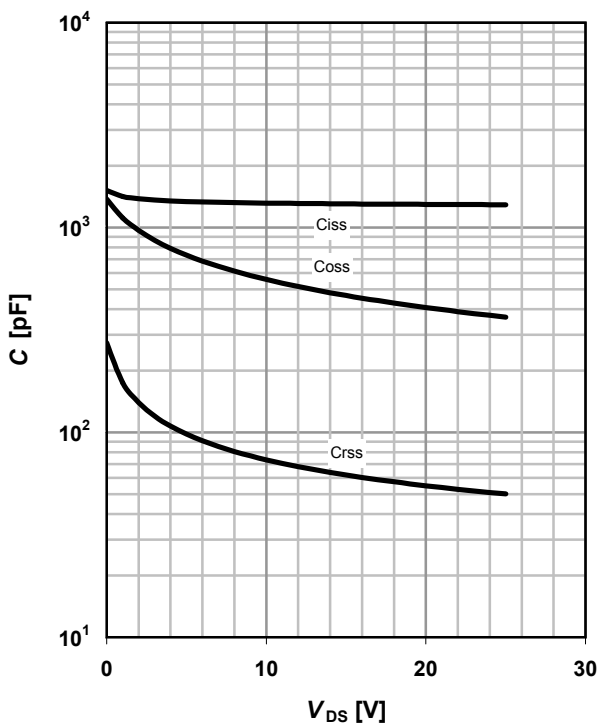
$V_{GS(th)}=f(T_j); V_{GS}=V_{DS}$

parameter:  $I_D$



**11 Typ. capacitances**

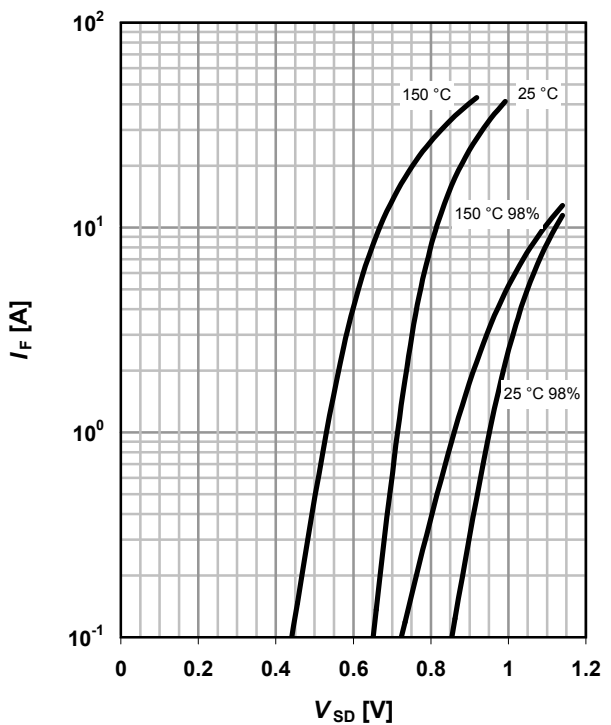
$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$



**12 Forward characteristics of reverse diode**

$I_F=f(V_{SD})$

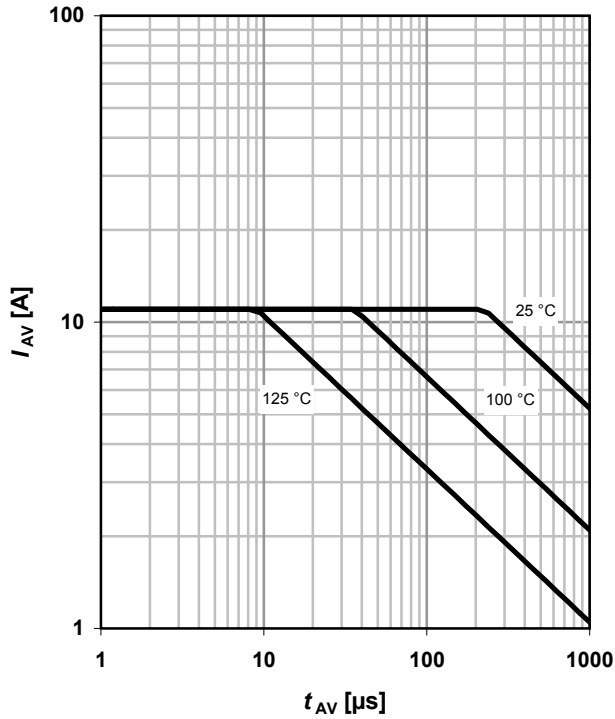
parameter:  $T_j$



**13 Avalanche characteristics**

$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$

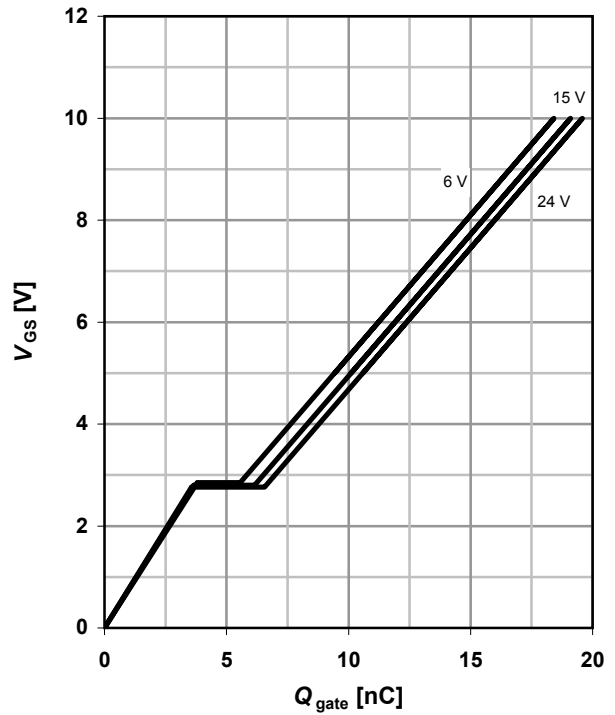
parameter:  $T_{j(start)}$



**14 Typ. gate charge**

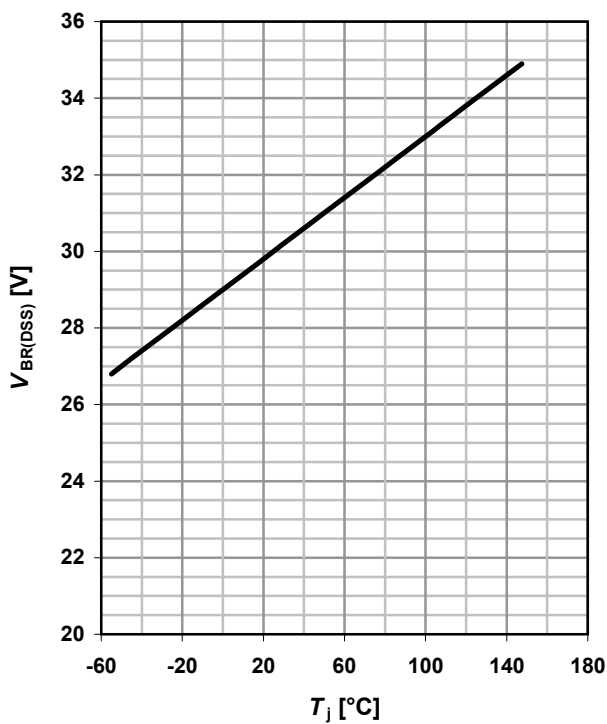
$V_{GS}=f(Q_{gate}); I_D=5.5 \text{ A pulsed}$

parameter:  $V_{DD}$

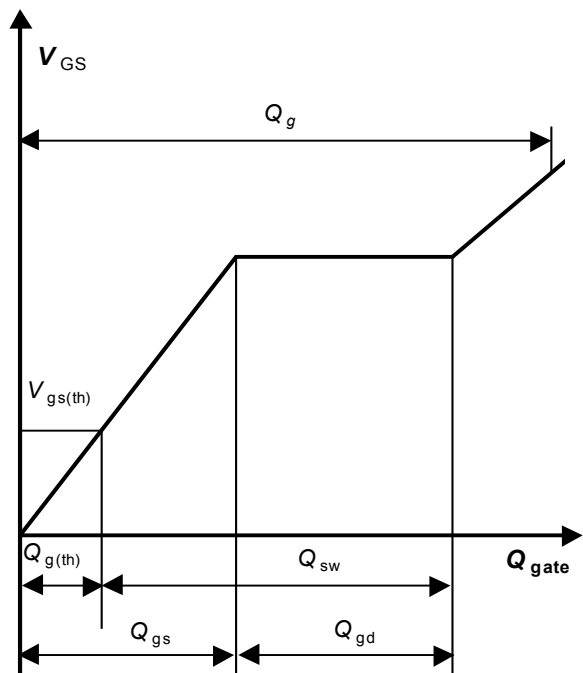


**15 Drain-source breakdown voltage**

$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

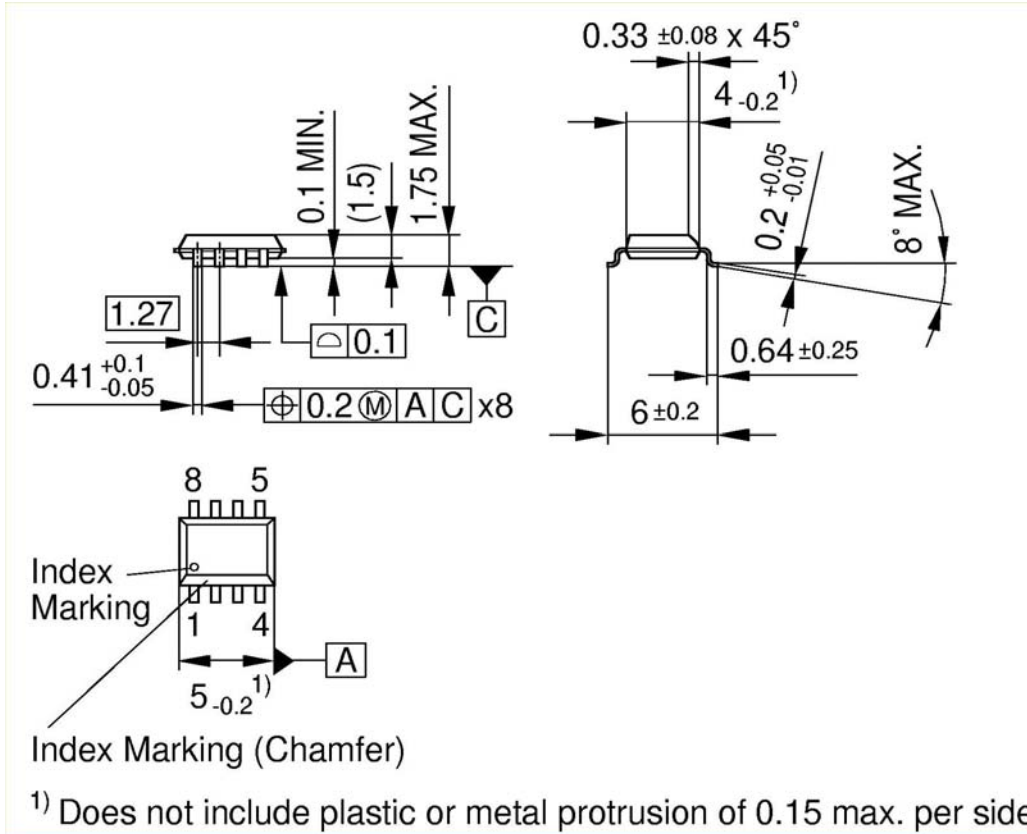


**16 Gate charge waveforms**



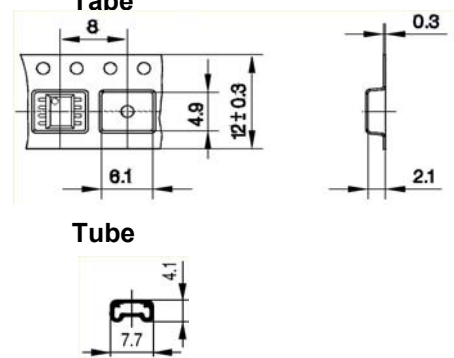
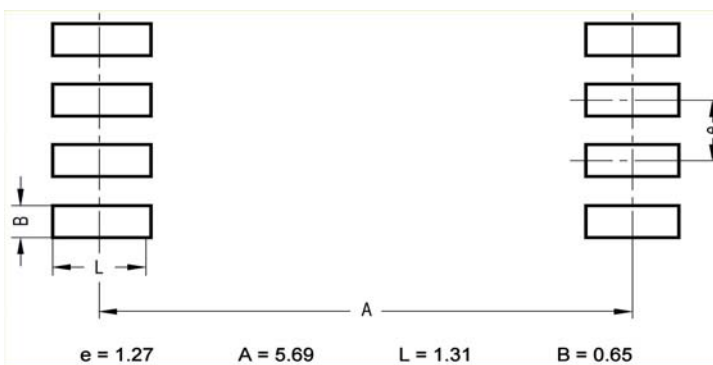
Package Outline

P-DSO-8: Outline



Footprint

Packaging



Dimensions in mm



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