19-2855; Rev 2; 4/05

MAXIM

2- to 8-Phase VRM 10/9.1 PWM Controllers with Precise Current Sharing and Fast Voltage Positioning

General Description

The MAX8525 (VRM 10/VRD 10)/MAX8524 (VRM 9.1/VRD 9.1) current-mode step-down controllers, the MAX8523 high-speed, dual-phase MOSFET gate driver, and the MAX8552 wide-input, single-phase MOSFET gate driver provide flexible, low-cost, low-voltage CPU core supplies. The MAX8523 and MAX8552 high-speed, high-current gate drivers allow operation at high switching frequencies to reduce external component size and cost for small-footprint, low-profile designs. Pin-selectable 2-, 3-, and 4-phase operation and master-slave 6- and 8-phase operation provide output-current scalability for servers, workstations, desktops, desk notes, and networking applications.

The switching frequency of the MAX8524/MAX8525 is adjustable from 150kHz to 1.2MHz, permitting loop bandwidths of up to 200kHz. Peak current-mode control provides fast transient response and reduces cost. A proprietary current-sharing scheme reduces current imbalance between phases to less than 5% at full load.

The MAX8524/MAX8525 offer 0.4% initial accuracy and remote-sense functionality. Both controllers also feature programmable no-load offset and output-voltage positioning to adjust the output voltage as a function of the output current. The fast-active voltage positioning further reduces bulk output capacitors and cost.

Current-mode control also simplifies compensation with a variety of capacitors by eliminating the output-filter double pole associated with voltage-mode controllers. Both devices are compatible with electrolytic, tantalum, polymer, and ceramic capacitors. Output current sensing eliminates issues associated with controllers that use high-side current sense and ensure stable and jitter-free operation. Temperature-compensated, lossless inductor current sense eliminates the need for a current-sense resistor and further reduces cost, while maintaining voltage-positioning accuracy and reducing power dissipation.

The MAX8525 features control VID voltage transition for dynamic VID changes and eliminate both undervoltage and overvoltage overshoot. The PWRGD signal is accurate during VID code changes for the MAX8525 to avoid any false fault signal.

Adjustable foldback current-limit and overvoltage protection provide for a robust design.

Applications

Servers, Workstations

Desktop Computers

Desk Notes and LCD PCs

Voltage-Regulator Modules

High-End Switches and Routers

Features

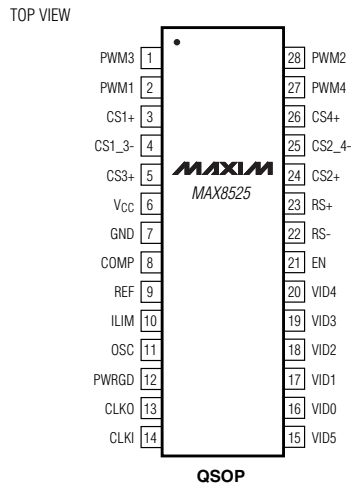
- **VRD/VRM 10 (MAX8525)**
- **VRD/VRM 9.1 (MAX8524)**
- **Fastest Load-Transient Response**
- **Rapid-Active Average Current Sensing**
  - **Better than 5% Current Balance**
  - **Fastest Voltage Positioning**
- **±0.4% Initial Output-Voltage Accuracy**
- **Pin-Selectable 2-/3-/4-Phase Operation**
- **Master-Slave 6-/8-Phase Operation**
- **Differential Remote Voltage Sensing**
- **Dynamic VID Change (MAX8525)**
- **Adjustable, Foldback Current Limit**
- **Soft-Start and Soft-Stop**
- **Power-Good Output**
- **150kHz to 1.2MHz Switching Frequency per Phase**
- **28-Lead QSOP Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX8524EEI	-40°C to +85°C	28 QSOP
MAX8524EEI+	-40°C to +85°C	28 QSOP
MAX8525EEI	-40°C to +85°C	28 QSOP
MAX8525EEI+	-40°C to +85°C	28 QSOP

+Denotes lead-free package.

Pin Configurations



Pin Configurations continued at end of data sheet.

Functional Diagram appears at end of data sheet.

2- to 8-Phase VRM 10/9.1 PWM Controllers with Precise Current Sharing and Fast Voltage Positioning

ABSOLUTE MAXIMUM RATINGS

REF, COMP, VID0 to VID5, OSC, CLKI, CLKO to GND ..... -0.3V to V_{CC} + 0.3V
RS+, RS-, ILIM to GND ..... -0.3V to V_{CC} + 0.3V
PWM_ to GND ..... -0.3V to V_{CC} + 0.3V
EN, PWRGD, V_{CC} to GND ..... -0.3V to +6V
CS1_3-, CS2_4-, CS_+ to GND ..... -0.3V to V_{CC} + 0.3V
Continuous Power Dissipation (T_A = +70°C)
28-Pin QSOP (derate 10.8mW/°C above +70°C) 860mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V, VID_ = high, ILIM = 1.5V, EN = open, RS- = GND = 0V, CLKI = open, CLKO = open, R_{OSC} = 95.3kΩ to GND, PWRGD = 100kΩ to V_{CC}, PWM_ = open, COMP = 1V, CS_+ = 1.1V, CS1_3- = CS2_4- = RS+ = 1.1V, **T_A = 0°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL					
V_{CC} Operating Range		4.5		5.5	V
V_{CC} UVLO Trip Level	Rising	4.0	4.25	4.5	V
	Hysteresis		270		mV
V_{CC} Shutdown Supply Current	V_{CC} < 3.75V, VID_ = GND		0.7	3	mA
V_{CC} Standby Supply Current	EN = 0V, V_{CC} = 5.5V		13	20	mA
V_{CC} Operating Supply Current	RS+ = 1.2V (no switching), set VID code for 1.100V		13	20	mA
Thermal Shutdown	Rising temperature, typical hysteresis = 15°C		165		°C
REFERENCE					
Reference Voltage	I_{REF} = 200µA	2.0 - 0.4%	2.0	2.0 + 0.4%	V
Reference Load Regulation	100µA < I_{REF} < 500µA			-0.05	%
Reference Line Regulation	4.5V < V_{CC} < 5.5V	-0.05		+0.05	%
Reference UVLO Trip Level	Rising edge, has 80mV typical hysteresis	1.74	1.84	1.95	V
SOFT-START					
Soft-Start Step Size			12.5		mV
Soft-Start Time per Step	Soft-start counts from EN rising (Note 1)	17	20	23	µs
VOLTAGE REGULATION					
RS+ Input Bias Current	V_{RS+} = 1.1V		0.1	1	µA
RS- Input Bias Current	V_{RS-} = 0.2V		0.1	1	µA
V_{OUT} Initial Accuracy	VID_ = 1.1V, T_A = +25°C	-0.4		+0.4	%
	VID_ = 1.1V	-0.6		+0.6	
V_{OUT} Droop Accuracy	(CS_+) = 1.125V		±5		%
COMP Output Current	(VO+) - (RS+) = 200mV		385		µA
GMV Amplifier Transconductance			2		mS
GMV Amplifier Gain-Bandwidth Product			5		MHz

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 5V, VID_ = high, ILIM = 1.5V, EN = open, RS- = GND = 0V, CLKI = open, CLKO = open, R_{OSC} = 95.3kΩ to GND, PWRGD = 100kΩ to V_{CC}, PWM_ = open, COMP = 1V, CS_+ = 1.1V, CS1_3- = CS2_4- = RS+ = 1.1V, **T_A = 0°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT-SENSE AMPLIFIERS					
CS_+, CS_- Input Bias Current	CS_+ = CS_- = 2V, RS+ = 0V		0.2	5	µA
Average Current-Limit Trip Level Accuracy	V_{ILIM} = 1.5V, T_A = +85°C	-10		+10	%
ILIM Input Bias Current	V_{ILIM} = 1.5V		0.01	1	µA
ILIM Default Program Level	$V_{ILIM} \geq V_{CC}$ - 0.2V		1		V
Peak Current-Limit Delay Time			20		ns
OSCILLATOR					
Oscillator Frequency Accuracy			10		%
Switching Frequency Range (per Phase)		150		1200	kHz
Slave-Mode CLKI/Set Frequency Ratio		0.8		4.0	
Maximum CLKO Duty-Cycle Skew	CLKO load < 50pF and R_{OSC} = 40.2kΩ		2		%
LOGIC INPUTS (EN)					
Input Low Level	V_{CC} = 4.5V to 5.5V			0.8	V
Input High Level	V_{CC} = 4.5V to 5.5V	2.8			V
Input Pullup Level	Internal pullup		V_{CC}		V
Input Pullup Resistance	Internal pullup	50	100	200	kΩ
LOGIC INPUTS (CLKI)					
Input Low Level	V_{CC} = 4.5V to 5.5V			1.2	V
Input High Level	V_{CC} = 4.5V to 5.5V	3.6			V
Input Pulldown Level	Internal pulldown		GND		V
Input Pulldown Resistance	Internal pulldown	50	100	200	kΩ
MAX8524 LOGIC INPUTS (VID0–VID4)					
Input Low Level	V_{CC} = 4.5V to 5.5V			0.8	V
Input High Level	V_{CC} = 4.5V to 5.5V	1.6			V
Input Pullup Level			V_{CC}		V
Input Pullup Resistance	Internal pullup resistance	10	15	20	kΩ
MAX8525 LOGIC INPUTS (VID0–VID5)					
Input Low Level	V_{CC} = 4.5V to 5.5V			0.4	V
Input High Level	V_{CC} = 4.5V to 5.5V	0.8			V
PWRGD OUTPUT					
Output Low Level	I_{PWRGD} = 4mA			0.4	V
Output High Leakage	V_{PWRGD} = 5.5V			1	µA
PWRGD Blanking Time	From EN rising, tracks CLKO	3		5	ms

2- to 8-Phase VRM 10/9.1 PWM Controllers with Precise Current Sharing and Fast Voltage Positioning

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 5V, VID_ = high, ILIM = 1.5V, EN = open, RS- = GND = 0V, CLKI = open, CLKO = open, R_{OSC} = 95.3kΩ to GND, PWRGD = 100kΩ to V_{CC}, PWM_ = open, COMP = 1V, CS_+ = 1.1V, CS1_3- = CS2_4- = RS+ = 1.1V, **T_A = 0°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
PWRGD Upper Threshold	Output rising	VID + 0.125		VID + 0.175	V
	Output falling	VID + 0.075		VID + 0.125	
PWRGD Lower Threshold	Output falling	VID - 0.250		VID - 0.200	V
	Output rising	VID - 0.175		VID - 0.125	
OVP PROTECTION					
Output Overvoltage Trip Threshold, OVP Action	MAX8524 output rising	VID + 0.20		VID + 0.25	V
	MAX8525 output rising	VID + 0.175		VID + 0.225	
PWM, CKLO OUTPUTS					
Output Low Level	$I_{PWM\_}$ = -5mA		0.1	0.4	V
Output High Level	$I_{PWM\_}$ = +5mA	4.5	4.9		V
Source Current	$V_{PWM\_}$ = V_{CC} - 2V		84		mA
Sink Current	$V_{PWM\_}$ = 2V		83		mA
Rise/Fall Times			10		ns
PWM Selection Threshold	V_{CC} = 4.5V to 5.5V	0.8	2.3	3.1	V

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V, VID_ = high, ILIM = 1.5V, EN = open, RS- = GND = 0V, CLKI = open, CLKO = open, R_{OSC} = 95.3kΩ to GND, PWRGD = 100kΩ to V_{CC}, PWM_ = open, COMP = 1V, CS_+ = 1.1V, CS1_3- = CS2_4- = RS+ = 1.1V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL					
V_{CC} Operating Range		4.5		5.5	V
V_{CC} UVLO Trip Level	Rising, typical hysteresis 270mV	4.0		4.5	V
V_{CC} Shutdown Supply Current	V_{CC} < 3.75V, VID_ = high			3	mA
V_{CC} Standby Supply Current	EN = 0V, V_{CC} = 5.5V			20	mA
V_{CC} Operating Supply Current	RS+ = 1.2V (no switching), set VID code for 1.100V			20	mA
REFERENCE					
Reference Voltage	I_{REF} = 200µA	2.0 - 0.5%		2.0 + 0.4%	V
Reference Load Regulation	100µA < I_{REF} < 500µA			-0.05	%
Reference Line Regulation	4.5V < V_{CC} < 5.5V	-0.05		+0.05	%
Reference UVLO Trip Level	Rising edge, has 80mV typical hysteresis	1.74		1.95	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 5V, VID_ = high, ILIM = 1.5V, EN = open, RS- = GND = 0V, CLKI = open, CLKO = open, R_{OSC} = 95.3kΩ to GND, PWRGD = 100kΩ to V_{CC}, PWM_ = open, COMP = 1V, CS_+ = 1.1V, CS1_3- = CS2_4- = RS+ = 1.1V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SOFT-START					
Soft-Start Time per Step	Soft-start counts from EN rising (Note 1)	17		23	µs
VOLTAGE REGULATION					
RS+ Input Bias Current	V_{RS+} = 1.1V			1	µA
RS- Input Bias Current	V_{RS-} = 0.2V			1	µA
V_{OUT} Initial Accuracy	VID_ = 1.1V	-1		+1	%
CURRENT-SENSE AMPLIFIERS					
CS_+, CS_- Input Bias Current	CS_+ = CS_- = 2V, RS+ = 0V			5	µA
ILIM Input Bias Current	V_{ILIM} = 1.5V			1	µA
OSCILLATOR					
Switching Frequency Range (per Phase)		150		1200	kHz
Slave-Mode CLKI/Set Frequency Ratio		0.8		4.0	
LOGIC INPUTS (EN)					
Input Low Level	V_{CC} = 4.5V to 5.5V			0.8	V
Input High Level	V_{CC} = 4.5V to 5.5V	2.8			V
Input Pullup Resistance	Internal pullup	50		200	kΩ
LOGIC INPUTS (CLKI)					
Input Low Level	V_{CC} = 4.5V to 5.5V			1.2	V
Input High Level	V_{CC} = 4.5V to 5.5V	3.6			V
Input Pulldown Resistance	Internal pulldown	50		200	kΩ
MAX8524 LOGIC INPUTS (VID0–VID4)					
Input Low Level	V_{CC} = 4.5V to 5.5V			0.8	V
Input High Level	V_{CC} = 4.5V to 5.5V	1.7			V
Input Pullup Resistance	Internal pullup resistance	10		20	kΩ
MAX8525 LOGIC INPUTS (VID0–VID5)					
Input Low Level	V_{CC} = 4.5V to 5.5V			0.4	V
Input High Level	V_{CC} = 4.5V to 5.5V	0.8			V

2- to 8-Phase VRM 10/9.1 PWM Controllers with Precise Current Sharing and Fast Voltage Positioning

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 5V, VID_ = high, ILIM = 1.5V, EN = open, RS- = GND = 0V, CLKI = open, CLKO = open, R_{OSC} = 95.3kΩ to GND, PWRGD = 100kΩ to V_{CC}, PWM_ = open, COMP = 1V, CS_+ = 1.1V, CS1_3- = CS2_4- = RS+ = 1.1V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

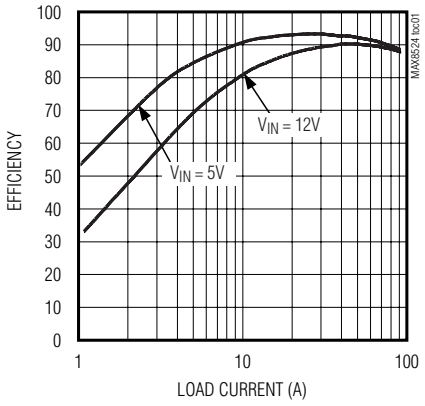
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
PWRGD OUTPUT					
Output Low Level	I_{PWRGD} = 4mA			0.4	V
Output High Leakage	V_{PWRGD} = 5.5V			1	µA
PWRGD Blanking Time	From EN rising, tracks CLKO	3		5	ms
PWRGD Upper Threshold	Output rising	VID + 0.125		VID + 0.175	V
	Output falling	VID + 0.075		VID + 0.125	
PWRGD Lower Threshold	Output falling	VID - 0.250		VID - 0.200	V
	Output rising	VID - 0.175		VID - 0.125	
OVP PROTECTION					
Output Overvoltage Trip Threshold, OVP Action	MAX8524 output rising	VID + 0.20		VID + 0.25	V
	MAX8525 output rising	VID + 0.175		VID + 0.225	
PWM, CLKO OUTPUTS					
Output Low Level	$I_{PWM\_}$ = -5mA			0.4	V
Output High Level	$I_{PWM\_}$ = +5mA	4.5			V
PWM Selection Threshold	V_{CC} = 4.5V to 5.5V	0.8		3.1	V

Note 1: Total soft-start time equals the soft-start time per step times the VID voltage divided by 12.5mV.
Note 2: Specifications at -40°C are guaranteed by design.

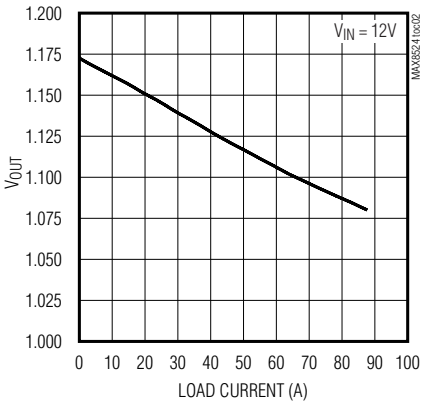
Typical Operating Characteristics

(V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT_MAX} = 80A, f_{SW} = 250kHz, T_A = +25°C, unless otherwise noted.)

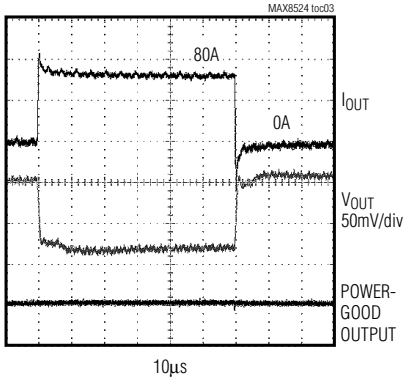
EFFICIENCY vs. LOAD CURRENT AT 1.45V OUTPUT



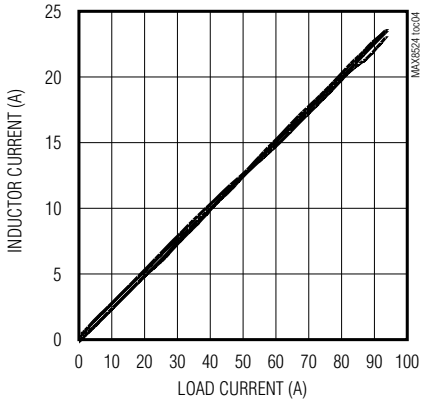
OUTPUT VOLTAGE vs. LOAD CURRENT



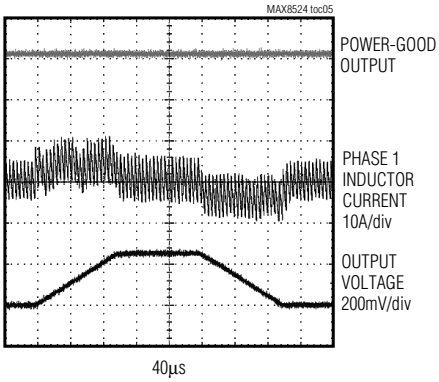
OUTPUT LOAD TRANSIENT



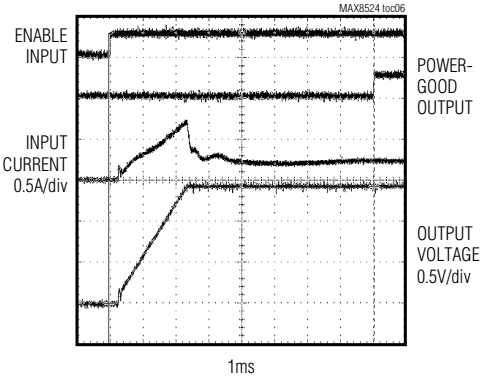
4-PHASE ACTIVE CURRENT SHARING



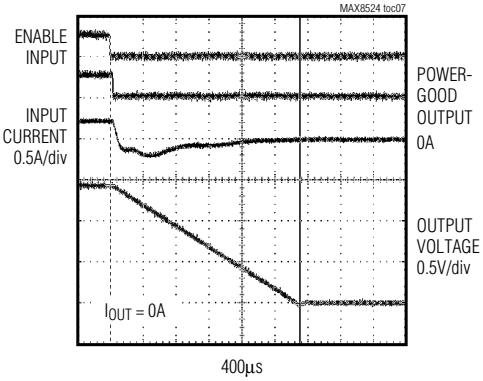
DYNAMIC VID RESPONSE, 250mV STEP VOLTAGE



SOFT-START WAVEFORMS AT 1.45V OUTPUT



SOFT-STOP WAVEFORMS AT 1.45V OUTPUT

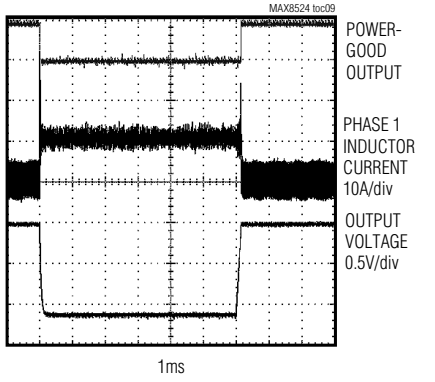


2- to 8-Phase VRM 10/9.1 PWM Controllers with Precise Current Sharing and Fast Voltage Positioning

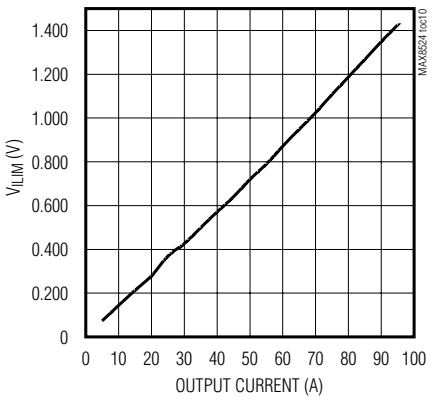
Typical Operating Characteristics (continued)

(V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT_MAX} = 80A, f_{SW} = 250kHz, T_A = +25°C, unless otherwise noted.)

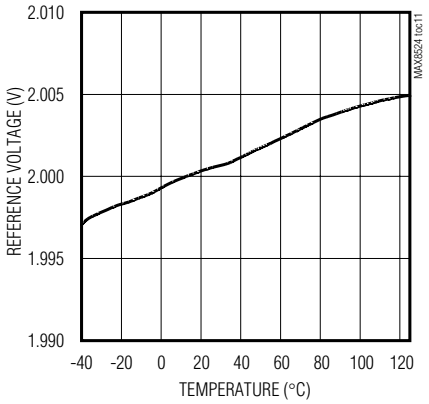
SHORT-CIRCUIT AND RECOVERY WAVEFORMS



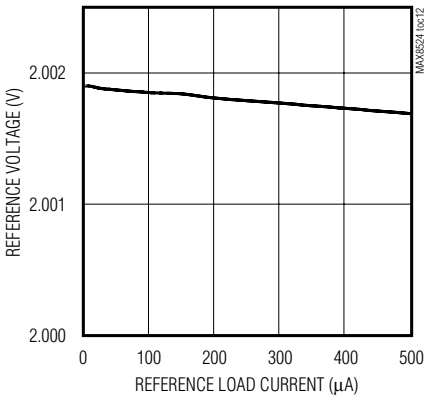
CURRENT-SENSE THRESHOLD vs. V_{ILIM}



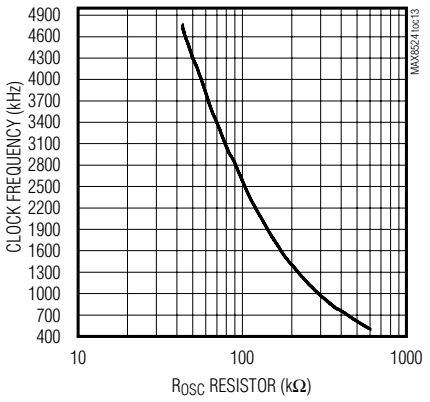
REFERENCE VOLTAGE vs. TEMPERATURE



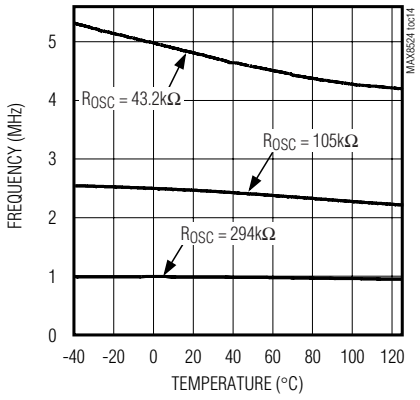
REFERENCE VOLTAGE LOAD REGULATION



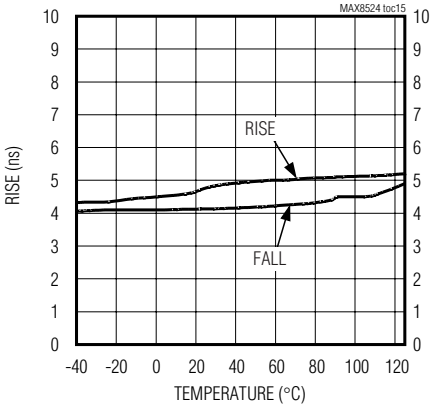
CLOCK FREQUENCY vs. R_{OSC}



CLOCK FREQUENCY vs. TEMPERATURE



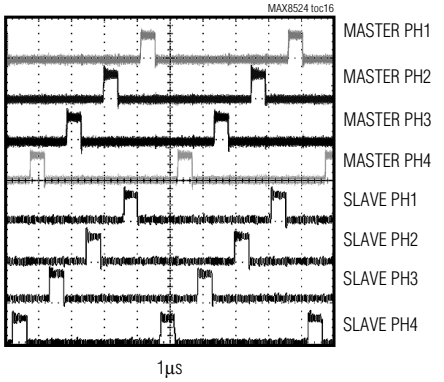
CLKO RISE AND FALL TIME vs. TEMPERATURE



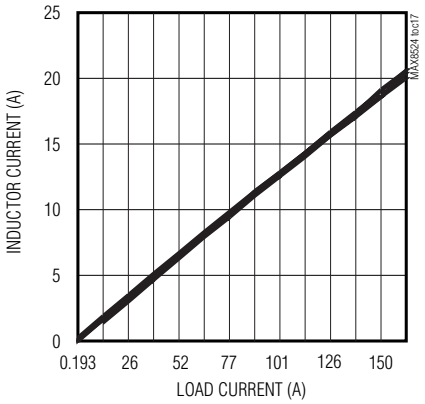
Typical Operating Characteristics (continued)

(V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT_MAX} = 80A, f_{SW} = 250kHz, T_A = +25°C, unless otherwise noted.)

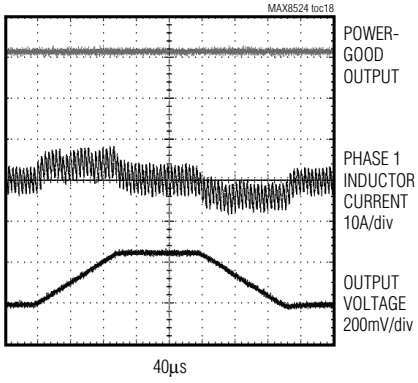
INTERLEAVED 8-PHASE OPERATION: LX WAVEFORMS



8-PHASE ACTIVE CURRENT SHARING



8-PHASE OPERATION: DYNAMIC VID RESPONSE



Pin Description

PIN		NAME	FUNCTION
MAX8524	MAX8525		
1	1	PWM3	PWM Signal Output for Phase 3. Logic low during shutdown.
2	2	PWM1	PWM Signal Output for Phase 1. Logic low during shutdown
3	3	CS1+	Positive Input of the Output Current Sense of Phase 1. Connect to the inductor side of the output current-sense resistor.
4	4	CS1_3-	Common Negative Input of the Output Current Sense of Phases 1 and 3. Connect to the load side of the output current-sense resistors.
5	5	CS3+	Positive Input of the Output Current Sense of Phase 3. Connect to the inductor side of the output current-sense resistor.
6	6	V_{CC}	IC Supply Input. Bypass to GND with a ceramic capacitor of at least 1µF.
7	7	GND	IC Ground. Single connection to system ground.
8	8	COMP	Error-Amplifier Output. Connect to a tap in a resistor-divider from REF to GND to set the finite DC gain for active voltage positioning. Add a series RC network from COMP to GND to compensate the control loop. For 6- or 8-phase operation, connect COMP pins of two controllers together for active current sharing.
9	9	REF	2.0V ±0.4% Reference Output. Bypass REF to GND with a ≤2.2µF low-ESR capacitor. REF can source 0.5mA for external loads. REF is alive when EN is low if V_{CC} is above UVLO.
10	10	ILIM	Output Current-Limit Set. Connect to a tap of a resistor-divider from REF to GND to set the cycle-by-cycle average current-limit threshold. Current limit (per phase) = V_{ILIM} / (50 x R_{SENSE}). Connect to V_{CC} to set the default 20mV current-limit threshold.
11	11	OSC	Internal Clock Oscillator Frequency-Set Input. Connect a resistor from OSC to GND to set the switching frequency. OSC must be connected to an external resistor even if the IC is used in slave mode. This pin is operational in shutdown if V_{CC} is above UVLO.
12	12	PWRGD	Open-Drain Power-Good Indicator. PWRGD pulls low until the output voltage is in regulation. PWRGD is low in shutdown and during UVLO.

2- to 8-Phase VRM 10/9.1 PWM Controllers with Precise Current Sharing and Fast Voltage Positioning

Pin Description (continued)

PIN		NAME	FUNCTION
MAX8524	MAX8525		
13	13	CLKO	Clock Synchronization Output for Master-Mode Operation. Connect CLKO of the master controller to CLKI of the slave controller. CLKO is active when EN is low, if V_{CC} is above UVLO to permit synchronized slave startup. CLKO is connected to the internal oscillator in both master and slave mode.
14	14	CLKI	Clock Synchronization Input. Connect CLKI to CLKO of the master controller for interleaved dual controller systems or to an external synchronization clock. Internal 100kΩ pulldown to GND permits floating this pin. See the *Paralleling Operation* section for detailed clocking operation.
15–19	16–19	VID0–VID4	DAC Code Input. The MAX8524 has a 15kΩ internal pullup resistor to V_{CC}. The MAX8525 requires an external pullup resistor.
—	15	VID5	DAC Code Input. The MAX8525 requires an external pullup resistor. Connect to V_{CC} for the MAX8524.
20	—	N.C.	No Connection
21	21	EN	Enable Input, Active High. Pulls up to V_{CC} through an internal 100kΩ resistor when UVLO is satisfied. Pull low with an external open-drain or open-collector input to shut down the controller. For master/slave operation, the EN pins of the MAX8524/MAX8525 controllers should be connected together.
22	22	RS-	Output-Voltage Remote-Sense, Negative Input. Connect to GND directly at the load.
23	23	RS+	Output-Voltage Remote-Sense, Positive Input. Connect to V_{OUT}+ directly at the load.
24	24	CS2+	Positive Input of the Output Current Sense of Phase 2. Connect to the inductor side of the output current-sense resistor. Short CS4+ to CS2_4- for 2-phase operation.
25	25	CS2_4-	Common Negative Input of the Output Current Sense of Phases 2 and 4. Connect to the load side of the output current-sense resistors.
26	26	CS4+	Positive Input of the Output Current Sense of Phase 4. Connect to the inductor side of the output current-sense resistor. Short CS4+ to CS2_4- for 2-, 3-, or 6-phase operation.
27	27	PWM4	PWM Signal Output for Phase 4. Connect this pin to V_{CC} for 2-, 3-, or 6-phase operation. Logic low during shutdown.
28	28	PWM2	PWM Signal Output for Phase 2. Connect this pin to V_{CC} for 2-phase operation. Logic low during shutdown.

Detailed Description

The MAX8524/MAX8525 are synchronous, scalable 2-/3-/4-phase, current-mode, step-down controllers. The MAX8524/MAX8525 can be used to implement either an embedded VRD design or a voltage regulator module (VRM) design with external MOSFET driver, such as the MAX8523.

The switching frequency of each phase can be set from 150kHz to 1.2MHz, permitting control bandwidth of up to 200kHz. The 5MHz gain-bandwidth product of the voltage-error amplifier ensures sufficient loop gain for most applications. In VRM applications, current balance between modules is within 5% at full load, maximizing the benefits of multiphase operation. Lossless inductor current sensing with temperature compensation can be used to reduce power dissipation while maintaining droop accuracy.

The MAX8524/MAX8525 controllers can be configured for 3-phase or 2-phase VRD or VRM applications by connecting one or two PWM pin(s) to the logic-supply pin (V_{CC}). In these modes, internal phasing is automatically adjusted for optimal ripple cancellation. The CLKI (clock in) and CLKO (clock out) features provided by the MAX8524/MAX8525 permit true 6- or 8-phase interleaved operation when two MAX8524/MAX8525 con-

Table 1. VID Programmed Output Voltage (VRM 10.0)

VID5	VID4	VID3	VID2	VID1	VID0	V_{OUT}
0	0	1	0	1	0	0.8375
1	0	1	0	0	1	0.8500
0	0	1	0	0	1	0.8625
1	0	1	0	0	0	0.8750
0	0	1	0	0	0	0.8875
1	0	0	1	1	1	0.9000
0	0	0	1	1	1	0.9125
1	0	0	1	1	0	0.9250
0	0	0	1	1	0	0.9375
1	0	0	1	0	1	0.9500
0	0	0	1	0	1	0.9625
1	0	0	1	0	0	0.9750
0	0	0	1	0	0	0.9875
1	0	0	0	1	1	1.0000
0	0	0	0	1	1	1.0125
1	0	0	0	1	0	1.0250
0	0	0	0	1	0	1.0375
1	0	0	0	0	1	1.0500
0	0	0	0	0	1	1.0625
1	0	0	0	0	0	1.0750
0	0	0	0	0	0	1.0875
1	1	1	1	1	1	OFF
0	1	1	1	1	1	OFF
1	1	1	1	1	0	1.1000
0	1	1	1	1	0	1.1125
1	1	1	1	0	1	1.1250
0	1	1	1	0	1	1.1375
1	1	1	1	0	0	1.1500
0	1	1	1	0	0	1.1625
1	1	1	0	1	1	1.1750
0	1	1	0	1	1	1.1875
1	1	1	0	1	0	1.2000
0	1	1	0	1	0	1.2125
1	1	1	0	0	1	1.2250
0	1	1	0	0	1	1.2375
1	1	1	0	0	0	1.2500
0	1	1	0	0	0	1.2625
1	1	0	1	1	1	1.2750
0	1	0	1	1	1	1.2875
1	1	0	1	1	0	1.3000
0	1	0	1	1	0	1.3125
1	1	0	1	0	1	1.3250
0	1	0	1	0	1	1.3375
1	1	0	1	0	0	1.3500
0	1	0	1	0	0	1.3625
1	1	0	0	1	1	1.3750
0	1	0	0	1	1	1.3875
1	1	0	0	1	0	1.4000
0	1	0	0	1	0	1.4125
1	1	0	0	0	1	1.4250
0	1	0	0	0	1	1.4375
1	1	0	0	0	0	1.4500
0	1	0	0	0	0	1.4625
1	0	1	1	1	1	1.4750
0	0	1	1	1	1	1.4875
1	0	1	1	1	0	1.5000
0	0	1	1	1	0	1.5125
1	0	1	1	0	1	1.5250
0	0	1	1	0	1	1.5375
1	0	1	1	0	0	1.5500
0	0	1	1	0	0	1.5625
1	0	1	0	1	1	1.5750
0	0	1	0	1	1	1.5875
1	0	1	0	1	0	1.5875

trollers are utilized, further reducing input and output ripple current. In 4-phase operation, the effective switching frequency is 0.6MHz to 4.8MHz. For 8-phase operation, the effective switching frequency is 1.2MHz to 9.6MHz.

The MAX8525 includes a 6-bit DAC (Intel VRM 10.0 compliant) and the MAX8524 includes a 5-bit DAC (Intel VRM 9.1 compliant), both able to achieve ±0.4% initial voltage accuracy. The power-good signal is accurate during VID code changes for the MAX8525 to avoid any fault signal due to the output voltage change requested by the CPU.

The MAX8524/MAX8525 also include programmable no-load offset and output-voltage positioning to adjust the output voltage as a function of the output current.

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Table 2. VID Programmed Output Voltage (VRM 9.1)

VID4	VID3	VID2	VID1	VID0	V_{OUT}
0	0	0	0	0	1.850
0	0	0	0	1	1.825
0	0	0	1	0	1.800
0	0	0	1	1	1.775
0	0	1	0	0	1.750
0	0	1	0	1	1.725
0	0	1	1	0	1.700
0	0	1	1	1	1.675
0	1	0	0	0	1.650
0	1	0	0	1	1.625
0	1	0	1	0	1.600
0	1	0	1	1	1.575
0	1	1	0	0	1.550
0	1	1	0	1	1.525
0	1	1	1	0	1.500
0	1	1	1	1	1.475
1	0	0	0	0	1.450
1	0	0	0	1	1.425
1	0	0	1	0	1.400
1	0	0	1	1	1.375
1	0	1	0	0	1.350
1	0	1	0	1	1.325
1	0	1	1	0	1.300
1	0	1	1	1	1.275
1	1	0	0	0	1.250
1	1	0	0	1	1.225
1	1	0	1	0	1.200
1	1	0	1	1	1.175
1	1	1	0	0	1.150
1	1	1	0	1	1.125
1	1	1	1	0	1.100
1	1	1	1	1	Shutdown

Clock Frequency (OSC)

The clock frequency of the MAX8524/MAX8525 is set by an external resistor from OSC to ground. After selecting the switching frequency per phase, f_{SW}, and the number of phases, using Table 3, select the clock frequency. For 6- or 8-phase operation, connect an external resistor to OSC of both master and slave controllers even if the MAX8524/MAX8525 is operated in slave mode. A 1% resistor is recommended for the R_{OSC} to maintain good frequency accuracy, and R_{OSC} should be placed as close as possible to the OSC pin.

Table 3. Clock Frequency Setting vs. Switching Frequency and Number of Phases

NO. OF PHASES	PIN CONNECTIONS	f_{CLKO}
2	PWM2 = PWM4 = V_{CC}	4 x f_{SW}
3	PWM4 = V_{CC}	3 x f_{SW}
4	—	4 x f_{SW}
6	PWM4 = V_{CC}	3 x f_{SW}
8	—	4 x f_{SW}

Voltage Reference (REF)

A precision 2V reference is provided by the MAX8524/MAX8525 at the REF pin. REF is capable of sourcing up to 500µA for external loads. REF stays alive when EN is low and while V_{CC} is above UVLO. Connect a 0.22µF ceramic capacitor from REF to GND. The capacitor should be placed as close to the REF pin as possible.

An internal REFOK monitors the reference voltage. The reference voltage must be above the REFOK threshold of 1.85V to activate the controller. The controller is disabled if the reference voltage falls below 1.81V.

Output Current Sensing (CS_+, CS_-)

The output current of each phase is sensed differentially with a shared common return for each phase pair. A low offset voltage and high-gain (50V/V) differential current amplifier at each phase allow low-resistance current-sense resistors to be used to minimize power dissipation. Sensing the current at the output of each phase offers advantages, including less noise sensitivity, more accurate current sharing between phases, and the flexibility of using either a current-sense resistor or the DC resistance of the output inductor.

Using the DC resistance, R_{DC}, of the output inductor allows higher efficiency. In this configuration, the initial tolerance and temperature coefficient of R_{DC} must be accounted for in the output-voltage droop-error budget. An RC filtering network is needed to extract the current information from the output inductor, as shown in Figure 1. The time constant of the RC network is governed by equation 1:

$$RC = \frac{L}{R_{DC}} \qquad \text{(Eq 1)}$$

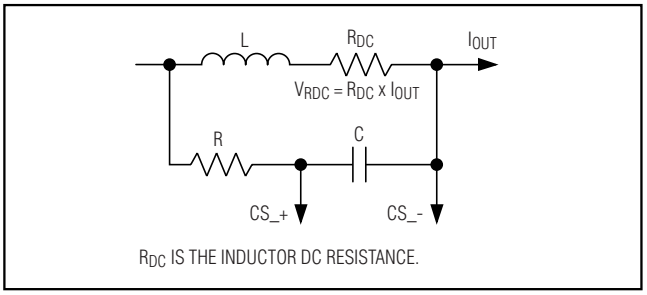


Figure 1. Inductor R_{DC} Current Sense

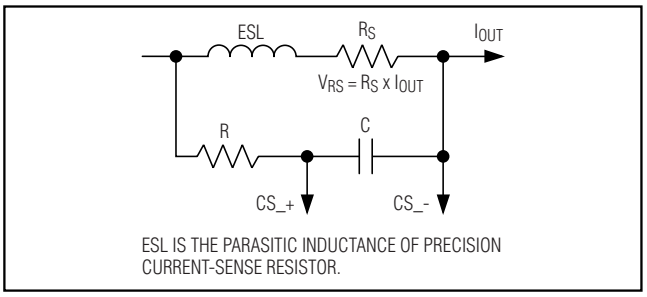


Figure 2. Current-Sense Resistor

where L is the inductance of the output inductor. For 20A or higher current-per-phase applications, the DC resistance of commercially available inductors is about 1mΩ, as shown in Table 4. To minimize current-sense error due to the bias current at current-sense pins, choose R less than 2kΩ (Figure 1). Determine the value for C from equation 1. Choose the capacitor with 5% tolerance and the resistor with 1% tolerance. Temperature compensation is recommended for this current-sense scheme. See the *Loop Compensation and Output-Voltage Positioning* section for detailed information.

When a current-sense resistor is used for more accurate output-voltage positioning, similar RC filtering circuits should be used to cancel the equivalent series inductance of the current-sense resistor, as shown in Figure 2. Using criteria similar to that stated in the previous paragraph, the value of C can be determined by equation 2:

$$C = \frac{ESL}{R_S \times R} \qquad \text{(Eq 2)}$$

where ESL is the equivalent series inductance of the current-sense resistor, R_S is the value of the current-sense resistor, and C is the value of the compensation capacitor. For example, a 1mΩ 2025-package sense resistor has an ESL of 1.6nH.

Output Current-Limit and Short-Circuit Protection (ILIM)

The MAX8524/MAX8525 provide a cycle-by-cycle current limit to control the average output current as programmed by the user at the ILIM pin. This approach is insensitive to input-voltage variation and inductor tolerance. Once the current-limit threshold is exceeded, the duty cycle is terminated immediately and the output inductor current starts to ramp down. At the next switching cycle, the PWM pulse is skipped if the output inductor current is still above the current-limit threshold. The current-limit threshold is adjustable over a wide range by connecting a resistor-divider from the REF pin to GND with the center tap connected to ILIM. Connecting ILIM to V_{CC} sets the default current threshold to 20mV at the current-sense resistor.

The MAX8524/MAX8525 offer current foldback protection under soft-start and overload conditions. This feature allows the VRM to safely operate under short-circuit conditions and to automatically recover once the short-circuit condition is removed. Once the output voltage falls below the low PWRGD threshold, the foldback current threshold is set to half the current-limit threshold.

Output Voltage Differential Sensing (RS+, RS-)

The MAX8524/MAX8525 feature differential output-voltage sensing to achieve the highest possible output accuracy. This allows the controllers to sense the actual voltage at the load, so the controller can compensate for losses in the power output and ground lines.

Table 4. Output Inductor List

MANUFACTURER AND PART NO.	BI Technologies HM73-40R50 0.5µH/50A	Panasonic ETQP1H0R6BFA 0.6µH/30A	Sumida CDEP149(H) 0.45µH/32A	Coiltronics HC2-0R68 0.68µH/50A
R_{DC} (mΩ)	0.78 (typ) 1.0 (max)	0.9 (max)	0.9 (typ) 1.1 (max)	0.6 (max)

2- to 8-Phase VRM 10/9.1 PWM Controllers with Precise Current Sharing and Fast Voltage Positioning

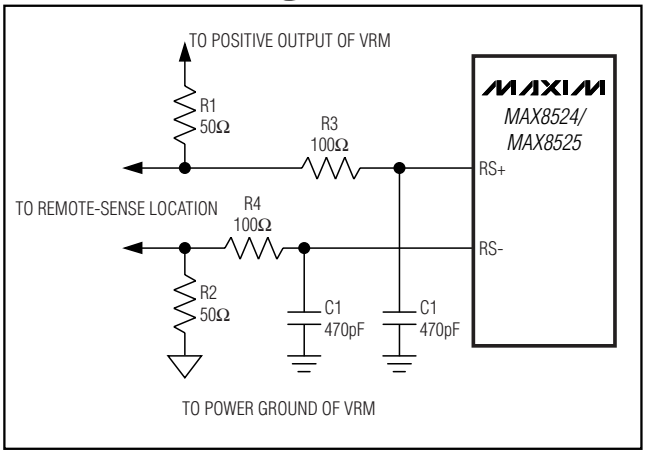


Figure 3. Recommended Filtering for Output-Voltage Remote Sensing

Traces from the load point back to RS+ and RS- should be routed close to each other and as far away as possible from noise sources (such as inductors and high di/dt traces). Use a ground plane to shield the remote-sense traces from noise sources. To filter out common-mode noise, RC filtering is recommended for these pins as shown in Figure 3. For VRD applications, a 100Ω resistor with a 470pF capacitor should be used. For VRM applications, additional 50Ω resistors should be connected from these pins to the local outputs of the converter before the VRM connector. This avoids excessive voltage at the CPU in case the remote-sense connections get disconnected.

Loop Compensation (COMP)

During a load transient, the output voltage instantly changes due to the ESR of the output capacitors by an amount equal to their ESR times the change in load current ($\Delta V_{OUT} = -R_{ESR\_CO} \times \Delta I_{LOAD}$). The voltage-positioning method allows better utilization of the output regulation window, resulting in fewer output capacitors. The MAX8524/MAX8525 employ rapid-active average scheme, a proprietary current-mode architecture that adjusts the output current based on instantaneous output voltage, resulting in fast voltage positioning.

The voltage-error amplifier consists of a high bandwidth and high-accuracy transconductance amplifier (GMV). See the *Functional Diagram*. The negative input of the transconductance amplifier is connected to the output of the remote-voltage differential amplifier, and the positive input is connected to the output of an internal DAC controlled by VID inputs. The DC gain of the transconductance amplifier is set to a finite value to achieve fast output-voltage positioning by connecting an equivalent resistor, R_E, from the COMP pin to GND ($R_E = R_U//R_B$). The value of R_E is determined by the amount of droop required at full load, which is specified as the output impedance or the load line in Intel VRM specifications.

According to the Intel VRM specifications, the output voltage at no load cannot exceed the voltage specified by the VID code, including the initial set tolerance, ripple voltage, and other errors. Therefore, the actual output voltage should be biased lower to compensate for these errors. Connect a resistor-divider, R_U and R_B, from REF to GND, with the tap connected to COMP, to set the offset voltage.

For 6- or 8-phase operations, connect COMP pins of the two controllers together for active current sharing.

Dynamic VID Change (MAX8525 Only)

The MAX8525 offers the ability to dynamically change the VID inputs while the controller is operating (on-the-fly, or OTF). This feature allows the processor to adjust its core voltage in a 250mV window. The MAX8525 output voltage changes in 12.5mV steps when a VID change is detected.

The VID inputs of the MAX8525 comply with Intel's 400ns logic-skew timing specifications to prevent false code changes. Once the timer expires, the controller starts to change the DAC output. Figure 4 shows the output voltage step during a VID OTF event. The MAX8525 controller accepts both step-by-step changes of VID inputs or all-at-once VID inputs changes. For all-at-once VID input changes, the output-voltage slew rate is the same as 12.5mV per step and 2µs duration.

Paralleling Operation (CLKI and CLKO)

Two MAX8524/MAX8525s can be connected together to generate 6-phase or 8-phase core supplies. In this configuration, one MAX8524/MAX8525 serves as a master and the other serves as a slave. Connect the CLKI pin of the slave controller to the CLKO pin of the master controller. Interleaved operation is achieved by synchronizing the master controller to the CLKO rising edge and the slave controller to the CLKO falling edge. Figure 5 shows the clock timing between the phases of both master and slave controllers.

2-Phase and 3-Phase Operation Selection (PWM3 and PWM4)

The MAX8524/MAX8525 can operate in 2-, 3-, and 4-phase operation. Connect PWM4 to V_{CC} for 2-, 3-, or 6-phase operation. Also connect PWM2 to V_{CC} for 2-phase operation. All PWM outputs are held low during shutdown.

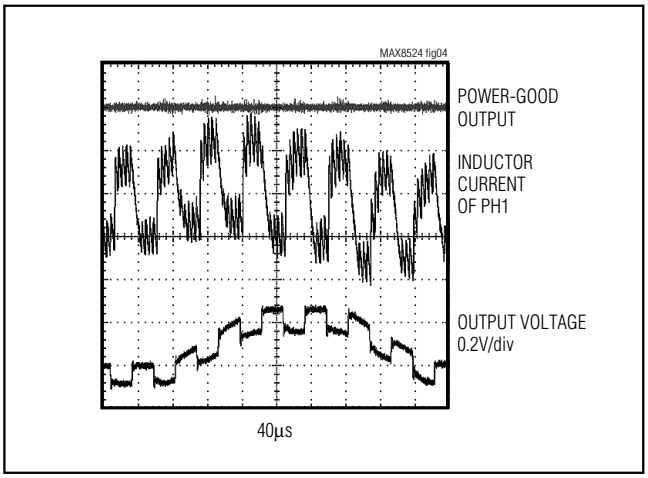


Figure 4. Output-Voltage Waveform During VID On-the-Fly Change with Load Transients

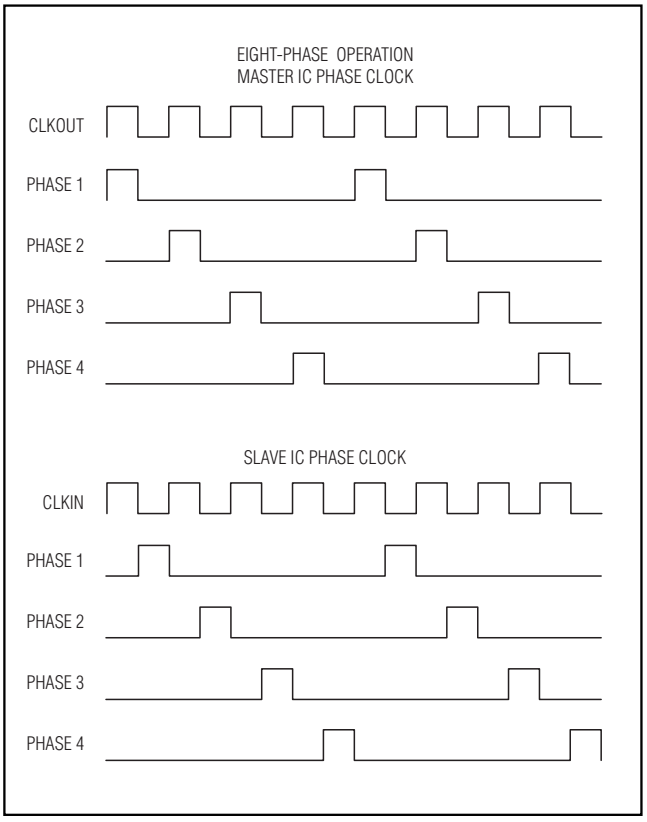


Figure 5. Clock Relationships Between the Master and Slave Controllers

Power-Good Output (PWRGD)

PWRGD is an open-drain output that is pulled low when the output voltage rises above the PWRGD upper threshold or falls below the PWRGD falling threshold. PWRGD is held low in shutdown, V_{CC} < UVLO, and during soft-start conditions. For logic-level output voltages, connect an external pullup resistor between PWRGD and the logic power supply. A 100kΩ resistor works well in most applications.

UVLO, Output Enable (EN), and Soft-Start

When the IC supply voltage (V_{CC}) is less than the UVLO threshold, all PWM outputs are held low and most internal circuitry is shut down to reduce the quiescent current. When EN is released and V_{CC} > UVLO, the internal 100kΩ resistor pulls EN to V_{CC} and soft-start is initiated. During soft-start, the output of the internal DAC ramps up at 12.5mV per step. For 6- or 8-phase operation, connect EN of two MAX8524/MAX8525s together and drive it by an open-drain signal, as shown in Figure 6.

Output Overvoltage Protection (OVP)

When the output voltage exceeds the regulation voltage by 225mV for the MAX8524 or 200mV for the MAX8525, all PWM outputs are pulled low and the controller is latched off. To discharge the output voltage, the MOSFET drivers must keep the low-side MOSFETs on and high-side MOSFETs off. The MAX8523 dual-phase and the MAX8552 single-phase MOSFET drivers fulfill this requirement. The latch condition can only be cleared by cycling the input voltage (V_{CC}).

Thermal Protection

The MAX8524/MAX8525 feature a thermal-fault-protection circuit. When the junction temperature rises above +150°C, an internal thermal sensor activates the shutdown circuit to hold all PWM outputs low to disable switching. The thermal sensor reactivates the controller after the junction temperature cools by 15°C.

Design Procedure

Setting the Switching Frequency

The switching frequency determines the switching loss and the size of the power components. Higher switching frequency results in smaller external components and more compact design. However, switching loss and magnetic core loss are directly proportional to the switching frequency. Select a switching frequency as a tradeoff of the efficiency and size. The clock frequency can be selected from Table 3.

2- to 8-Phase VRM 10/9.1 PWM Controllers with Precise Current Sharing and Fast Voltage Positioning

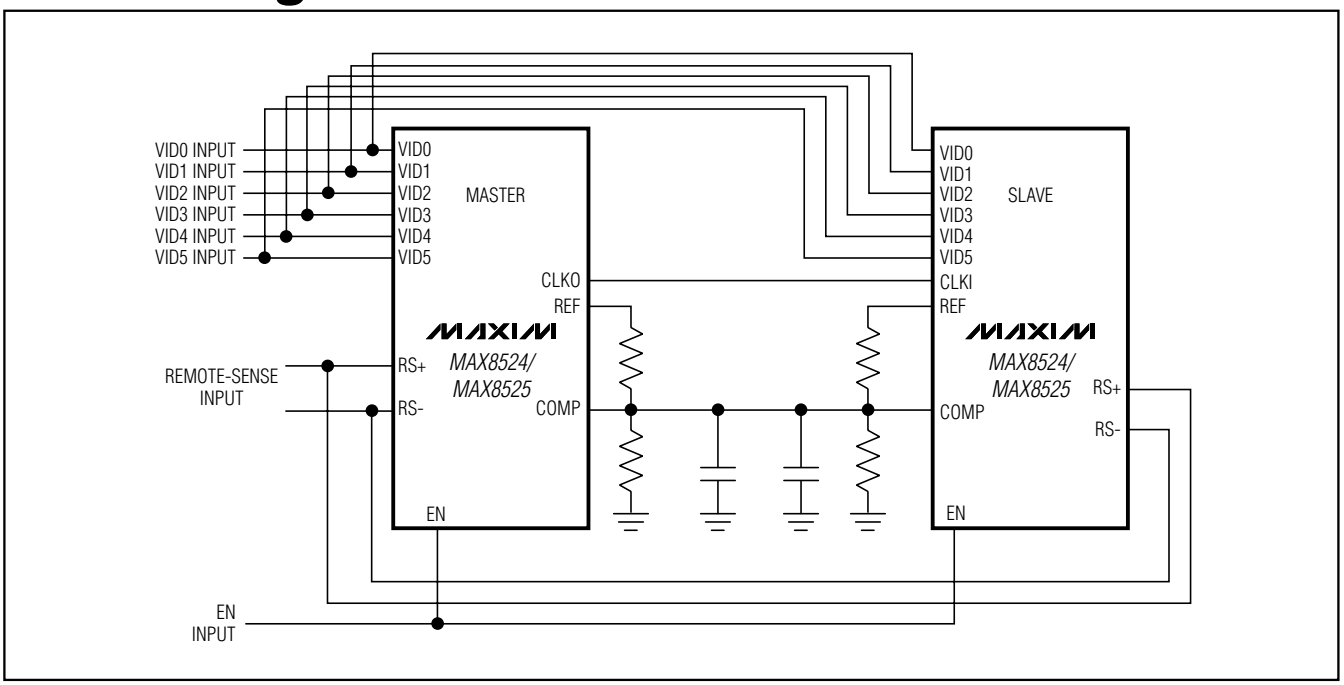


Figure 6. Master and Slave Controller Connections

See the Clock Frequency vs. R_{OSC} graph in the *Typical Operating Characteristics* section for the relationship between the clock frequency and the value of the frequency-setting resistor, R_{OSC}. The value of R_{OSC} for a given clock frequency can also be approximated from equation 3:

$$R_{OSC} = 277.704 \times f_{OSC(MHz)}^{-1.197}\ k\Omega \quad \text{(Eq 3)}$$

Output Inductor Selection

Output inductance is set by the desired amount of inductor current ripple (LIR) and the slew rate of the inductor current during a load transient. A larger inductance value minimizes output ripple current and increases efficiency but slows down the current slew rate. For the best tradeoff of size, cost, and efficiency, an LIR of 30% to 60% is recommended (LIR = 0.3 to 0.6). Choose LIR close to the high end when more phases are used. The inductor value is determined from:

$$L \geq \frac{V_{OUT} \times (1 - D) \times N}{LIR \times f_{SW} \times I_{OUT\_MAX}}\ H \quad \text{(Eq 4)}$$

where f_{SW} is the switching frequency, I_{OUT_MAX} is the maximum-rated output current, D is the duty ratio, and V_{OUT} is the output voltage at a given VID code. Check the output-inductance ripple current for the ripple voltage it produces across the output capacitor ESR. For an n-phase VRM converter, the output ripple voltage, V_{RIPPLE}, can be calculated using:

$$V_{RIPPLE} = \frac{V_{OUT} \times R_{ESR\_CO} \times (1 - (N \times D))}{f_{SW} \times L} \quad \text{(Eq 5)}$$

For ripple voltage estimate, it is safe to replace R_{ESR_CO} with R_O, the VRM output impedance. If the output ripple voltage is not satisfied, a larger value of output inductance should be chosen. The selected inductor should have the lowest possible DC resistance and the saturation current should be greater than the peak inductor current, I_{PEAK}. I_{PEAK} is found from:

$$I_{PEAK} = I_{OUT\_MAX} \frac{(2 + LIR)}{2 \times N} \quad \text{(Eq 6)}$$

When the DC resistance of the output inductor is used for current sensing, the range of DC resistances is limited by the following constraints:

$$R_{DC} \le \frac{5 \times N}{50 \times I_{OUT\_MAX} \times (2 + LIR)} \quad \text{(Eq 7)}$$

and

$$R_{DC} \ge \frac{N}{50 \times I_{OUT\_MAX} \times (2 + LIR)} \quad \text{(Eq 8)}$$

Output Capacitor Selection

In most cases, selection of the output capacitor is dictated by the ESR requirement to meet the core-supply transient responses. The target equivalent series resistance is $R_{ESR\_CO} = R_O$. The minimum output capacitance, $C_O(min)$, based on the energy balance, is then calculated from:

$$C_O(min) \ge \frac{1}{2} \times \frac{L \times I_{OUT\_MAX}}{N \times R_O \times V_{OUT}} \quad \text{(Eq 9)}$$

There is also an upper limit on the amount of output capacitance to meet the OTF VID change requirement. Too much output capacitance may prevent the output voltage from reaching the new VID output voltage within the OTF time window:

$$C_O(max) \le \frac{(I_{LIM} - I_{OUT\_MAX})^2 \times t_{OTF}}{V_{OTF}} \quad \text{(Eq 10)}$$

where t_{OTF} is the time window to reach V_{OTF}, the OTF voltage steps. If $C_O(max)$ is less than $C_O(min)$, the system does not meet the VID OTF specification.

Combinations of different types of capacitors, such as SPCAPs, POSCAPs, or low-ESR aluminum electrolytic capacitors may be needed to achieve the required R_{ESR_CO} and the output capacitance simultaneously. If the combination cannot be reached, the output inductance must be adjusted.

Input Capacitor Selection

The input capacitor reduces the peak current drawn from the power source and reduces the noise and voltage ripple on the input caused by the circuit's switching. The input capacitors must meet the ripple current requirement, I_{RMS}, imposed by the switching currents as defined by equation 11:

$$I_{RMS} = D \times I_{OUT\_MAX} \times \sqrt{\frac{1}{N \times D} - 1} \quad \text{(Eq 11)}$$

Use the minimum input voltage to calculate the input ripple current. Low-ESR capacitors, such as low-ESR aluminum electrolytic capacitors, polymer capacitors, and ceramic capacitors, should be used to avoid large voltage transients at the input during a large step load change at the output. The capacitors' ripple-current specifications provided by the manufacturer should be carefully reviewed. Additional small-value low-ESL ceramic capacitors (1µF to 10µF/16V) can be used in parallel to reduce the high-frequency ringing.

Power MOSFET Selection

MOSFET power dissipation depends on the gate-drive voltage (V_G), the on-resistance (R_{DSON}), the total gate charge (Q_{GT}), and the gate threshold voltage (V_{TH}). The supply voltage range for MOSFET drivers (MAX8523) is from 4.5V to 6.5V. With V_{GATE} < 10V, logic-level threshold MOSFETs are recommended.

Power dissipation in the high-side MOSFET consists of two parts: the conduction loss and the switching loss. The conduction loss for each high-side switch can be calculated from equation 12:

$$P_{COND\_HS} = D \times \frac{I^2_{OUT\_MAX2}}{N^2} \times \left(1 + \frac{LIR^2}{12}\right) \times \frac{R_{DSON\_HS}}{M_{HS}} \quad \text{(Eq 12)}$$

where M_{HS} is the number of MOSFETs in parallel for each high-side switch. Total high-side conduction loss equals the number of phases times P_{COND_HS}. Switching loss is the major contributor to the high-side MOSFET power dissipation due to the hard switching transition every time it turns on. The switching loss can be found from the following:

$$P_{SW\_HS} = \frac{2 \times V_{IN} \times I_{OUT\_MAX}}{N} \times \frac{R_{GATE} \times Q_{MILLER}}{V_D - V_{TH}} \times f_{SW} \times M_{HS} \quad \text{(Eq 13)}$$

where V_D is the gate-drive voltage and R_G is the total gate resistance including the driver's on-resistance from the MAX8523 (0.8Ω) and the MOSFET's gate resistance. Q_{MILLER} is the MOSFET's Miller charge, which can be found in the MOSFET's data sheet. For a logic-level power MOSFET, the gate resistance is about 2Ω. Note that adding more MOSFETs in parallel at the high-side switch increases the switching loss. Smaller gate charge and lower gate resistance usually result in lower switching loss.

The low-side MOSFET power dissipation is mostly attributed to the conduction loss. Switching loss is negligible due to the zero voltage switching at turn-on and body diode clamp at turn-off. Power dissipation in the

2- to 8-Phase VRM 10/9.1 PWM Controllers with Precise Current Sharing and Fast Voltage Positioning

low-side MOSFETs of each phase can be calculated from the following equation:

$$P_{COND\_LS} = (1\text{-}D) \times \frac{I^2_{OUT\_MAX2}}{N^2} \times \left(1+\frac{LIR^2}{12}\right) \times \frac{R_{DSON\_LS}}{M_{LS}} \quad \text{(Eq 14)}$$

where R_{DSON_LS} is the on-resistance of the low-side MOSFET and M_{LS} is the number of MOSFETs in parallel for the low-side switch. Total power dissipation for the low-side switches equals the number of phases times the low-side conduction loss of each phase. Even though the switching loss is insignificant in the low-side MOSFETs, R_{DSON} is not the only parameter that should be considered in selecting the low-side MOSFET. Large Miller capacitance (C_{RSS}) could turn on the low-side MOSFETs momentarily when the drain-to-source voltage goes high at fast slewing rates if the driver cannot hold the gate low. The ratio of C_{RSS}/C_{ISS} should be less than 1/10th for the low-side MOSFETs to avoid shoot-through current due to momentary turn on of the low-side switch.

The gate-driver power dissipation is also important. The MAX8523 is a 0.8Ω/0.6Ω dual-channel driver, whereas the MAX8552 is a 0.8Ω/0.6Ω single-channel driver. Power dissipation in each driver is given by:

$$P_{DRIVER} = V_D \times \left[2 \times f_{SW} \times (M_{LS} \times Q_{G\_LS} + M_{HS} \times Q_{G\_HS}) + I_{CC}\right] \quad \text{(Eq 15)}$$

where I_{CC} is the supply current of the MAX8523. Ensure the power loss does not exceed the package power dissipation.

Loop Compensation and Output-Voltage Positioning

Once the current-sense resistance (R_{SENSE}), the output impedance (R_O), and the output offset voltage (V_{OS}) are known, the values of R_U and R_B are calculated from equations 16 and 17:

$$R_U = \frac{1}{\frac{G_M}{2}\left[\frac{NR_O}{R_{SENSE} \times 50} - V_{OS}\right]} \quad \text{(Eq 16)}$$

$$B = \frac{1}{\frac{G_M}{2}\left[\frac{NR_O}{R_{SENSE} \times 50} + V_{OS}\right] - \frac{1}{20 \times 10^6}} \quad \text{(Eq 17)}$$

where G_M is the transconductance (2ms). A capacitor, C_C, must be connected from COMP to ground to roll off the gain at high frequency. The capacitor value can be found from the following equation once the output capacitor's ESR zero frequency is known to obtain first-order rolloff at zero across frequency:

$$C_C = \frac{R_{ESR\_CO} \times C_O}{R_E} \quad \text{(Eq 18)}$$

where R_{ESR_CO} is the total equivalent series resistance and C_O is the total capacitance of the output capacitors, respectively. R_E is the parallel equivalent resistance of R_U and R_B.

Setting the Current Limit

Current-limit threshold sets the maximum available output DC current. To meet the OTF operation, the output current limit, I_{LIM}, should be set at least 15% higher than the maximum rated output current, I_{OUT_MAX}. The voltage at ILIM and the value of the current-sense resistor or the DC resistance of the output inductors set the current-limit threshold:

$$V_{ILIM} = 50 \times R_{SENSE} \times \frac{I_{LIM}}{N} \quad \text{(Eq 19)}$$

for the resistor current sensing and:

$$V_{ILIM} = 50 \times R_{DC} \times \frac{I_{LIM}}{N} \quad \text{(Eq 20)}$$

for DC resistance of the output inductor current sensing. In equation 22, the value of R_{DC} at the high ambient temperature must be used to guarantee the rated output current. V_{ILIM} can be set by connecting ILIM to a resistor-divider from REF to GND. Select resistors R26 and R27 from the schematics in Figure 7 so the current through the divider is at least 10µA:

$$R26 + R27 \le 200k\Omega \quad \text{(Eq 21)}$$

A typical value for R27 is 100kΩ; then solve for R26 using:

$$R26 = R27 \times \frac{2 - V_{ILIM}}{V_{ILIM}} \quad \text{(Eq 22)}$$

Applications Information

PC Board Layout Guidelines

A properly designed PC board layout is important in any switching DC-DC converter circuit. If possible, mount the MOSFETs, inductors, input/output capacitors, and current-sense resistor on the top side of the PC board. Connect the ground for these devices close together on a power ground plane. Make all other ground connections to a separate analog ground plane. Connect the analog ground plane to power ground at a single point.

To help dissipate heat, place high-power components (MOSFETs and inductors) on a large PC board area, or use a heat sink. Keep high-current traces short, wide, and tightly coupled to reduce trace inductances and resistances. Also, make the gate-drive connections (DH_ and DL_) short, wide, and tightly coupled to reduce EMI and ringing induced by high-frequency gate currents.

Use Kelvin-sense connections for the current-sense resistors. All signal traces of the current sense and the remote-voltage sense should be tightly coupled and as far away as possible from the inductors and other switching noise sources. Use the ground plane to shield the current-sense traces and the feedback from noise sources.

Place the REF capacitor, the V_{CC} capacitor, the current-sense decoupling capacitors, and the remote-sense decoupling capacitors as close to the MAX8524/MAX8525 as possible.

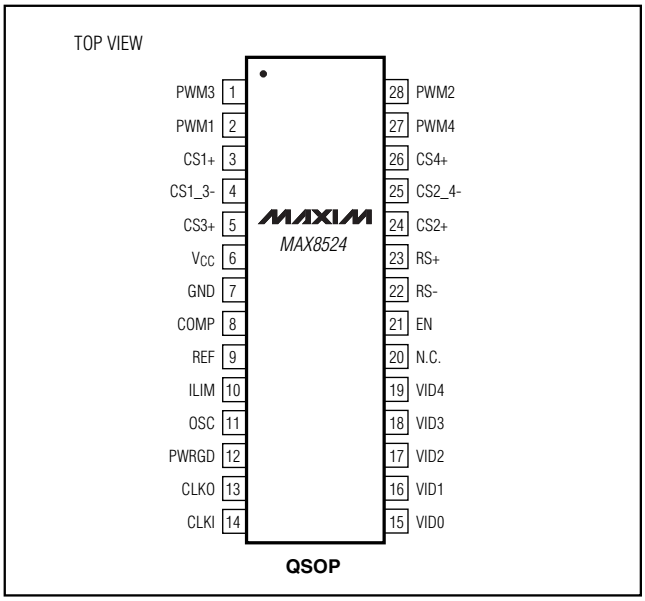
For an example PC board layout, refer to the MAX8525 evaluation kit.

Chip Information

TRANSISTOR COUNT: 9021

PROCESS: BiCMOS

Pin Configurations (continued)



2- to 8-Phase VRM 10/9.1 PWM Controllers with Precise Current Sharing and Fast Voltage Positioning

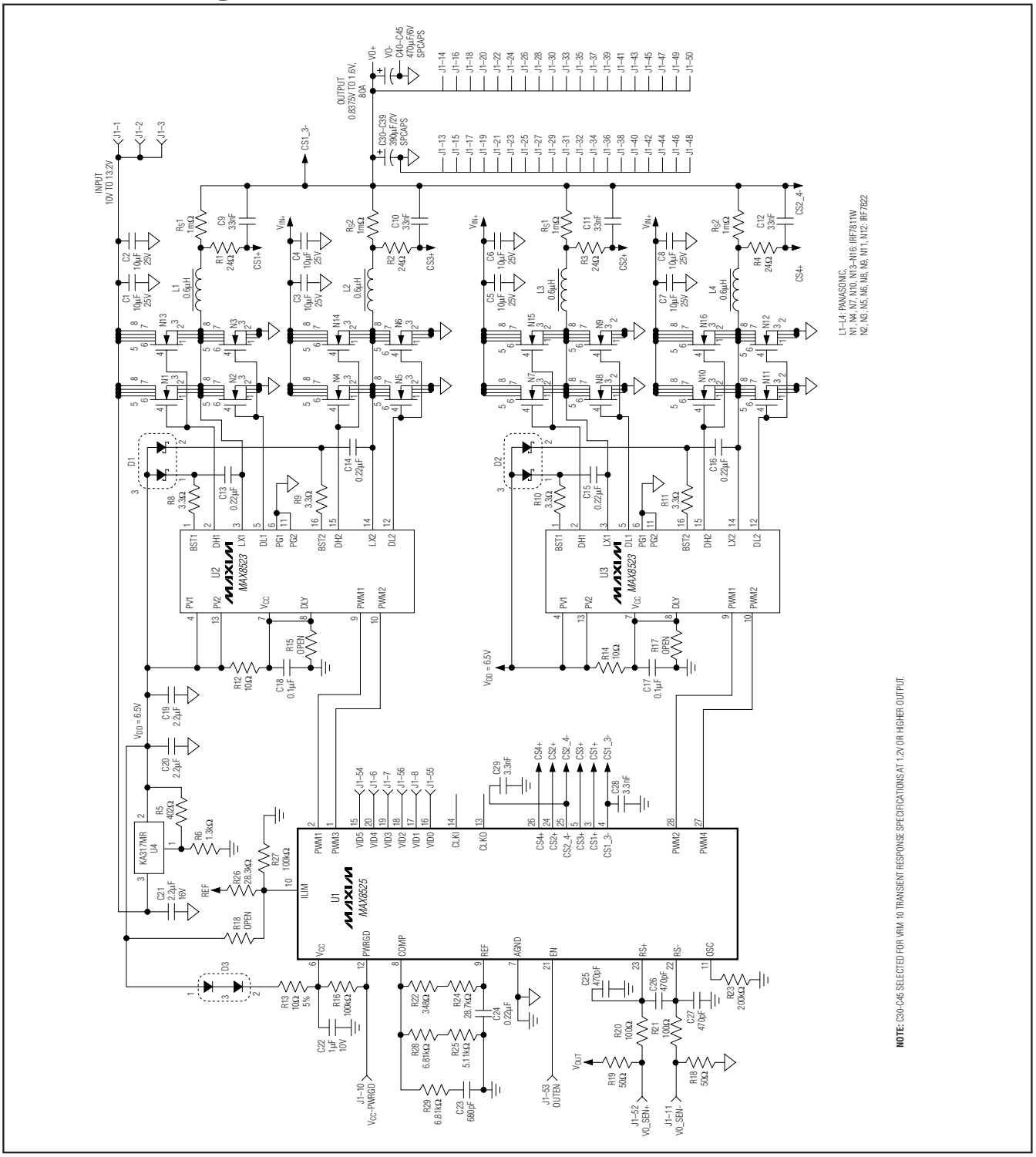


Figure 7. Typical Application Circuit for VRM 10 Using a Sense Resistor for Output Current Sensing and 8-Pin SO MOSFET Packages

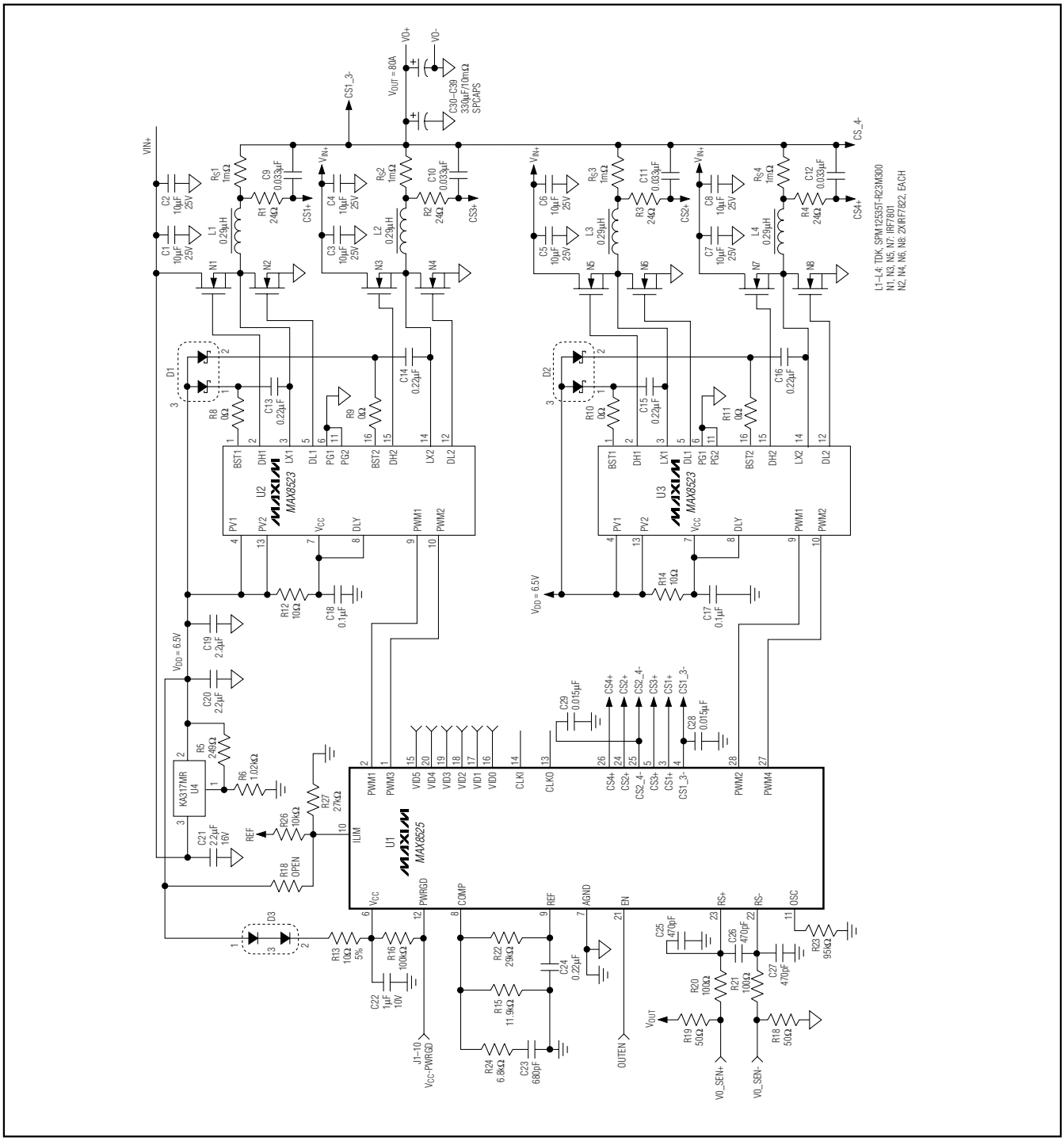
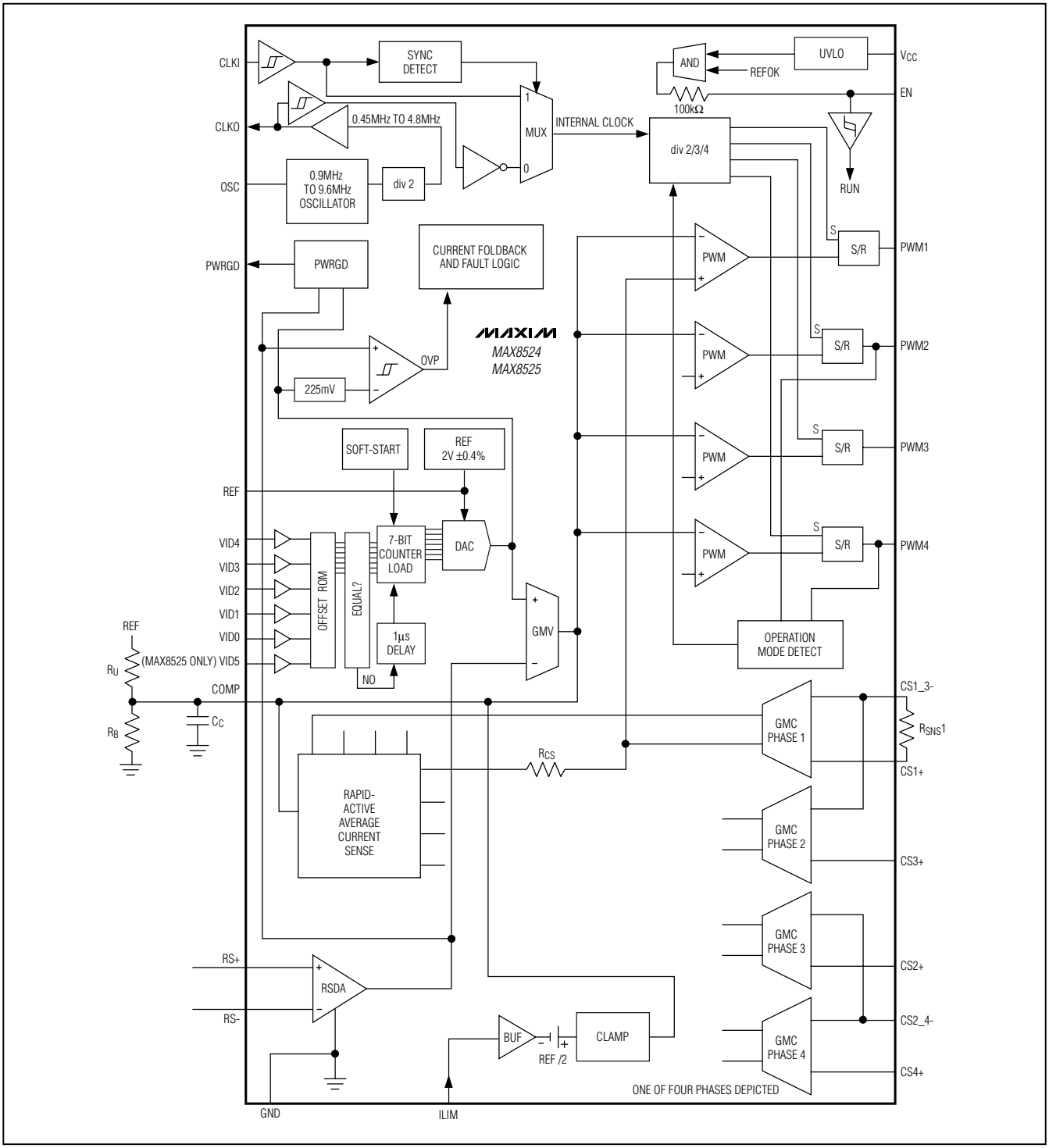


Figure 8. 600kHz Application Circuit with Direct MOSFETs for Compact VRM 10 Design

2- to 8-Phase VRM 10/9.1 PWM Controllers with Precise Current Sharing and Fast Voltage Positioning

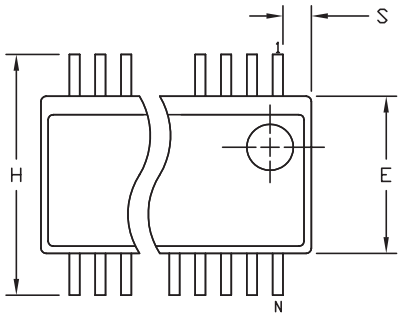
Functional Diagram



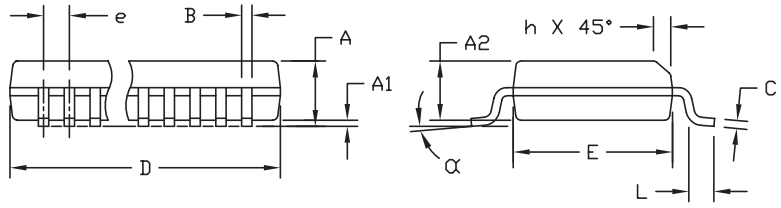
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QSOP.EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.30
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
α	0°	8°	0°	8°



VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AB
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	AD
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AE
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AF
S	.0250	.0300	0.635	0.762		

NOTES:
1). D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2). MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3). CONTROLLING DIMENSIONS: INCHES.
4). MEETS JEDEC MO137.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, QSOP .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0055	E	1/1