AKM

AK2351F

Integrated Base Band LSI for Cordless Telephone Sets

Features

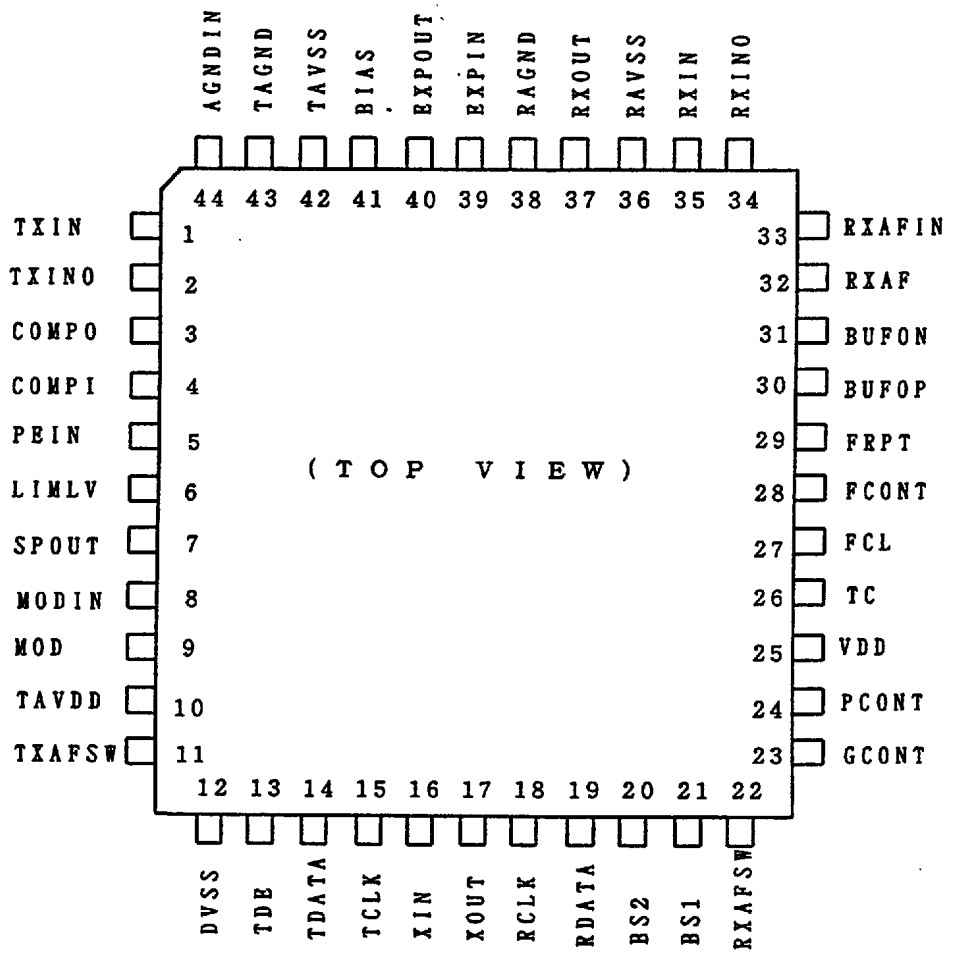
- ☐ Integrated voice band filters with MSK MODEM(2400bps) and COMPANDOR for cordless telephone sets
- ☐ Low voltage operation (1.9V～5.5V)
- ☐ Fully integrated COMPANDOR, only two external capacitors are required
- ☐ Buffer amplifier for direct drive of a ceramic receiver
- ☐ Switchable expander reception level (0/+6dB)
- ☐ Transmission and reception voice mute
- ☐ Adjustable limiter level
- ☐ Gain setting amplifiers for receiver and transmitter sections
- ☐ Power down mode
- ☐ 3.58MHz oscillator
- ☐ Pre-emphasis/De-emphasis bypass mode
- ☐ Compandor bypass mode
- ☐ Scrambler chip interface
- ☐ Two cutoff frequencies are selectable for splatter filter
- ☐ Low power CMOS
- ☐ Integrated frame detection function in MSK demodulator
- ☐ Minimal external components
- ☐ Packaged : 44 PIN QFP, 64 PIN SQFP

General Description

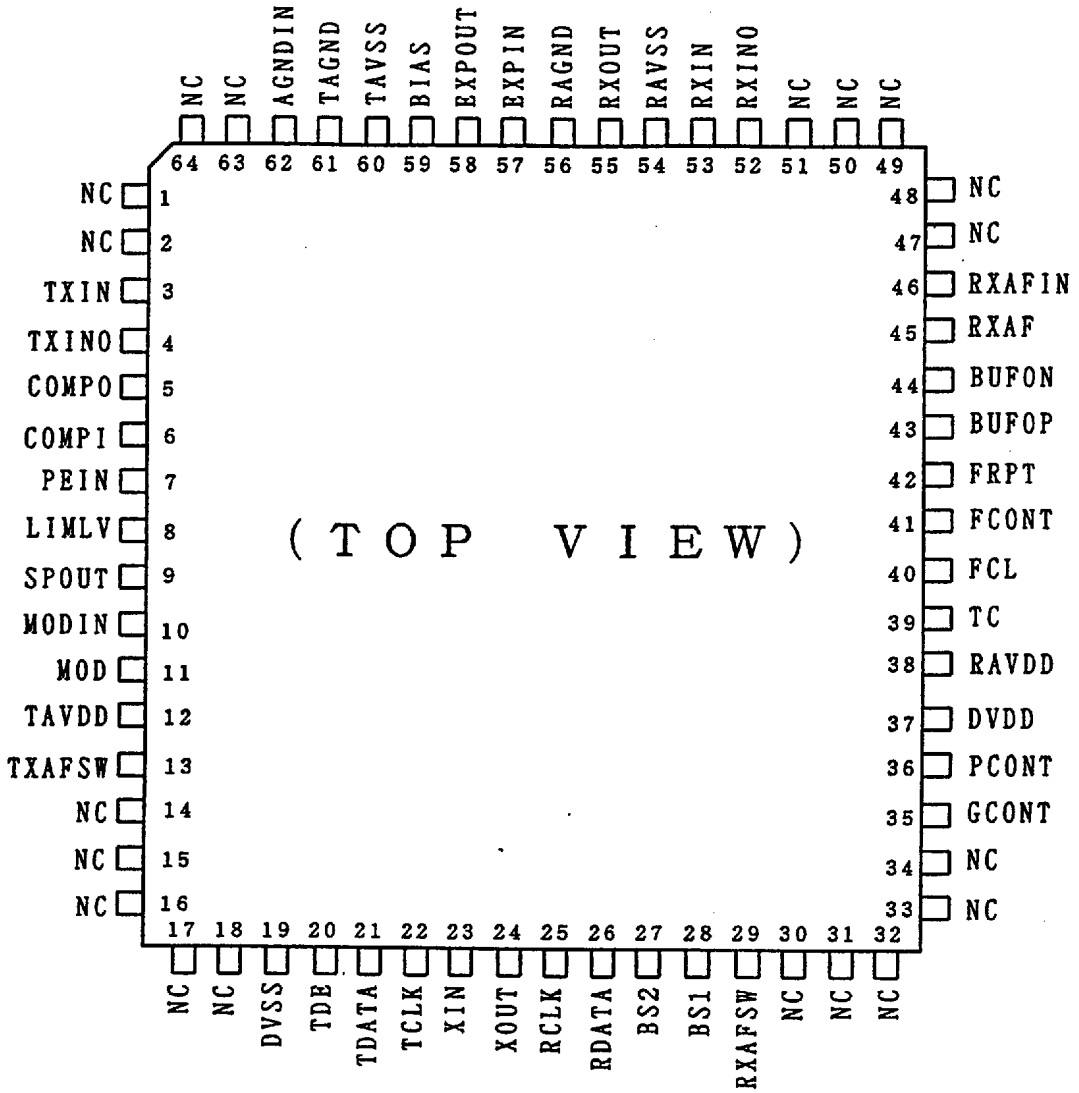
AK2351F is an integrated base band LSI for cordless telephone sets. Not only voice band filters but also a 2400bps MSK MODEM (for data communication) and a COMPANDOR (for noise reduction) are integrated into monolithic CMOS LSI.
The COMPANDOR circuit is fully integrated. Therefore, only an external capacitor is required for each compressor and expander. The fully integrated COMPANDOR is also free from aging problem.
The 2400bps MSK MODEM can assure reliable high speed data communication. A 3.58MHz oscillator circuit is integrated, which may also be used for DTMF tone generator clock. No special clock is required for the MSK MODEM.
Scrambler chip interface and pre-emphasis/de-emphasis circuits bypass mode are available for easy interface with external scrambler device.
Cut-off frequency of splatter filter can be selected from 3kHz and 3.4kHz.
High-pass filter, compressor, pre-emphasis, limiter, MSK modulator, splatter filter, etc. are integrated for transmitter.
Band-pass filter, de-emphasis, expander, buffer, MSK demodulator, etc. for voice/data, and band-pass filter, rectifier, etc. for the squelch are integrated for receiver.

Pin Assignments

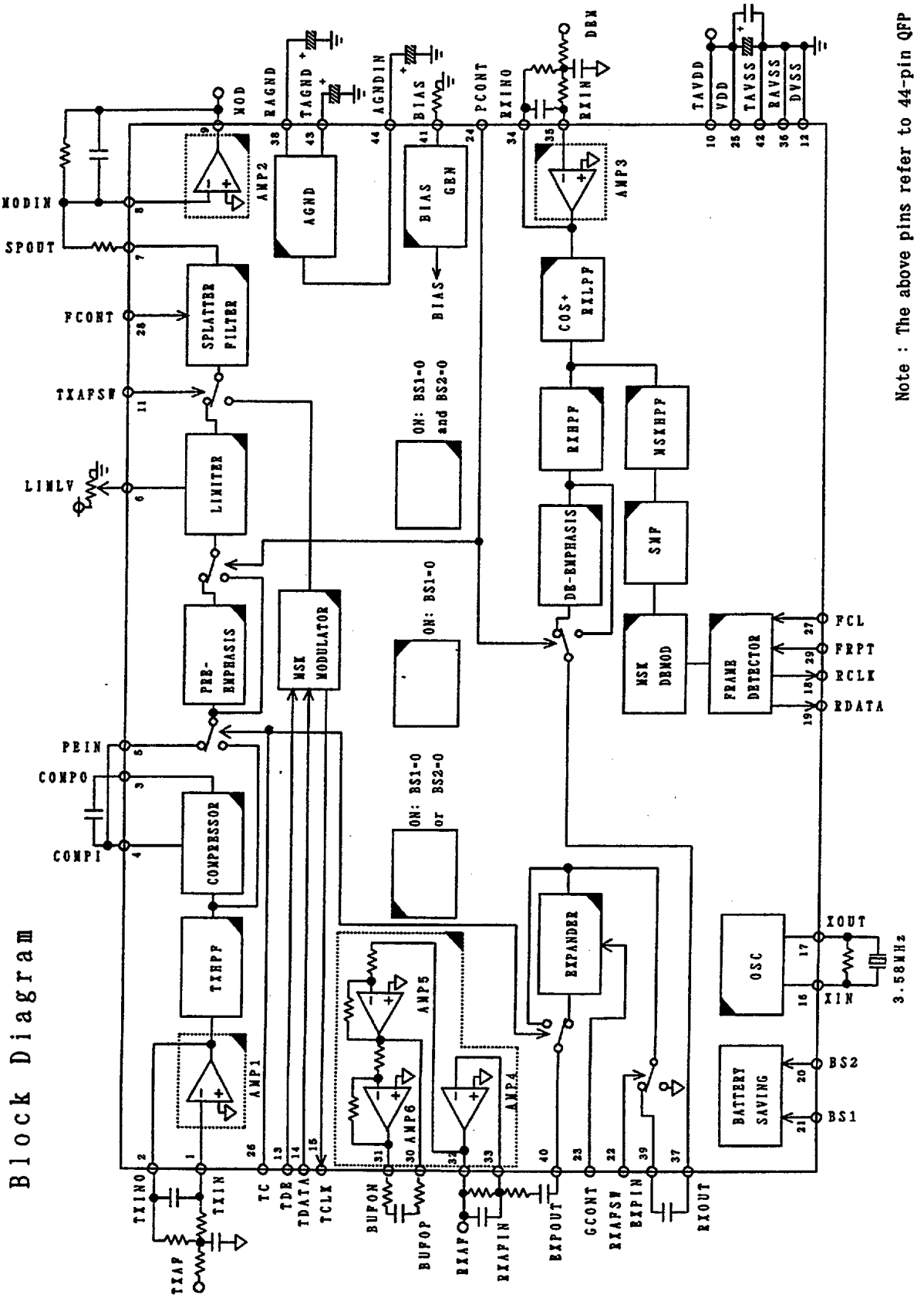
☐ 44 pin QFP



☐ 64 pin SQFP


NC 64
NC 63
AGNDIN 62
TAGND 61
TAVSS 60
BIAS 59
EXPOUT 58
EXPIN 57
RAGND 56
RXOUT 55
RAVSS 54
RXIN 53
RXINO 52
NC 51
NC 50
NC 49
NC 1
NC 2
TXIN 3
TXINO 4
COMPO 5
COMPI 6
PEIN 7
LIMLV 8
SPOUT 9
MODIN 10
MOD 11
TAVDD 12
TXAFSW 13
NC 14
NC 15
NC 16
48 NC
47 NC
46 RXAFIN
45 RXAF
44 BUFON
43 BUFOP
42 FRPT
41 FCONT
40 FCL
39 TC
38 RAVDD
37 DVDD
36 PCONT
35 GCONT
34 NC
33 NC
(T O P V I E W)
17 NC
18 NC
19 DVSS
20 TDE
21 TDATA
22 TCLK
23 XIN
24 XOUT
25 RCLK
26 RDATA
27 BS2
28 BS1
29 RXAFSW
30 NC
31 NC
32 NC

Block Diagram



Note : The above pins refer to 44-pin QFP

Block Diagram

Functional Block	Functions
AMP1	An Op-Amp for transmit voice signal gain adjustment and anti-aliasing filtering for the succeeding switched capacitor filters (SCF). Adjust the gain to 30dB or less and the cut-off frequency to around 10kHz by properly selecting external capacitor and resistor values.
TxHPF	SCF high pass filter to eliminate 300Hz or lower components contained in the transmit voice signal.
Compress-or	Compress the amplitude of the transmit voice signal.
Emphasis	Emphasize the high frequency components in the transmit voice signal in order to improve the signal-to-noise performance of the modulated signal.
Limiter	Amplitude limiting circuit to limit the maximum frequency deviation of the modulated signal. Limiter level is adjustable by varying DC level applying to "LIMLV" pin. The limiter level is set to a pre-fixed level if "LIMLV" pin is left open.
Splatter Filter	SC filter to reject 3.4kHz or higher components contained in the limiter output signal or MSK Modulator signal.
AMP2	An Op-Amp to form a smoothing filter for the transmit SCF output. Adjust the gain to 0dB and the cut-off frequency to around 10kHz by properly selecting external capacitor and resistor values.
MSK Modulator	Generate 2400bps MSK signal in accordance with digital input signal applied on TDATA pin. "H" : 1.2kHz "L" : 2.4kHz
AMP3	An Op-Amp for received signal gain adjustment and anti-aliasing filtering for the succeeding SC filters. Adjust the gain to 10～20dB or less and the cut-off frequency to around 40kHz by properly selecting external capacitor and resistor values.
COS + RxLPF	SC filter to reject 3.4kHz or higher components contained in the received signal.
RxHPF	SC filter to reject 300Hz or lower components contained in the receive voice signal.
De-Emphasis	Equalize the pre-emphasized voice signal to original.
Expander	Expand the signal amplitude, which was compressed by the compressor to original. GCONT pin sets the expander gain 0dB or 6dB.

Functional Block	Function
AMP4	Op Amp to form a smoothing filter for the receiver SCF output. Adjust the gain to 0dB and set the cut-off frequency to around 20KHz by properly selecting external capacitor and resistor values.
MSK HPF	SC filter to reject 100Hz or lower components contained in the received MSK signal.
SMF	Active filter to smooth out the output signal from the MSK HPF.
MSK Demodulator	To recover 2400 bps receive data and clock from the MSK signal fed on RXIN pin. 1.2KHz : "H" 2.4KHz : "L"
AMP5 AMP6	Inverting, non-inverting buffers to directly drive a ceramic receiver.
BIAS GEN	Bias generator circuit for internal Op Amps.
AGND	Ground Reference voltage generator circuit for internal analog signal processing.
OSC Circuit	A 3.58MHz reference clock generator with an external quartz Crystal resonator and a resistor.
Battery Saving	Battery save mode selection circuit. 1 of 4 modes is selectable by BS1 & BS2 pins.
Frame detection Circuit	Frame detection circuits to detect pattern from received MSK signal. FRPT="H" : 1001001100110110 (Handset) FRPT="L" : 1100010011010110 (Base station)

Pin#	Name	I/O	Function
- (1)	NC	-	No connection.
- (2)	NC	-	No connection.
1 (3)	TXIN	I	Transmit voice signal input pin (inverted input pin of AMP1). With external capacitors and resistors, a microphone AMP is formed.
2 (4)	TXINO	O	Output pin of AMP1.
3 (5)	COMPO	O	Compressor output pin. Can drive 50kΩ load or more.
4 (6)	COMPI	I	Compressor rectifier input pin. Connect to COMPO through an external capacitor. Input impedance of the pin is 150kΩ or more.
5 (7)	PEIN	I	Pre-emphasis input pin. The output from the scrambler chip is connected to this pin. Connect to COMPI if the scrambler is not used.
6 (8)	LIMLV	I	Limiter level adjust pin. Limiter level is adjustable by varying DC level applying to this pin. The limiter level is set to pre-fixed level if this pin is left open.
7 (9)	SPOUT	O	Splatter filter output pin.
8 (10)	MODIN		Transmit signal input pin to be modulated (inverted input pin of AMP2). Form the smoothing filter by external capacitor and resistors.
9 (11)	MOD	O	Transmit signal output pin to be modulated. Can drive 10kΩ load or more.
10 (12)	TAVDD	-	Positive power supply pin for transmit section.
11 (13)	TXAFSW	I	Transmit signal select pin. (with built-in pull-up) "H" : MSK signal "L" : Voice signal
- (14)	NC	-	No connection.
- (15)	NC	-	No connection.
- (16)	NC	-	No connection.
- (17)	NC	-	No connection.
- (18)	NC	-	No connection.
12 (19)	DVSS	-	Negative power supply pin for digital circuit.
13 (20)	TDE	I	Transmit MSK signal control pin. (with built-in pull-up) "H" : MSK MUTE "L" : MSK ON
14 (21)	TDATA	I	Transmit MSK data input pin. (with built-in pull-up) Data is sampled at the rising edge of TCLK clock.

Pin#	Name	I/O	Function
15 (22)	TCLK	O	Clock output pin for transmit MSK data. (open-drain output) 2.4kHz clock is output when TDE pin is "LOW". It goes to "HIGH" when TDE is "HIGH".
16 (23) 17 (24)	XIN XOUT	I O	Quartz Crystal resonator pins. By connecting a 3.58MHz resonator and 1MΩ resistor between these pins, a reference clock is generated internally. For external clock operation, connect XIN pin to DVSS and external clock source to XOUT pin.
18 (25)	RCLK	O	Recovered clock output pin. (open-drain output) A 2.4kHz clock is output which is recovered from the received MSK signal.
19 (26)	RDATA	O	Receive MSK MODEM data output pin. (open-drain output) Data is output at the falling edge of RCLK clock.
20 (27) 21 (28)	BS2 BS1	I I	Battery save control pins. (with built-in pull-up) BS1 BS2 "H" "H" : Mode 0 (Refer to Block Diagram) "H" "L" : Mode 1 "L" "H" : Mode 2 "L" "L" : Mode 3
22 (29)	RXAFSW	I	Received voice signal control pin. (with built-in pull-up) "H" : Received voice "MUTE" "L" : Received voice "ON"
- (30)	NC	-	No connection.
- (31)	NC	-	No connection.
- (32)	NC	-	No connection.
- (33)	NC	-	No connection.
- (34)	NC	-	No connection.
23 (35)	GCONT	I	Expander gain control pin. (with built-in pull-up) "H" : 0dB "L" : 6dB
24 (36)	PCONT	I	Emphasis/de-emphasis circuits bypass control pin. (with built-in pull-up) "H" : Normal mode "L" : Bypass mode
25 (-)	VDD	-	Positive power supply pin for digital and analog receiver section.
- (37)	DVDD	-	Positive power supply pin for digital section.
- (38)	RAVDD	-	Positive analog power supply for receiver section.
26 (39)	TC	I	Compressor bypass control pin.(with built-in pull-up) "H" : Normal mode "L" : Bypass mode

Pin#	Name	I/O	Function
27 (40)	FCL	I	Frame detection function control pin. (with built-in pull-up) "H" : do not use frame detection function "L" : use frame detection function In case of not using frame detection function, RCLK, RDATA always are output. In case of using frame detection function, RCLK, RDATA become "H" level. After detecting synchronization frame, RCLK, RDATA with be output.
28 (41)	FCONT	I	Filter cutoff control pin. (with built-in pull-up) To select cutoff frequency of splatter filter. "H" : 3.4kHz (Compatible with AK2351E) "L" : 3kHz (Compatible with AK2351)
29 (42)	FRPT	I	Frame pattern selection pin. (with built-in pull-up) To select frame pattern of frame detection circuit. "H" : 1001001100110110 (Handset) "L" : 1100010011010110 (Base station)
30 (43) 31 (44)	BUFOP BUFON	O O	Buffer amp for ceramic receiver output pins. Connect a ceramic receiver to these pins.
32 (45)	RXAF	O	Received voice signal output pin. Can drive 10kΩ load or more.
33 (46)	RXAFIN	I	Received voice signal input pin (inverted input of AMP4). A smoothing filter is formed with external capacitors and resistors.
- (47)	NC	-	No connecting.
- (48)	NC	-	No connecting.
- (49)	NC	-	No connecting.
- (50)	NC	-	No connecting.
- (51)	NC	-	No connecting.
34 (52)	RXINO	O	AMP3 output pin.
35 (53)	RXIN	I	Received de-modulated signal input pin (inverted input of AMP3). A pre-filter is formed with external capacitors and resistors.
36 (54)	RAVSS	-	Negative analog power supply for receiver section.
37 (55)	RXOUT	O	Received voice filter output pin. Can drive 50kΩ load or more.
38 (56)	RAGND	O	Analog ground pin for receiver section. To stabilize the analog ground, connect to the ground through an external capacitor.
39 (57)	EXPIN	I	Expander input pin. Input impedance of the pin is 150kΩ or more.
40 (58)	EXPOUT	O	Expander output pin.

Pin#	Name	I/O	Function
41 (59)	BIAS	I	Bias resistor pin. A 47kΩ resistor is connect between VSS and this pin.
42 (60)	TAVSS	-	Negative analog power supply pin for transmitter section.
43 (61)	TAGND	O	Analog ground pin for transmitter section. To stabilize the analog ground, connect to the ground through an external capacitor.
44 (62)	AGNDIN	I	Analog ground input pin. To stabilize the analog ground, connect to the ground through an external capacitor.
- (63)	NC	-	No connecting.
- (64)	NC	-	No connecting.

() indicate the pin# for 64 pin SQFP.

Absolute Maximum Ratings

TAVSS, RAVSS, DVSS=0V ; (Note①)

Parameter	Symbol	Min	Max	Units
Power Supply Voltages (VDD,TAVDD,RAVDD,DVDD)	VA+	-0.3	7	V
Input Current (Excluding power supply pins)	I_{IN}	-	±10	mA
Analog Input Voltage	V_{INA}	-0.3	(VA+)+0.3	V
Digital Input Voltage	V_{IND}	-0.3	(VA+)+0.3	V
	V_{INDO} (Note②)	-0.3	7	V
Storage Temperature	Tstg	-55	130	℃

Notes ① : All voltages are referenced to VSS pin
② : TCLK, RCLK, RDATA

Note : Exceeding absolute maximum ratings may cause permanent damage.
Normal operation is not guaranteed at these extremes.

Recommended Operating Conditions

TAVSS, RAVSS, DVSS=0V ; (Note①)

Parameter		Symbol	min	typ	max	Units
Ambient Operating Temp.		Ta	-10		70	℃
Power Supply Voltage : R_{BIAS}=47KΩ (VDD,TAVDD,RAVDD,DVDD)		VDD	1.9	2.2	5.5	V
Analog Ground Reference Voltage		AGND		1/2VDD		V
Power Supply Current	Mode0	Idd0		0.1	0.25	mA
	Mode1	Idd1		0.8	1.5	
	Mode2	Idd2		1.4	2.5	
	Mode3	Idd		6.2	10	

Note① : All voltages are referenced to VSS pin.

Analog Characteristics

f=1kHz TC="H" PCONT="H" GCONT="H" FCONT="H" 0dBm=0.775Vrms
0dBx=-5dBm @ 2V (note⑧)

1) TX Section

Parameter	min	typ	max	Units
Reference Input Signal Level @TXINO		-10		dBx
Absolute Gain TXINO→MOD 1kHz (Note①)	-1.5	0	1.5	dB
Limiter Level TXINO→MOD 1kHz (Note①)				
without External R	-9	-8	-7	dBx
Adjustable Range with R			-7	
Compressor linearity TXINO→MOD (Note①,②)				
TXINO=-44dBx	-20		-14	dB
TXINO=-50dBx	-24		-16	
Noise Level TXIN→MOD (Note①,③)			-40	dBm
Compressor distortion TXINO→COMPO				
TXINO=0dBx			-35	dB
MSK Output Signal Level TDATA→MOD (Note①)	-9	-8	-7	dBx
1.2kHz Output				
MSK Signal Distortion TDATA→MOD (Note①)			-28	dB
1.2kHz Output				

2) RX Section

Parameter	min	typ	max	Units
Reference Input Signal Level @RXINO		-10		dBx
Absolute Gain RXINO→BUFON,BUFOP (Note①)	-1.5	0	1.5	dB
Receive Gain RXINO→BUFON,BUFOP (Note④)				
GCONT="L"	6		7	dB
Expandor linearity RXINO→BUFON,BUFOP				
RXINO=-25dBx (Note①,⑤)	-33		-27	dB
RXINO=-30dBx	-44		-35	
Noise Level RXINO→BUFON,BUFOP (Note①,③)			-70	dBm
Expandor distortion RXINO→RXAF				
RXINO=-5dBx			-35	dB
MSK Input Signal Level RXINO→RDATA	-14	-8	-2	dBx
1.2kHz Input				

3) General Characteristics

Parameter	min	typ	max	Units
Absolute gain TXINO→BUFON,BUFOP				
TXINO=-10dBx (Note⑥)	-0.5		+2.5	dB
Distortion TXINO→BUFON,BUFOP				
TXINO=-10dBx (Note⑥)		-50	-45	dB
Crosstalk @BUFON,BUFOP (Note①,⑦)				
Transmit→Receive TXINO=0dBx			-60	dBm
Crosstalk @MOD (Note①,⑦)				
Receive→Transmit RXINO=0dBx			-60	dBm

4) Filter Characteristics

Parameter		min	typ	max	Units
Transmitter Over-All Responsel (Fig.1)	100Hz			-40	
TXINO→MOD	300Hz	-12	-10.5	-9	
TC="L" PCONT="H"	3kHz	8	9.5	11	dB
FCONT="H"	3.4kHz	8	9.5	11	
Referenced to 0dB at 1kHz	6kHz			-12	
Transmitter Over-All Response2 (Fig.2)	100Hz			-40	
TXINO→MOD	300Hz	-12	-10.5	-9	
TC="L" PCONT="H"	2.5kHz	6.5	8	9.5	dB
FCONT="L"	3kHz	6.5	8	9.5	
Referenced to 0dB at 1kHz	5kHz			-7	
Receiver Over-All Response (Fig.3)	100Hz			-4	
RXINO→LPF3OUT	250Hz		12	13.5	
PCONT="H"	300Hz	9	10.5		dB
Referenced to 0dB at 1kHz	3.4kHz	-12	-10.5	-9	
	5kHz			-15	

Note① : Including external parts, see "Application Circuit Examples".
Note② : 0dB is the Reference level at MOD.
Note③ : C-Message weighted.
Note④ : Difference between the gain with GCONT="H" and GCONT="L".
Note⑤ : 0dB is the Reference level at BUFON and BUFOP.
Note⑥ : Including external parts, see "Application Circuit Examples".
AMP3 gain is 0dB and MOD pin connected to DEM.
Note⑦ : TC="L" PCONT="H" GCONT="H" FCONT="H"
Note⑧ : Definition of "dBx"

$$0dBx = -5 + 20\log(X/2)\ [dBm]$$

where, X: Power Supply Voltage [V]
Example: 0dBx = -5dBm @2V

☐ Filter Characteristics

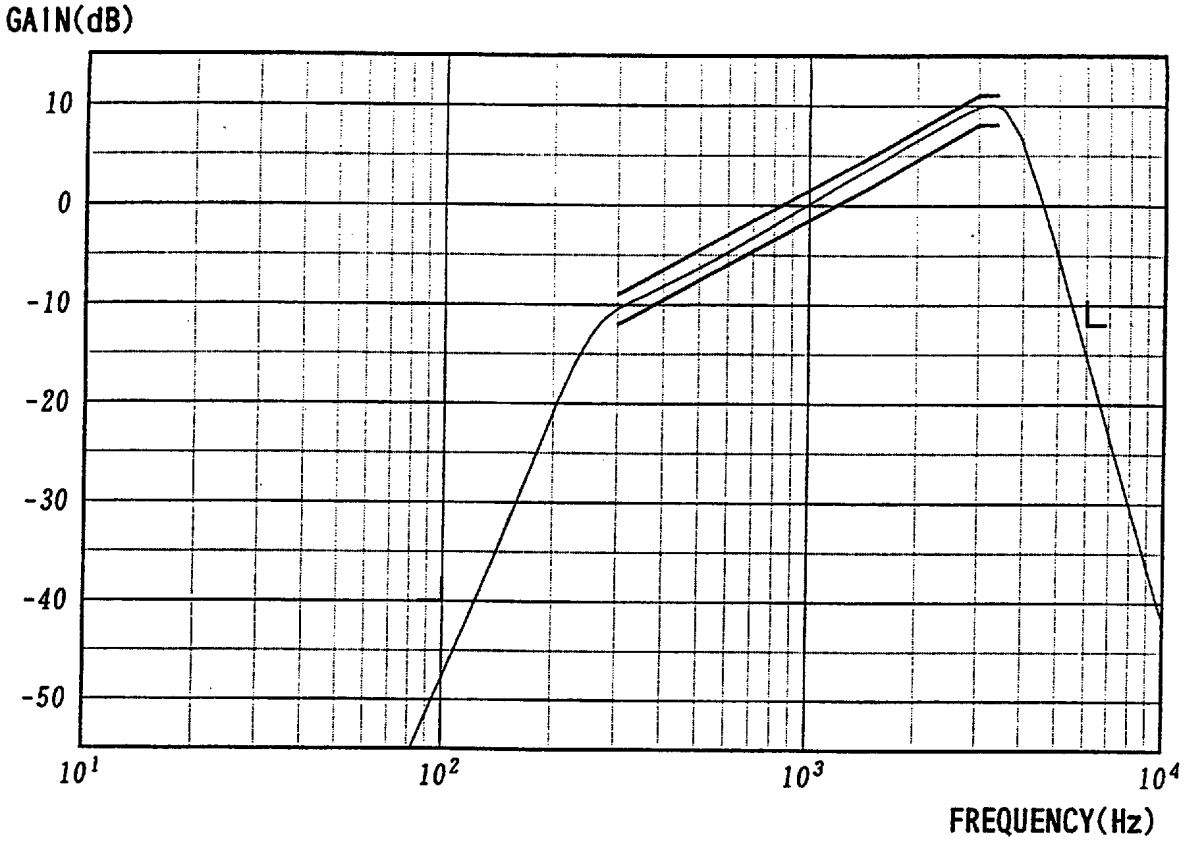


Fig.1 Total Frequency Response of Transmitter Section (FCONT="H")

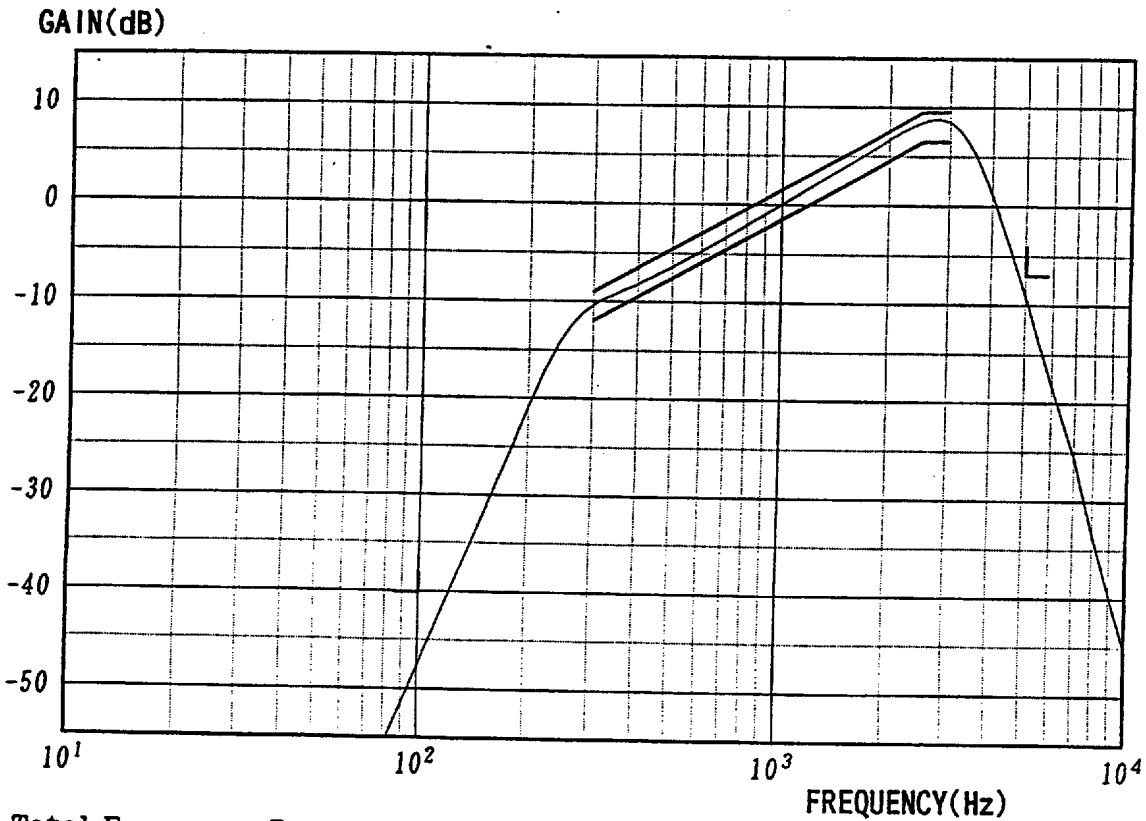


Fig.2 Total Frequency Response of Transmitter Section (FCONT="L")

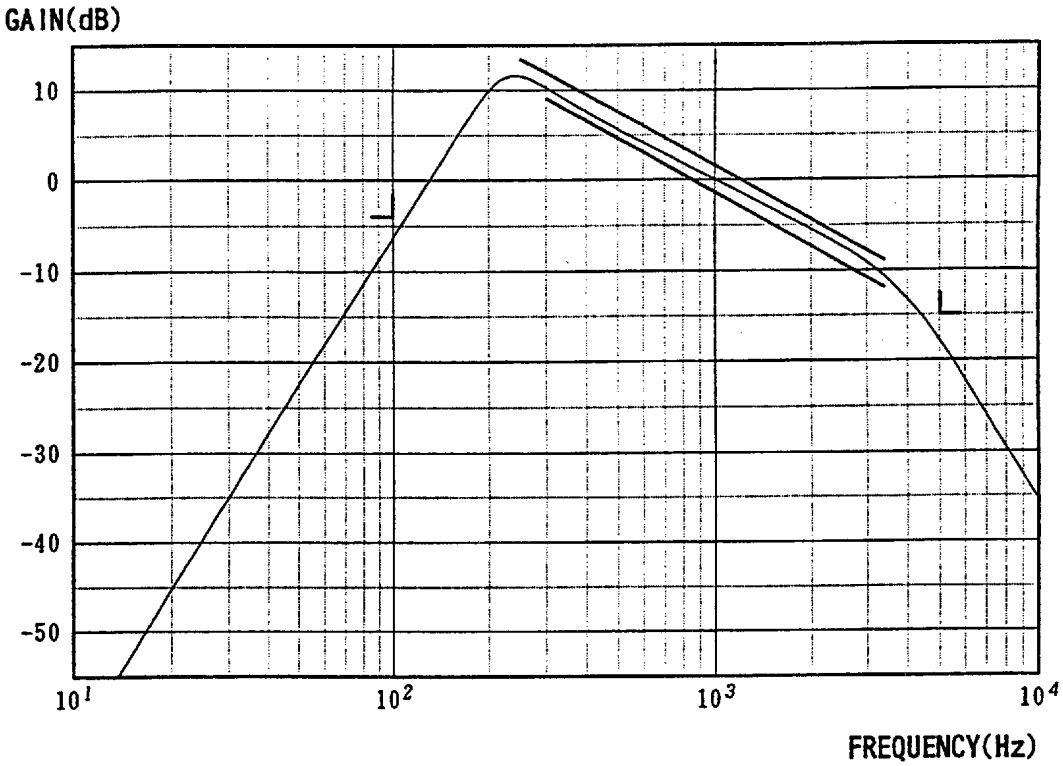
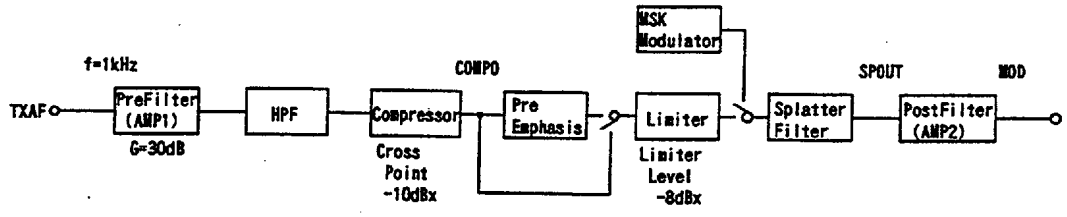
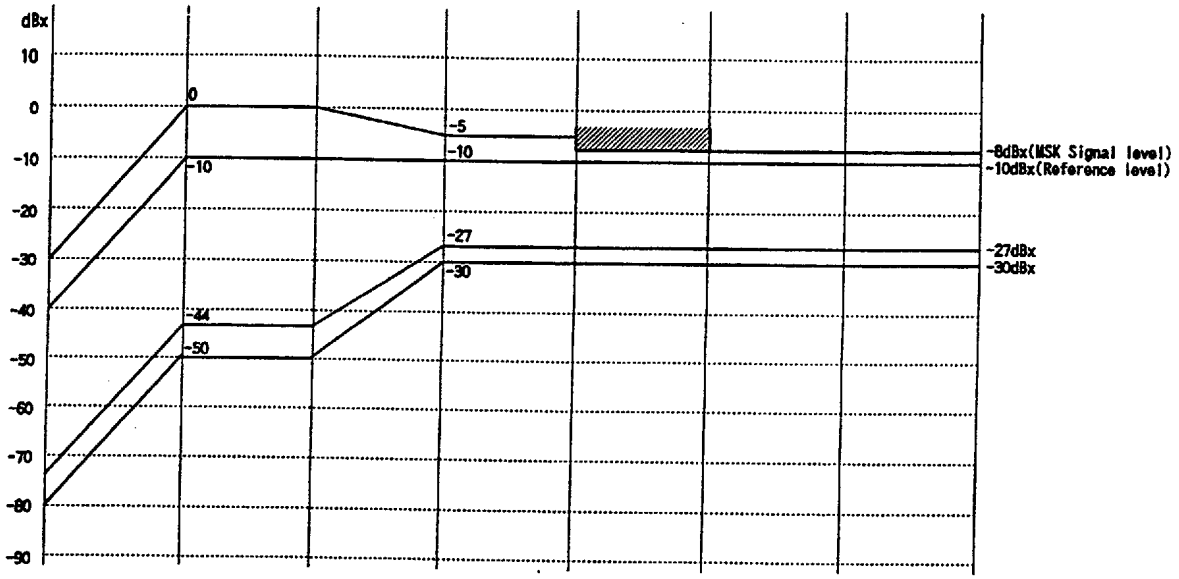


Fig.3 Total Frequency Response of Receiver Section

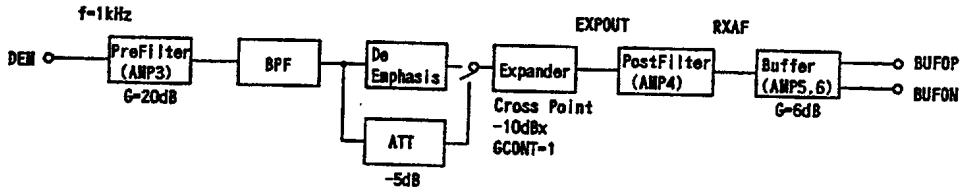
Level Diagram

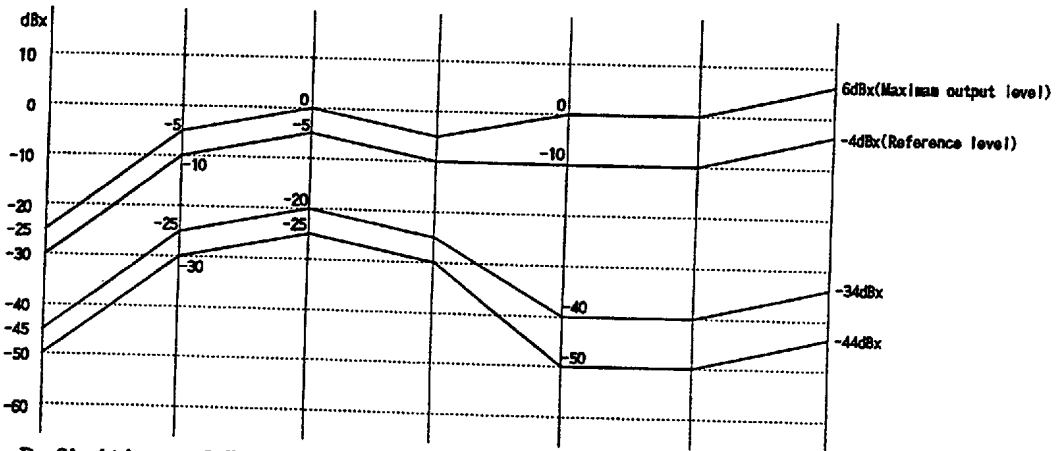
1) TX Section





2) RX Section





Note : Definition of "dBx"

0dBx = -5 + 20log(X/2) [dBm]

where, X: Power Supply Voltage [V]

Example: 0dBx = -5dBm @2V

Digital Characteristics

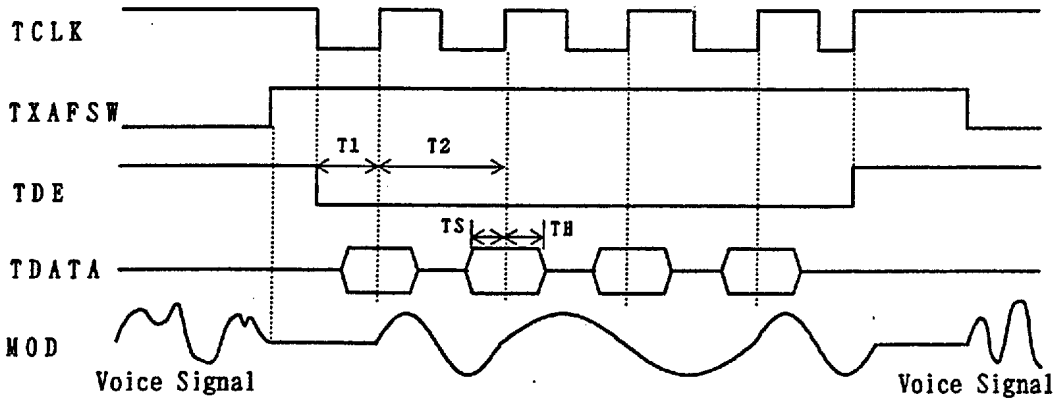
1. DC Characteristics

Parameter	Pin	Symbol	min	typ	max	Units
High Level Input Voltage	(1)	V_{IH}	70%VDD			V
Low Level Input Voltage	(1)	V_{IL}			30%VDD	V
High Level Input Current V_{IH}=VDD	(1)	I_{IH}			10	μA
Low Level Input Current V_{IL}=0V	(1)	I_{IL}	-150			μA
Low Level Output Voltage I_{OL}=0.6mA	(2)	V_{OL}			0.3	V
On-Chip pull-up Resistor	(1)	R_{UP}	50		200	kΩ

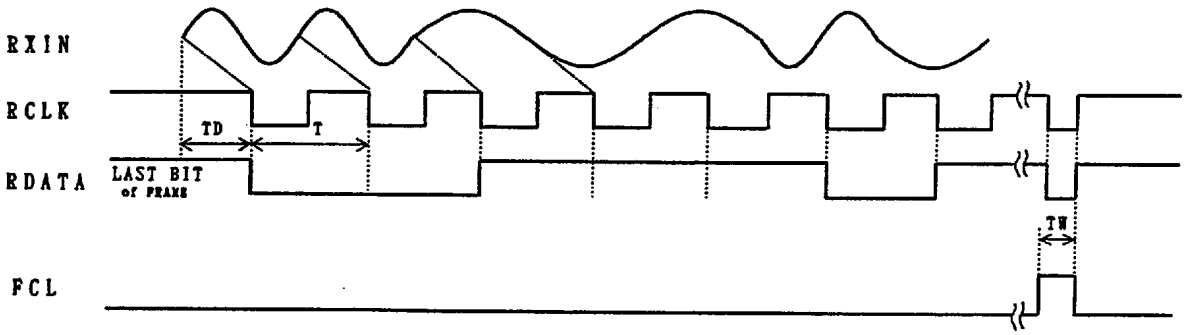
(1) TDE, TDATA, BS1, BS2, TXAFSW, RXAFSW, TC, GCONT, PCONT, FCL, FCONT, FRPT
(2) TCLK, RDATA, RCLK

2. Switching Characteristics

Parameter	Symbol	min	typ	max	Units
Master Clock Frequency	fclk		3.579545		MHz
MSK Modulator Timing					
TDE Falling to TCLK Rising	T1		208.3		μs
TCLK Period	T2		416.7		μs
TDATA Set Up Time	TS	0			μs
TDATA Hold Time	TH	0			μs
MSK Demodulator Timing					
RCLK Period	T	402.2	416.7		μs
Analog Input to RDATA Edge	TD	400		900	μs
FCL pulse width	TW	1			μs



MSK Modulater



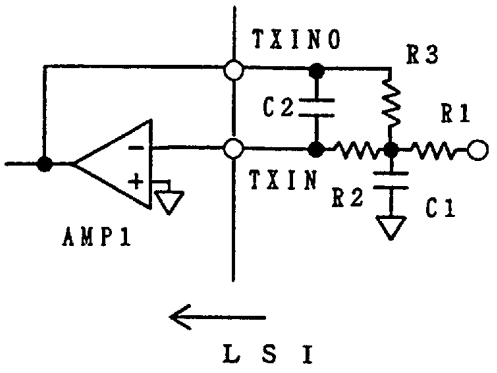
·RDATA and RCLK remain "H" until the synchronous frame is detected.
·RDATA and RCLK output normal data after the synchronous frame is detected.
·When FCL receives high pulse, RDATA and RCLK go "H" and wait for next synchronous frame.

MSK demodulator

External circuit examples

① AMP1

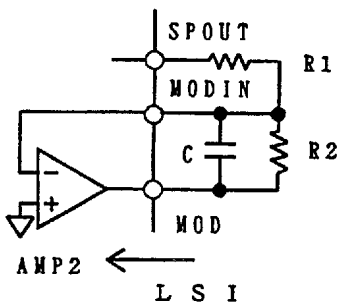
- AMP1 may be used as a transmit microphone amplifier.
- Set the gain to 30dB or less.
- If 50kHz or higher frequency noise is expected on input signal, an anti-aliasing filter must be configured.
- A circuit configuration example below shows a 2nd order low pass filter with the cut-off frequency at 10kHz. The filter also has 30dB gain.



C1=2200pF
C2=33pF
R1=R2=10k Ω
R3=330k Ω

② AMP2

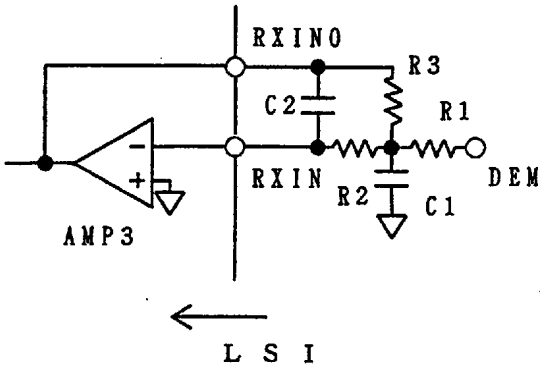
- AMP2 may be used as a smoothing filter and gain adjustment of the transmit signal.
- Smoothing filter is used to eliminate a 112kHz clock component contained in the splatter filter output.
- Another transmit signal may also be added using this OP-amp.
- The circuit example below shows a 1st order low pass filter with 13kHz cut-off frequency and 0dB gain.



C=220pF
R1=R2=56k Ω

③ AMP3

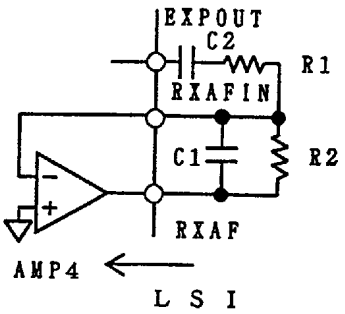
- AMP3 may be used as gain adjustment of receive signal and an anti-aliasing filter to eliminate 100kHz or higher noise.
- Set the gain to be 30dB or less.
- Following circuit shows a 2nd order low pass filter with 40kHz cut-off frequency and 20dB gain.



C1=560pF
C2=27pF
R1=10k Ω
R2=9.1k Ω
R3=100k Ω

④ AMP4

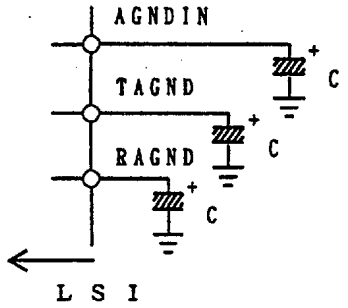
- AMP4 may configure a smoothing filter and a gain adjustment circuit for the receive signal.
- The smoothing filter is used to reject 448kHz clock component contained in the expander output (EXPOUT).
- Following circuit example shows a 1st order low pass filter with 19kHz cut-off frequency and 0dB gain.



C1=150pF
C2=0.1 μF
R1=R2=56k

⑤ AGND stabilization capacitor

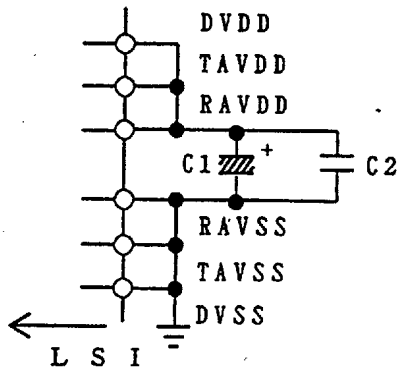
- 0.3 μF or larger capacitors should be connected between TAGND pin and AVSS, RAGND pin and AVSS respectively in order to stabilize analog ground.
- In order to minimize effect of ripple on power-supply, an appropriate capacitor is also recommended to place between AGNDIN pin and AVSS.
- Connection Example is shown below.



C=1 μF

⑥ Power supply stabilization capacitor

- To minimize the effect of power supply noise, a couple of capacitors should be placed between DVDD, TAVDD, RAVDD pins and DVSS, TAVSS, RAVSS pins.

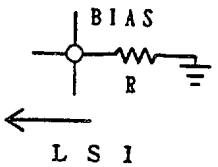


C1=22 μF(Electrolytic Cap.)

C2=0.1 μF(Seramic Cap.)

⑦ Bias-current setting resistor

- Bias-current of Op Amp is set by connecting a 47kΩ resistor between Bias pin and VSS.



R=47k Ω

⑧ Crystal Oscillator

- Crystal resonator and a resistor should be connected as shown Fig.3 for on-chip oscillator operation.
- For external clock operation, if the high(H) level of the input clock signal amplitude equals to or is greater than 1.5V, and the low(L) level equals to or is smaller than 0.5V, then connection should be made as shown in Fig.4.
  If the input clock signal amplitude (peak-to-peak) equals to or is smaller than 1V, and equals to or is greater than 200mV, then AC coupling should be as illustrated in Fig.5.

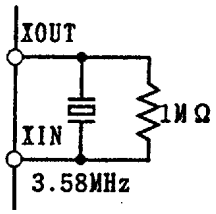


Fig.3

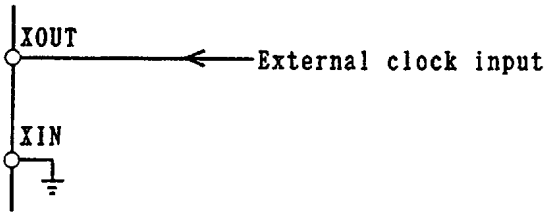


Fig.4

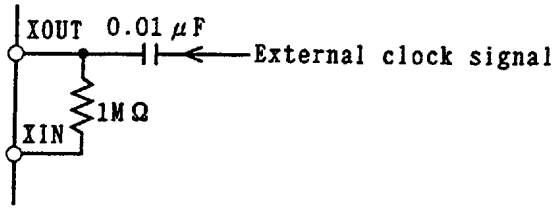
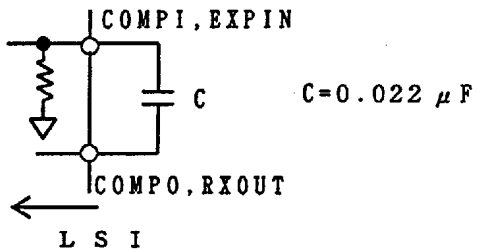


Fig.5

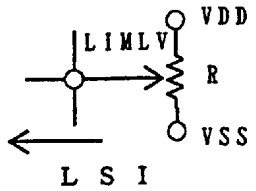
⑨ AC Coupling Capacitors

-In order to cut the DC off-set voltages generated in each function block, AC coupling capacitors are recommended for inter-block connections.
-COMPI pin and PEIN pin should be connected directly when a scrambler chip is not used.



⑩ Limiter Level Adjusting Resistor

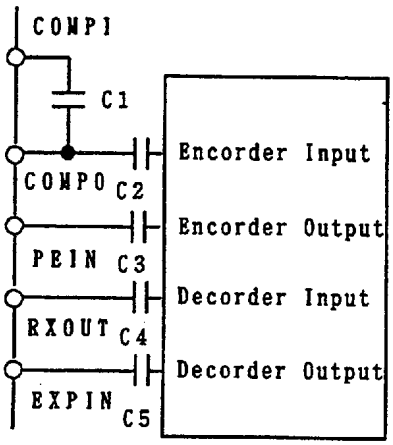
- Limiter level is adjustable by varying the DC level on LIMLV pin. The DC level applied on this pin must be above TAGND voltage.
- The limit level is as follows :
  TAGND ± aV (a= | LIMLV-TAGND |)
- If this pin is left open, a pre-determined level is set.



R=50k Ω

B. Scrambler Chip Connection

When external scrambler is connected, please refer to the schematic below. When the frequency inverter is used, bypassing the pre-emphasis and de-emphasis circuits is recommended in order to keep dynamic range.



Scrambler IC

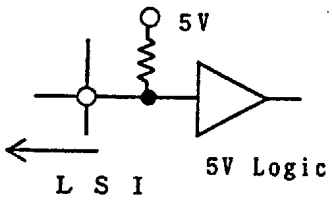
C1, C3, C5=0.022 μF

C. Logic Interface

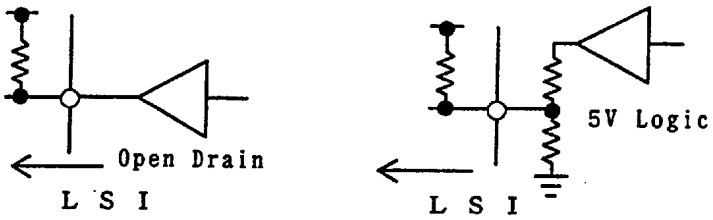
① Digital Pins of AK2351F

-Output pins : Open-Drain type
-Input pins : All pins have on-chip pull-up resistors.

② Following logic interface is recommended when AK2351F operates at 3V power supply and it interfaces with +5V logic circuit.



Output Pin



Input Pin

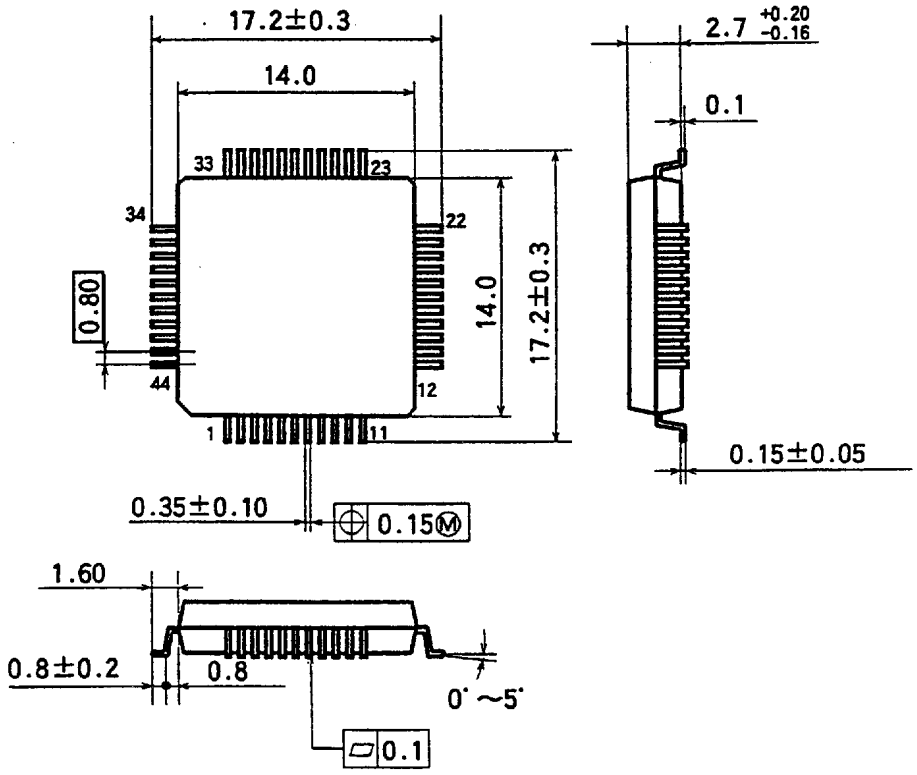
Package

☐ 44 pin QFP

■ Marking

(1) Date Code: xxxxxxx (7 digits)
(2) Marketing Code: AK2351F
(3) Country of Origin: JAPAN
(4) Asahi Kasei Logo

■ Outline Dimensions



☐ 64 pin SQFP

■ Marking

(1) Pin # 1 indication
(2) Date Code : 5 Digits
(3) Marketing Code : AK2351FV
(4) Country of Origin
(5) Asahi Kasei Logo

■ Outline Dimensions