PRODUCT SPECIFICATION

Z84011/C11

PARALLEL I/O CONTROLLER

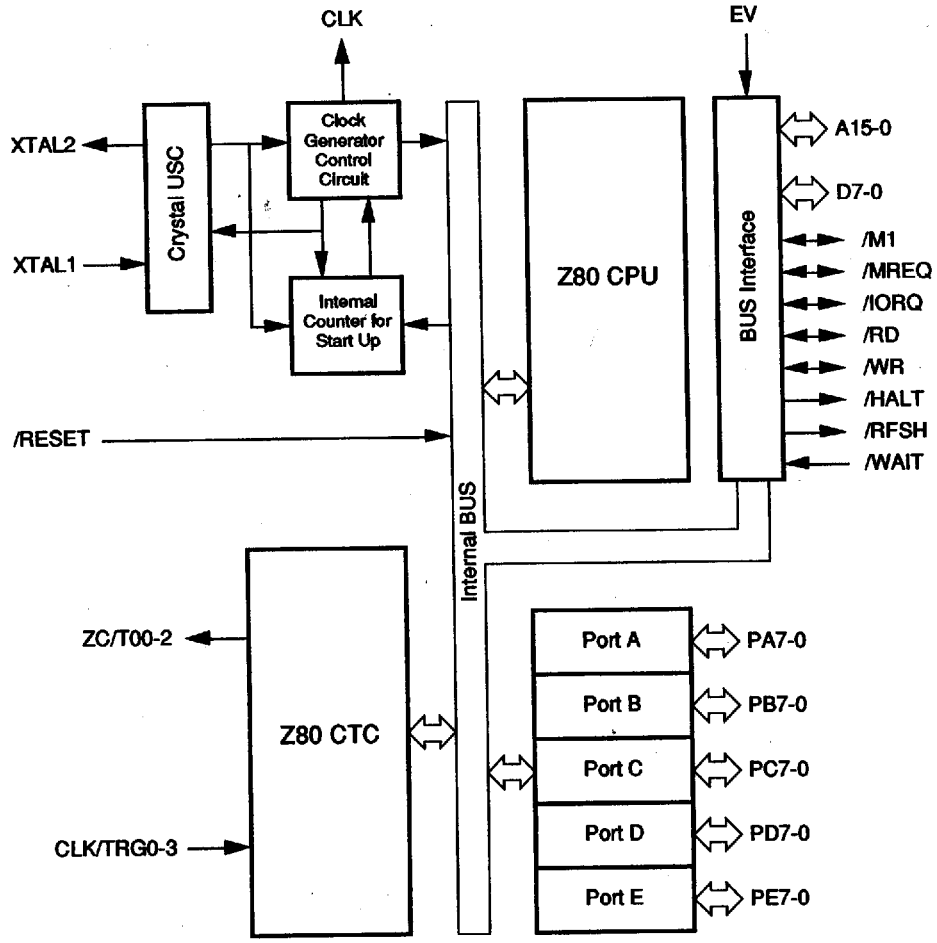
FEATURES

- Z84C00 Z80 CPU with CGC, Z84C30 Z80 CTC, five 8-bit parallel ports.
- High speed operation (6/10 MHz).
- Low power consumption in four operation modes:
  - 45 mA Typ. (Run mode)
  - 6 mA Typ. (Idle1 mode)
  - 9 mA Typ. (Idle2 mode; not applicable to Z84011)
  - 1 µA Typ. (Stop mode)
- Wide operational voltage range (5V ±10%).
- TTL/CMOS compatible.
- Z84011 features:
  - Z84C00 Z80 CPU.
  - On-chip four channel Counter Timer Controller(Z80 CTC).
  - Built-in Clock Generator Controller(CGC).
  - Five 8-bit parallel ports.
  - 100-pin QFP Package.
  - Noise filter to CLK/TRG inputs of the Z80 CTC.
- Z84C11 features:
  - All Z84011 features.
  - Support of Idle 2 Mode.
  - Built-in Watch Dog Timer (WDT).
  - Power-on Reset and Reset Extension.
  - Wait State Generator.
  - Simplified EV Mode Selection.
  - Crystal Divide-by-One Option.
  - External Clock Input Option.

GENERAL DESCRIPTION

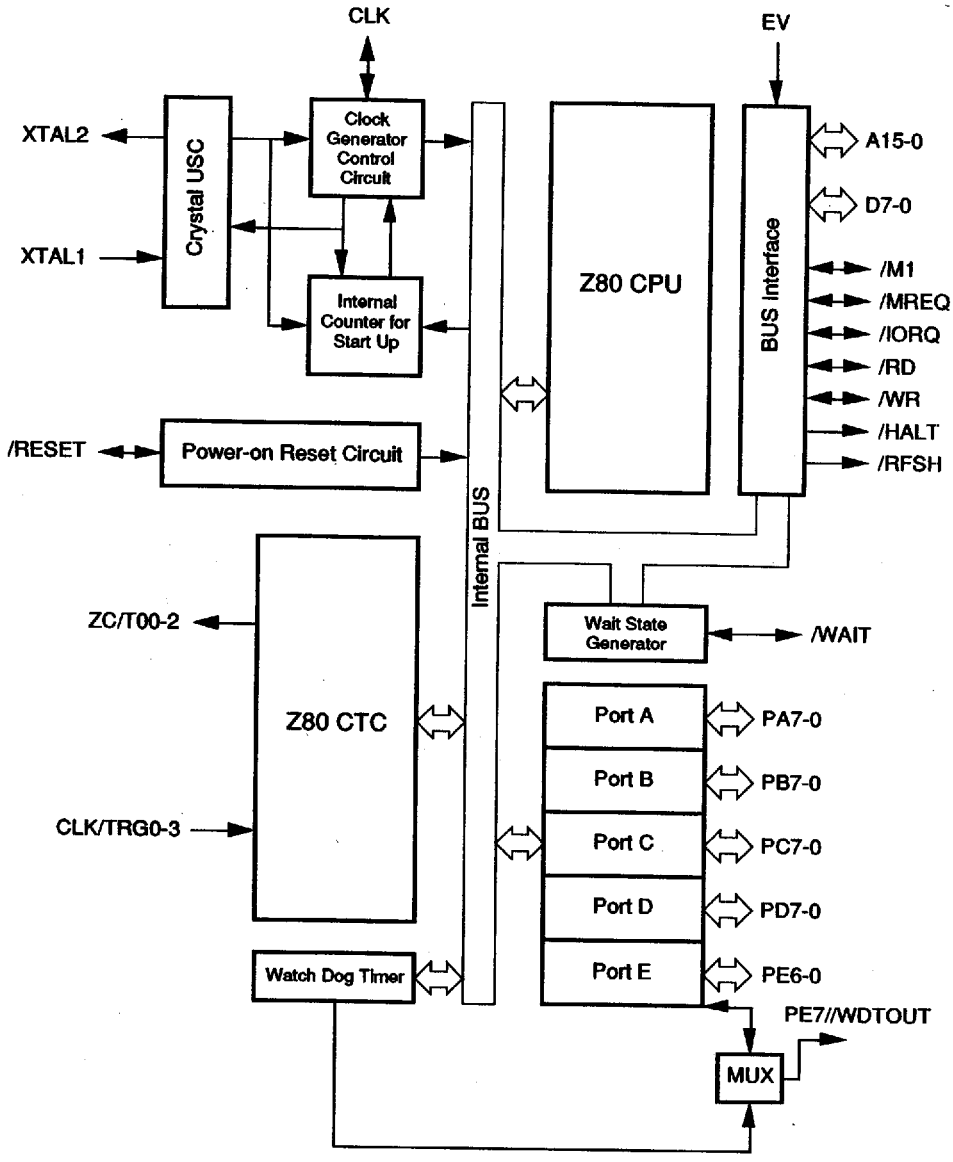
The Z84011 and Z84C11 Parallel I/O Controllers (PIC) are CMOS 8-bit microprocessors. They are integrated with the CTC and five 8-bit parallel ports into a single 100-pin QFP (Quad Flat Pack) package. The Z84C11 is an upward compatible version of the Z84011. Figure 1(a) shows the block diagram of Z84011, and Figure 1(b) shows the block diagram of the Z84C11. Figure 2 has pin assignments for both versions. These high end superintegrated Parallel I/O Controllers are targeted for a broad range of applications ranging from embedded controller to enhancement/cost reductions of existing hardware using Z80 based discrete peripherals.

Hereinafter, the word PIC on the description covering both versions (Z84C11 and Z84011)is used. Use Z84C11 on the description which applies only to the Z84C11, and use Z84011 which applies only to the Z84011.



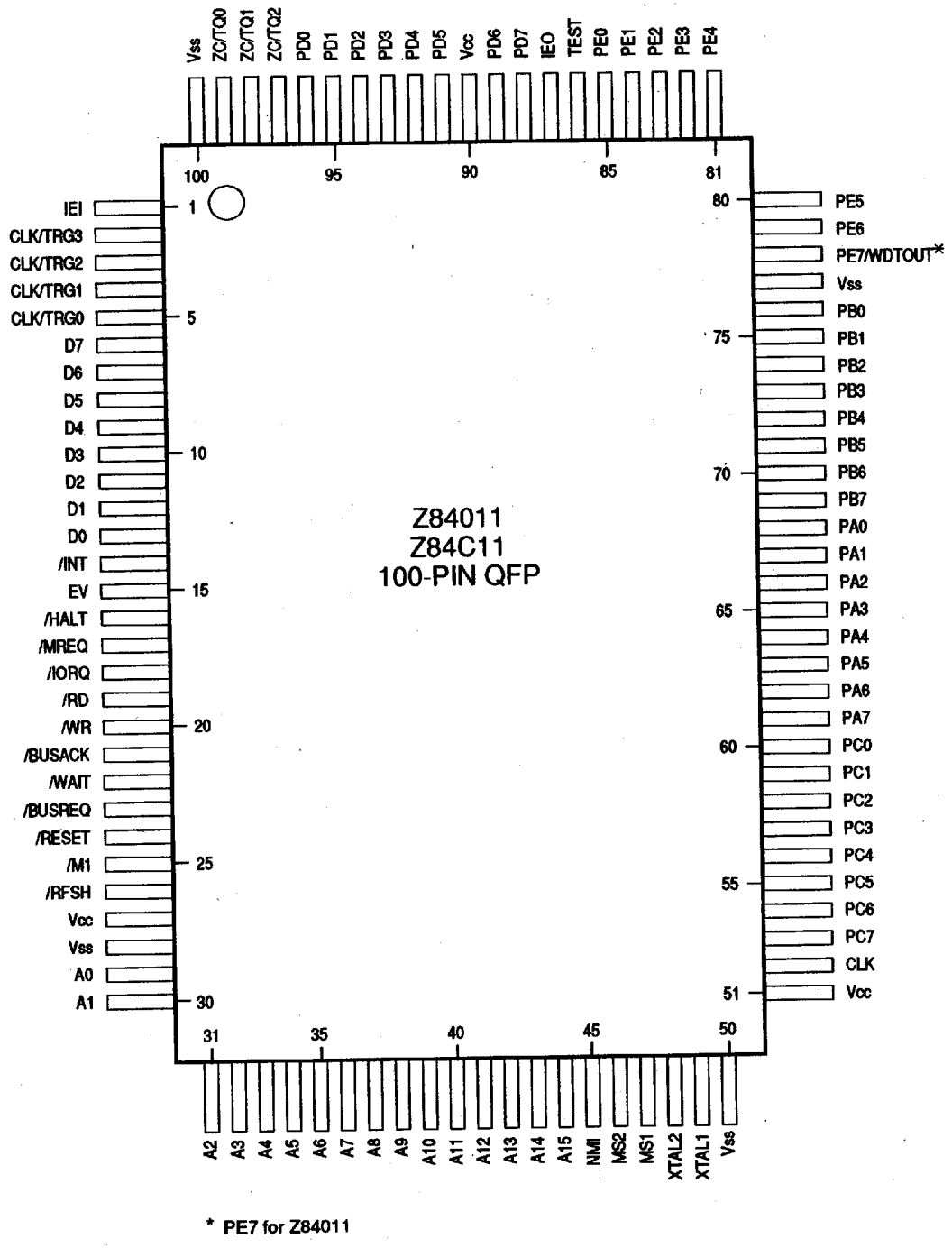
(a) Z84011 Functional Block Diagram

Figure 1. PIC Functional Block Diagram



(b) Z84C11 Functional Block Diagram

Figure 1. PIC Functional Block Diagram (Continued)



* PE7 for Z84011

Figure 2. PIC Pin Assignment

PIN DESCRIPTION

The pin assignment is shown in Figure 2. Following is the description on each pin. For the description and the pin number, if stated as "X11", it applies to both the Z84C11/ Z84011. Otherwise, C11 for Z84C11 and 011 for Z84011.

CPU SIGNALS

Signal Name	# of Pins	Pin #	I/O, 3-State	Description
A15-A0	16	(44-29)	I/O	16-bit address bus. Specifies I/O and memory addresses to be accessed. During the refresh period, addresses for refreshing are output. The bus is an input when the external bus is accessing the on-chip peripherals.
D7-D0	8	(6-13)	I/O	8-bit bidirectional data bus. When the on-chip CPU is accessing on-chip peripherals, these lines are set to output and hold the data to/from on-chip peripherals.
/RD	1	(19)	I/O	Read signal. CPU read signal for accepting data from a memory or I/O device. When an external master is accessing the on-chip peripherals, it is an input signal.
/WR	1	(20)	I/O	Write Signal. This signal is output when data, to be stored in a specified memory or peripheral LSI, is on the MPU data bus. When an external master is accessing the on-chip peripherals, it is an input signal.
/MREQ	1	(17)	Output, 3-State	Memory request signal. When an effective address for memory access is on the address bus, "0" is output. When an external master controls the bus, this signal is tri-stated.
/IORQ	1	(18)	I/O	I/O request signal.When addresses for I/O are on the lower 8 bits (A7-A0) of the address bus in the I/O operation, "0" is output. In addition, the /IORQ signal is output with the /M1 signal at the time of the interrupt acknowledge cycle. This informs peripheral LSI of the interrupt response vector state when on the data bus. When an external master controls the bus, it is an input signal.
/M1	1	(25)	I/O	Machine Cycle "1". /MREQ and "0" are output together in the operation code fetch cycle. /M1 is output for every op-code fetch when a two byte op-code is executed. In the maskable interrupt acknowledge cycle, this signal is output together with /IORQ. When an external master controls the bus, it is an input signal.

CPU SIGNALS

Signal Name	# of Pins	Pin #	I/O, 3-State	Description
/RFSH	1	(26)	Output(011), Output/3-State (C11)	The refresh signal. When the dynamic memory refresh address is on the low order byte on the address bus, this pin goes active along with /MREQ signal.

Note:
For the Z84011 the /RFSH is not tri-stated during EV mode.

Note:
For the Z84C11 the /RFSH is tri-stated during EV mode.

/INT	1	(14)	I/O (Open Drain)	Maskable interrupt request signal. Interrupt is generated by peripheral LSI. This signal is accepted if the Interrupt enable Flip-Flop (IFF) is set to "1". The /INT signal of the CTC is internally wired-OR without pull-up resistors and requires external pull-up. The interrupts from on-chip CTC go out from this pin.
/NMI	1	(45)	Input	Non-maskable interrupt request signal. This interrupt request has a higher priority than the maskable interrupt request and does not rely upon the state of the Interrupt enable Flip-Flop (IFF).
/HALT	1	(16)	Output, 3-State	Halt signal. Indicates that the CPU has executed a HALT instruction. This signal is tri-stated in EV mode.
/BUSREQ	1	(23)	Input	Bus request signal. /BUSREQ requests placement of the address bus, data bus, /MREQ, /IORQ, /RD and /WR signals into the high impedance state. /BUSREQ is normally wired-OR and a pull-up resistor is externally connected.
/BUSACK	1	(21)	Output(011), Output, 3-State (C11)	Bus acknowledge signal. In response to /BUSREQ signal, /BUSACK informs a peripheral LSI that the address bus, data bus, /MREQ, /IORQ, /RD, and /WR signals have been placed in the high impedance state.

Note:
For the Z84011 the /BUSACK will not be tri-stated during EV mode. For the Z84C11 the /BUSACK will be tri-stated during EV mode.

/WAIT	1	(22)	Input(011), I/O(C11)	Wait signal. /WAIT informs the CPU that specified memory or peripheral is not ready for data transfer. As long as /WAIT signal is active, MPU is continuously kept in the wait state.

Note:
For the Z84C11, the /WAIT pin becomes an output to bring out on-chip Wait State Generator during EV mode.

CTC SIGNALS

Signal Name	# of Pins	Pin #	I/O, 3-State	Description
CLK/TRG0 - CLK/TRG3	4	(2-5)	Input.	External Clock/Trigger input. These four CLK/TRG pins correspond to four Counter/Timer Channels. In the counter mode, each active edge causes the downcounter to decrement by one. In timer mode, an active edge starts the timer. It is program selectable whether the active edge is rising or falling.
ZC/TO0 - ZC/TO2	3	(97-99)	Output.	Zero count/timer out signal. In either timer or counter mode, pulses are output when the down counter has reached zero. The Counter/Timer Channel 3 does not have this output.

GENERAL PURPOSE I/O PORT

Signal Name	# of Pins	Pin #	I/O, 3-State	Description
PA7-PA0	8	(61-68)	I/O	General purpose I/O port (Port A). These lines are configured as an input or an output, bit by bit. On Reset, set as "all input."
PB7-PB0	8	(69-76)	I/O	General purpose I/O port (Port B). These lines are configured as an input or an output, bit by bit. On Reset, set as "all Input."
PC7-PC0	8	(53-60)	I/O	General purpose I/O port (Port C). These lines are configured as an input or an output, bit by bit. On Reset, set as "all Input."
PD7-PD0	8	(88, 89, 91-96)	I/O	General purpose I/O port (Port D). These lines are configured as an input or an output, bit by bit. On Reset, set as "all Input."
PE6-PE0	7	(85-79)	I/O	General purpose I/O port (Port E) These lines are configured as an input or an output, bit by bit. On Reset, set as "all Input."
PE7 (011 Only)	1	(78)	I/O	General purpose I/O port (Port E 7). This pin is configured as an input or an output. On Reset, set as "Input."
PE7/WDTOUT (C11 Only)	1	(78)	I/O (Open-drain I/O when /WDTOUT)	Port E 7/Watchdog Timer Output (Multiplexed). This pin is configured as a Watch Dog output pin, or as a general purpose input or an output pin. When Watch Dog Timer is enabled, this pin becomes /WDTOUT regardless of the programming as an I/O port, and also becomes an Open-drain output. If /WDTOUT is connected other than a /RESET pin, an external pull-up resistor may be required. On Power-on Reset, this pin is set as PE7 and "Input."

SYSTEM CONTROL SIGNALS

Signal Name	# of Pins	Pin #	I/O, 3-State	Description
IEI	1	(1)	Input	Z80 CTC Interrupt enable input signal. This signal is used with the IEO to form an interrupt priority daisy chain when there is more than one interrupt-driven peripheral.
IEO	1	(87)	Output	Z80 CTC interrupt enable output signal. In the daisy chain interrupt control, IEO controls the interrupt of external peripherals. IEO is active when IEI is "1" and the CPU is not servicing an interrupt from the on-chip peripherals.
/RESET	1	(24)	Input (011), I/O (Open Drain) on C11	Reset signal. /RESET signal is used for initializing MPU and other devices in the system. Also used to return from the steady state in the STOP or IDLE modes.

Note:
For the Z84011 the /RESET is kept in active state for a period of at least three system clock cycles.

Note:
For the Z84C11, during the power-up sequence, the /RESET becomes Open-drain output and the Z84C11 will drive this pin to "0" for 25 to 75 msec after the power supply passes through approx. 2.2V and then reverts to input. If it receives the /RESET signal after power-on sequence, it will drive the /RESET pin for 16-processor clock cycles depending on the status of the Reset Output Disable bit in the Watch Dog Timer Master Register. If this Reset output is disabled, it must be kept in an active state for a period of at least three system clock cycles. Note, that if using Z84C11 in the Z84011 socket, modification may be required on the Reset circuit since this pin is a "pure input pin" on the Z84011. The /RESET pin does not have internal pull-up resistors and requires external pull-up. For more details of the function, refer to "Functional Description."

Signal Name	# of Pins	Pin #	I/O, 3-State	Description
XTAL1	1	(49)	Input	Crystal oscillator connecting terminal. A parallel resonant crystal is recommended. If an external clock source is used as an input to the CGC unit, supply clock goes into this terminal.

Note:
For the Z84C11, a crystal presence is automatically detected by the Z84C11; oscillator and divide-by-two circuits are activated. The single phase clock generated is output on the CLK pin if the external clock is not applied on CLK pin.

Signal Name	# of Pins	Pin #	I/O, 3-State	Description
XTAL2	1	(48)	Output	Crystal oscillator connecting terminal.
CLK	1	(52)	Output (011), I/O(C11)	System Clock

Note:
For the Z84011, CLK provides Single Phase system clock generated by CGC. For the Z84C11, if the clock is applied on this pin, the internal oscillator and divide-by-two circuits are bypassed. Otherwise, CLK provides System Clock to the system.

SYSTEM CONTROL SIGNALS

Signal Name	# of Pins	Pin #	I/O, 3-State	Description
MS1, MS2	2	(47,46)	I	Mode select 1 and 2. The mode select input pins. The status on these pins determine one of four power save modes.(Run, Idle1, Idle2 or STOP).
EV	1	(15)	Input	Evaluator signal. When "1" is applied to this pin, PIC is put in Evaluation mode. For details, refer to "Functional Description" on EV mode.

Note:
For the Z84011, together with /BUSREQ, the EV signal puts the Z84011 into the evaluation mode. When this signal becomes active, the status of /M1, /HALT and /RFSH change to input. When using Z84011 as an evaluator chip, the CPU is electrically disconnected after one machine cycle is executed with the EV signal "1" and the /BUSREQ signal "0". It follows the instructions from the other CPU (of ICE). Upon receiving /BUSREQ; A15-A0, /MREQ, /IORQ, /RD and /WR are changed to input and D7-D0 changes its direction. /BUSACK is NOT tri-stated so it should be disconnected by an externally connected circuit.

Note:
For the Z84C11, to access on-chip resources from the CPU (e.g., ICE CPU), the CPU is electrically disconnected; A15-A0, /MREQ, /IORQ, /RD and /WR are changed to input; D7-D0 changes its direction; /M1, /HALT and /RFSH are put into the high impedance state when the EV pin is set to "1." Also, /BUSACK is tri-stated.

Signal Name	# of Pins	Pin #	I/O, 3-State	Description
V_{cc}	3	(27, 51, 90)	Power	+5 Volts
V_{ss}	4	(28, 50, 77, 100)	GND	0 Volts
TEST	1	(86)	Input	Test pin. This pin should be tied to "0".

Note:
The following pins have different functions between Z84011 and Z84C11:

Pin Name	Pin #	Function
/RESET	24	Functionality is different.
/WAIT	22	Functionality is different in EV mode.
EV	15	Functionality is different.
PE7	78	(Port E 7) on Z84011; PE7/WDTOUT on Z84C11.
/BUSACK	21	In EV mode, tri-stated on Z84C11; remains active on Z84011.

FUNCTIONAL DESCRIPTION

As shown in Figure 1(a), the Z84011 has a Z80 CPU, CTC, Clock Generator/Controller and Five 8-bit General Purpose I/Os. In addition to these, the Z84C11 has a Watch Dog Timer, Wait State Generator, and Power-on Reset circuit (Figure 1b).

Functionally, the on-chip Z80 CPU and the Z80 CTC are the same as the discrete devices. Therefore, for detailed description of each individual unit, refer to the Product Specification/Technical Manual of each discrete product.

The following subsections describe each individual functional unit of the PIC.

Z84C00/01 Logic Unit

The CPU unit provides all the capabilities and pins of the Zilog Z80 CPU. This allows 100% software compatibility with existing Z80 software. Refer to "Z84C01 Z80 CPU with CGC" Product Specification.

Z84C30 Counter/Timer Logic Unit

This logic unit provides the user with four individual 8-bit Counter/Timer Channels that are compatible with the Z84C30 CTC (Figure 3). The Counter/Timers are programmed by the CPU for a broad range of counting and timing applications. Typical applications include event counting, interrupt and interval counting, and serial baud rate clock generation.

Each of the Counter/Timer Channels, designated Channels 0-3, have an 8-bit prescaler (when used in timer mode) and its own 8-bit counter to provide a wide range of count resolution. Each of the channels have their own Clock/Trigger input to quantify the counting process and an output to indicate zero crossing/timeout conditions. Note that Channel 3 doesn't have its output pin. With only one interrupt vector programmed into the logic unit, each channel can generate a unique interrupt vector in response to the interrupt acknowledge cycle.

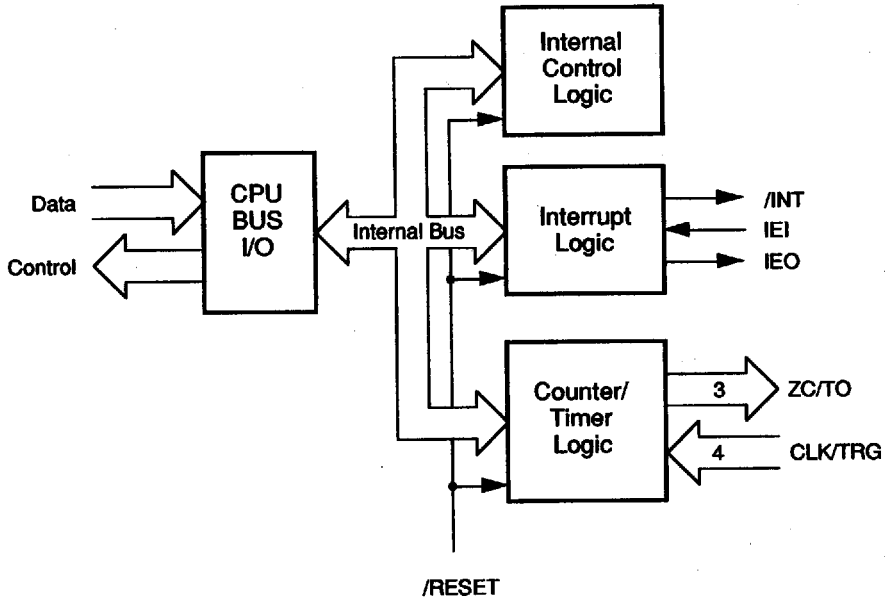


Figure 3. CTC Block Diagram

General Purpose I/O Ports

The PIC has five 8-bit General Purpose I/O ports (a total of 40 I/O lines). Each bit is configured as input or output individually. Figure 4 has the block diagram for General Purpose I/O ports. Each port has 2 associated registers. One is the Port Data Port, which latches the data to the port, and the other is the Data Direction Register, which defines the direction of data flow for the individual bits of its port. While the port bit is assigned as output, the contents of Port Data register can be read back through I/O instructions. For the addresses of these registers, refer to Table 1.

Note: For Z84C11, Port 7 bit 7 is multiplexed with Watch Dog Timer Output (WDTOUT). When enabling the Watch Dog Timer, the /WDTOUT is overriding the function as an I/O port. When used as /WDTOUT, a write to Port Data Register has no effect on the PE7//WDTOUT pin, but changes the contents of the Port E data register. A read to this bit returns the status of the /WDTOUT. For more details about Watch Dog Timer, refer to the "Watch Dog Timer" Section.

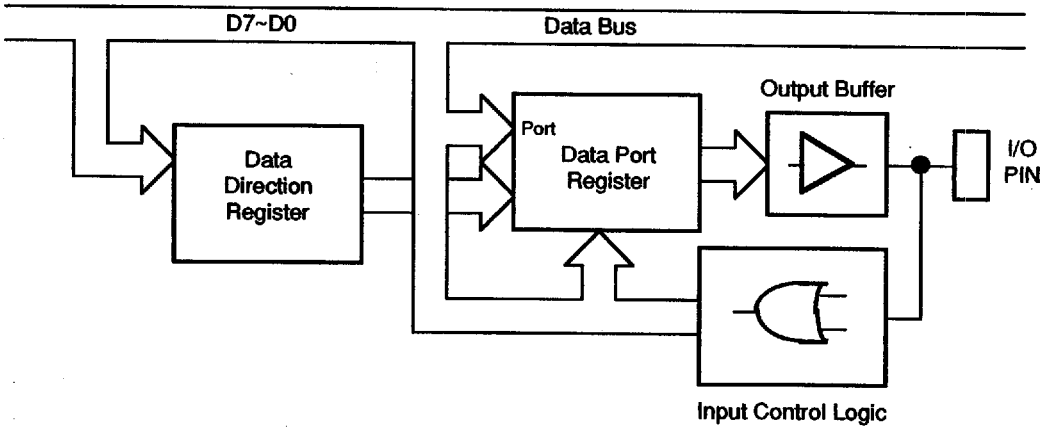


Figure 4. I/O Port Block Diagram

Watch Dog Timer (WDT) Logic Unit (Z84C11 Only)

This logic unit is being superintegrated into the Z84C11 as an enhanced feature to the Z84011. It detects an operation error, caused by the program runaway, and returns to normal operation. Figure 5, shows the block diagram of the WDT. While WDT is enabled, the signal PE7//WDTOUT acts as /WDTOUT. During power down mode of operation (either IDLE1/2 or Stop), Watch Dog Timer is halted. Upon Power-on Reset, it is disabled.

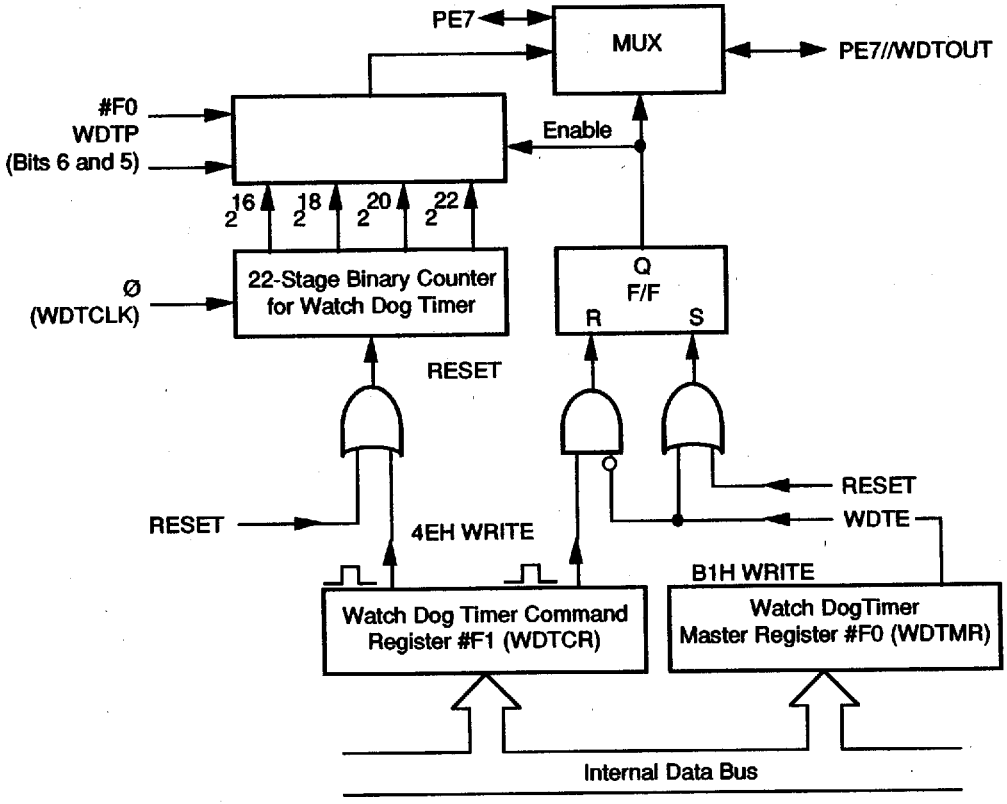


Figure 5. Watch Dog Timer Block Diagram

WDT Output (PE7//WDTOUT)

Since the Z84C11 doesn't have a dedicated WDT output pin, the WDT output is multiplexed with Port E bit 7. When enabling the Watch Dog Timer, the WDTOUT function overrides PE7 function.

When the WDT is used, the "0" level signal is output from the PE7//WDTOUT pin after a duration of time specified in the WDTP in the WDTMR. The output pulse width is one of the following, depending on the PE7//WDTOUT pin connection.

The PE7//WDTOUT is connected to the /RESET pin: The "0" level is pulsed for 5TcC (System Clock cycles).

The PE7/WDTOUT is connected to a pin other than the /RESET pin: The "0" level is kept until the Watch Dog timer is cleared by software, or reset by /RESET pin.

CGC Logic Unit

The PIC has a CGC (Clock Generator/Controller) unit. The PIC allows crystal input (XTAL1, XTAL2) or System Clock Input on the XTAL1 pin. It has clock divide-by-two circuits and generates half-speed clock to the input.

Z84011 Only. The CGC unit is not supporting "Idle 2" mode of operation.

Z84C11 Only. External clock can be also applied from CLK pin. If external clock is provided on the CLK pin, the oscillator and the divide-by-two circuit are bypassed. On Power-on Reset, it comes up in divide-by-two mode. If the external clock or crystal input is provided on the XTAL pins, the internal oscillator is used and the divide-by-two circuit is activated depending upon bit D4 of the WDTMR (See "Programming" section). Power Down modes of the Z84C11 vary based on whether the clock is input on the XTAL1 pin or the CLK pin. If the clock is input on the crystal pin, all of the modes in "halt" state are available. If the system clock is provided from the CLK pin, only the IDLE2 mode is applicable (CTC is kept on running but the internal CPU and Watch Dog Timer are stopped).

Generating the System Clock

The PIC has a built-in oscillator circuit and the required clock is easily generated by connecting a crystal to the external terminals (XTAL1, XTAL2). Clock output is the half speed of the clock source. Example of an oscillator connection is shown in Figure 6.

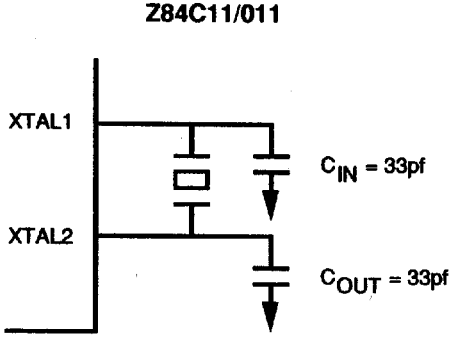


Figure 6. Circuit Configuration for Crystal

Z84C11. Clock speed is the same, or half, the frequency of the clock source.

Recommended characteristics of the crystal and the values for the capacitor are as follows, (the values will change with crystal frequency).

- Type of crystal: Fundamental, parallel type crystal (AT cut is recommended).
- Frequency tolerance: Application dependent.
- CL, Load capacitance: Approximately 22pf. (Acceptable range is 20-30pf.)
- Rs, equivalent-series resistance: ≤ 60 ohms
- Drive level: 10mW (for ≤ 10MHz crystal) 5mW (for ≥ 10MHz crystal)
- CIN = COUT = 33pf.

Power-on Reset Logic Unit (Z84C11 Only)

The Z84C11 has the enhanced feature of a Power-on Reset circuit. During the power-up sequence, the Open-drain gate of the on-chip Power-on Reset circuit drives /RESET pin to "0" for 25 to 75 msec after the power supply passes through approx. 2.2V. After the termination of the "Power-on Reset" cycle, the Open-drain gate of the on-chip Power-on Reset circuit stops to drive the /RESET pin. It is required to have external pull-up resistor on the /RESET pin.

If it receives /RESET input from outside after the power-on sequence, and while Reset Output Disable bit in Watch Dog Master Register is cleared to "0", it drives the /RESET pin for 16 processor clock cycles from the falling edge of external /RESET input. Otherwise, /RESET pin must be kept in active state for a period of at least 3 system clock cycles.

If there are power-on reset circuits outside of this device, drive this pin with OPEN-DRAIN type gates and pull-up resistors because the /RESET signal is driven low for the period mentioned above during the Power-on sequence. If the external Power-on Reset circuit has push-pull type drivers and they drive the /RESET pin to "1" during that period, it may cause damage. In particular, when using Z84C11 in the Z84011 socket, modification may be required on the external reset circuit.

Wait State Generator Unit (Z84C11 Only)

The Z84C11 has the enhanced feature of a Wait State Generator circuit. It is capable of generating /WAIT signals to the CPU internally. The status of the External /WAIT input line is sampled after the insertion of software wait states, except the wait states insertion for Interrupt Daisy Chain Wait (for this cycle, insertion of a wait state is complex). The Wait State Control Register can be programmed to generate multiple Wait states during different CPU cycles as listed as follows.

Memory Wait and Op-code Wait
The Wait State Generator can put 0 to 3 wait states in memory accesses. Additionally, one added wait state can be inserted during an /M1 (Op-code fetch) cycle, because /M1 cycles' timing requirement is tighter than memory Read/Write cycles. It generates wait states to the Memory Access in a specified address range, which is programmed in Memory Wait Boundary Register.

I/O Wait
The Wait State Generator can put 0, 2, 4 or 6 wait states to I/O accesses. Regardless of the programming of this field, no I/O wait states are inserted for accesses to on-chip peripherals.

Interrupt Vector Wait
During Interrupt acknowledge cycle, the Wait State Generator can insert one wait state after /IORQ goes active, to extend the time between /IORQ fall to vector fetch by CPU. It allows a slow vector response device.

Interrupt Daisy Chain Wait and RETI Sequence Extension
During Interrupt acknowledge cycle, the Wait State Generator can insert 0, 2, 4 or 6 wait states between /M1 falling to the /IORQ falling edge. This extends the time required to settle the daisy chain. This also allows a longer daisy chain. Further, this field controls the number of wait states inserted during RETI (Return From Interrupt) cycle. If specified to insert 4 or 6 wait states during Interrupt Acknowledge cycle, the Wait State Generator also inserts wait states during the RETI fetch sequence. This sequence is generated with two op-code fetch cycles (Op-code is EDh followed by 4Dh). It inserts 2 or 4 wait states, respectively, if op-code followed by EDh is 4Dh. One wait state if the following op-code is not 4Dh.

Other Functional Features (Z84C11 Only)

For more system design flexibility, the Z84C11 has the following unique features. These features are controlled by WDTMR (Watch Dog Master Register; Address:FOh) For more details, refer to "Programming section."

- Clock Divide-By-One option
- Reset Output Disable
- Control Register Initialize Option

Clock Divide-by-One Option
This feature is programmed through Bit D4 of WDTMR. Upon Power-on Reset, the Clock from on-chip CGC is passed through a divide-by-two circuit. By setting this bit to one, the divide-by-two circuit is bypassed so that the system clock is equal to XTAL input. If the clock is applied to the CLK pin from external clock source, the status of this bit is ignored. Upon power-on reset, it is cleared to 0. For details, refer to "Programming" section.

Reset Output Disable
This feature is programmed by Bit D3 of WDTMR. If this bit is cleared to "0", the /RESET pin is driven to "0" for 16 clock cycles from the falling edge of /RESET input. This feature is for the cases where /RESET is used to get out from the "HALT" state. If this bit has been set to one, the on-chip reset circuit will not drive the /RESET pin except during power-on sequence.

Control Register Initialize Option
This feature is programmed by Bit D2 of WDTMR. This bit determines whether or not to initialize system control registers to initial value on /RESET. An ideal application for using the Watch Dog Timer.

Evaluation Mode

The PIC has a built-in evaluation (or development) mode feature which allows the users to utilize standard Z80 development systems conveniently. This mode virtually replaces the on-chip Z80 CPU with the external CPU. In this mode, the on-chip CPU is electrically disconnected from the internal bus and all tri-state signals 15-A0, D7-D0, /MREQ, /IORQ, /RD, /WR, /HALT, /M1, (for C11, /RFSH and /BUSREQ as well) as they are tri-stated, or changed to input. This allows the development system CPU to take over and use the internal I/O registers of the PIC (like the CPU was on-chip).

Z84011 Only. When the EV pin is active, the /M1 and /HALT pins are put in the high-impedance state. In using the Z84011 as an evaluator chip, the CPU is electrically disconnected (put in high-impedance state) after one machine cycle is executed with the EV signal being "1" and the /BUSREQ signal being "0". Then, on-chip resources are accessed from outside. /BUSACK and /RFSH are disconnected by an externally connected circuit.

Z84C11 Only. If the EV pin is tied to Vcc on power-up, the Z84C11 enters into an evaluation mode. In this mode, the internal CPU is immediately disconnected from the internal bus and all tri-state signals listed above, and /BUSACK and /RFSH signals are tri-stated, or changed to input. Note that the /WAIT pin became the OUTPUT pin in EV mode, and Wait State Generator generates wait states only as programmed. If the target application board has a separate wait state generator, modification of the target may be required.

The Z84C11 acts like regular operation where the /BUSREQ signal is asserted by an external master. This causes all tri-state signals to be tri-stated by the Z84C11 after one clock delay. For this case, /RFSH, /M1, /HALT and /BUSREQ remain active. The /BUSREQ approach was not used for the evaluation mode.This avoided significant external circuitry to work around the time period before the external CPU uses the bus for the Z84C11 accesses.

PROGRAMMING

I/O Address Assignment

The PIC 's on-chip peripherals' I/O addresses are listed in Table 1. They are fully decoded from A7-A0 and have no image. The registers with Z84C11 located at I/O Address EEh, EFh, F0h and F1h control enhanced features to the Z84C11, and are not assigned on Z84011.

Table 1. I/O Control Register Address

Address	Device	Channel	Register
10h	CTC	Ch 0	Control Register
11h	CTC	Ch 1	Control Register
12h	CTC	Ch 2	Control Register
13h	CTC	Ch 3	Control Register
50h	PIA	Port A	Port A Data Port (PADP)
54h	PIA	Port A	Port A Data Direction Register (PADR)
51h	PIA	Port B	Port B Data Port (PBDP)
55h	PIA	Port B	Port B Data Direction Register (PBDR)
52h	PIA	Port C	Port C Data Port (PCDP)
56h	PIA	Port C	Port C Data Direction Register (PCDR)
30h	PIA	Port D	Port D Data Port (PDDP)
34h	PIA	Port D	Port D Data Direction Register (PDDR)
40h	PIA	Port E	Port E Data Port (PEDP)
44h	PIA	Port E	Port E Data Direction Register (PEDR)
F0h	WDT		Watch Dog Timer Master Register (WDTMR; Not with Z84011)
F1h	WDT		Watch Dog Timer Control Register (WDTCR; Not with Z84011)
EEh	Misc		System Control Register Pointer (SCRP; Not with Z84011)
EFh	Misc		System Control Data Port (SCDP; Not with Z84011) Through SCRP and SCDP Control Register 00 - Wait State Control register (WCR) Control Register 01 - Memory Wait state Boundary Register (MWBR)

CTC Control Registers

For more detailed information, refer to the CTC Technical Manual.

Channel Control Word

This word sets the operating modes and parameters as described below. Bit D0 is a "1" to indicate that this is a Control Word (Figure 7).

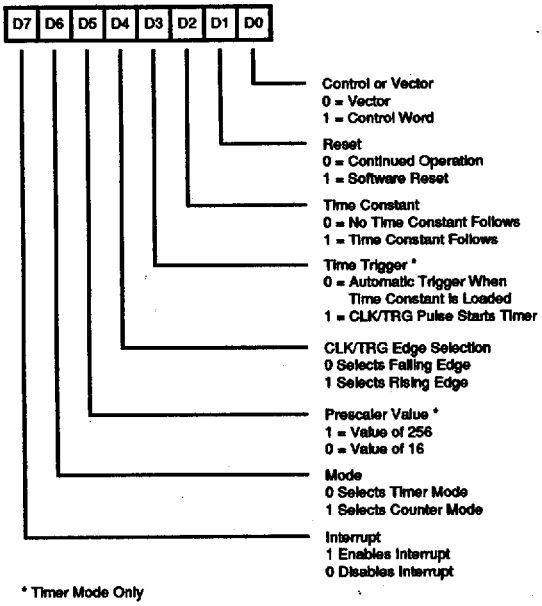


Figure 7. CTC Channel Control Word

Bit D7. *Interrupt Enable.* This bit enables the interrupt logic so that an internal INT can be generated at zero count. Interrupts are programmed in either mode and may be enabled or disabled at any time.

Bit D6. *Mode Bit* This bit selects either Timer Mode or Counter Mode.

Bit D5. *Prescaler Factor.* This bit selects the prescaler factor for use in the timer mode. Either divide-by-16 or divide-by-256 is available.

Bit D4. *Clock/Trigger Edge Selector.* This bit selects the active edge of the CLK/TRG input pulses.

Bit D3. *Timer Trigger.* This bit selects the trigger mode for timer operation. Either automatic or external trigger is selected.

Bit D2. *Time Constant.* This bit indicates that the next word programmed is time constant data for the downcounter.

Bit D1. *Software Reset.* Writing 1 to this bit indicates a software reset operation, which stops counting activities until another time constant word is written.

Time Constant Word

Before a channel starts counting, it must receive a time constant word. The time constant value is anywhere between 1 and 256, with "0" being accepted as a count of 256 (Figure 8).

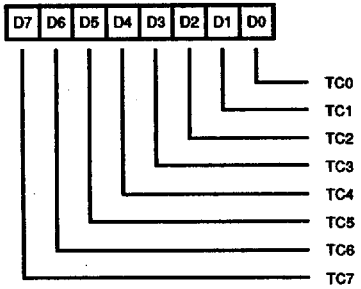


Figure 8. CTC Time Constant Word

Interrupt Vector Word

If one or more of the CTC channels have interrupt enabled, then the Interrupt Vector Word must be programmed. Only the five most significant bits of this word are programmed, and bit D0 must be "0". Bits D2-D1 are automatically modified by the CTC channels when it responds with an interrupt vector (Figure 9).

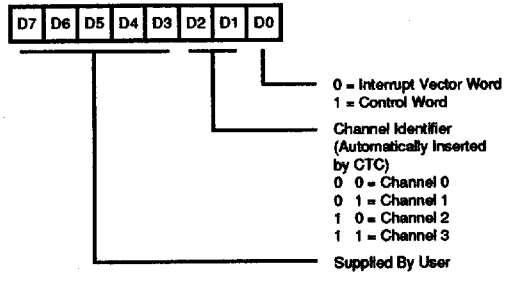


Figure 9. CTC Interrupt Vector Word

PIA Registers

Port Direction Registers

The PIA ports can be configured for any combination of input and output bits. The direction is controlled by writing to the Port Direction Registers (PADR, PBDR, PCDR, PDDR, PEDR). A "1" written to a bit position indicates that the respective bit is an Output. All bits are inputs on reset. This register is write only (Figure 10).

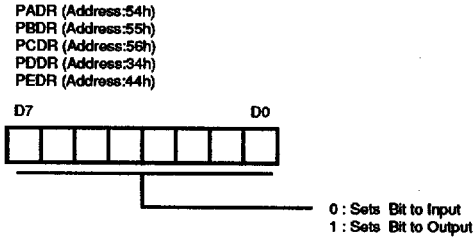


Figure 10. Port Direction Register

Port Data Port

This register holds the data to the port bit assigned as output. It holds the data until modified by the CPU. If the bit is assigned as an output, a read to this register gives the current value on the port pin, or reads back the contents of this register (Figure 11).

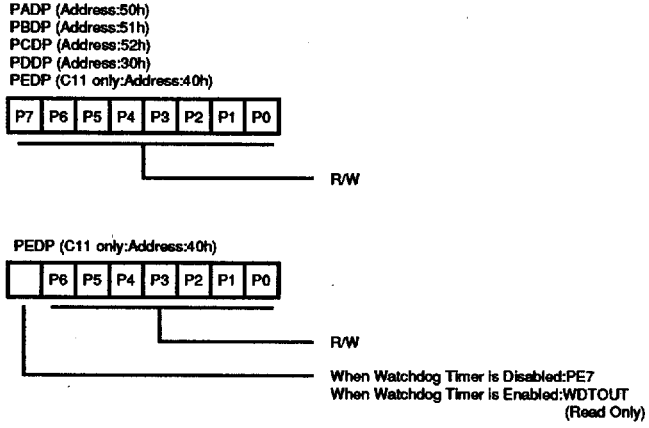


Figure 11. Port Data Port

Writing a Port Data Port. If the bit location is assigned as an input, A write to the bit location, assigned as an input, changes the contents of the Port Data Port Register without affecting the port's operation.

If the bit location is assigned as an output. A write to the bit location, assigned as an output, latches the data into the Port Data Port register, and the content of the register is output on the pin.

Z84C11 Only. If Port E bit 7 has been assigned as Watch Dog Timer Output (/WDTOUT), a write to PE7 location will not change the status of the PE7, but changes the bit 7 of PEDR.

Reading a Port Data Port. If the bit location is assigned as an input, a read to the bit location, assigned as an input reads the data on the port directly. The contents of the Port Data Port Register are not changed.

If the bit is assigned as an output. A read to the bit location, assigned as an output, reads back the contents of the Port Data Port Register.

Z84C11 Only. If Port E bit 7 has been assigned as Watch Dog Timer Output (/WDTOUT), a read to PE7 location returns the status of WDTOUT.

As mentioned above, a write to the bit location assigned as input, will not affect the port's operation. When changing its mode to output from input, write data to be output into port data port before programming Data Direction Register to Output, or there may be a glitch in the port pin.

Watch Dog Timer Control Registers (Z84C11 Only)

There are two registers to control Watch Dog Timer operations; Watch Dog Timer Master Register (WDTMR; I/O Address F0h) and the WDT Command Register (WDTCR; I/O Address F1h). Watch Dog Timer Logic has a "double key" structure to prevent the WDT disabling error which could lead to WDT operation stop page due to program runaway. Also, these registers program the power-down mode of operation. The "Second Key" is needed when turning off the Watch Dog Timer.

Enabling the WDT. The WDT is enabled by setting the WDT Enable Bit (D7:WDTE) to "1" and the WDT Periodic field (D5,D6:WDTP) to the desired time period. These command bits are in the Watch Dog Timer Master Register (WDTMR; I/O Address F0h).

Disabling the WDT. The WDT is disabled by clearing WDT Enable bit (WDTE) in the WDTMR to "0" followed by writing "B1h" to the WDT Command Register (WDTCR; I/O Address F1h).

Clearing the WDT. The WDT can be cleared by writing "4Eh" into the WDTCR.

Watch Dog Timer Master Register

(WDTMR; I/O address F0h)
This register controls the activities of the Watch Dog Timer and system functions (Figure 12).

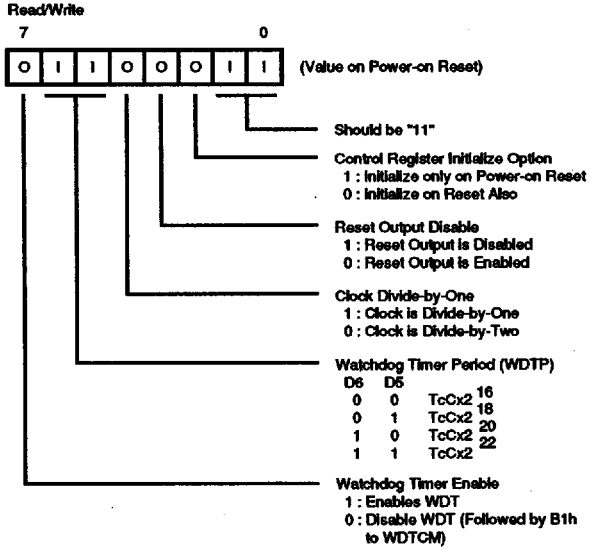


Figure 12. Watch Dog Timer Master Register

Bit D7. *Watch Dog Timer Enable* (WDTE). This bit controls the activities of Watch Dog Timer. The WDT is enabled by setting this bit to "1". To disable WDT, write "0" to this bit followed by writing "B1h" in the WDT Command Register. Watch Dog Timer Logic has a "double key" structure to prevent the WDT disabling error which may lead to WDT operation stop page, due to program runaway. Upon Power-On Reset, this bit is cleared to "0" and the WDT is disabled.

Bit D6-D5. *WDT Periodic field* (WDTP). This two bit field determines the desired time period. Upon Power-on reset, this field is set to "11" and the time period is (TcC x 222).

00 - Period is (TcC x 2^{16})
01 - Period is (TcC x 2^{18})
10 - Period is (TcC x 2^{20})
11 - Period is (TcC x 2^{22})

Bit D4. *Clock Divide-by-one option.* "0"-Disable ,"1"-enable. On-chip CGC unit has a divide-by-two circuit. By setting this bit to one, this circuit is bypassed and clock on CLK pin is equal to XTAL oscillation frequency (or external clock input on the XTAL1 pin). This bit has no effect when the on-chip CGC unit is not in use and external system clock is fed from CLK pin. Upon Power-on reset, this bit is cleared to "0" and the clock is divided by two.

Bit D3. *Reset Output Disable.* "0"-Reset output is enabled, "1"-Reset output is disabled. This bit controls the /RESET signal and is driven out when /RESET input is used to take the Z84C11 out of the "Halt" state. The reset pulse is driven out for 16-clock cycles from the falling edge of /RESET input, unless this bit is set. Upon Power-on reset, this bit is cleared to "0".

Bit D2. *Control Register Initialize Option.* "0"- Initialize control registers on Reset; "1"- Initialize control registers only on Power-on Reset. D2 determines whether to initialize system control registers to initial values on /RESET. If this bit is cleared to 0, contents of control registers are initialized at /RESET. If this bit is set to 1, contents of control registers are initialized ONLY on Power-on Reset (/RESET will not initialize the control registers). Upon Power-on Reset, this bit is cleared to "0".

Bit D1-D0. *Reserved.* These two bits are reserved and are programmed as "11". A read to these bits returns "11".

Watch Dog Timer Command Register
(WDTCR; I/O address F1h)
In conjunction with the WDTMR, this register works as a "Second Key" for the Watch Dog Timer. This register is write only (Figure 13).

Write B1h after clearing WDTE to "0" - Disable WDT.
Write 4Eh - Clear WDT.

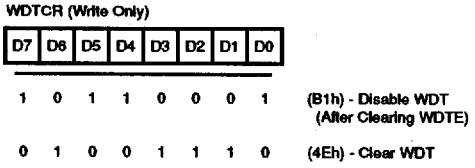


Figure 13. Watch Dog Timer Command Register

Registers for the Wait State Generator

(The following registers are not available on Z84011).

There are two indirectly accessible registers to program wait states; Wait State Control Register (WCR, Control Register 00h) and Memory Wait Boundary Register (MWBR, Control Register 01h). To access these registers, Z84C11 writes "register number to be accessed" to the System Control Register Pointer (SCRP, I/O address EEh), and then accesses the target register through System Control Data Port (SCDP, I/O address EFh). The pointer which writes into SCRP is kept until modified.

System Control Register Pointer
(SCRP, I/O address EEh)
This register stores the pointer to access WCR and MWBR. This register is Read/Write and it holds the pointer value until modified. Upon Power-on reset, all bits are cleared to zero. The pointer value other than 00h and 01h, is reserved and not written. Upon Power-on reset, this register is set to "00h" and points to WCR (Figure 14).

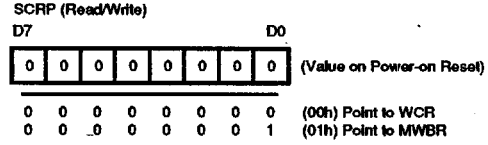


Figure 14. System Control Register Pointer

System Control Data Port
(SCDP, I/O address EFh)
This register accesses WCR and MWBR (Figure 15).

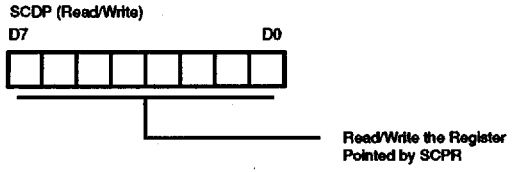


Figure 15. System Control Data Port

Wait State Control Register
(WCR, register number 00h)
This register accessed through SCDP with the pointer value 00h in SCRP (Figure 16). To maintain compatibility with the Z84011, the Z84C11 inserts the maximum number of wait states (set all bits of this register to one) for sixteen/M1 cycles after Power-on Reset. It automatically clears the contents of this register (move to no-wait state insertion) on the trailing edge of the 16th /M1 signal unless software has programmed a value. If automatic wait state insertion is needed, the wait state is programmed within this time period. A read to WCR during this period will return FFh, unless programmed.

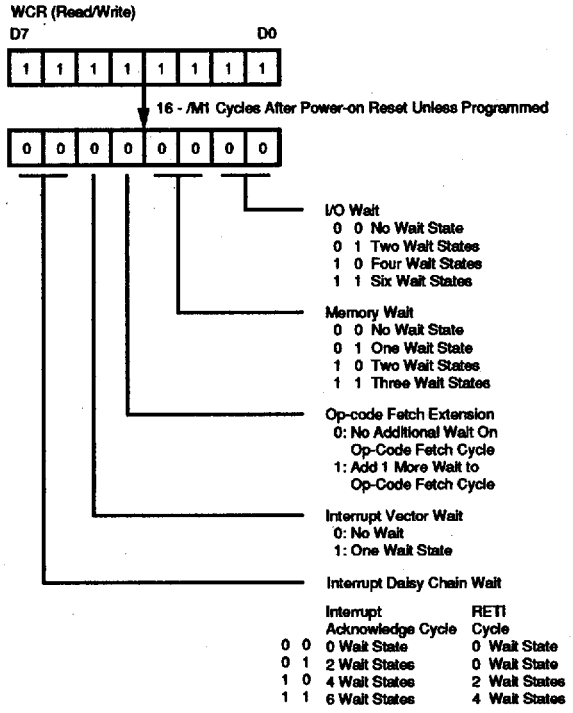


Figure 16. Wait State Control Register

The Wait State Control register has the following fields:

Bit 7-6. *Interrupt Daisy Chain Wait.* This 2-bit field specifies the number of wait states to be inserted during an Interrupt Daisy Chain settle period of the Interrupt Acknowledge cycle. Which means /IORQ goes low after the settling period from /M1 going active. Also, this field controls the number of wait states inserted during the RETI (Return From Interrupt) cycle. If specified to insert four or six wait states during Interrupt Acknowledge cycle, the Wait State Generator also inserts wait states during the RETI fetch sequence. This sequence is formed with two op-code fetch cycles (Op-code is EDh followed by 4Dh). It inserts one wait state if op-code followed by EDh is NOT 4Dh, and inserts two or four wait states, respectively, if the following op-code is 4Dh.

Interrupt Acknowledge	RETI cycle
00 - No Wait states	No wait states
01 - 2 Wait states	No wait states
10 - 4 Wait states	2 Wait states
11 - 6 Wait states	4 Wait states

For sixteen /M1 cycles from Power-on Reset, bits 7-6 are set to "11". They clear to "00" on the trailing edge of the 16th /M1 signal unless programmed.

Bit 5. *Interrupt Vector Wait.* While this bit is set to one, the wait state generator inserts one wait state after the /IORQ signal goes active during the Interrupt Acknowledge cycle. This gives more time for the vector read cycle. While this bit is clear to zero, no wait state is inserted (Standard timing). For sixteen /M1 cycles from Power-on Reset, this bit is set to "1." It then clears to "0" on the trailing edge of the 16th /M1 signal, unless programmed.

Bit 4. *Op-code fetch Extension.* If this bit is set to "1", one additional wait state is inserted during the Op-code fetch cycle in addition to the number of wait states programmed in the Memory Wait field. For sixteen /M1 cycles from Power-on Reset, this bit is set to "1", then clear to "0" on the trailing edge of the 16th /M1 signal, unless programmed.

Bit 3-2. *Memory Wait states.* This 2-bit field specifies the number of wait states inserted during I/O transactions.

00 - No Wait states
01 - 1 Wait states
10 - 2 Wait states
11 - 3 Wait states

For sixteen /M1 cycles from Power-on Reset, these bits are set to "11", then cleared to "00" on the trailing edge of the 16th /M1 signal, unless programmed.

Bit 1-0. *I/O Wait states.* This 2-bit field specifies the number of wait states inserted during I/O transactions.

00 - No Wait states
01 - 2 Wait states
10 - 4 Wait states
11 - 6 Wait states

For sixteen /M1 cycles from Power-on Reset, these bits are set to "11", then cleared to "00" on the trailing edge of the 16th /M1 signal, unless programmed. For the accesses to the on-chip I/O registers, no Wait states are inserted regardless of the programming of this field.

Memory Wait Boundary Register
(MWBR, register number 01h)
This register specifies the address range to insert memory wait states. When accessed memory addresses are within this range, the Wait State Generator inserts Memory Wait States specified in the Memory Wait field in WCR (Figure 17).

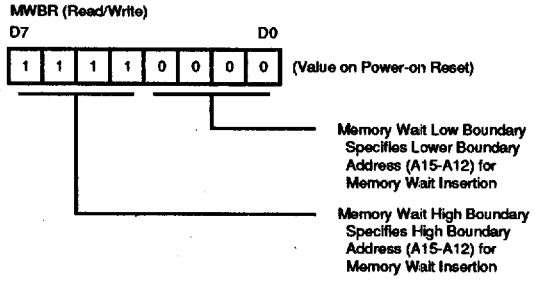


Figure 17. Memory Wait Boundary Register

Bit D7-D4. *Memory Wait High Boundary.* This field specifies A15-A12 of the upper address boundary for Memory wait.

Bit D3-D0. *Memory Wait Low Boundary.* This field specifies A15-A12 of the lower address boundary for Memory wait.

Memory wait states are inserted for the address range:

(D7-D4 of MWBR) ≥ A15-A12 ≥ (D3-D0 of MWBR)

This register is set to "F0h" on Power-on Reset, which specifies the address range for Memory wait as "0000h to FFFFh".

OPERATION MODES

There are four kinds of operation modes available for the PIC in connection with clock generation; RUN Mode, IDLE1/2 Modes and STOP Mode.

The Operation mode is effective when the halt instruction executes. Restart of MPU from the stopped state under IDLE1/2 Mode or STOP mode is effected by inputting either /RESET or interrupt (/NMI or /INT). The mode selection of these power-down modes is made by two external pins (MS1/MS2).

Note: Z84011 is not supporting IDLE 2 mode of operation. Do not use the MS1/MS2 combination of 0 1 with Z84011.

Operation Mode	MS1	MS2	Description at HALT State
RUN Mode	1	1	The PIC continues the operation. If CLK is an output, it supplies clocks to the outside, continuously.
IDLE1 Mode	0	0	The internal oscillator's operation is continued and supplies clocks to the outside, continuously. Clock output (CLK) (and internal clock to the CTC and the Watch Dog Timer) is stopped at "0" level of T4 state in the halt instruction operation code fetch cycle. This mode is not supported with Z84C11 when external clock is applied to the CLK pin.
IDLE2 Mode (C11 Only)	0	1	The internal oscillator and the CTC's operation continues. If the CLK pin has been selected as output, it supplies clock to the outside continuously. But the internal clock to the CPU and the Watch Dog Timer is stopped at "0" level of the T4 state. This is in the cycle immediately after the halt instruction op-code fetch cycle. This mode is also valid when external clock is applied to the CLK pin.
STOP Mode	1	0	All operations of the internal oscillator, clock (CLK) output, internal clock to the CTC, and the Watch Dog Timer are stopped at the "0" level of the T4 state. This is in the cycle immediately after the halt instruction op-code fetch cycle.

Table 2. Device Status in Halt State
(When clock is supplied by on-chip CGC unit)

Mode	CGC	CPU	CTC	WDT	CLK	Note
IDLE1	O	X	X	X	X	
IDLE2	O	X	O	X	O	[1]
STOP	X	X	X	X	X	
RUN	O	O	O	O	O	

O: Operating
X: Stop

Note:
[1] Not supported on 011.

011 Only. All operating modes, except IDLE 2 (Table 2), are valid with Crystal Input (Crystal connected between XTAL1/2 or external Clock input on XTAL1).

C11 Only. All the operating modes in Table 3 are valid with crystal input (Crystal connected between XTAL1/2 or external clock input on XTAL1). For the external clock on the CLK pin, only the IDLE2 and RUN modes are applicable.

TIMING

Basic Timing

The basic timing is explained here with emphasis placed on the halt function relative to the on-chip Clock Generator. The following items are identical to those for the Z84C00. For details, refer to the data sheet of the Z84C00.

- Operation Code Fetch Cycle
- Memory Read/Write Operation
- Input/Output Operation
- Bus Request/Acknowledge Operation
- Maskable Interrupt Request Operation
- Non-Maskable Interrupt Request Operation
- Reset Operation

Operation When HALT Instruction Is Executed

When the CPU fetches a halt instruction in the op-code fetch cycle, /HALT goes active (Low). This is in synchronization with the falling edge of T4 state before the peripheral LSI and CPU stops the operation. After this, the system clock generation differs, depending upon the operation mode (RUN Mode, IDLE1/2 Mode or STOP Mode). If the internal system clock is running, the CPU continues to execute NOP instructions even in the halt state.

RUN Mode (MS1=1, MS2=1)
Shown in Figure 18 is the basic timing when the halt instruction is executed in RUN Mode.

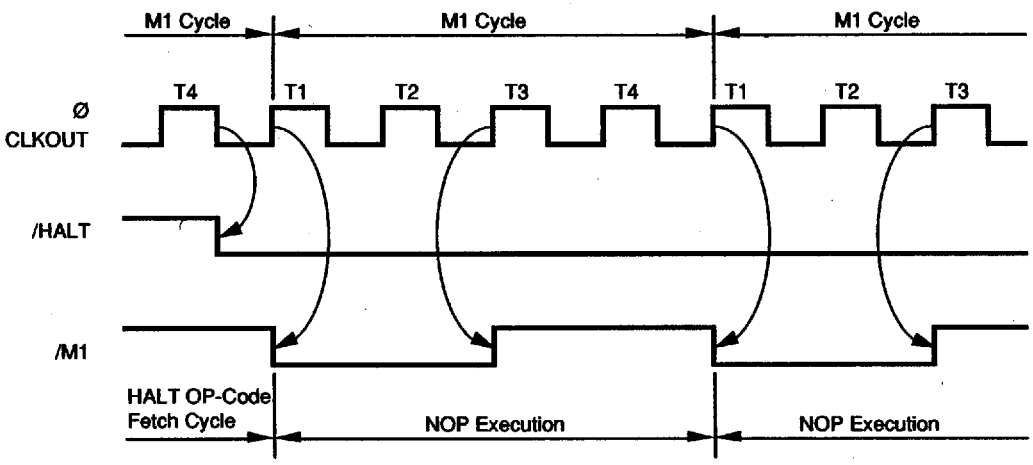


Figure 18. Timing of RUN Mode
(At Halt Instruction Command Execution)

In RUN Mode, internal system clock (Ø) and clock output (CLK) continues even after the halt instruction is executed. Therefore, until the halt state is released by the interrupt signal (/NMI or /INT) or /RESET signal, MPU continues to execute HALT instruction (internally executing NOP instructions).

IDLE1 Mode (MS1=0, MS2=0)
Shown in Figure 19 is the basic timing when the halt instruction is executed in IDLE1 Mode.

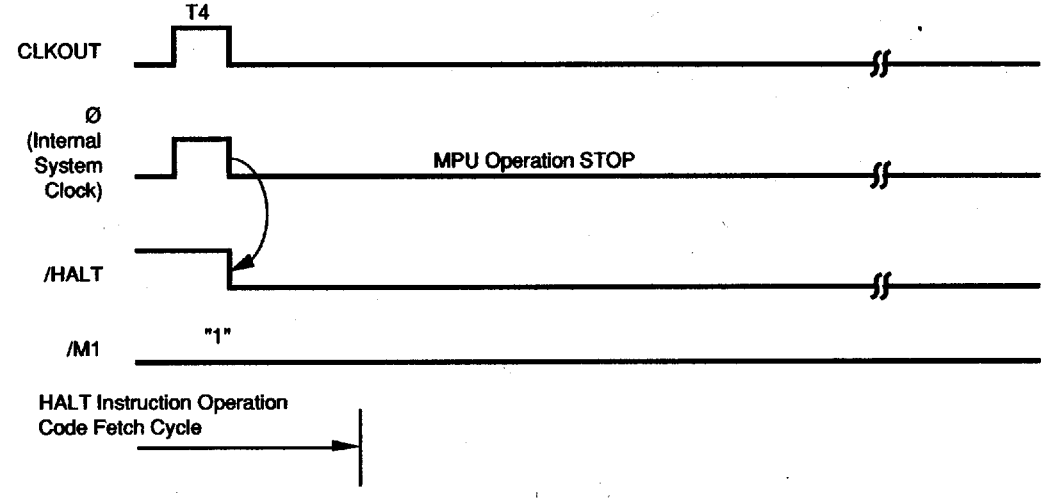


Figure 19. IDLE1 Mode Timing
(At Halt Instruction Execution)

In IDLE1 Mode, the internal oscillator continues to operate, but system clock (Ø) in MPU and clock output (CLK) is stopped at T4 Low state of HALT instruction execution. Then all components in the MPU stop their operation. This mode is not supported when the CGC unit is inactive and the external clock is fed from CLK pin.

IDLE2 Mode (C11 Only; MS1=0, MS2=1)
Shown in Figure 20 is the basic timing when the halt instruction is executed in IDLE2 Mode. This mode is not supported on 011, and not with C11 when external clock is applied onto the CLK pin.

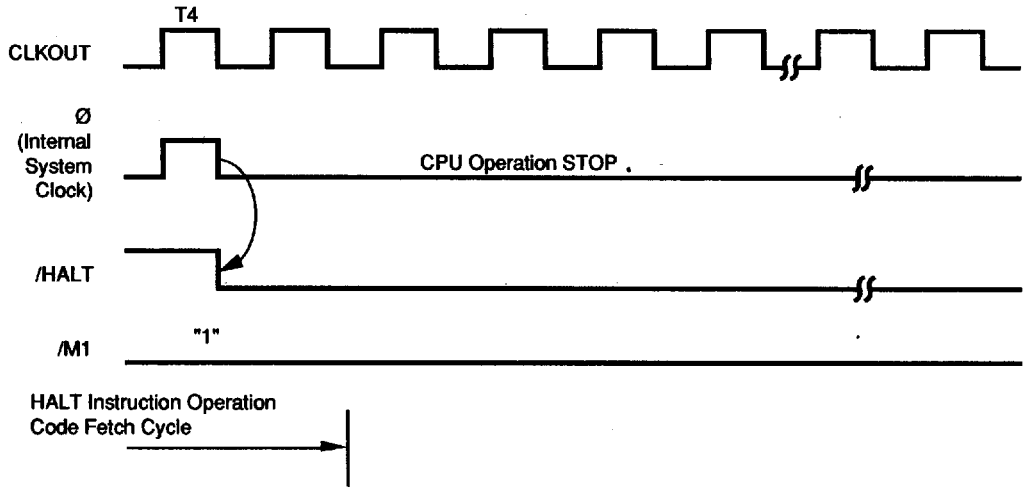


Figure 20. IDLE2 Mode Timing
(At Halt Instruction Execution)

In IDLE2 Mode, the internal oscillator, clock to CTC and clock output (CLK) to the outside of Z84C11, continues to operate. System Clock (Ø) in the Z84C11 is stopped at the T4 Low state of HALT instruction execution. Then the CPU and Watch Dog Timer stop their operation.

STOP Mode (MS1=1, MS2=0)

Shown in Figure 21 is the basic timing when the halt instruction is executed in STOP Mode.

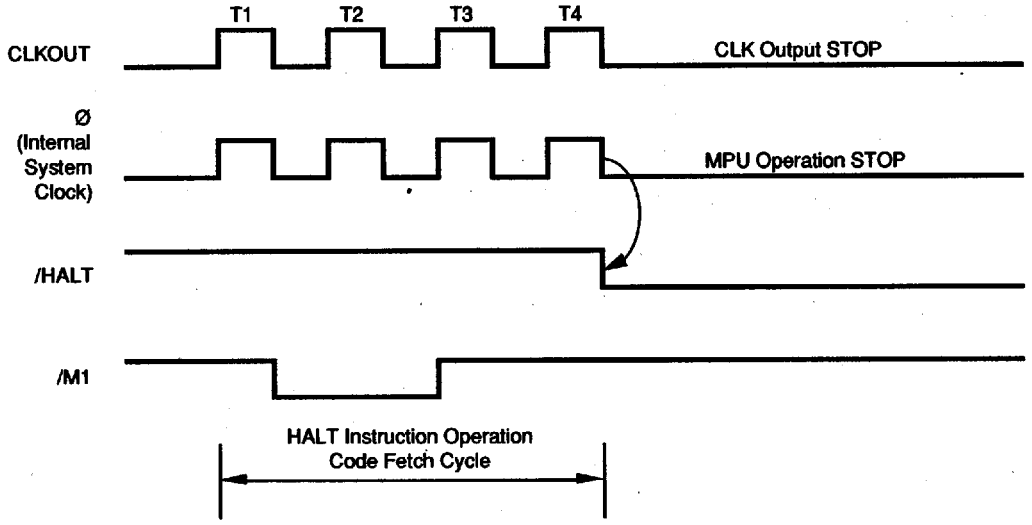


Figure 21. STOP Mode Timing
(At Halt Instruction Execution)

In STOP Mode, the on-chip CGC unit is stopped at T4 Low state of HALT instruction execution. Therefore, System Clock (Ø) in the IPC, operation of Watch Dog timer, CPU, CTC and clock output (CLK) to the outside of the IPC are stopped.

Release From Halt State

The halt state of the CPU is released when "0" is input to the /RESET signal and the MPU is reset or an interrupt request is accepted. An interrupt request signal is sampled at the leading edge of the last clock cycle (T4 state) of NOP instruction. In the case of maskable interrupt, interrupt is accepted by an active /INT signal ("0" level). Also, the interrupt enable flip-flop is set to "1". The accepted interrupt process is started from the next cycle.

Further, when the internal system clock is stopped (IDLE1/2 Mode, STOP Mode), it is necessary first to restart the internal system clock. The internal system clock is restarted when /RESET or interrupt signal (/NMI or /INT) is asserted.

RUN Mode (MS1, MS2=1)

The halt release operation by acceptance of interrupt request in RUN Mode is shown in Figure 22.

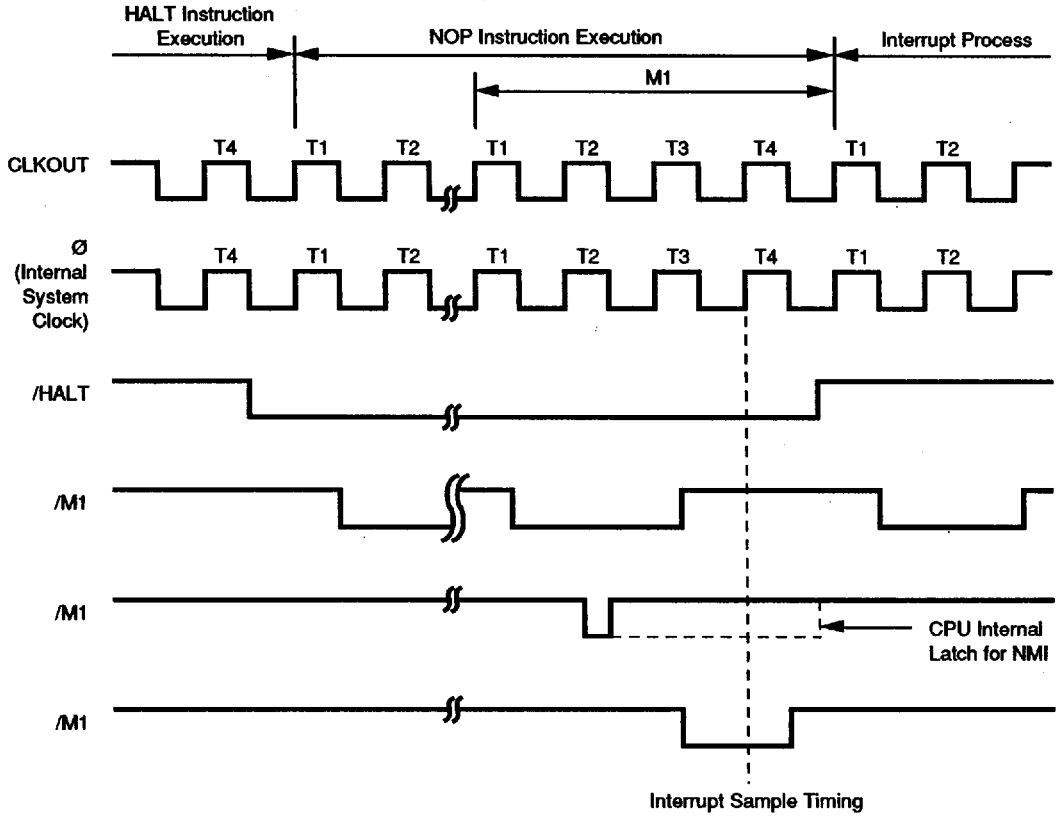


Figure 22. Halt Release Operation Timing By Interrupt Request Signal in RUN Mode

In RUN Mode the internal system clock is not stopped. If the interrupt signal is recognized on the rising clock edge of T4 of the continued NOP instruction, the CPU will execute the interrupt process from the next cycle.

The halt release operation by resetting the CPU in RUN Mode is shown in Figure 23. After Reset, the CPU executes an instruction starting from address 0000H. However, in order to reset CPU, it is necessary to keep /RESET signal at "0" for at least three system clock cycles (For Z84C11: three clock cycles if Reset output is disabled,). In addition, if the /RESET signal becomes "1", after the dummy cycle for at least two T states, the CPU executes an instruction from address 0000H.

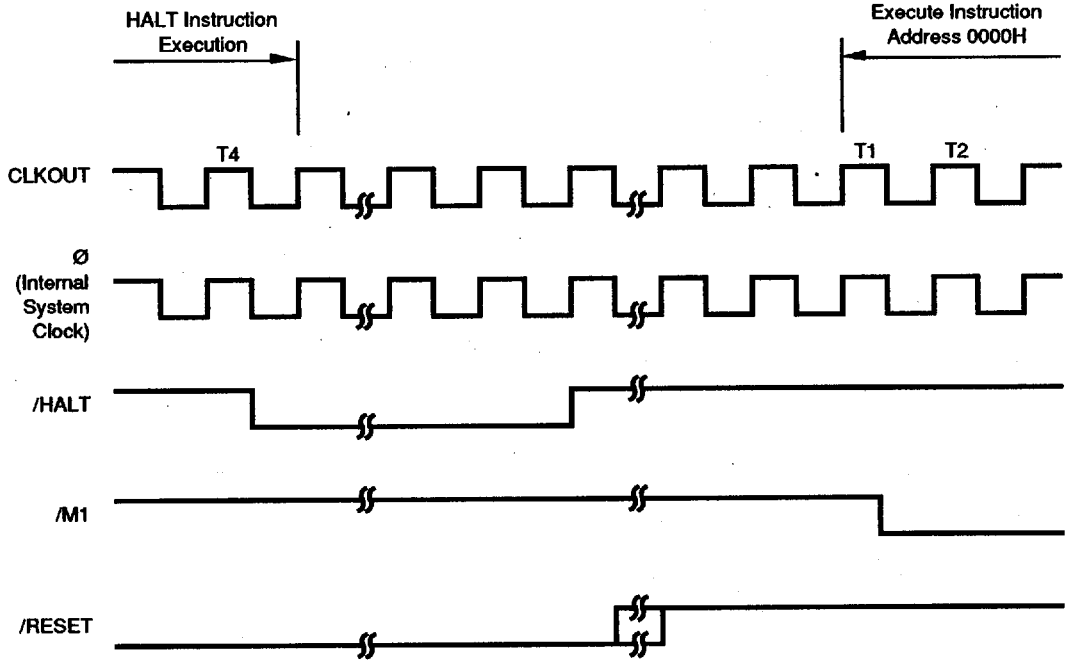
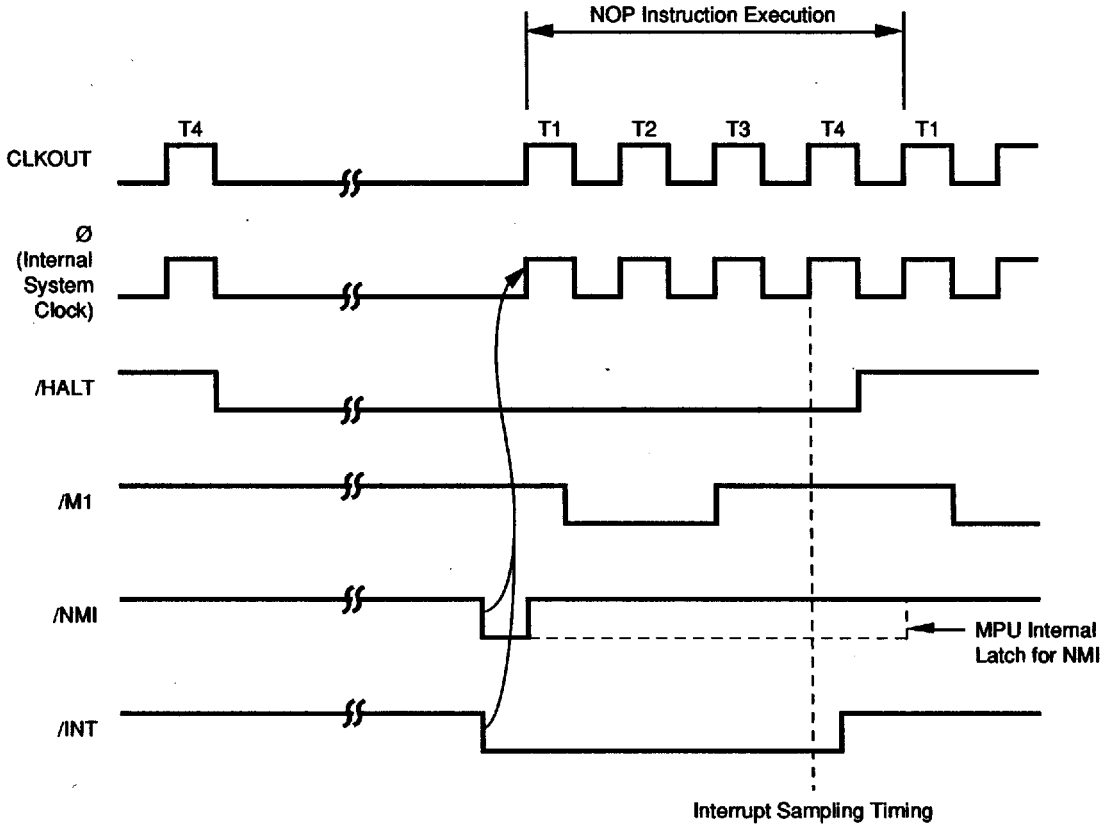


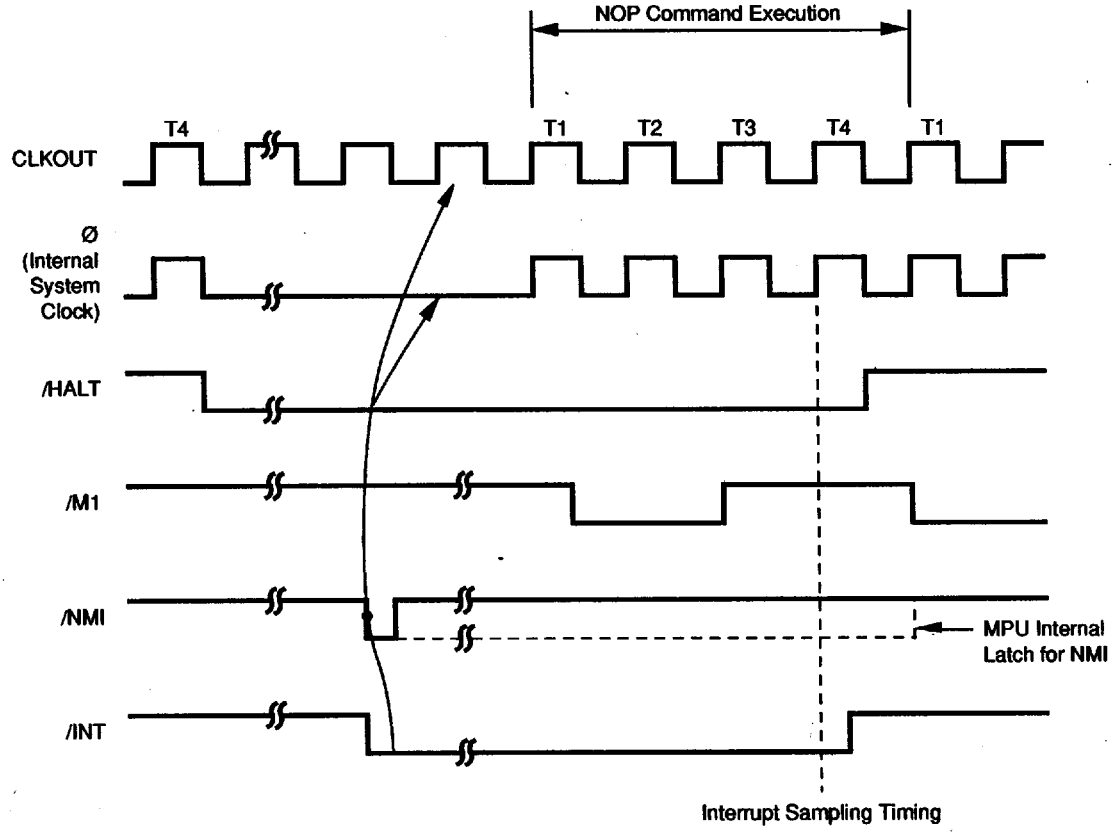
Figure 23. Halt Release Operation Timing By Reset in RUN Mode

IDLE1 Mode (MS1=0, MS2=0)
IDLE2 Mode (MS1=0, MS2=1)
The halt release operation by interrupt signal in IDLE1 Mode is shown in Figure 24(a) and in IDLE2 Mode in Figure 24(b).



(a) IDLE1 Mode

Figure 24. Halt Release Operation Timing By Interrupt Request Signal In IDLE1/2 Mode



(b) IDLE2 Mode

Figure 24. Halt Release Operation Timing By Interrupt Request Signal In IDLE1/2 Mode (Continued)

When receiving /NMI or /INT signal, the stopped internal system clock starts to feed. In IDLE1 Mode, the PIC starts clock output to the outside at the same time.

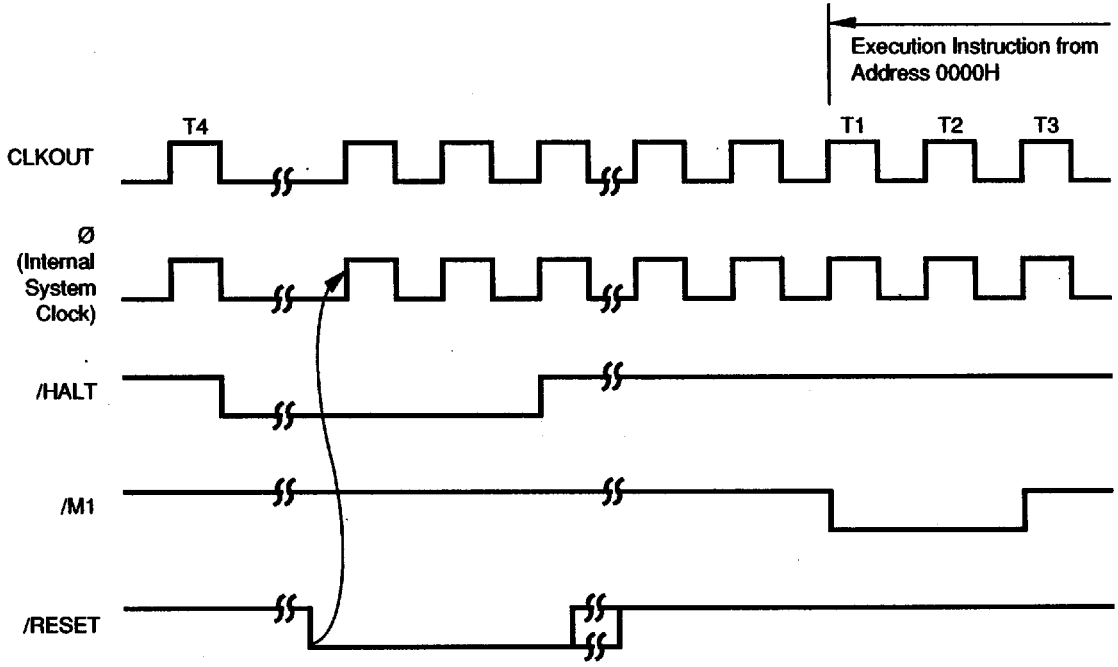
The operation stop of CPU in IDLE2 mode is taking place at "0" level during T4 state in the halt instruction op-code fetch cycle. Therefore, after being restarted by the interrupt signal, CPU executes one NOP instruction and samples an interrupt signal at the rise of T4 state during the execution of this NOP instruction. It then executes the interrupt process from the next cycle.

If no interrupt signal is accepted during the execution of the first NOP instruction after the internal system clock is restarted, CPU is not released from the halt state. It is placed in IDLE1/2 Mode again at "0" level during T4 state of the NOP instruction, stopping the internal system clock. If /INT signal is not at "0" level at the rise of T4 state, no interrupt request is accepted.

The Halt Release Operation By RESET in IDLE1/2 Modes

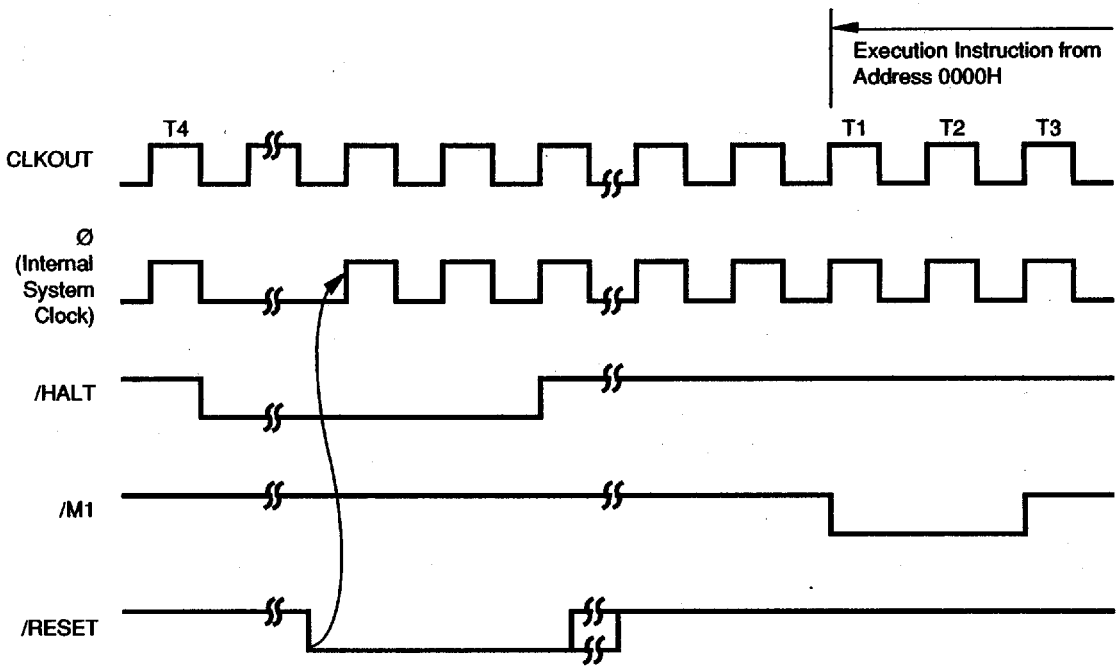
When /RESET signal at "0" level is input into the PIC, the internal system clock is restarted and the PIC will execute an instruction stored in address 0000H.

At time of /RESET signal input, it is necessary to take the same care as that in resetting the PIC in RUN Mode (Figures 25a and 25b).



(a) IDLE1 Mode

Figure 25. Halt Release Operation Timing By Reset In IDLE1/2 Mode



(b) IDLE2 Mode

Figure 25. Halt Release Operation Timing By Reset in IDLE1/2 Mode (Continued)

Halt Release in STOP Mode (MS1=1, MS2=0) By Interrupt

The halt release operation by interrupt signal in STOP Mode is shown in Figure 26.

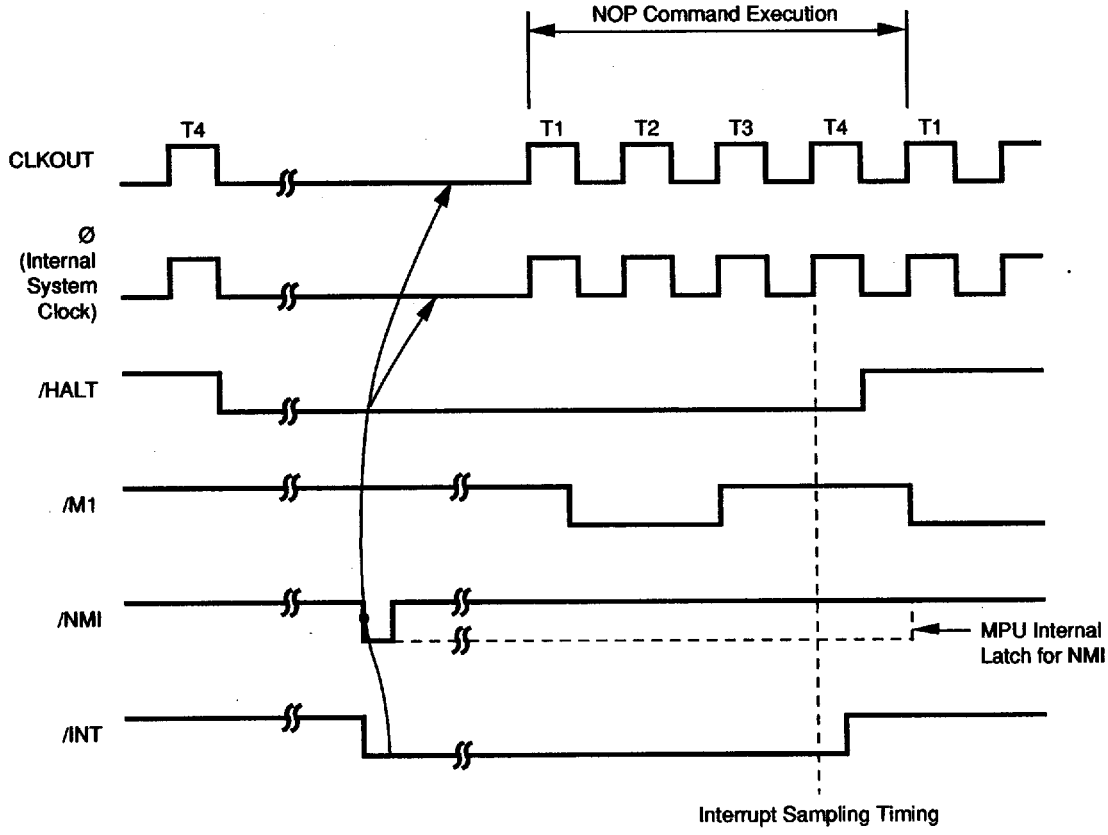


Figure 26. Halt Release Operation Timing By Interrupt Request Signal in STOP Mode

When the PIC receives an interrupt signal, the internal oscillator is restarted. To obtain stabilized oscillation, the internal system clock and clock output (CLK) to the outside are started after a start-up time of (2^{14}+2.5) TcC (TcC: Clock Cycle) by the internal counter.

CPU executes one NOP instruction after the internal system clock is restarted. At the same time, it samples an interrupt signal at the rise of T4 state during the execution of this NOP instruction. If the interrupt signal is accepted, CPU executes the interrupt process operation from the next cycle.

Note: During interrupt signal input, care should be taken like the care of the interrupt signal input in IDLE1/2 Mode.

The halt release operation by the Z84C11 resetting in STOP Mode is shown in Figure 27.

Halt Release in STOP Mode (MS2=0, MS1=1) By /RESET

When /RESET at "0" level is input into the PIC, the internal oscillator is restarted. However, the internal clock counter for warm-up does not operate. Therefore, the operation is not carried out properly due to unstable clock oscillation. It is necessary to hold the /RESET signal at "0" level for sufficient time. The halt release operation by the PIC resetting in STOP Mode is shown in Figure 27.

Z84C11 Only. The /RESET pulse is stretched to a minimum of 16 cycles and driven out of the Z84C11 on the /RESET pin if Reset output is enabled (bit D3 of WDTMR is cleared to "0"). Setting bit D2 disables the driving out of /RESET. If the Control Initialization Option has not been selected (cleared bit D2 of WDTMR), the values programmed in the control registers (WDTMR, SCRP, WCR and MWBR) are not initialized on /RESET. Otherwise, contents of these registers are initialized to the default value.

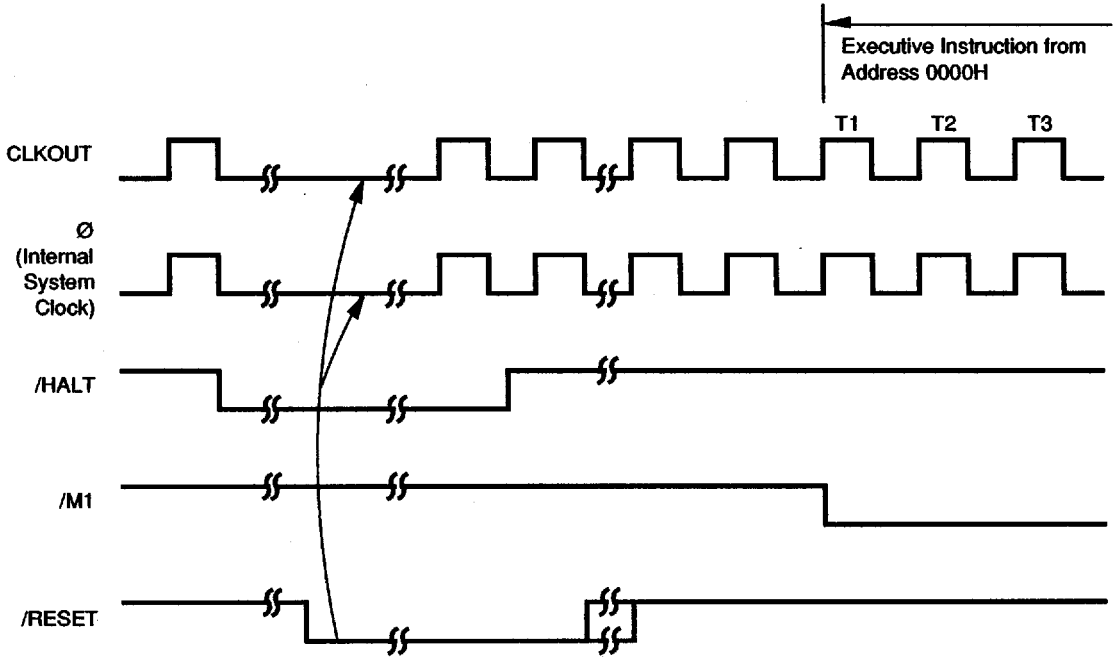


Figure 27. Halt Release Operation Timing By Reset in STOP Mode

Start-up Time At Time of Restart (STOP Mode). When the MPU is released from the halt state by accepting an interrupt request, it executes an interrupt service routine. Therefore, when an interrupt request is accepted, it starts the generating clock on the CLK pin (after a start-up time), by the internal counter [(2^{14}+2.5) TcC (TcC:Clock Cycle)]. This obtains a stabilized oscillation for operation.
Further, in case of restart by the /RESET signal, the internal counter does not operate.

Evaluation Operation

Each of the CPU signals (15-A0, 7-D0, /MREQ, /IORQ, /RD, /WR, /HALT, /M1) can be tri-stated by activating the EV pin. The Z84C11 enhances the counter part by eliminating the requirement of activating /BUSREQ.

Instruction set. The Instruction set of the PIC is the same for the Z84C00. For details, refer to the Data Sheet/Technical Manual of the Z84C00.

AC TIMING

The following section describes the timing of the PIC. The numbers appearing in the figures refer to the parameters on the Table A - F.

CPU Timing

The PIC's CPU executes instructions by proceeding through the following specific sequence of operations:

- Memory read or write
- I/O device read or write
- Interrupt Acknowledge

The basic clock period is referred to as a Time or Cycle and three or more T cycles make up a machine cycle (e.g., M1, M2 or M3). Machine cycles are extended either by the CPU automatically inserting one or more wait states or by the insertion of one or more wait states by the user.

Instruction Op-code Fetch

The CPU places the contents of the Program Counter (PC) on the address bus at the start of the cycle (Figure 28). Approximately one-half clock cycle later, /MREQ goes active. When active, /RD indicates that the memory data can be enabled onto the CPU data bus.

The CPU samples the /WAIT input with the falling edge of clock state T2. During clock states T3 and T4 of an M1 cycle, dynamic RAM refresh can occur while the CPU starts decoding and executing the instruction.

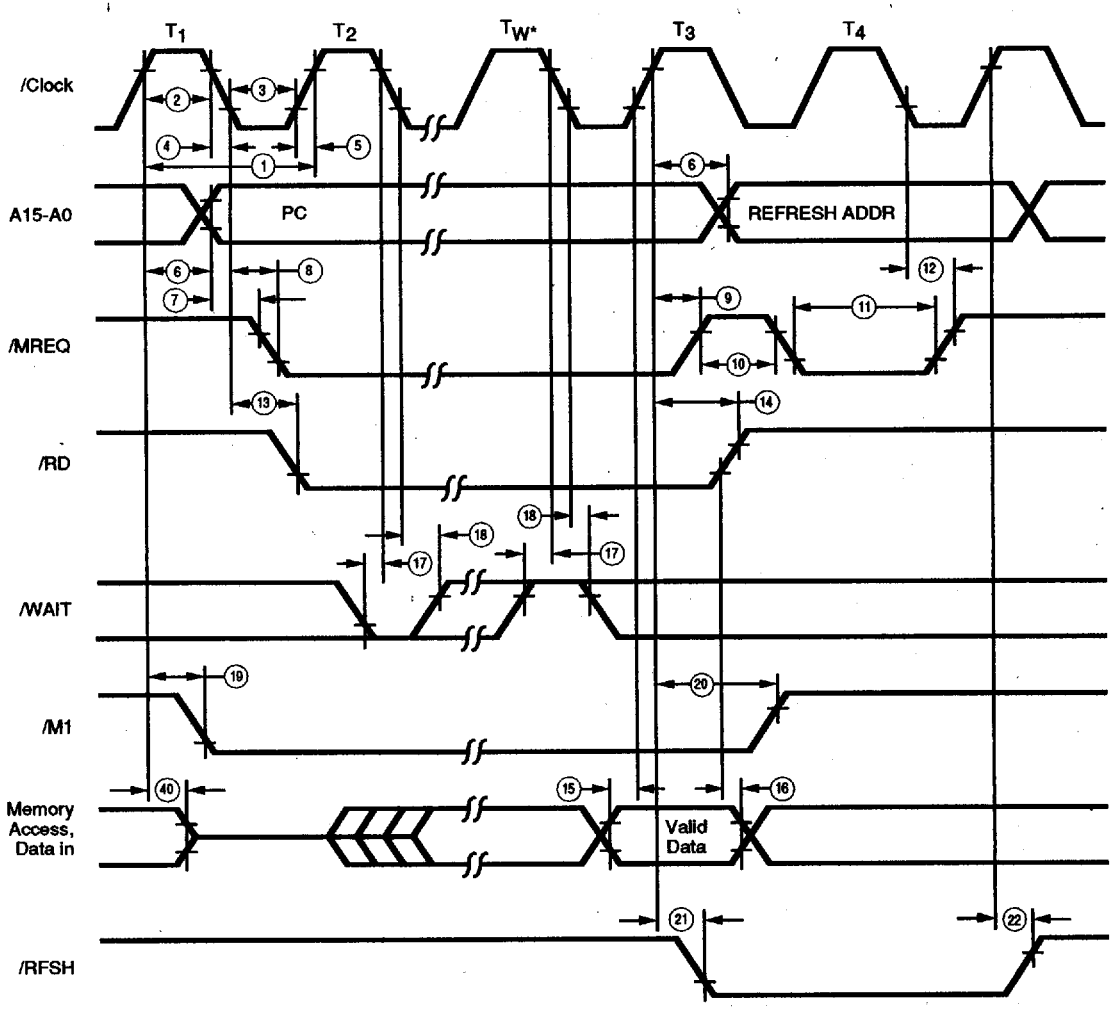


Figure 28. Instruction Op-code Fetch
(See Table A)

Memory Read or Write Cycles

Figure 29 shows the timing of memory read or write cycles other than an Op-code fetch (/M1) cycle. The /MREQ and /RD signals function like the Op-code fetch cycle.

In a memory write cycle, /MREQ also becomes active when the Address Bus is stable. The /WR line is active when the Data Bus is stable, so that it is used directly as an R/W pulse to most semiconductor memories.

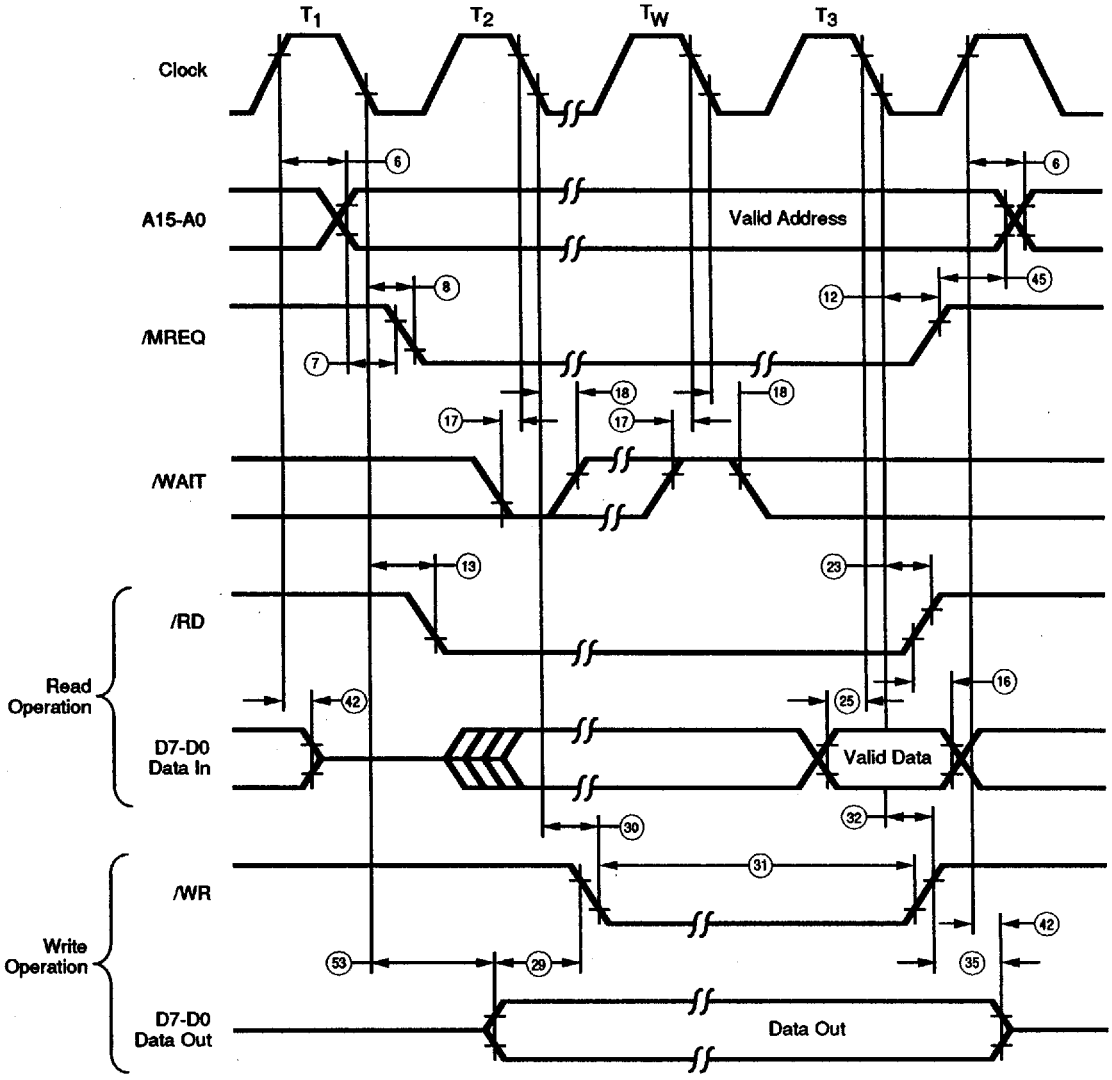
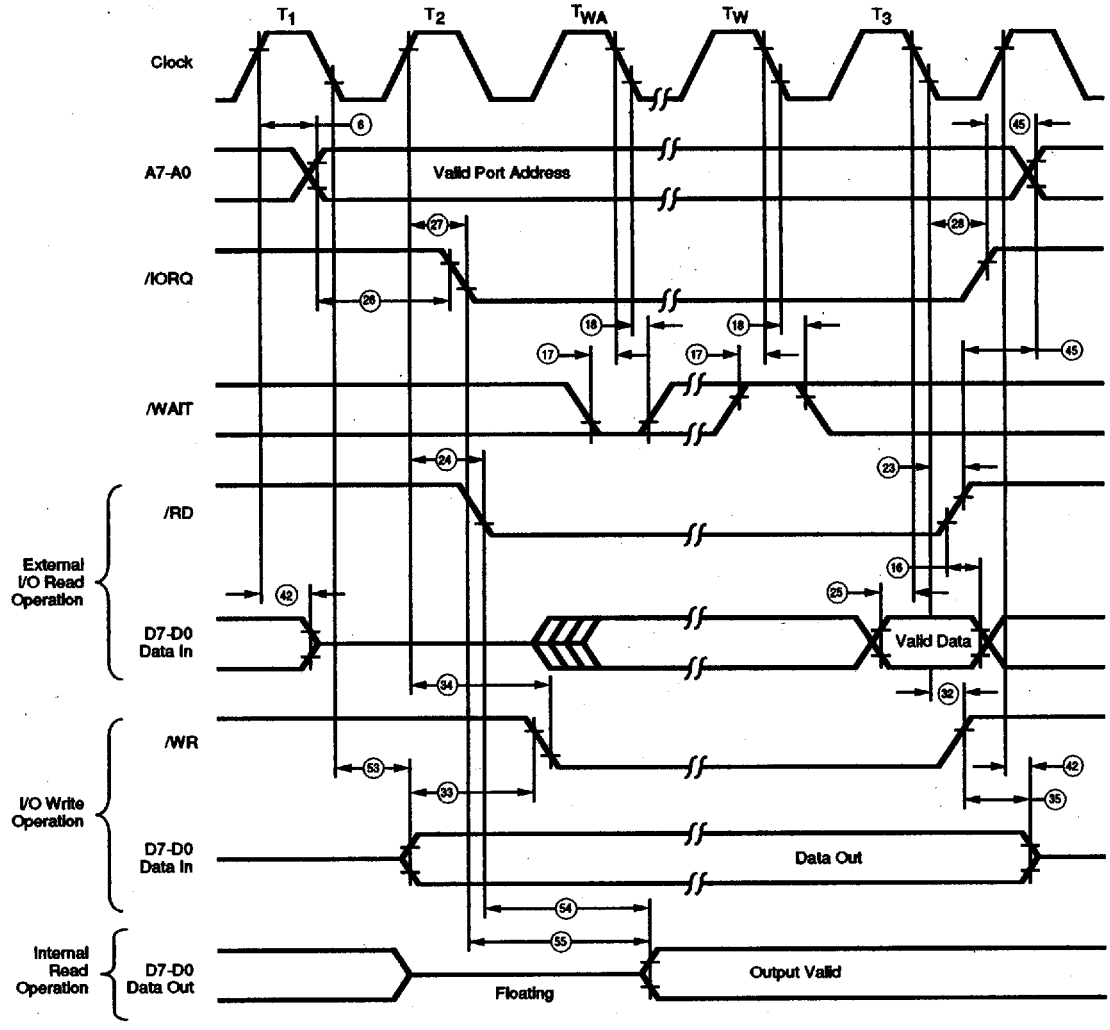


Figure 29. Memory Read or Write Cycle
(See Table A)

Input or Output Cycles

Figure 30 shows the timing for an I/O read or I/O write operation. During I/O operations, the CPU automatically inserts a single wait state (TWA). This extra wait state allows sufficient time for an I/O port to decode the address from the port address lines.

When the CPU is accessing the on-chip I/O registers (CTC, PIA and system control registers), the data from/to these registers also appears on the data bus, or data bus is output during an I/O cycle.



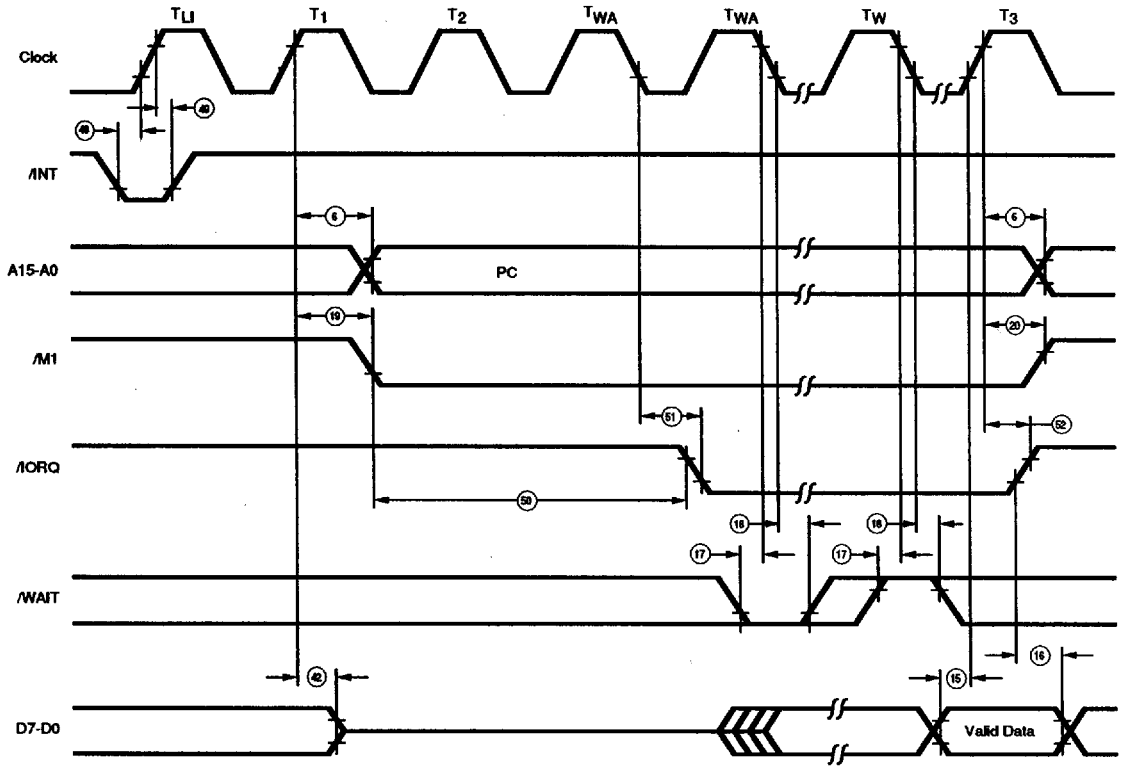
Note: T_{WA} = One wait cycle automatically inserted by CPU

Figure 30. Input or Output Cycle
(See Table A)

Interrupt Request/Acknowledge Cycle

The CPU samples the interrupt signal with the rising edge of the last clock cycle at the end of any instruction (Figure 31). When an interrupt is accepted, a special /M1 cycle is generated.

During this special /M1 cycle, /IORQ becomes active (instead of /MREQ) to indicate that the interrupting device can place an 8-bit vector on the data bus. The CPU automatically adds two wait states to this cycle.



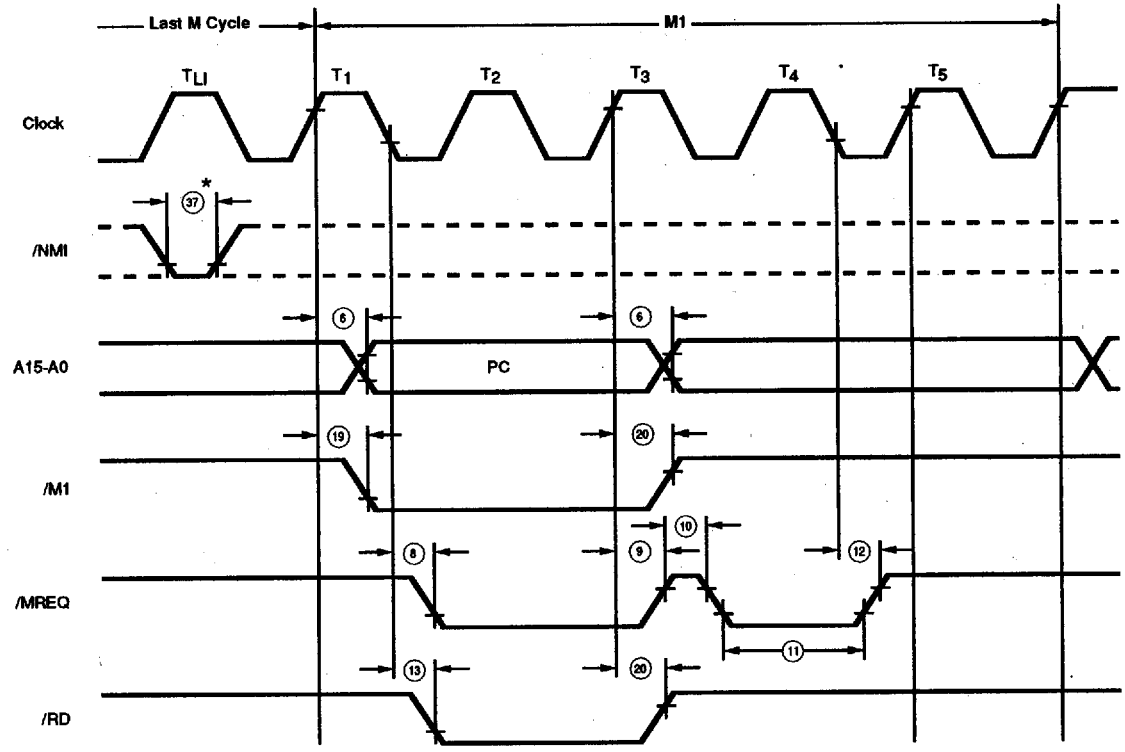
NOTE: 1) T_{LI} = Last state of any instruction cycle

2) T_{WA} = Wait cycle automatically inserted by CPU

Figure 31. Interrupt Request/Acknowledge Cycle
(See Table A)

Non-Maskable Interrupt Request Cycle

/NMI is sampled at the same time as the maskable interrupt input /INT, but has higher priority and cannot be disabled under software control. The subsequent timing is similar to that of a normal memory read operation except that data put on the bus by the memory is ignored. Instead the CPU executes a restart (RST) operation and jumps to the /NMI service routine located at address 0066H (Figure 32).

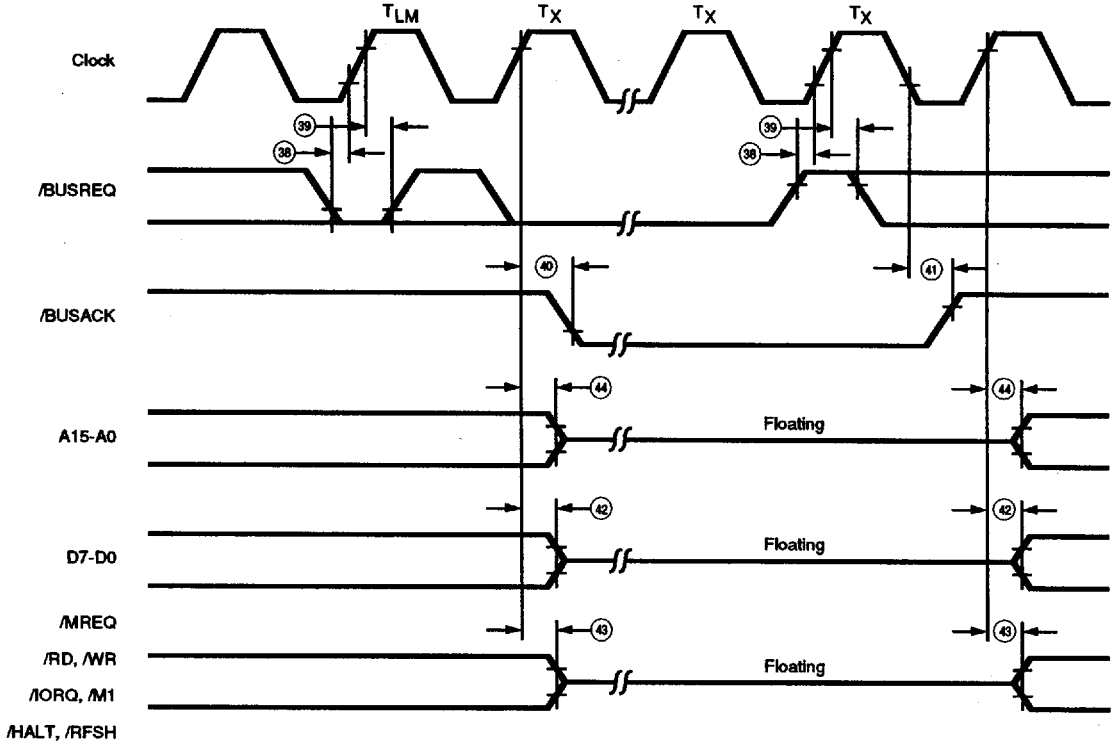


* Although /NMI is an asynchronous input, to guarantee its being recognized on the following machine cycle, /NMI's falling edge must occur no later than the rising edge of the clock cycle preceding the last state of any instruction cycle (T_{LI}).

Figure 32. Non-Maskable Interrupt Request Operation
(See Table A)

Bus Request/Acknowledge Cycle

The CPU samples /BUSREQ with the rising edge of the last clock period of any machine cycle (Figure 33). If /BUSREQ is active, the CPU sets its address, data, and /MREQ to a high-impedance state. The /IORQ, /RD and /WR lines are set to an input for on-chip peripheral access from external bus master with the rising edge of the next clock pulse. At that time, any external device can take control of these lines, usually to transfer data between memory and I/O devices.



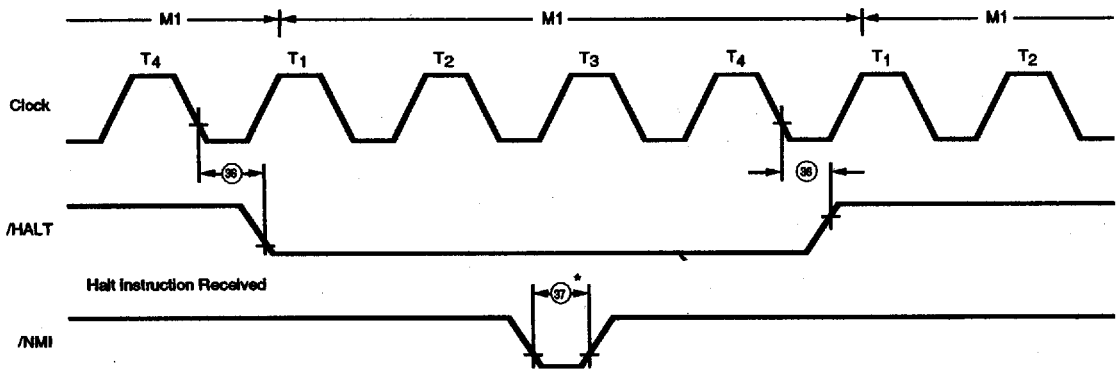
Notes: 1) T_{LM} = Last state of any M cycle

2) T_X = An arbitrary clock cycle used by requesting device

Figure 33. BUS Request/Acknowledge Cycle
(See Table A)

Halt Acknowledge Cycle

Figure 34 shows the timing for the Halt acknowledge cycle.



* Although /NMI is an asynchronous input, to guarantee its being recognized on the following machine cycle, /NMI's falling edge must occur no later than the rising edge of the clock preceding the last state of any instruction cycle (T_{LI}).

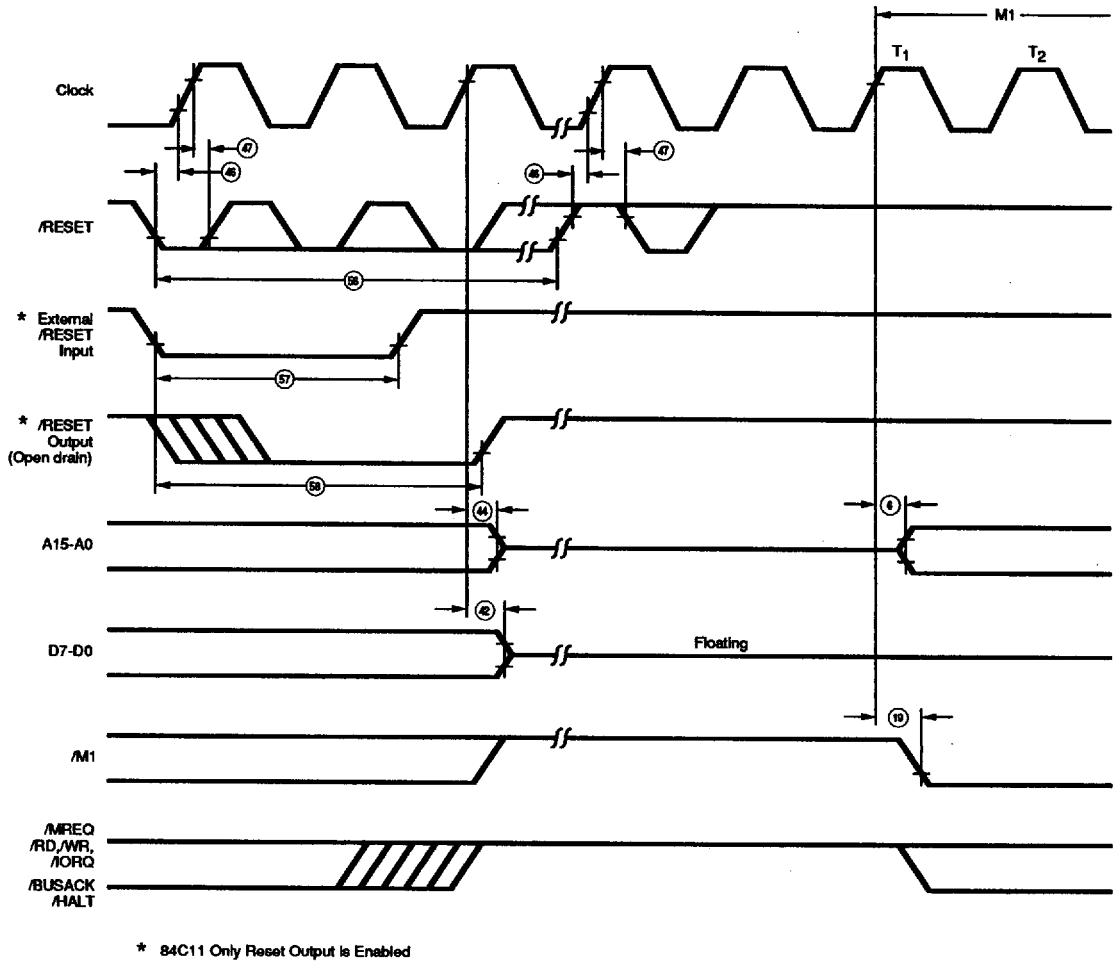
Figure 34. Halt Acknowledge
(See Table A)

Reset Cycle

/RESET must be active for at least three clock cycles for the CPU to properly accept it. As long as /RESET remains active, the address and data buses float, and the control outputs are inactive.

Once /RESET goes inactive, two internal T cycles are consumed before the CPU resumes normal processing operation. /RESET clears the PC register, so the first op-code fetch location is 0000H (Figure 35).

Z84C11 Only. If Reset output is disabled, /RESET must be active for at least three clock cycles for the CPU to properly accept it. Otherwise, /RESET must be active for at least two clock cycles and the on-chip reset circuit extends /RESET signal to at least a minimum of 16 clock cycles.



* 84C11 Only Reset Output is Enabled

Figure 35. Reset Cycle
(See Table A)

CGC Timing

Figures 36-39 show the timing related CGC and Power-on Reset circuits. Idle 2 mode of operation is not supported on the Z84011.

Parameters referenced in Figures 36-39 appear in Table B.

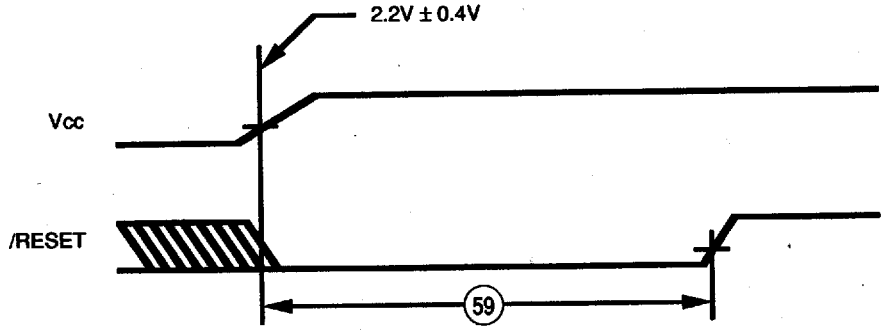


Figure 36. Reset On Power-up
(Applies Only for Z84C11)

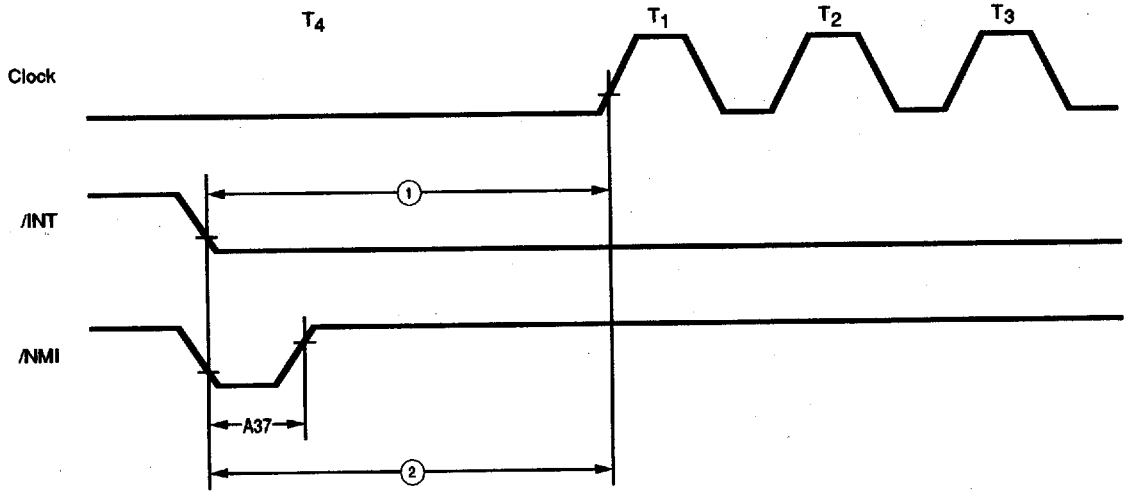
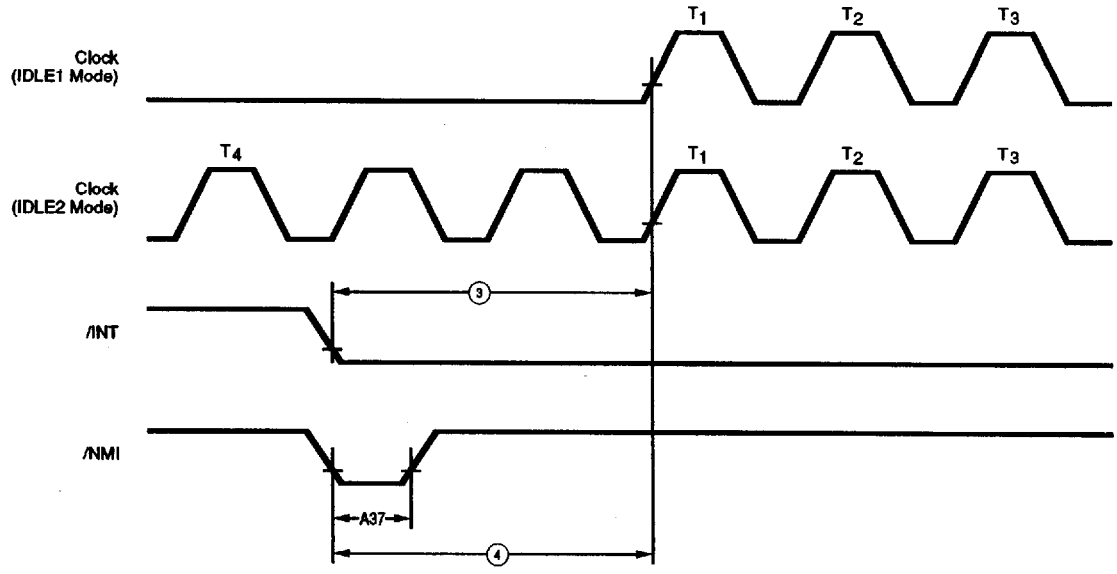
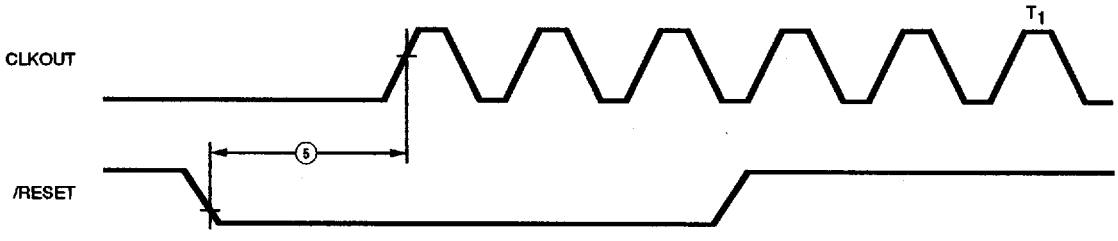


Figure 37. Clock Restart Timing (STOP Mode)
(See Table B)

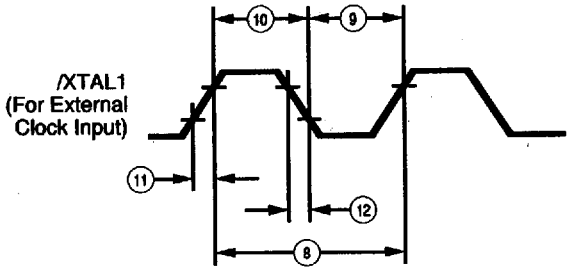


(a) Clock Restart Timing By /INT, /NMI (IDLE1/2 Mode)

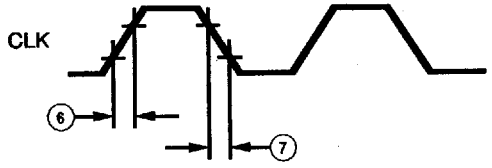


(b) Clock Restart Timing By /RESET (IDLE1/2 Mode)

Figure 38. Clock Restart Timing (IDLE1/2 Mode)
(See Table B)



(a) XTAL1 Timing for External Clock Input

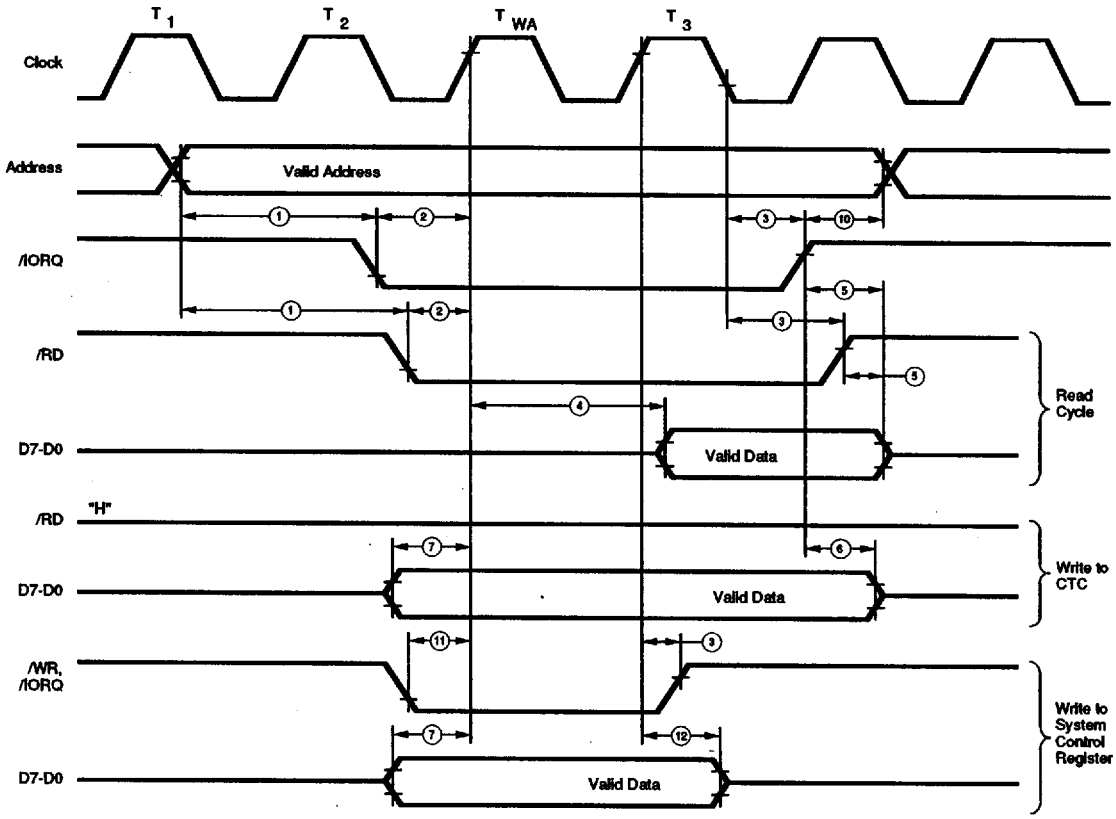


(b) CLK Timing (011 and C11 CLK Pin as Output)

Figure 39. Clock Timing
(See Table B)

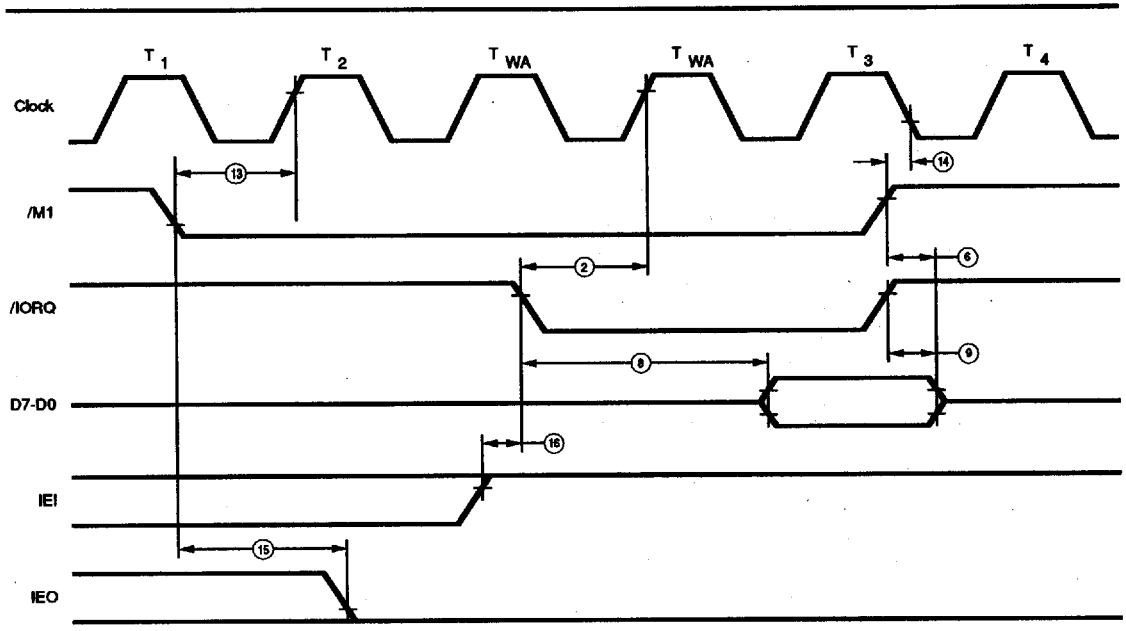
On-chip Peripheral Access From External Bus Master

The timing for the on-chip I/O device access from the external bus master is shown in Figure 40. This timing also applies to the timing during EV mode of operation.



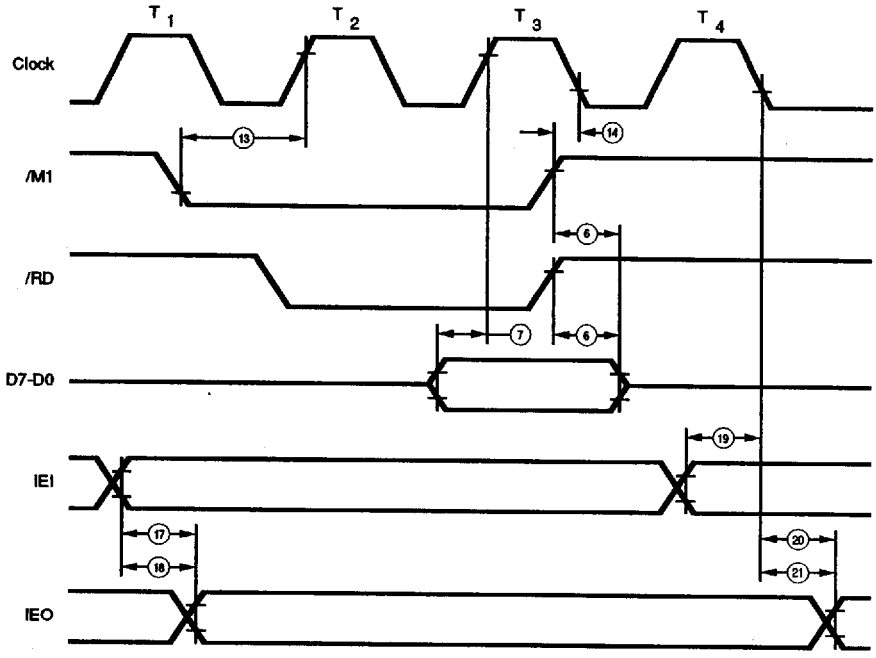
(a) On-chip Peripheral I/O Access From External Bus Master (See Table C)

Figure 40. On-chip Peripheral Timing From External Bus Master



(b) Interrupt Acknowledge Cycle Timing
For On-chip peripheral From External Bus Master
(See Table C)

Figure 40. On-chip Peripheral Timing From External Bus Master (Continued)



(c) Op-code Fetch Cycle Timing for On-chip Peripheral From External Bus Master (See Table C)

Figure 40. On-chip Peripheral Timing From External Bus Master (Continued)

CTC Timing

Figure 41 shows the timing for on-chip CTC.

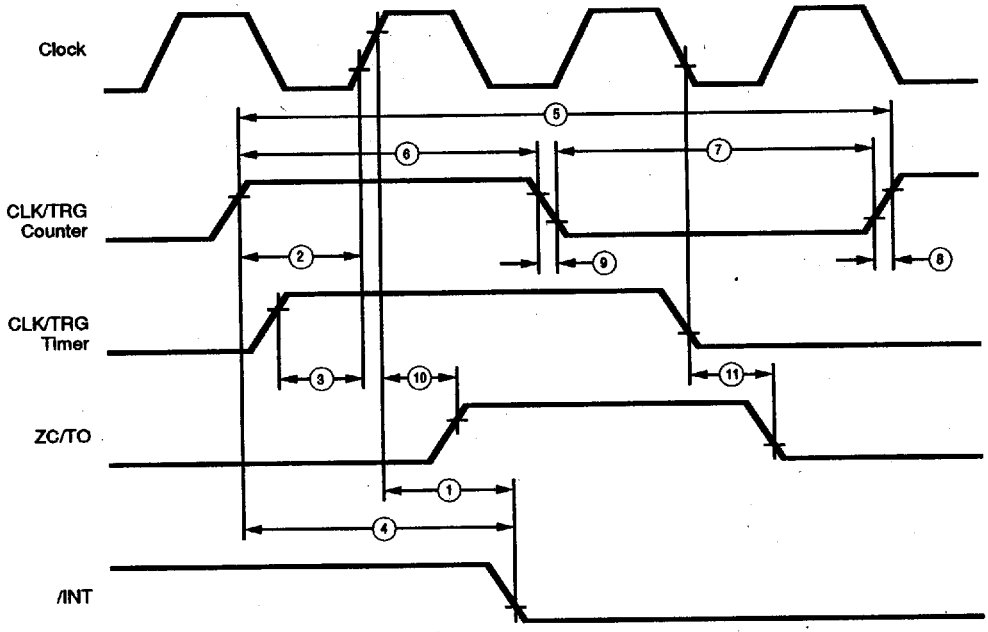
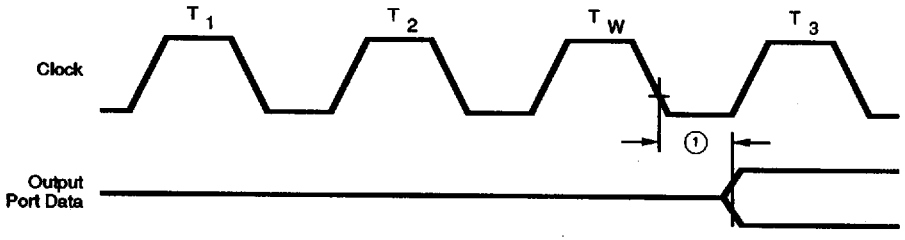


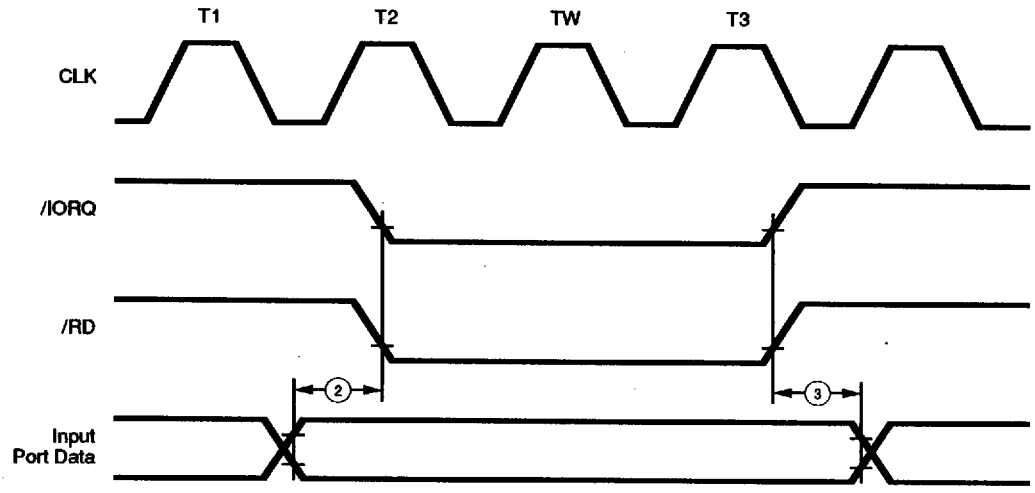
Figure 41. Counter/Timer Timing
(See Table D)

General I/O Port Timing

Figure 42(a) has the Output timing for General I/O port timing while Figure 42(b) has the Input timing.



(a) I/O Port Output Timing
(See Table E)



(b) I/O Port Input Timing
(See Table E)

Figure 42. I/O Port Timing

Watch Dog Timer Timing (Z84C11 Only)

Figure 43 shows the timing for Watch Dog Timer.

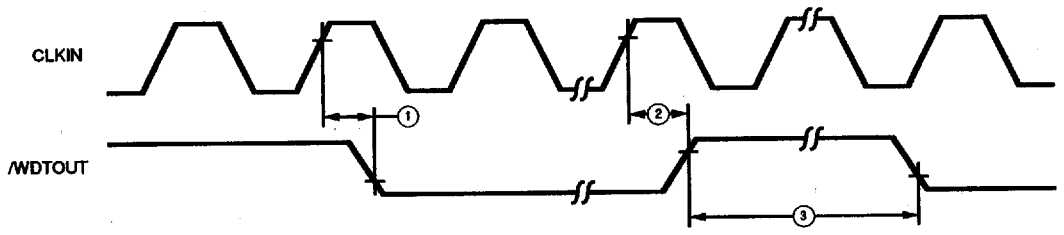


Figure 43. Watch Dog Timer Timing
(See Table F)

Precautions

(1) To release the HALT state by /RESET signal in STOP Mode, hold the /RESET signal at "0" until the output from the internal oscillator stabilizes.

Z84011 Only. To reset MPU, it is necessary to hold /RESET signal input at "0" level for at least three clocks.

Z84C11 Only. If Reset output is disabled, /RESET must be active for at least three clock cycles for the CPU to properly accept it. Otherwise, the on-chip Reset circuit extends /RESET signal to at least a minimum of 16 clock cycles.

(2) Releasing the MPU from the HALT state by an interrupt signal in IDLE1/2 Mode and STOP Mode, does not release the MPU from the HALT state. The internal system clock will stop again unless an interrupt signal is accepted during the execution of a NOP instruction (even when the internal system clock is restarted by the interrupt signal input). Be careful when using /INT.

Other precautions are identical to those for the Z84C00. Refer to the data sheet for the Z84C00.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Voltage on Vcc with respect to Vss .....-0.3V to +7.0V
Voltages on all inputs
with respect to Vss .....-0.3V to Vcc +0.3V

Operating Ambient

Temperature .....See Ordering Information
Storage Temperature .....-65 °C to + 150 °C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The DC Characteristics and capacitance sections below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows into the referenced pin.

Available operating temperature range is:

E = -40°C to 100°C
Voltage Supply Range:
+4.50V ≤ Vcc ≤ + 5.50V

All AC parameters assume a load capacitance of 100 pf. Add 10 ns delay for each 50 pf increase in load up to a maximum of 150 pf for the data bus and 100 pf for address and control lines. AC timing measurements are referenced to 1.5 volts (except for clock, which is referenced to the 10% and 90% points). Maximum capacitive load for CLK is 125 pf.

The Ordering Information section lists temperature ranges and product numbers. Package drawings are in the Package Information section. Refer to the Literature List for additional documentation.

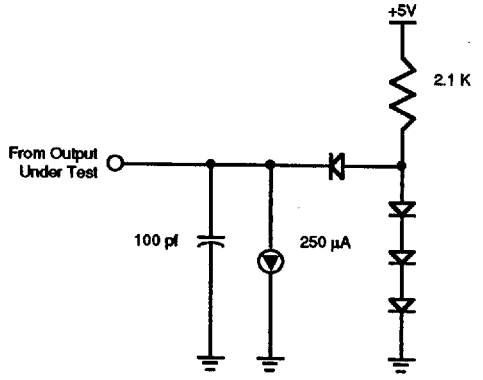


Figure 44. Standard Test Load

CAPACITANCE

Guaranteed by design and characterization.

Symbol	Parameter	Min	Max	Unit
C_{CLOCK}	Clock Capacitance	35	pf	
C_{IN}	Input Capacitance	5	pf	
C_{OUT}	Output Capacitance	15	pf	

DC CHARACTERISTICS

Z84011/Z84C11

V_{CC}=5.0V ±10% unless otherwise specified

Symbol	Parameter	Min	Max	Unit	Condition
V_{OLC}	Clock Output High Voltage	V_{CC}-0.6		V	-2.0mA
V_{OHC}	Clock Output Low Voltage		0.4	V	+2.0mA
V_{IL}	Input High Voltage	2.2	V_{CC}	V	
V_{IH}	Input Low Voltage	-0.3	0.8	V	
V_{OL}	Output Low Voltage		0.4 [5]	V	I_{LO}=2.0mA
V_{OH1}	Output High Voltage	2.4 [4]		V	I_{OH}=-1.6mA
V_{OH2}	Output High Voltage	V_{CC}-0.8 [5]		V	I_{OH}=-250µA
I_{CC1}	Power Supply Current				V_{CC}=5V
	XTALIN=10MHz		TBD	mA	V_{IH}=V_{CC}-0.2V
	XTALIN= 6MHz		30	mA	V_{IL}=0.2V
I_{CC2}	Power Supply Current (STOP Mode)		50	µA	V_{CC}=5V
I_{CC3}	Power Supply Current (IDLE1 Mode)				V_{CC}=5V
	XTALIN=10MHz		TBD	mA	V_{IH}=V_{CC}-0.2V
	XTALIN= 6MHz		4	mA	V_{IL}=0.2V
I_{CC4}	Power Supply Current (IDLE2 Mode; C11 only)				V_{CC}=5V
	XTALIN=10MHz		TBD [1]	mA	V_{IH}=V_{CC}-0.2V
	XTALIN= 6MHz		TBD [1]	mA	V_{IL}=0.2V
I_{LI}	Input Leakage Current	-10	10 [4]	µA	V_{IN}=0.4V to V_{CC}
I_{LO}	Tri-state Output Leakage Current in Float	-10	10 [2]	µA	V_{OUT}=0.4V to V_{CC}
I_{OHD}	CTC ZC/TO Darlington Drive Current	-1.5	-5.0	mA	V_{OH} = 1.5 V
					R_{EXT} = 1.1 K Ω

Notes:

[1] Measurements made with outputs floating

[2] A15-A0, D7-D0, /MREQ, /IORQ, /RD and /WR.

[3] I_{CC2} Standby Current is guaranteed when the halt pin is low in STOP mode

[4] All Pins except XTAL1, where I_{LI} = ±25µA

[5] A15-A0, D7-D0, /MREQ, /IORQ, /RD, /WR, /HALT, /M1 and /BUSACK.

AC CHARACTERISTICS
Z84011/Z84C11

Table A. CPU Timing (Figure 28 to 36)

No	Symbol	Parameter	Z84x1106 Min	Z84x1106 Max	Z84x1110 Min	Z84x1110 Max	Unit	Note
1	TcC	Clock Cycle Time	162**	DC	100**	DC	ns	[A1]
2	TwCh	Clock Pulse Width (high)	65	DC	40	DC	ns	[A1]
3	TwCl	Clock Pulse Width (low)	65	DC	40	DC	ns	[A1]
4	TfC	Clock Fall Time		20		10	ns	[A1]
5	TrC	Clock Rise Time		20		10	ns	[A1]
6	TdCr(A)	Address Valid From Clock Rise		90		65	ns	
7	TdA(MREQf)	Address Valid To /MREQ Fall	35**		5**		ns	
8	TdCf(MREQf)	Clock Fall To /MREQ Fall Delay		70		55	ns	
9	TdCr(MREQr)	Clock Rise To /MREQ Rise Delay		70		55	ns	
10	TwMREQh	/MREQ Pulse Width (high)	65**		30**		ns	[A2]
11	TwMREQl	/MREQ Pulse Width (low)	132**		75**		ns	[A2]
12	TdCf(MERQr)	Clock Fall To /MREQ Rise Delay		70		55	ns	
13	TdCf(RDf)	Clock Fall To /RD Fall Delay		80		65	ns	
14	TdCr(RDr)	Clock Rise To /RD Rise Delay		70		55	ns	
15	TsD(Cr)	Data Setup Time To Clock Rise	30		25		ns	
16	ThD(RDr)	Data Hold Time After /RD Rise	0		0		ns	
17	TsWAIT(Cf)	/WAIT Setup Time To Clock Fall	60		20		ns	
18	ThWAIT(Cf)	/WAIT Hold Time After Clock Fall	10		10		ns	
19	TdCr(M1f)	Clock Rise To /M1 Fall Delay		80		65	ns	
20	TdCr(M1r)	Clock Rise To /M1 Rise Delay		80		65	ns	
21	TdCr(RFSHf)	Clock Rise To /RFSH Fall Delay		110		80	ns	
22	TdCr(RFSHr)	Clock Rise To /RFSH Rise Delay		100		80	ns	
23	TdCf(RDr)	Clock Fall To /RD Rise Delay		70		55	ns	
24	TdCr(RDf)	Clock Rise To /RD Fall Delay		70		55	ns	
25	TsD(Cf)	Data Setup To Clock Fall During M2, M3, M4 Or M5 Cycles	40		25		ns	
26	TdA(IORQf)	Address Stable Prior To /IORQ Fall	107**		50**		ns	
27	TdCr(IORQf)	Clock Rise To /IORQ Fall Delay		65		50	ns	
28	TdCf(IORQr)	Clock Fall To /IORQ Rise Delay		70		55	ns	
29	TdD(WRf)Mw	Data Stable Prior To /WR Fall	22**		40**		ns	
30	TdCf(WRf)	Clock Fall To /WR Fall Delay		70		55	ns	
31	TwWR	/WR Pulse Width	132**		75**		ns	
32	TdCf(WRr)	Clock Fall To /WR Rise Delay		70		55	ns	
33	TdD(WRf)IO	Data Stable Prior To /WR Fall	-55**		-10**		ns	
34	TdCr(WRf)	Clock Rise To /WR Fall Delay		60		50	ns	
35	TdWRr(D)	Data Stable From /WR Rise	30**		10**		ns	
36	TdCf(HALT)	Clock Fall to /HALT '0' or '1'		260		90	ns	
37	TwNMI	/MNI Pulse Width	60		60		ns	
38	TsBUSREQ (Cr)	/BUSREQ Setup Time To Clock Rise	50		30		ns	

AC CHARACTERISTICS (Continued)
Z84011/Z84C11

Table A. CPU Timing (Figure 28 to 36) (Continued)

No	Symbol	Parameter	Z84x1106 Min	Z84x1106 Max	Z84x1110 Min	Z84x1110 Max	Unit	Note
39	ThBUSREQ (Cr)	/BUSREQ Hold Time After Clock Rise	10		10		ns	
40	TdCr (BUSACKf)	Clock Rise To /BASACK Fall Delay		90		75	ns	
41	TdCf (BUSACKr)	Clock Fall To /BASACK Rise Delay		90		75	ns	
42	TdCr(Dz)	Clock Rise To Data Float Delay		80		65	ns	
43	TdCr(CTz)	Clock Rise To Control Outputs Float Delay (/MREQ, /IORQ, /RD And /WR)		70		65	ns	
44	TdCr(Az)	Clock Rise To Address Float Delay		80		75	ns	
45	TdCTr(A)	Address Hold Time From /MREQ, /IORQ, /RD Or /WR	35**		20**		ns	
46	TsRESET(Cr)	/RESET To Clock Rise Setup Time	60		40		ns	
47	ThRESET(Cr)	/RESET To Clock Rise Hold Time	10		10		ns	
48	TsINTf(Cr)	/INT Fall To Clock Rise Setup Time	70		50		ns	
49	ThINTr(Cr)	/INT Rise To Clock Rise Hold Time	10		10		ns	
50	TdM1f (IORQf)	/M1 Fall To /IORQ Fall Delay	359**		220**		ns	
51	TdCf(IORQf)	Clock Fall To /IORQ Fall Delay		70		55	ns	
52	TdCf(IORQr)	Clock Rise To /IORQ Rise Delay		70		55	ns	
53	TdCf(D)	Clock Fall To Data Valid Delay		130		110	ns	
54	TRDf(D)	/RD Fall To Output Data Valid		TBD		60	ns	
55	TMI(D)	/IORQ Fall To Output Data Valid		TBD		70	ns	
56	TwRESET	/RESET Pulse Width 011, Or C11 With RESET Output Disabled	3TcC		3TcC		ns	[A3]
57	TwRESEToe	/RESET Pulse Width C11 Only; RESET Output Enabled	2TcC		2TcC		ns	[A3]
58	TwRESETdo	/RESET Drive Duration C11 Only; RESET Output Enabled	16TcC		16TcC		ns	[A3]
59	TwRESETpor	/RESET Drive Duration On Power-On Sequence (C11 Only)	25	75	25	75	ms	[A3]

Note for Table A.
** For clock period other than the minimum shown, calculate parameters using the formula on Footnotes to Table A.

[A1] These parameters apply to C11 and the external Clock input on CLK pin.
For cases where external Clock is fed from XTAL1, please refer to Table B.
[A2] For loading ≥ 50pf. Decrease width by 10nS for each additional 50pf.
[A3] Apply to Z84C11 only.

Footnotes to Table A

Number	Symbol	General Parameter	Z84x1106	Z84x1110
1	TcC	TwCh + TwCl + TrC + TfC		
7	TdA(MREQf)	TwCh + TfC	-50	-45
10	TwMREQh	TwCh + TfC	-20	-20
11	TwMREQl	TcC	-30	-25
26	TdA(IORQf)	TcC	-55	-50
29	TdD(WRf)	TcC	-140	-60
31	TwWR	TcC	-30	-25
33	TdD(WRf)	TwCl + TrC	-140	-60
35	TdWRr(D)	TwCl + TrC	-55	-40
45	TdCTr(A)	TwCl + TrC	-50	-30
50	TdM1f(IORQf)	2TcC + TwCh + TfC	-50	-30

AC CHARACTERISTICS (Continued)
Z84011/Z84C11

Table B. CGC Timing (Figure 36 to 39)

No	Symbol	Parameter	Z84x1106 Min	Z84x1106 Max	Z84X1110 Min	Z84X1110 Max	Unit	Note
1	TRST(INT)S	Clock Restart Time By /INT (STOP Mode)	(Typ) $(2^{14}+2.5)$ TcC		(Typ) $(2^{14}+2.5)$ TcC		ns	
2	TRST(MNI)S	Clock Restart Time By /NMI (STOP Mode)	(Typ) $(2^{14}+2.5)$ TcC		(Typ) $(2^{14}+2.5)$ TcC		ns	
3	TRST(INT)I	Clock Restart Time By /INT (IDLE Mode)	(Typ) 2.5TcT		(Typ) 2.5TcT		ns	
4	TRST(MNI)I	Clock Restart Time By /NMI (IDLE Mode)	(Typ) 2.5TcT		(Typ) 2.5TcT		ns	
5	TRST (RESET)I	Clock Restart Time By /RESET (IDLE Mode)	(Typ)1TcC		(Typ)1TcC		ns	
6	TfCLKOUT	CLK Rise Time		15		10	ns	[B1]
7	TrCLKOUT	CLK Fall Time		15		10	ns	[B1]
8	TcX1	XTAL1 Cycle Time (For External Clock Input On XTAL1)						
		Divide-By-Two Mode	81		50		ns	
		Divide-By-One Mode (C11 Only)	162		100		ns	[B2]
9	TwlX1	XTAL1 Low Pulse Width (For External Clock Input On XTAL1)						
		Divide-By-Two Mode	35		20		ns	
		Divide-By-One Mode (C11 Only)	65		40		ns	[B2]
10	TwhX1	XTAL1 High Pulse Width (For External Clock Input On XTAL1)						
		Divide-By-Two Mode	35		20		ns	
		Divide-By-One Mode (C11 Only)	65		40		ns	
11	TrX1	XTAL1 Rise Time (For External Clock Input On XTAL1)		25		25	ns	[B3]
12	TfX1	XTAL1 Fall Time (For External Clock Input On XTAL1)		25		25	ns	[B3]

Note for Table B.
[B1] These parameters apply for 011 CLK pin (as System Clock Output), and C11 when the CLK pin outputs the system clock.
[B2] Not appliable to Z84011
[B3] If the parameters B8 and B9 are not met, adjust parameters B11 and B12 to satisfy parameters 8 and 9.

Table C. Timing for On-chip Peripheral Access from External Bus Master and Daisy Chain Timing (See Figure 40)

No	Symbol	Parameter	Z84x1106 Min	Z84x1106 Max	Z84X1110 Min	Z84X1110 Max	Unit	Note
1	TsA(Rlf)	Address Setup Time To /RD, /IORQ Fall	50		40		ns	
2	TsRl(Cr)	/RD, /IORQ Rise To Clock Rise Setup	60		50		ns	
3	Th	Hold Time For Specified Setup	15		15		ns	
4	TdCr(DO)	Clock Rise To Data Out Delay		100		80	ns	
5	TdRlr(DOz)	/RD, /IORQ Rise To Data Out Float Delay		75		60	ns	
6	ThRDr(D)	/M1, /RD, /IORQ Rise To Data Hold	15	40	15	30	ns	[C1]
7	TsD(Cr)	Data In to Clock Rise Setup Time	30		25		ns	
8	TdIOf(DOI)	/IORQ Fall To Data Out Delay (INTACK Cycle)		95		95	ns	
9	ThIOr(D)	/IORQ Rise To Data Hold	15		15		ns	
10	ThIOr(A)	/IORQ Rise To Address Hold	15		15		ns	
11	ThWlf(Cr)	/IORQ, /WR Setup Time To Clock Rise	20		20		ns	[C2]
12	ThWRr(Cr)	Clock Rise To /IORQ, /WR Rise Hold Time	0		0		ns	[C2]
13	TsM1f(Cr)	/M1 Fall To Clock Rise Setup Time	40		40		ns	
14	TsM1r(Cf)	/M1 Rise To Clock Rise Setup Time (/M1 Cycle)	-15		-15		ns	
15	TdM1f(IEOf)	/M1 Fall To IEO Fall Delay (Interrupt Immediately Preceding /M1 Fall)		130		70	ns	
16	TsIEl(IOf)	IEI To /IORQ Fall Setup Time (INTACK Cycle)	100		70	nS		
17	TdIElf(IEOf)	IEI Fall To IEO Fall Delay		100		70	ns	
18	TdIElr(IEOr)	IEI Rise To IEO Rise Delay (After ED Decode)		110		70	ns	
19	TsIEl(Cr)	IEI to Clock Fall Setup (For 4D Decode)		160		150	ns	
20	TdCf(IEOr)	Clock Fall To IEO Rise Delay	50		40		ns	
21	TdCf(IEOf)	Clock Fall To IEO Rise Delay		90		75	ns	

Note to Table C.
[C1] For I/O write to CTC.
[C2] For I/O Write to system control registers.

AC CHARACTERISTICS (Continued)
Z84011/Z84C11

Table D. CTC Timing (Figure 42)

No	Symbol	Parameter	Z84x1106 Min	Z84x1106 Max	Z84X1110 Min	Z84X1110 Max	Unit	Note
1	TdCr(INTf)	Clock Rise To /INT Fall Delay		(TcC+100)		(TcC+80)	ns	[D1]
2	TsCTRr (Cr)c	CLK/TRG Rise To Clock Rise Setup Time For Immediate Count	90		90		ns	[D2]
3	TsCTR(Ct)	CLK/TRG Rise To Clock Rise Setup Time For Enabling Of Prescaler On Following Clock Rise	90		90		ns	[D1]
4	TdCTRr (INTf)	CLK/TRG Rise To /INT Fall Delay TsCTR(C) Satisfied TsCTR(C) Not Satisfied		 (1)+(2) TcC + (1)+(2)		 (1)+(2) TcC + (1)+(2)	 ns ns	 [D2] [D2]
5	TcCTR	CLK/TRG Cycle Time	(2TcC)	DC	(2TcC)	DC	ns	[D3]
6	TwCTRh	CLK/TRG Width (low)	90	DC	90	DC	ns	
7	TwCTRl	CLK/TRG Width (high)	90	DC	90	DC	ns	
8	TrCTR	CLK/TRG Rise Time		30		30	ns	
9	TfCTR	CLK/TRG Fall Time		30		30	ns	
10	TdCr(ZCr)	Clock Rise To ZC/TO Rise Delay		80		80	ns	
11	TdCf(ZCf)	Clock Fall To ZC/TO Fall Delay		80		80	ns	

Notes for Table D.
[D1] Timer Mode
[D2] Counter Mode
[D3] Counter Mode Only; When using a cycle time less than 3TcC, parameter D2 must be met.

Table E. General Purpose I/O Port Timing (Figure 43)

No	Symbol	Parameter	Z84x1106 Min	Z84x1106 Max	Z84X1110 Min	Z84X1110 Max	Unit	Note
1	TdCf(Pout)	Clock Fall to Port Data Valid Delay		300		300	ns	
2	TsPin (IORDf)	Port Data to /IORQ and /RD Fall Setup Time	0		0		ns	
3	ThPin	Port Input to /IORQ and /RD Fall Hold Time	0		0		ns	

Table F. Watchdog Timer Timing (C11 Only; Figure 44)

No	Symbol	Parameter	Z84x1106 Min	Z84x1106 Max	Z84X1110 Min	Z84X1110 Max	Unit	Note
1	TdC(WDTf)	Clock Rise To /WDTOUT Fall Delay		160		160	ns	
2	TwPl	Clock Rise To /WDTOUT Rise Delay		165		165	ns	
3	TcWDT	/WDTOUT Cycle Time						
		WDTP = 00	(Typ) 2^{16}TcC		(Typ) 2^{16}TcC		ns	
		WDTP = 01	(Typ) 2^{18}TcC		(Typ) 2^{18}TcC		ns	
		WDTP = 10	(Typ) 2^{20}TcC		(Typ) 2^{20}TcC		ns	
		WDTP = 11	(Typ) 2^{22}TcC		(Typ) 2^{22}TcC		ns	