Description

The μPD72067 Floppy-Disk Controller (FDC) is a CMOS device that integrates onto a single chip the peripheral logic necessary for todays's high-performance, low-power designs. It maintains complete microcode compatibility with the NEC μPD765 and μPD72065 devices, long established as the industry standard for floppy-disk control.

The μPD72067 incorporates on-chip clock generation/switching, selectable write precompensation, and all the circuitry required for directly interfacing four floppy- disk drives.

An internal high-performance digital phase-locked loop (DPLL) enables reliable data separation at data transfer rates up to 500 kb/s.

Features

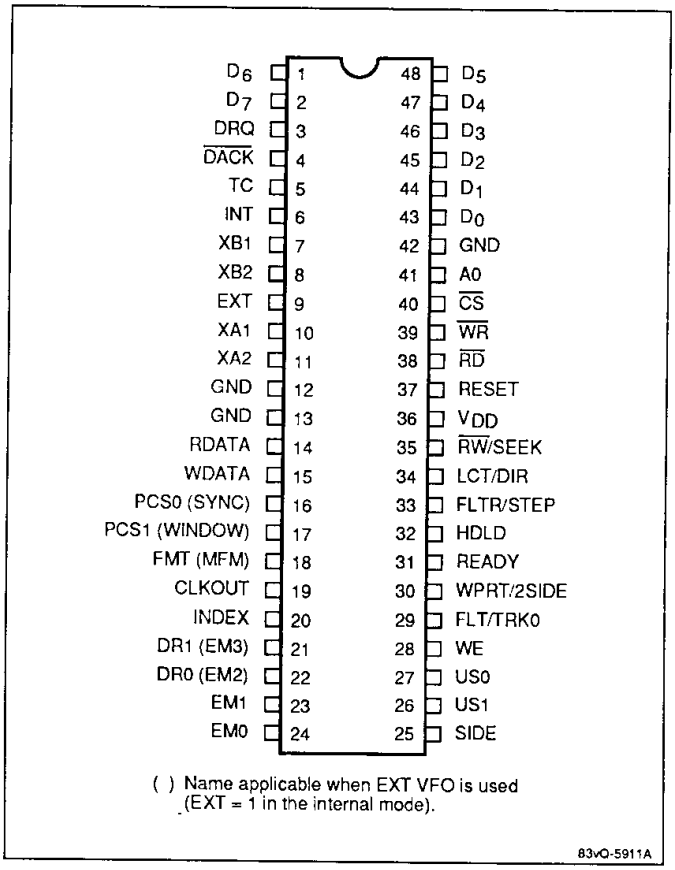
- Command compatible with μPD765A, 765A-2, 765B, 7265, 72065, 72065B, 72066
- IBM diskette compatible
  - — Single-sided, 128/256/512 bytes/sector
  - — Double-sided, 256 bytes/sector
  - — Double-sided, double-density, 256/1024 bytes/sector
- ECMA/ISO minifloppy-disk format compatible
  - — ECMA66 (ISO/TC 97/SC11 N419), single-sided, single-density, 256 bytes/sector
  - — ECMA70 (ISO/TC 97/SC11 N475), double-sided, double-density, 256 bytes/sector
- Data transfer rates: 125, 150, 250, 300, 500 kb/s
- Standby function
- On-chip peripheral circuits
  - — VFO (DPLL) for window signal generation
  - — Write precompensation
  - — System clock generator
  - — Write clock generator
- External VFO (such as μPD71065/71066) can be connected
- Spindle motor control
- FM, MFM control (specified in each command)
- Variable record length: 128, 256, 512, 1024, 2048, 4096, or 8192 bytes/sector
- Multisector and multitrack functions
- Controls up to four FDDs
- Mixed floppy-disks: single- and double-sided, single- and double-density
- Simultaneous seek operation on four FDDs
- Intermediate or incomplete sector read/write can be specified (FM, 128 bytes/sector)
- Internal CRC generation and check ($x^{16} + x^{12} + x^5 + 1$)
- Stepping speed programmable
- Head load and unlead times programmable
- Data scan function: detection of sector satisfying equal-to, greater-than, or less-than condition with main memory data)
- DMA or non-DMA (interrupt) data transfer
- CMOS
- Single +5-volt power supply

Ordering Information

Part Number	Package
μPD72067C	48-pin plastic DIP (600 mil)
μPD72067GC-3B6	52-pin plastic miniflat
μPD72067L	52-pin PLCC (plastic leaded chip carrier)

Pin Configurations

48-Pin Plastic DIP (600 mil)



( ) Name applicable when EXT VFO is used (EXT = 1 in the internal mode).

83vQ-5911A

50075

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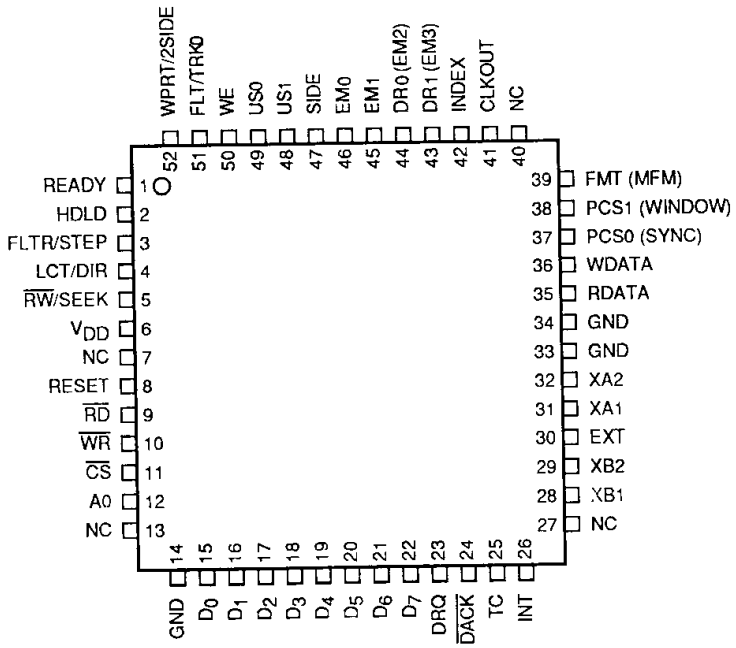
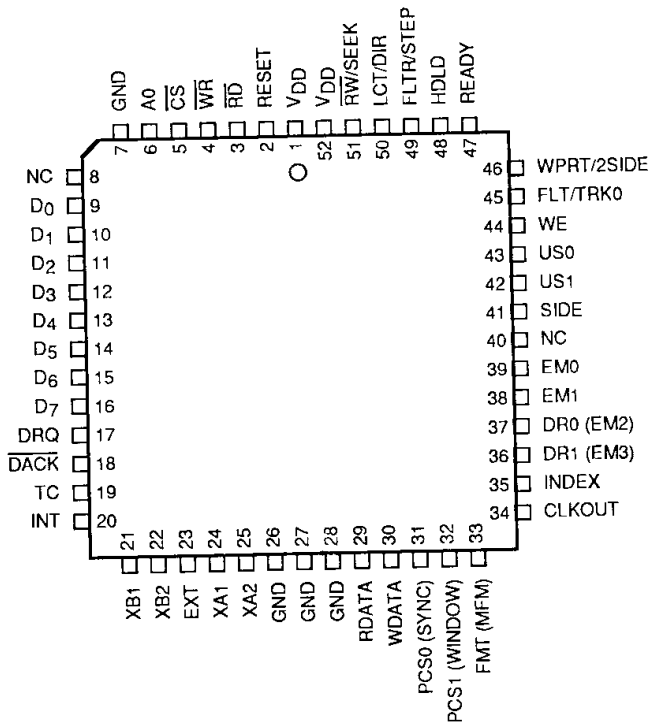
52-Pin Plastic Miniflat



( ) Name applicable when EXT VFO is used
(EXT = 1 in the internal mode)

83vQ-5918B

52-Pin PLCC



( ) Name applicable when EXT VFO is used
(EXT = 1 in the internal mode)

83vQ-5917B

Pin Identification

Symbol	I/O	Signal Function
A0	In	Address 0. Selects μPD72067 registers via address bus. A0 Registers 0 Status or auxiliary command 1 Data
CLKOUT	Out	When EXT = 1, supplies clock required by a μPD71065/71066 used as an external VFO. DR1 CLKOUT 0 16 MHz 1 19.2 MHz Note: CLKOUT goes low when EXT = 0.
$\overline{CS}$	In	Chip Select. Validates $\overline{RD}$ and $\overline{WR}$ signals.
D_0-D_7	I/O	Bidirectional, three-state data bus.
$\overline{DACK}$	In	DMA Acknowledge. Enables DMA cycle.
DR0, DR1	In	Data Rate. Sets data transfer rate in external mode.
(EM2, EM3)	Out	Enable Motor. Controls spindle motor in internal mode.
DRQ	Out	DMA Request. Requests data transfer in DMA mode.
EM0, EM1	Out	Enable Motor. Controls spindle motor.
EXT	In	External VFO. Selects VFO in internal mode. EXT VFO 0 Internal 1 External In external mode, the input to EXT is not significant.
FLTR/STEP	Out	FLTR (Fault Reset). When $\overline{RW}$/SEEK is set to 0, FLTR releases the drive fault state. STEP. When $\overline{RW}$/SEEK is set to 1, STEP generates seek pulses
FLT/TRK0	In	FLT (Fault). When $\overline{RW}$/SEEK is set to 0, FLT indicates whether the drive is in fault state or not. RK0 (Track 0). When $\overline{RW}$/SEEK is set to 1, TRK0 indicates whether the read/write head is positioned at cylinder 0 or not.
FMT	In	Format. Selects format in external mode. FMT Format 0 IBM 1 ECMA
(MFM)	Out	MFM Mode. In internal mode, format is specified by the SELECT FORMAT command. The MFM output signal specifies the VFO circuit operation mode. MFM Mode 0 FM 1 MFM
HDLD	Out	Head Load. Causes read/write head to contact the diskette.

Symbol	I/O	Signal Function
INDEX	In	Indicates read/write head is positioned at the physical starting point of the track on the medium.
INT	Out	Interrupt Request. Requests main system to process the transfer data and execution results.
LCT/DIR	Out	LCT (Low Current). When $\overline{RW}$/SEEK signal is set to 0, LCT indicates the read/write head selects the 43rd or later cylinder. DIR (Direction). When $\overline{RW}$/SEEK signal is set to 1, DIR specifies the seek direction. DIR Direction 0 Outer 1 Inner
PCS0	In	Precompensation. In external mode, PCS0 determines the amount of precompensation.
(SYNC)	Out	VFO Synchronize. In internal mode, SYNC indicates the μPD72067 operation mode. SYNC Mode 0 Read operation is inhibited 1 Read operation is being performed This pin should be pulled high or low by resistors if external mode is not used.
PCS1	In	Precompensation. In external mode, PCS1 (with PCS0) determines the amount of precompensation.
(WINDOW)	In	Data Window. In internal mode, the WINDOW signal generated by the VFO circuit samples the $\overline{RDATA}$ bits. The μPD72067 determines whether a bit is clock or data. This pin should be tied directly high or low if external mode is not used.
$\overline{RD}$	In	Read. Causes the main system to read data from the μPD72067 to the data bus.
RDATA	In	Read data (consisting of clock and data bits) from the drive. If both WINDOW and RDATA are not input at the read state, a deadlock state is entered.
READY	In	Indicates the drive is in a ready state.
RESET	In	Places μPD72067 in idle state. • Outputs are low except WDATA is undefined. • In main system, INT and DRQ are low. • D_0-D_7 are in the input state.
$\overline{RW}$/SEEK	Out	Specifies whether certain FDD interface signals are used for read/write or seek. RW/SEEK Signal function 0 Read/write 1 Seek
SIDE	Out	Selects head 0 or head 1 of screen-type drive. SIDE Selected 0 Head 0 1 Head 1
TC	In	Terminal Count. Indicates data transfer termination.

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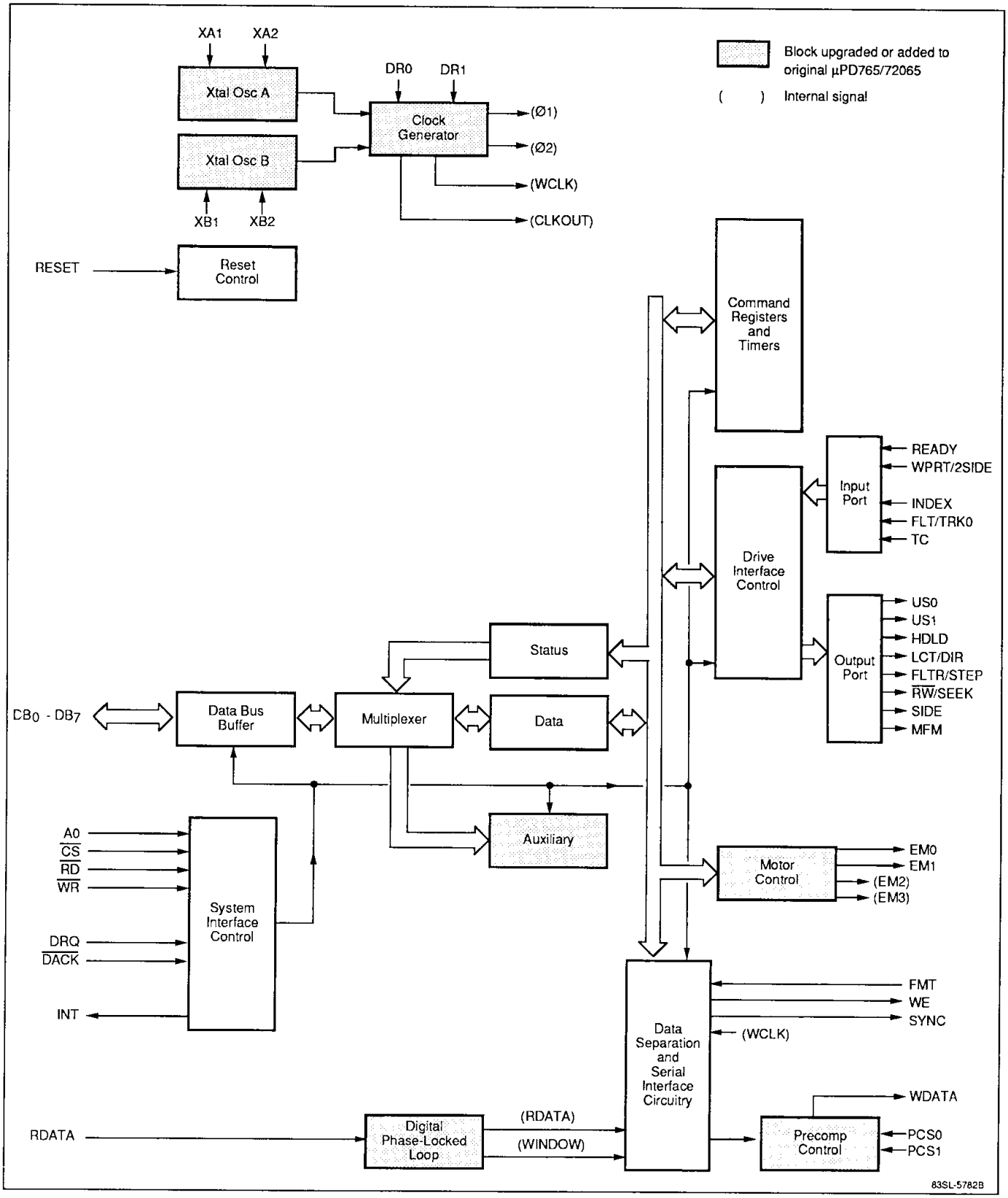
Pin Identification (cont)

Symbol	I/O	Signal Function
US0, US1	Out	Unit Select. One of four FDDs is selected by decoding US0 and US1.
WDATA	Out	Write data (clock and data bits) to FDD.
WE	Out	Write Enable. Requests FDD to write data.
WPRT/2SIDE	In	WPRT (Write Protected). When $\overline{RW}$/SEEK is set to 0, WPRT indicates whether the medium is write-protected. 2SIDE (Two Side). When $\overline{RW}$/SEEK is set to 1, 2SIDE indicates whether the medium is double-sided.
$\overline{WR}$	In	Write. Control signal that allows the main system to read data from the μPD72067 to the data bus.
XA1, XA2	In	Crystal A. To use internal VFO (EXT = 0), connect a 32-MHz quartz crystal resonator to XA1 and XA2. As an alternative, connect a 32-MHz external clock to XA1 and leave XA2 open. To use external VFO (EXT = 1), connect a 16-MHz quartz crystal resonator to XA1 and XA2. As an alternative, connect a 16-MHz external clock to XA1 and leave XA2 open.
XB1, XB2	In	Crystal B. To use the 300-kb/s data transfer rate, connect a 19.2-MHz quartz crystal resonator to XB1 and XB2. As an alternative, connect a 19.2-MHz external clock to XB1 and leave XB2 open.
NC		No Connection
GND		Ground
V_{DD}	In	+5-volt power supply

Note:

The pin symbol in parentheses applies when external VFO is used.

μPD72067 Block Diagram



Absolute Maximum Ratings

T_A = +25°C

Voltage on any pin	−0.5 to +7 V
Operating temperature, T_{OPT}	−10 to +70°C
Storage temperature, T_{STG}	−65 to 150°C

Capacitance

T_A = +25°C; V_{DD} = 0 V; f = 1 MHz

Parameter	Symbol	Min	Max	Unit	Conditions
Clock capacitance	C_ϕ		20	pF	Unmeasured pins returned to 0 V.
Input capacitance	C_{IN}		10	pF	
Output capacitance	C_{OUT}		20	pF	

DC Characteristics

T_A = −10 to +70°C; V_{DD} = +5 V ±10%

Parameter	Symbol	Min	Max	Unit	Conditions
Low-level input voltage	V_{IL}	−0.5	0.8	V	
High-level input voltage	V_{IH}	2.2	V_{DD} + 0.5	V	
Low-level output voltage	V_{OL}		0.45	V	I_{OL} = 2.0 mA
High-level output voltage	V_{OH}	0.7 V_{DD}	V_{DD}	V	I_{OH} = −200 μA
Low-level input leakage current	I_{LIL}		−10	μA	V_{IN} = 0 V
High-level input leakage current	I_{LIH}		+10	μA	V_{IN} = V_{DD}
Low-level output leakage current	I_{LOL}		−10	μA	V_{OUT} = +0.45 V
High-level output leakage current	I_{LOH}		+10	μA	V_{OUT} = V_{DD}
V_{DD} supply current	I_{DD}		60	mA	Note 1
Standby current	I_{DD1}		100	μA	
Oscillator stabilization time	t_{KS}		10	ms	

Notes:

(1) When a 32-MHz crystal is connected to XA1-XA2 or a 19.2-MHz crystal is connected to XB1-XB2.

AC Characteristics 1; Standard Floppy-Disk Control

T_A = −10 to +70°C; V_{DD} = +5 V ±10%;
MFM data transfer rate = 500 kb/s

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Main System Side							
A0, $\overline{CS}$, $\overline{DACK}$ setup time to $\overline{RD}$	2	t_{AR}	0			ns	
A0, $\overline{CS}$, $\overline{DACK}$ hold time from $\overline{RD}$	2	t_{RA}	0			ns	
$\overline{RD}$ pulse width	2	t_{RR}	200			ns	
Data access time from $\overline{RD}$ ↓	2	t_{RD}			140	ns	
Data float delay time from $\overline{RD}$ ↑	2	t_{DF}	10		85	ns	
INT delay time from $\overline{RD}$ ↑	2	t_{RI}			400	ns	Note 1
A0, $\overline{CS}$, $\overline{DACK}$ setup time to $\overline{WR}$	3	t_{AW}	0			ns	
A0, $\overline{CS}$, $\overline{DACK}$ hold time from $\overline{WR}$	3	t_{WA}	0			ns	
$\overline{WR}$ pulse width	3	t_{WW}	200			ns	
Data setup time to $\overline{WR}$	3	t_{DW}	100			ns	
Data hold time from $\overline{WR}$	3	t_{WD}	0			ns	
INT delay time from $\overline{WR}$ ↑	3	t_{WI}			400	ns	Note 1
DRQ cycle time	4	t_{MCY}	13			μs	DR1 = 0, DR0 = 1
$\overline{DACK}$ ↓ response time from DRQ ↑	4	t_{MA}	200			ns	
DRQ delay time from $\overline{DACK}$ ↓	4	t_{AM}			140	ns	
$\overline{DACK}$ pulse width	4	t_{AA}	8			ϕ_{CY}	Note 5
$\overline{RD}$ ↓ response time from DRQ ↑	4	t_{MR}	125			ns	DR1 = 0, DR0 = 1
$\overline{WR}$ ↓ response time from DRQ ↑	4	t_{MW}	250			ns	
$\overline{WR}$/$\overline{RD}$ response time from DRQ ↑	4	t_{MRW}			12	μs	
TC pulse width	4	t_{TC}	60			ns	
RESET pulse width	5	t_{RST}	60			ϕ_{CY}	Note 5

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AC Characteristics 1; Standard Floppy-Disk Control (cont)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Drive Side							
RDATA high-level width	6	t_{RDD}	40			ns	
WINDOW cycle time (Note 2)	6	t_{WCY}		2		μs	MFM = 0
				1		μs	MFM = 1
WINDOW setup time to RDATA (Note 2)	6	t_{WRD}	15			ns	
WINDOW hold time from RDATA (Note 2)	6	t_{RDW}	15			ns	
US0, US1 setup time to SEEK	7	t_{US}	12			μs	Note 3
SEEK setup time to DIR	7	t_{SD}	7			μs	
DIR setup time to STEP	7	t_{DST}	1			μs	
US0, US1 hold time from STEP	7	t_{STU}	5			μs	
STEP high-level width	7	t_{STP}	6	7	8	μs	
US0, US1 hold time from SEEK (Note 4)	7	t_{SU}	15			μs	
SEEK hold time from DIR	7	t_{DS}	30			μs	
DIR hold time from STEP	7	t_{STD}	24			μs	
STEP cycle time	7	t_{SC}	33			μs	
FLTR high-level width	8	t_{FR}	8		10	μs	
INDEX high-level width	8	t_{IDX}	16			ϕ_{CY}	Note 5

Notes:

(1) For data transfer in non-DMA mode.

(2) When external VFO is used.

(3) The minimum value for drive-side parameters is 50 ns less than the value expressed in μs. For example, 12 μs is actually 11.950 μs.

(4) While the unit under test is performing a seek operation, the SENSE DEVICE STATUS command is being executed for the other devices.

(5) The time ϕ_{CY} is a multiple of the period of a quartz crystal resonator connected to pins XA1-XA2 or an external clock connected to pin XA1. The multiple is four (EXT = 0) or two (EXT = 1).

(6) See figure 1 for timing measurement voltage thresholds.

AC Characteristics 2; Minifloppy-Disk Control

T_A = −10 to +70°C; V_{DD} = +5 V ±10%;
MFM data transfer rate = 250 kb/s

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Main System Side							
A0, $\overline{CS}$, $\overline{DACK}$ setup time to $\overline{RD}$	2	t_{AR}	0			ns	
A0, $\overline{CS}$, $\overline{DACK}$ hold time from $\overline{RD}$	2	t_{RA}	0			ns	
$\overline{RD}$ pulse width	2	t_{RR}	200			ns	
Data access time from $\overline{RD}$ ↓	2	t_{RD}			140	ns	
Data float delay time from $\overline{RD}$ ↑	2	t_{DF}	10		85	ns	
INT delay time from $\overline{RD}$ ↑	2	t_{RI}			400	ns	Note 1
A0, $\overline{CS}$, $\overline{DACK}$ setup time to $\overline{WR}$	3	t_{AW}	0			ns	
A0, $\overline{CS}$, $\overline{DACK}$ hold time from $\overline{WR}$	3	t_{WA}	0			ns	
$\overline{WR}$ pulse width	3	t_{WW}	200			ns	
Data setup time to $\overline{WR}$	3	t_{DW}	100			ns	
Data hold time from $\overline{WR}$	3	t_{WD}	0			ns	
INT delay time from $\overline{WR}$ ↑	3	t_{WI}			400	ns	Note 1
DRQ cycle time	4	t_{MCY}	26			μs	DR1 = 0, DR0 = 0
$\overline{DACK}$ ↓ response time from DRQ ↑	4	t_{MA}	400			ns	
DRQ delay time from $\overline{DACK}$ ↓	4	t_{AM}			140	ns	
$\overline{DACK}$ pulse width	4	t_{AA}	8			ϕ_{CY}	Note 5
$\overline{RD}$ ↓ response time from DRQ ↑	4	t_{MR}	250			ns	DR1 = 0, DR0 = 0
$\overline{WR}$ ↓ response time from DRQ ↑	4	t_{MW}	500			ns	
$\overline{WR}$/$\overline{RD}$ response time from DRQ ↑	4	t_{MRW}			24	μs	
TC pulse width	4	t_{TC}	60			ns	
RESET pulse width	5	t_{RST}	60			ϕ_{CY}	Note 5

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AC Characteristics 2; Minifloppy-Disk Control (cont)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Drive Side							
RDATA high-level width	6	t_{RDD}	40			ns	
WINDOW cycle time (Note 2)	6	t_{WCY}		4		μs	MFM = 0
				2		μs	MFM = 1
WINDOW setup time to RDATA (Note 2)	6	t_{WRD}	15			ns	
WINDOW hold time from RDATA (Note 2)	6	t_{RDW}	15			ns	
US0, US1 setup time to SEEK	7	t_{US}	24			μs	Note 3
SEEK setup time to DIR	7	t_{SD}	14			μs	
DIR setup time to STEP	7	t_{DST}	2			μs	
US0, US1 hold time from STEP	7	t_{STU}	10			μs	
STEP high-level width	7	t_{STP}	12	14	16	μs	
US0, US1 hold time from SEEK (Note 4)	7	t_{SU}	30			μs	
DIR hold time from STEP	7	t_{STD}	48			μs	
SEEK hold time from DIR	7	t_{DS}	60			μs	
STEP cycle time	7	t_{SC}	66			μs	
FLTR high-level width	8	t_{FR}	16		20	μs	
INDEX high-level width	8	t_{IDX}	16			ϕ_{CY}	Note 5

Notes:

(1) For data transfer in non-DMA mode.

(2) When external VFO is used.

(3) The minimum value for drive-side parameters is 50 ns less than the value expressed in μs. For example, 12 μs is actually 11.950 μs.

(4) While the unit under test is performing a seek operation, the SENSE DEVICE STATUS command is being executed for the other devices.

(5) ϕ_{CY} is a multiple of the period of a quartz crystal resonator connected to pins XA1-XA2 or an external clock connected to pin XA1. The multiple is eight (EXT = 0) or four (EXT = 1).

(6) See figure 1 for timing measurement voltage thresholds.

AC Characteristics 3; High-Speed Floppy-Disk Control

T_A = −10 to +70°C; V_{DD} = +5 V ±10%;
MFM data transfer rate = 300 kb/s

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Main System Side							
A0, $\overline{CS}$, $\overline{DACK}$ setup time to $\overline{RD}$	2	t_{AR}	0			ns	
A0, $\overline{CS}$, $\overline{DACK}$ hold time from $\overline{RD}$	2	t_{RA}	0			ns	
$\overline{RD}$ pulse width	2	t_{RR}	200			ns	
Data access time from $\overline{RD}$ ↓	2	t_{RD}			140	ns	
Data float delay time from $\overline{RD}$ ↑	2	t_{DF}	10		85	ns	
INT delay time from $\overline{RD}$ ↑	2	t_{RI}			400	ns	Note 1
A0, $\overline{CS}$, $\overline{DACK}$ setup time to $\overline{WR}$	3	t_{AW}	0			ns	
A0, $\overline{CS}$, $\overline{DACK}$ hold time from $\overline{WR}$	3	t_{WA}	0			ns	
$\overline{WR}$ pulse width	3	t_{WW}	200			ns	
Data setup time to $\overline{WR}$	3	t_{DW}	100			ns	
Data hold time from $\overline{WR}$	3	t_{WD}	0			ns	
INT delay time from $\overline{WR}$ ↑	3	t_{WI}			400	ns	Note 1
DRQ cycle time	4	t_{MCY}	21.7			μs	DR1 = 1, DR0 = 1
$\overline{DACK}$ ↓ response time from DRQ ↑	4	t_{MA}	333.3			ns	
DRQ delay time from $\overline{DACK}$ ↓	4	t_{AM}			140	ns	
$\overline{DACK}$ pulse width	4	t_{AA}	8			ϕ_{CY}	Note 5
$\overline{RD}$ ↓ response time from DRQ ↑	4	t_{MR}	208.3			ns	DR1 = 1, DR0 = 1
$\overline{WR}$ ↓ response time from DRQ ↑	4	t_{MW}	416.7			ns	
$\overline{WR}$/$\overline{RD}$ response time from DRQ ↑	4	t_{MRW}			12	μs	
TC pulse width	4	t_{TC}	60			ns	
RESET pulse width	5	t_{RST}	60			ϕ_{CY}	Note 5

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AC Characteristics 3; High-Speed Floppy-Disk Control (cont)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Drive Side							
RDATA high-level width	6	t_{RDD}	40			ns	
WINDOW cycle time (Note 2)	6	t_{WCY}		3.33		μs	MFM = 0
				1.67		μs	MFM = 1
WINDOW setup time to RDATA (Note 2)	6	t_{WRD}	15			ns	
WINDOW hold time from RDATA (Note 2)	6	t_{RDW}	15			ns	
US0, US1 setup time to SEEK	7	t_{US}	20			μs	Note 3
SEEK setup time to DIR	7	t_{SD}	11.7			μs	
DIR setup time to STEP	7	t_{DST}	1.7			μs	
US0, US1 hold time from STEP	7	t_{STU}	8.3			μs	
STEP high-level width	7	t_{STP}	10	11.7	13.3	μs	
US0, US1 hold time from SEEK (Note 4)	7	t_{SU}	25			μs	
DIR hold time from STEP	7	t_{STD}	40			μs	
SEEK hold time from DIR	7	t_{DS}	50			μs	
STEP cycle time	7	t_{SC}	55			μs	
FLTR high-level width	8	t_{FR}	13.3		16.7	μs	
INDEX high-level width	8	t_{IDX}	16			ϕ_{CY}	Note 5

Notes:

(1) For data transfer in non-DMA mode.

(2) When external VFO is used.

(3) The minimum value for drive-side parameters is 50 ns less than the value expressed in μs. For example, 12 μs is actually 11.950 μs.

(4) While the unit under test is performing a seek operation, the SENSE DEVICE STATUS command is being executed for the other devices.

(5) ϕ_{CY} is a multiple of the period of a quartz crystal resonator connected to pins XB1-XB2 or an external clock connected to pin XB1. The multiple is four (EXT = 0) or two (EXT = 1).

(6) See figure 1 for timing measurement voltage thresholds.

Figure 1. Voltage Thresholds for Timing Measurements

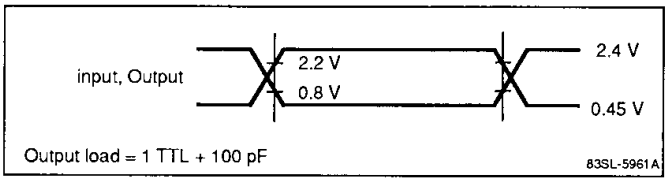

Figure 2. Read Operation

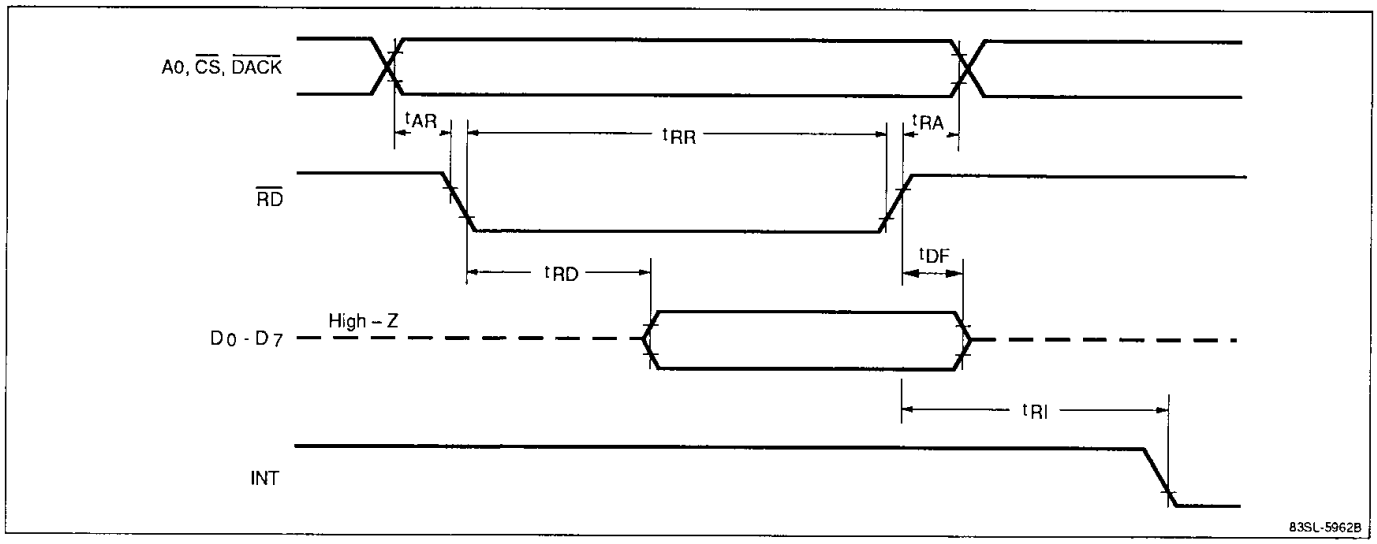

Figure 3. Write Operation

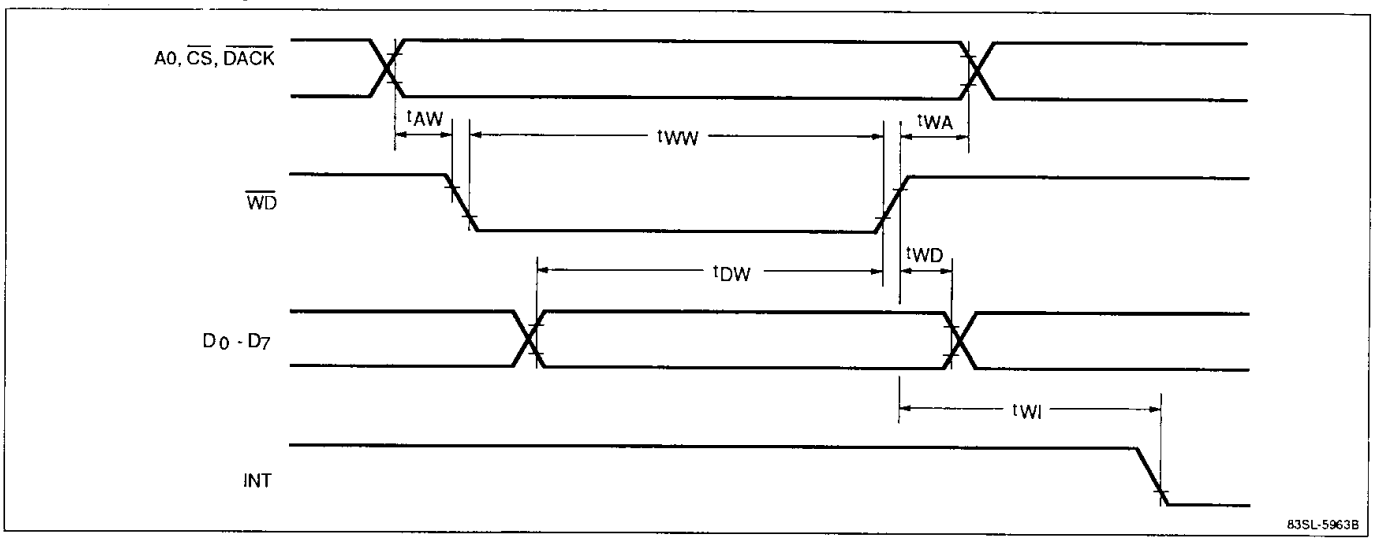

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Figure 4. DMA Operation

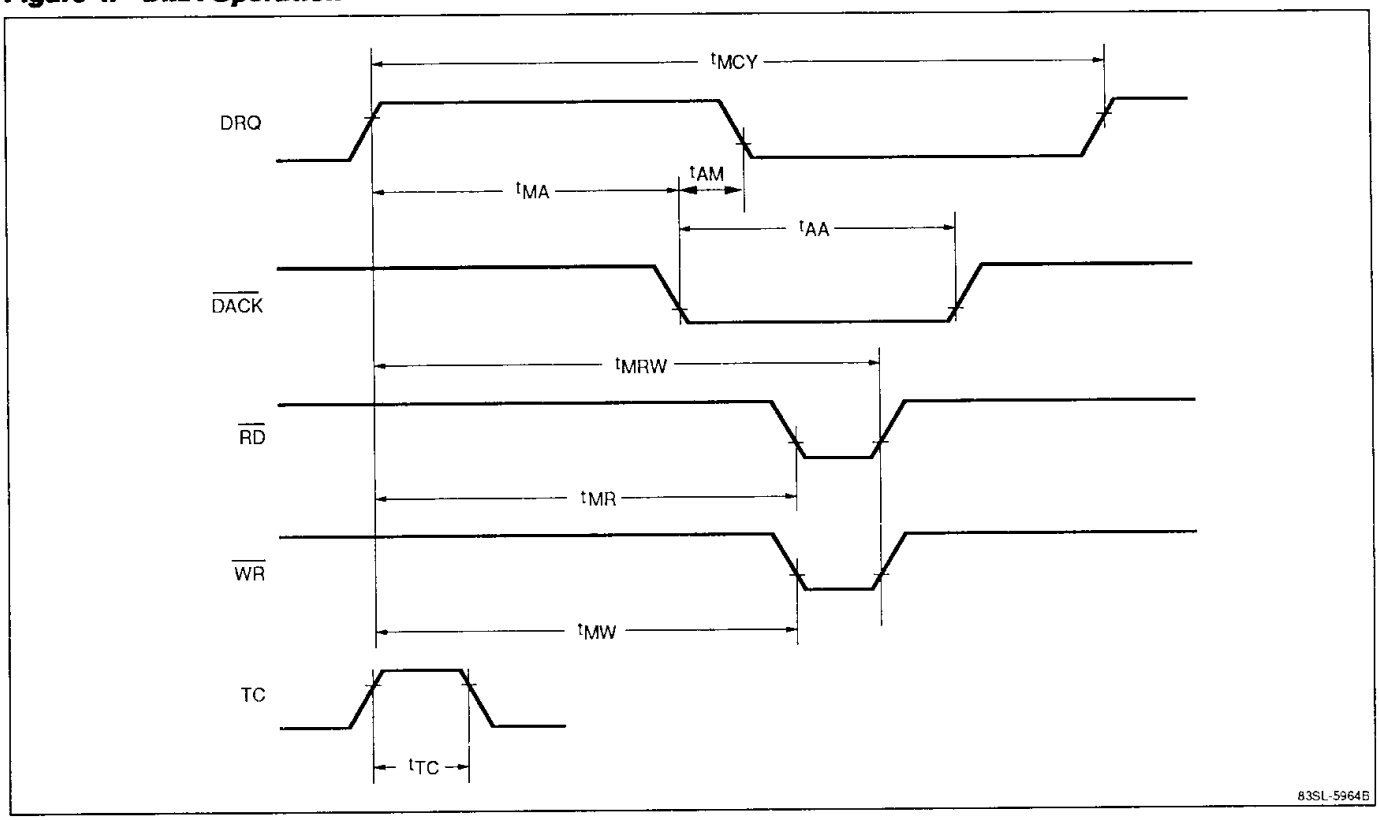


Figure 5. RESET Waveform

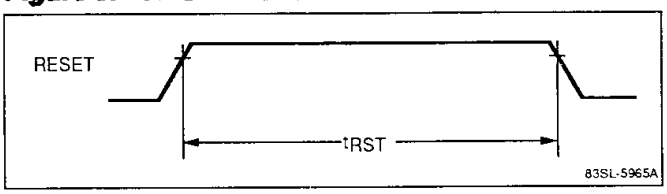


Figure 6. Device Read Operation

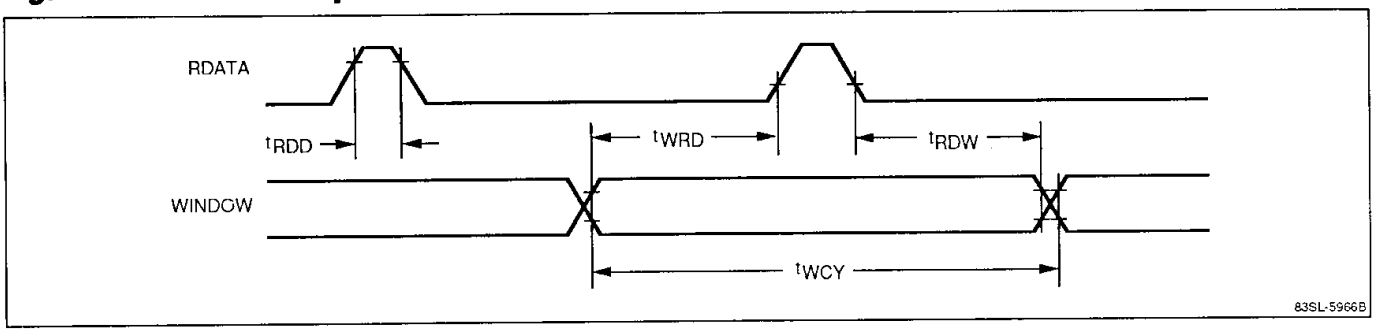


Figure 7. Seek Operation

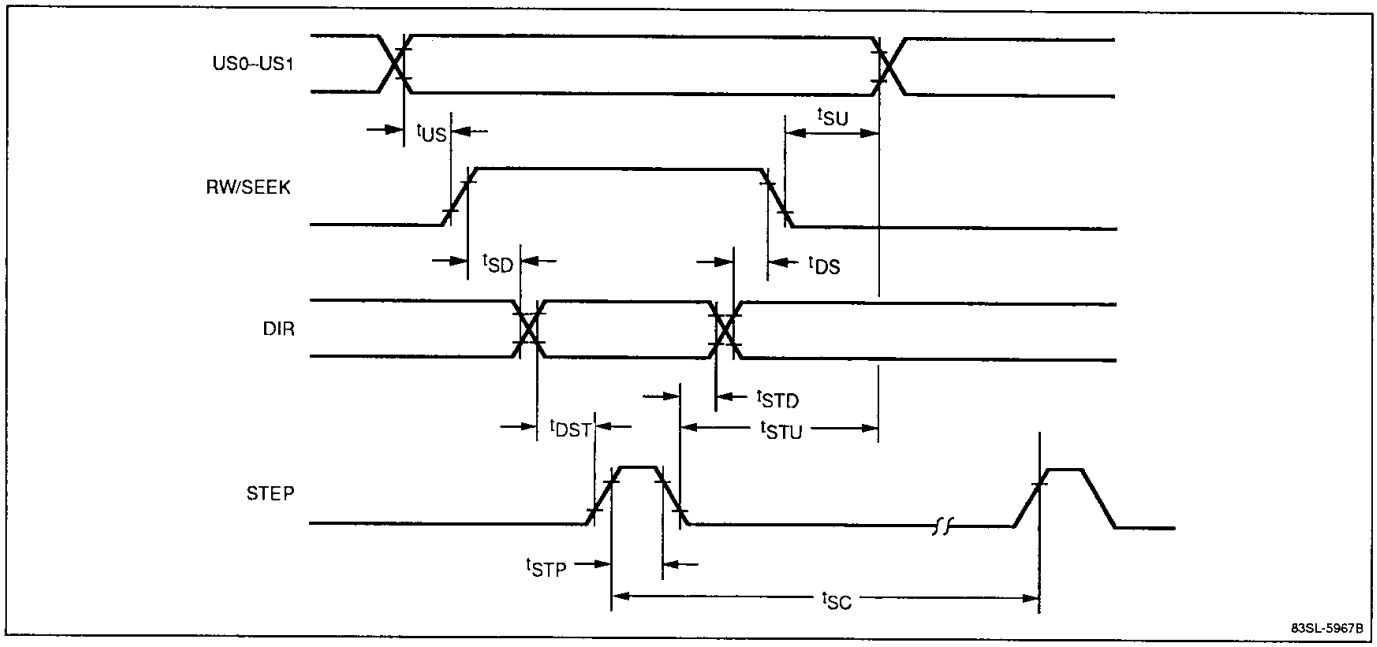
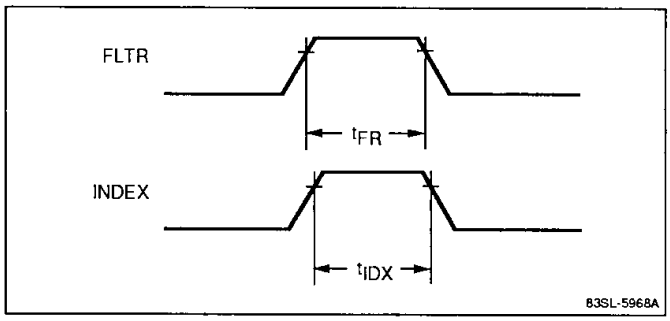


Figure 8. FLTR and INDEX Waveforms



Registers

The μPD72067 contains three 8-bit registers for interfacing the main system—data, status, and auxiliary command. Control signals $\overline{CS}$, A0, $\overline{RD}$, and $\overline{WR}$ select a particular register operation as shown in table 1.

(1) The data register temporarily stores information (command, parameter, data, or result status) transferred between the μPD72067 and the main system.

(2) The status register (table 2) indicates the state of the μPD72067. The main system can read the status register contents at any time.

(3) The auxiliary command register temporarily stores auxiliary commands given the μPD72067.

Table 1. Register Selection

$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	Operation
0	0	0	1	Read status register
0	0	1	0	Write auxiliary command register
0	1	0	1	Read data register
0	1	1	0	Write data register
1	x	x	x	Not defined

x = Don't care

Notes:

(1) When the DACK input is active low, data register selection is independent of $\overline{CS}$ and A0.

(2) When both $\overline{CS}$ and A0 are set to 0, a write of code other than auxiliary command code ($\overline{WR}$ = 0) is inhibited.

5

Table 2. Status Register Contents

Bit	Name	Symbol	Description
D7	Request for master	RQM	Indicates μPD72067 is ready to transfer data to and from the main system. Operation depends on the DIO bit D6. When DIO = 0, the main system sends data to μPD72067. When the main system writes data into μPD72067, RQM is set to 0; when μPD72067 reads the data, RQM is set to 1. • C-phase, wait for command • Non-DMA write E-phase • SEEK type E-phase When DIO = 1, μPD72067 sends data to the main system. When μPD72067 places data in the data register, RQM is set to 1; when the main system reads the data, RQM is set to 0. • R-phase • Non-DMA read E-phase (except for READ ID)
D6	Data input/output	DIO	Indicates the data transfer direction between the main system and μPD72067. DIO Direction 0 Main system to μPD72067 1 μPD72067 to main system
D5	Non-DMA mode	NDM	Indicates data is being transferred in non-DMA mode (E-phase). In C- or R-phase, bit D5 is cleared.
D4	μPD72067 busy	CB	Indicates μPD72067 is in C-phase, R-phase, or read/write command E-phase. (In SEEK type E- phase, the CB bit D4 is not set to 1.) When bit D4 is set to 1, the next command is not acknowledged.
D3	FD3 busy	D3B	Indicates that device 3 performs seek operation or that a seek operation termination interrupt is pending (E-phase).When bit D3 is set to 1, a read/write type command must not be written.
D2	FD2 busy	D2B	Same as bit D3 for device 2.
D1	FD1 busy	D1B	Same as bit D3 for device 1.
D0	FD0 busy	D0B	Same as bit D3 for device 0.

Digital Phase-Locked Loop (DPLL)

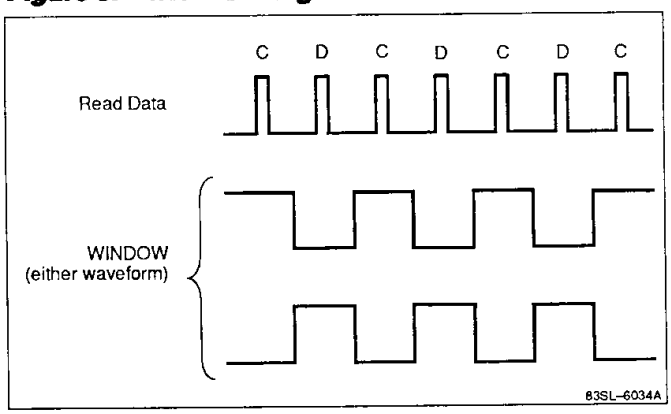
From the external 32-MHz system clock, the DPLL generates a WINDOW signal and synchronizes it with the phase and frequency of read data from a disk drive.

The frequency correction range and peak shift margin of the DPLL are affected by the data transfer rate (pin DR1).

DR1	Range	Margin
0	±25%	81.5
1	±25%	88.6

As shown in figure 9, read data is separated into data bits and clock bits by sampling with the WINDOW signal. The bits are centered in the window. If WINDOW is low for data bits, it is high for clock bits, and vice versa.

Figure 9. WINDOW Signal Waveform



Data Shift Register

In the read mode, the data shift register converts serial data into parallel form and outputs it to the 8-bit internal bus. In the write mode, the process is reversed and serial data is output to the CRC generator/checker and output mixer.

Clock Shift Register

In the read mode, the clock shift register converts serial clock bits into parallel form and outputs them to the 8-bit internal bus. In the write mode, the clock shift register converts parallel clock bits from the internal bus into a serial stream and sends it to the output mixer.

Cyclic Redundancy Check (CRC)

The CRC generator/checker operates with the polynomial $x^{16} + x^{12} + x^5 + 1$. In the read mode, the CRC of read data is calculated and compared with the CRC byte added following sector ID information and data. A mismatch produces an error indication.

In the write mode, CRC is calculated and two CRC bytes are added following ID information and data.

Precompensation

Because of the magnetic chracteristics of the media, read data is shifted from data write timing. Because the shift can be predicted according to the data pattern, it can be compensated by preshifting write data in the opposite direction.

Preshifting is used only for MFM mode, which has a data window half the width of the window in FM mode. The precompensation value (shift) is determined in the external mode by the input signals to pins PCS0 and PCS1, or in the internal mode by bits PS0 and PS1 of the CONTROL INTERNAL MODE command. See table 3.

Table 3. Precompensation Values

DR1	PCS1	PCS0	Shift
0	0	0	0.0
0	0	1	125.0
0	1	0	187.0
0	1	1	250.0
1	0	0	0.0
1	0	1	208.3
1	1	0	312.5
1	1	1	416.7

System Clocks

The system clock frequencies depend on the type of VFO and the type of floppy-disk. See table 4.

Table 4. System Clocks

VFO	Floppy-Disk	Clock XA	Clock XB
Internal	Standard or mini	32 MHz	
	High-density	32 MHz	19.2 MHz
External	Standard or mini	16 MHz	
	High-density	16 MHz	19.2 MHz

If a 32- or 16-MHz system clock is required, connect a quartz crystal resonator to pins XA1 and XA2, or connect an external clock signal to pin XA1 and leave XA2 open.

If a 19.2-MHz system clock is required, connect a quartz crystal resonator to pins XB1 and XB2, or connect an external clock signal to pin XB1 and leave XB2 open.

Internal Clocks

From the system clock, the μPD72067 generates the five internal clocks listed below.

(1) Internal system clock: controls internal operations and determines the data transfer rate.

(2) Write clock: frequency is twice the data transfer rate.

(3) DPLL clock: based on the 32-MHz system clock; source of the WINDOW signal.

(4) Precompensation clock

(5) 71065/66 clock: required if μPD71065 or μPD71066 is the external VFO.

Clock Selection

The system clock—32 or 16 MHz at the XA input or 19.2 MHz at the XB input—is selected by the state of the DR1 pin in external mode or the DR1 bit of the CONTROL INTERNAL MODE command in the internal mode.

For the selected system clock, the generated internal clock frequencies (table 5) are specified according to mode as follows.

(1) External mode: state of DR0 pin and command MFM bit.

(2) Internal mode: state of DR0 bit of CONTROL INTERNAL MODE command and MFM command bit.

When μPD71065 or μPD71066 is used as external VFO, the clock selected by the DR1 pin is output from the CLKOUT pin as the 71065/66 operation clock.

Table 5. Control Signals and Internal Clocks

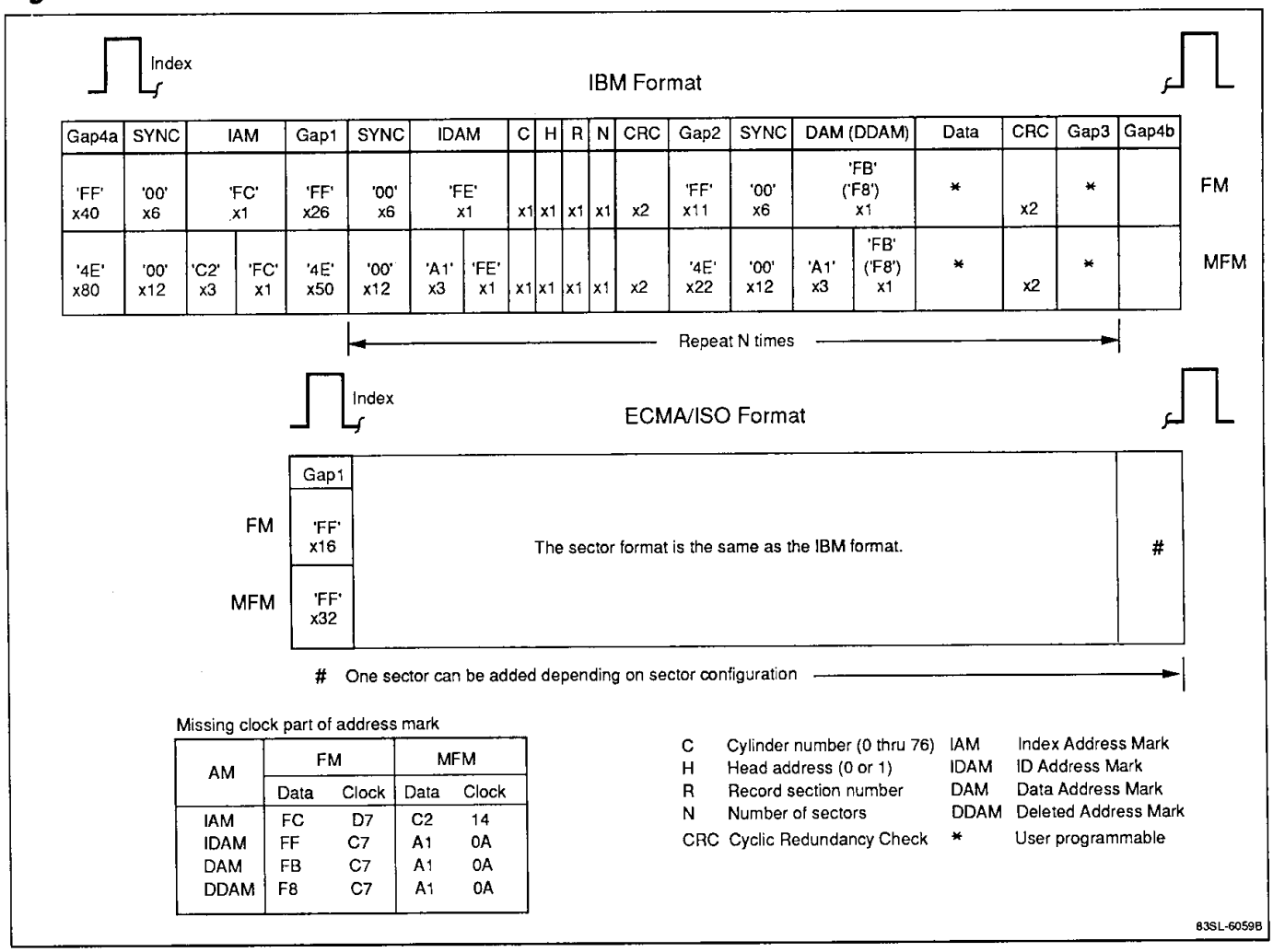
System Clock	DR1	DR0	MFM Bit	Data Transfer Rate (kb/s)	Internal Clocks: System (MHz)	Write (kHz)	DPLL (MHz)	Precomp	71065/66
32 MHz (Note 1) or 16 MHz (Note 2)	0	0	0	125	4	250	8	16 MHz	16 MHz
	0	0	1	250	4	500	16		
	0	1	0	250	8	500	16		
	0	1	1	500	8	1 MHz	32		
19.2 MHz	1	0	0	75	2.4	150	4.8	9.6 MHz	19.2 MHz
	1	0	1	150	2.4	300	9.6		
	1	1	0	150	4.8	300	9.6		
	1	1	1	300	4.8	600	19.2		

Notes:

(1) Internal VFO; internal mode with EXT = 0, or external mode.

(2) External VFO; internal mode with EXT = 1.

Figure 10. Track Formats



Format

The track format (IBM or ECMA/ISO) is specified by the FMT bit of the SELECT FORMAT command in internal mode or by the input signal to the FMT pin in external mode. See figure 10.

Commands

Table 6 describes the 15 commands and 8 auxiliary commands of the μPD72067.

System Bus Interface

Figure 11 is a reference circuit diagram of the interface between the μPD72067 and a system bus for data transfer in the DMA mode. The DMA controller is μPD71071. To prevent I/O port misselection during the DMA cycle, the Address Enable (AEN) output of μPD71071 inhibits other I/O ports.

Floppy-Disk Drive Interface

Figure 12 is a reference circuit diagram of the interface between a floppy-disk drive and the μPD72067 when the VFO is internal.

Figure 13 is a reference circuit diagram of the interface between a floppy-disk drive and the μPD72067 when the external VFO is μPD71065 or μPD71066. Special signal functions for this application are described below.

MFM	Recording system change signal
SYNC	Read enable/inhibit
CLKOUT	System clock to operate μPD71065/66
DRQ	Lock internal VFO (DPLL)
US0, US1	Drive select decoded by 74139
RW/SEEK	Select signal for demultiplexer (NAND gates) and multiplexer(LS157)

Table 6. List of Commands

Command Name	Function
Read Commands	
READ DATA	Specifies a sector and transfers its data to the host.
READ DELETED DATA	
READ ID	Reads a sector ID.
READ DIAGNOSTIC	Checks the track format.
SCAN EQUAL	Compares each sector data with host data and detects a sector that satisfies the set condition.
SCAN LOW OR EQUAL	
SCAN HIGH OR EQUAL	
Write Commands	
WRITE DATA	Specifies a sector and transfers its data to the host.
WRITE DELETED DATA	
WRITE ID	Writes the format of a track.
Seek Commands	
RECALIBRATE	Moves the read/write head to the outermost track (track 0).
SEEK	Moves the read/write head to the specified cylinder.
Sense Commands	
SENSE INTERRUPT STATUS	Reads the interrupt factor (seek end/state change) in the μPD72067.
SENSE DEVICE STATUS	Reads the FDD status.
Initialize Command	
SPECIFY	Defines a μPD72067 operation mode.
Auxiliary Commands	
SET STANDBY	Drives the μPD72067 in the standby status.
RESET STANDBY	Releases the μPD72067 from the standby status.
SOFTWARE RESET	Initializes the μPD72067.
ENABLE EXTERNAL MODE	Sets the μPD72067 in External Mode.
CONTROL INTERNAL MODE	Sets the μPD72067 in Internal Mode and sets both data transmission rate and precompensation value.
ENABLE MOTORS	Controls On/Off of the spindle motor.
SELECT FORMAT	Selects either IBM or ECMA/ISO format.
START CLOCK	Starts the clock generator operation.

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Figure 11. μPD72067 to System Bus Interface

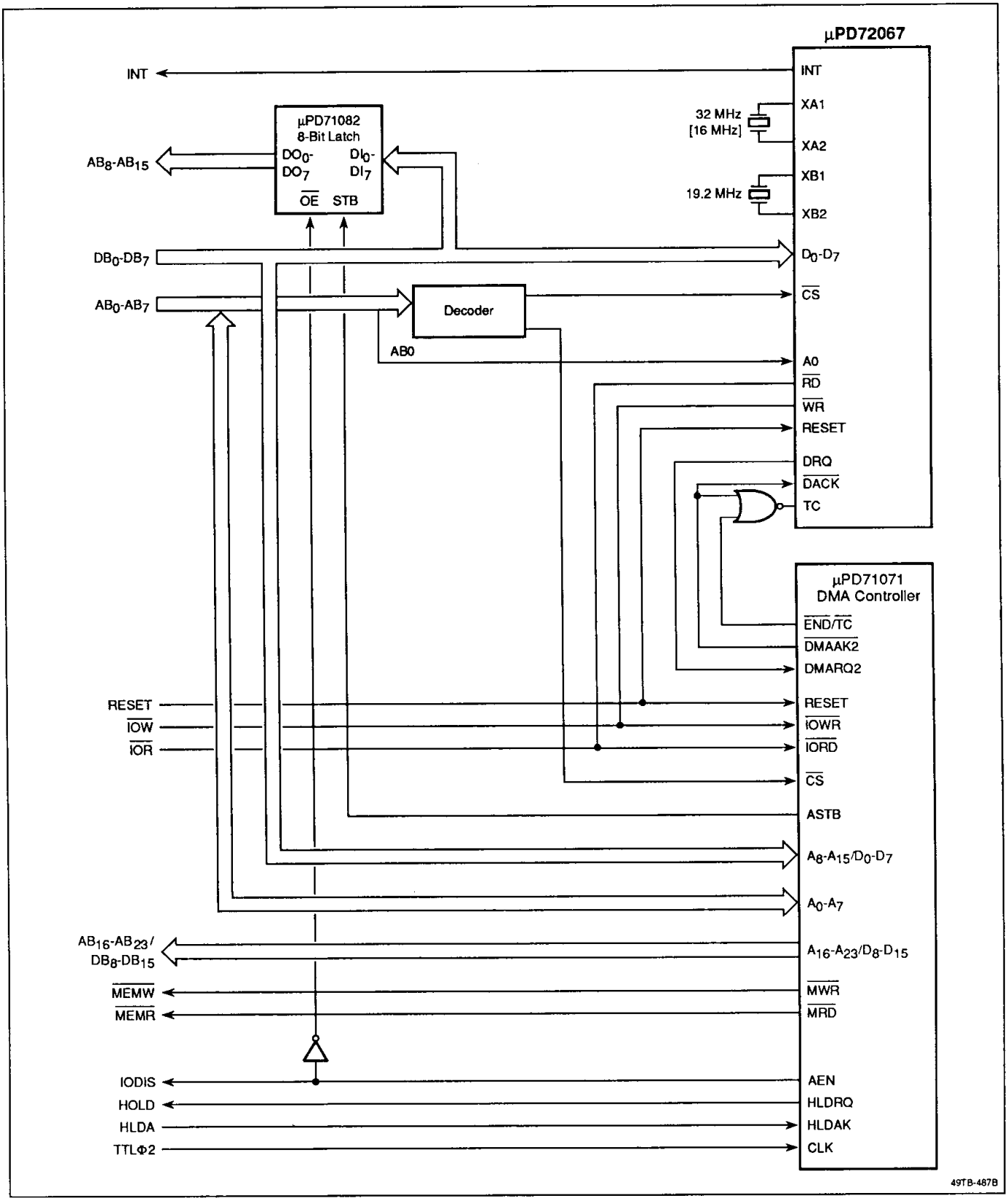

Figure 12. μPD72067 to FDD Interface 1

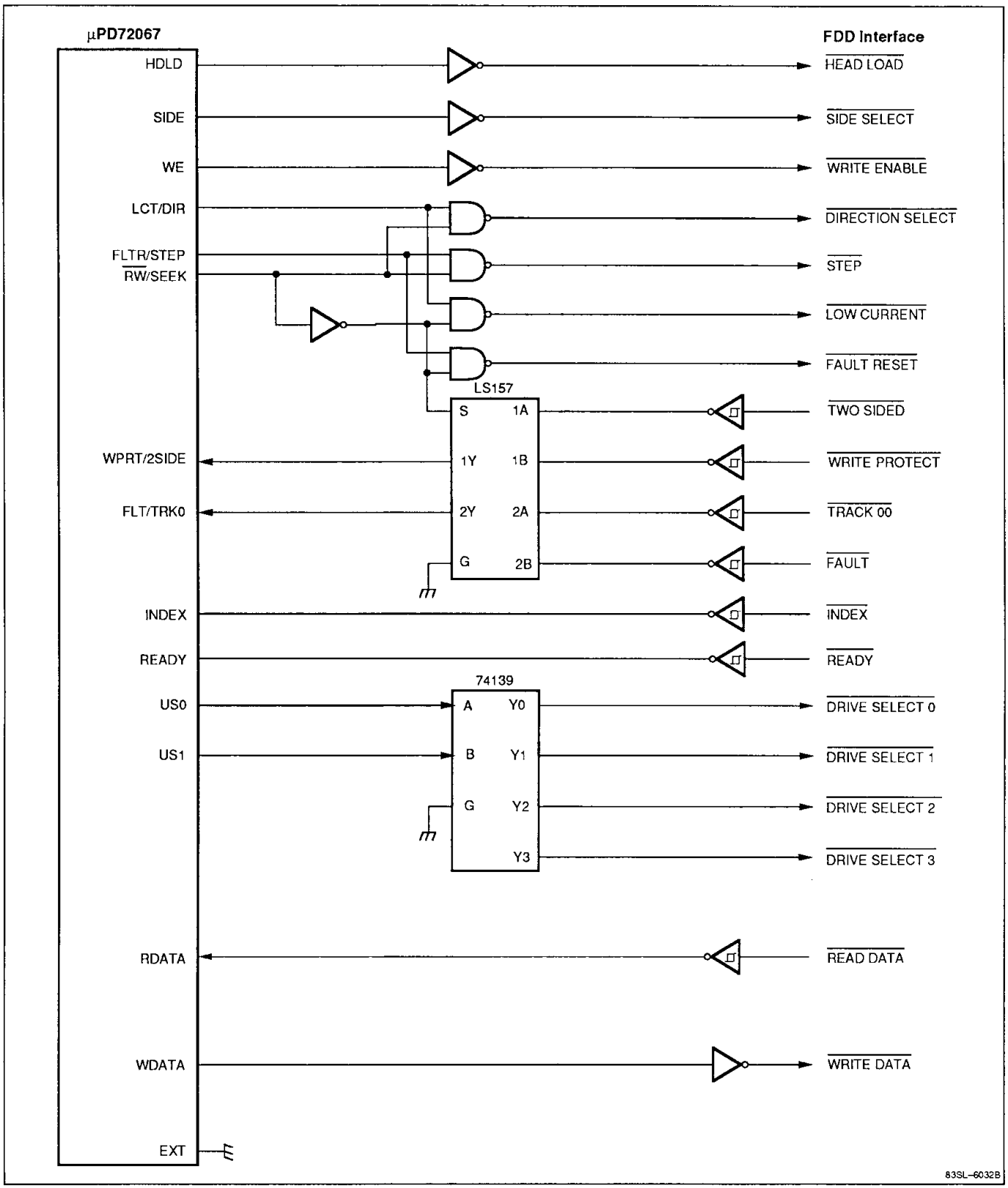

Figure 13. μPD72067 to FDD Interface 2