DUAL CML/PECL/LVPECL-to-LVDS TRANSLATOR

FEATURES

- Guaranteed f_{MAX} >750MHz over temperature
- 1.5Gbps throughput capability
- 3.0V to 5.7V power supply
- Guaranteed <700ps propagation delay over temperature
- Guaranteed <50ps within-device skew over temperature
- LVDS compatible outputs
- Fully differential I/O architecture
- Wide operating temperature range: –40°C to +85°C
- Available in a tiny 10-pin MSOP package

SuperLite™

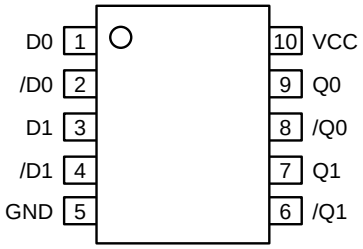
DESCRIPTION

The SY55855V is a fully differential, CML/PECL/LVPECL-to-LVDS translator. It achieves LVDS signaling up to 1.5Gbps, depending on the distance and the characteristics of the media and noise coupling sources. LVDS is intended to drive 50Ω impedance transmission line media such as PCB traces, backplanes, or cables.

SY55855V inputs can be terminated with a single resistor between the true and the complement pins of a given input.

The SY55855V is a member of Micrel's new SuperLite™ family of high-speed logic devices. This family features very small packaging, high signal integrity, and operation at many different supply voltages.

PIN CONFIGURATION

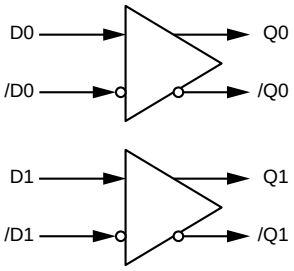


10-Pin MSOP

APPLICATIONS

- High-speed logic
- Data communications systems
- Wireless communications systems
- Telecom systems

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

Pin	Function
D0, /D0	CML/PECL/LVPECL Input Data
D1, /D1	CML/PECL/LVPECL Input Data
Q0, /Q0	LVDS Output Data
Q1, /Q1	LVDS Output Data
GND	Ground
V_{CC}	V_{CC}

PIN DESCRIPTIONS

D0, /D0 – CML/PECL/LVPECL Input (Differential)

This is one of the inputs. It is converted to LVDS onto the Q0 and /Q0 outputs.

D1, /D1 – CML/PECL/LVPECL Input (Differential)

This is the other input. It is converted to LVDS onto the Q1 and /Q1 outputs.

Q0, /Q0 – LVDS Output (Differential)

This is one LVDS output. It buffers the CML input that appears at D0, /D0.

Q1, /Q1 – LVDS Output (Differential)

This is the other LVDS output. It buffers the CML input that appears at D1, /D1.

FUNCTIONAL DESCRIPTION

Establishing Static Logic Inputs

The true pin of an input pair is internally biased to ground through a 75kΩ resistor. The complement pin of an input pair is internally biased halfway between V_{CC} and ground by a voltage divider consisting of two 75kΩ resistors. In this way, unconnected inputs appear as logic zeros. To keep an input at static logic zero at V_{CC} > 3.0V, leave both inputs unconnected. For $V_{CC} \leq 3.0V$, connect the complement input to V_{CC} and leave the true input unconnected. To make an input static logic one, connect the true input to V_{CC}, leave the complement input unconnected. These are the only two safe ways to cause inputs to be at a static value. In particular, no input pin should be directly connected to ground. All NC (no connect) pins should be unconnected.

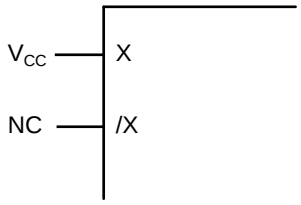
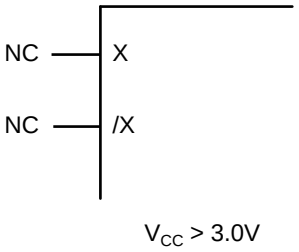


Figure 1. Hard Wiring a Logic "1" (1)

Note 1. X is either D0 or D1 input. /X is either /D0 or /D1 input.



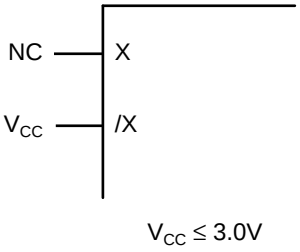


Figure 2. Hard Wiring a Logic "0" (1)

Note 1. X is either D0 or D1 input. /X is either /D0 or /D1 input.

TRUTH TABLE

D0	D1	Q0	/Q0	Q1	/Q1
0	0	0	1	0	1
0	1	0	1	1	0
1	0	1	0	0	1
1	1	1	0	1	0

LVDS OUTPUTS

LVDS stands for Low Voltage Differential Swing. LVDS specifies a small swing of 350mV typical, on a nominal 1.25V common mode above ground. The common mode voltage has tight limits to permit large variations in ground between an LVDS driver and receiver. Also, change in common mode voltage, as a function of data input, is also kept tight, to keep EMI low.

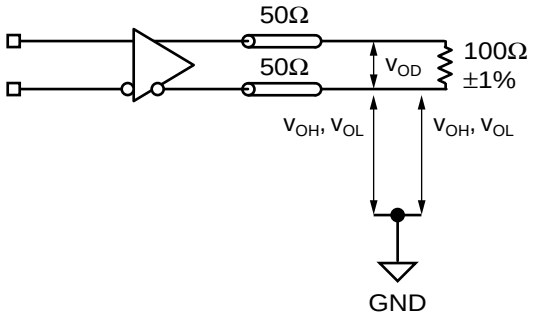


Figure 3. LVDS Differential Measurement

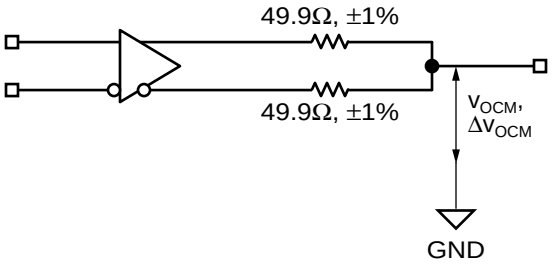


Figure 4. LVDS Common Mode Measurement

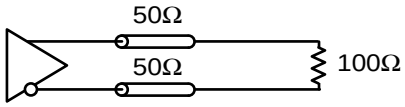


Figure 5. LVDS Output Termination

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
V_{CC}	Power Supply Voltage	–0.5 to +6.0	V
V_{IN}	Input Voltage	–0.5 to V_{CC} +0.5	V
I_{OUT}	LVDS Output Current	±10%	mA
T_A	Operating Temperature Range	–40 to +85	°C
T_{store}	Storage Temperature Range	–65 to +150	°C

Note 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS(1)

V_{CC} = 3.0V to 5.7V; GND = 0V; T_A = –40°C to +85°C(2)

		T_A = –40°C		T_A = +25°C			T_A = +85°C		
Symbol	Parameter	Min.	Max.	Min.	Typ.	Max.	Min.	Max.	Unit
V_{CC}	Power Supply Voltage	3.0	5.7	3.0	—	5.7	3.0	5.7	V
I_{CC}	Power Supply Current								mA
	3.6V <V_{CC} <5.7V	—	80	—	—	80	—	80	
	V_{CC} ≤3.6V	—	50	—	30	50	—	50	

Note 1. Specification for packaged product only.

Note 2. Equilibrium temperature.

CML DC ELECTRICAL CHARACTERISTICS(1)

V_{CC} = 3.0V to 5.7V; GND = 0V; T_A = –40°C to +85°C(2)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{ID}	Differential Input Voltage	100	—	—	mV	
V_{IH}	Input HIGH Voltage	1.6	—	V_{CC}	V	
V_{IL}	Input LOW Voltage	1.5	—	V_{CC} – 0.1	V	

Note 1. Specification for packaged product only.

Note 2. Equilibrium temperature.

LVDS DC ELECTRICAL CHARACTERISTICS(1)

V_{CC} = 3.0V to 5.7V; GND = 0V; T_A = –40°C to +85°C(2)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{OD}	Differential Output Voltage(4)	250	—	450	mV	100Ω Termination
V_{OCM}	Output Common Mode Voltage(3)	1.125	—	1.375	V	
ΔV_{OCM}	Change in Common Mode Voltage(3)	–50	—	+50	mV	
V_{OH}	Output HIGH Voltage(4), (5)	—	—	1.474	V	I_{OH} = –4.0mA
V_{OL}	Output LOW Voltage(4), (5)	0.925	—	—	V	I_{OL} = 4.0mA

Note 1. Specification for packaged product only.

Note 2. Equilibrium temperature.

Note 3. Measured as per Figure 4.

Note 4. Measured as per Figure 3.

Note 5. Do not short output to GND.

AC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = 3.0V to 5.7V; GND = 0V; T_A = –40°C to +85°C[2]

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
f_{MAX}	Maximum Operating Frequency	750	—	—	MHz	
t_{PLH} t_{PHL}	Propagation Delay D0 to Q0, D1 to Q1	300	—	700	ps	
t_{SKEW}	Within-Device Skew[3] Part-to-Part Skew (Diff.)	— —	— —	50 250	ps	
t_r t_f	LVDS Output Differential Rise/Fall Times (20% to 80%)	100	—	300	ps	

Note 1. Specification for packaged product only.

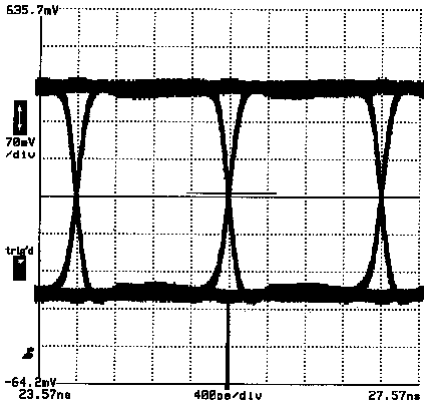
Note 2. Equilibrium temperature.

Note 3. Worst case difference between Q0 and Q1 from either D0 or D1, when both outputs have the same transition.

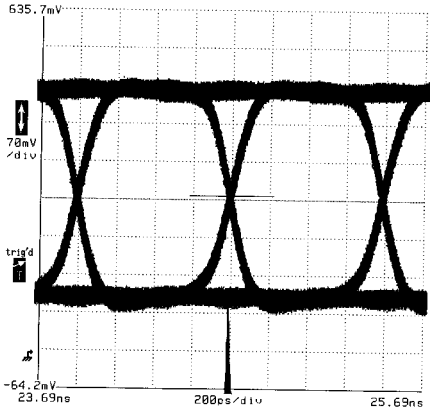
PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range	Package Marking
SY55855VKI	K10-1	Industrial	855V

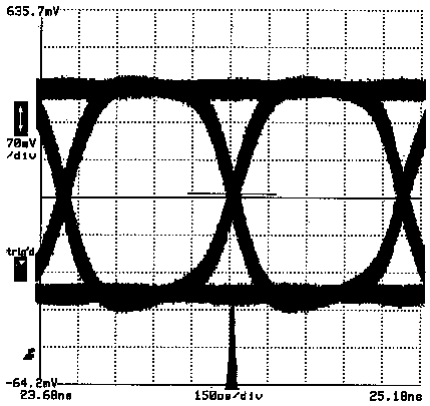
EYE DIAGRAMS[1]



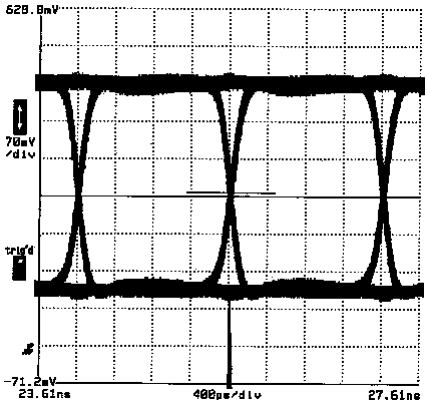
622Mbps
3.3V LVPECL-to-LVDS



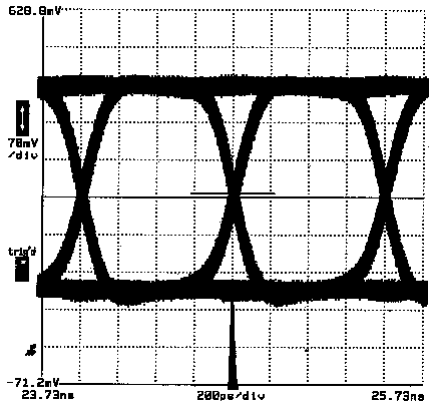
1.25Gbps
3.3V LVPECL-to-LVDS



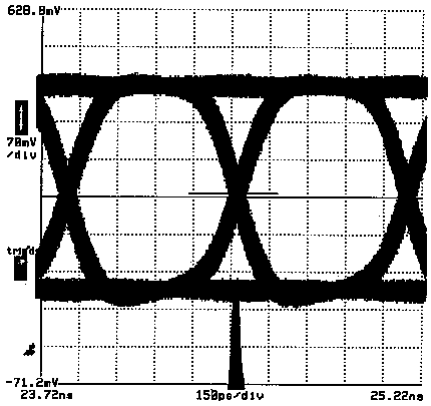
1.5Gbps
3.3V LVPECL-to-LVDS



622Mbps
3.3V CML-to-LVDS



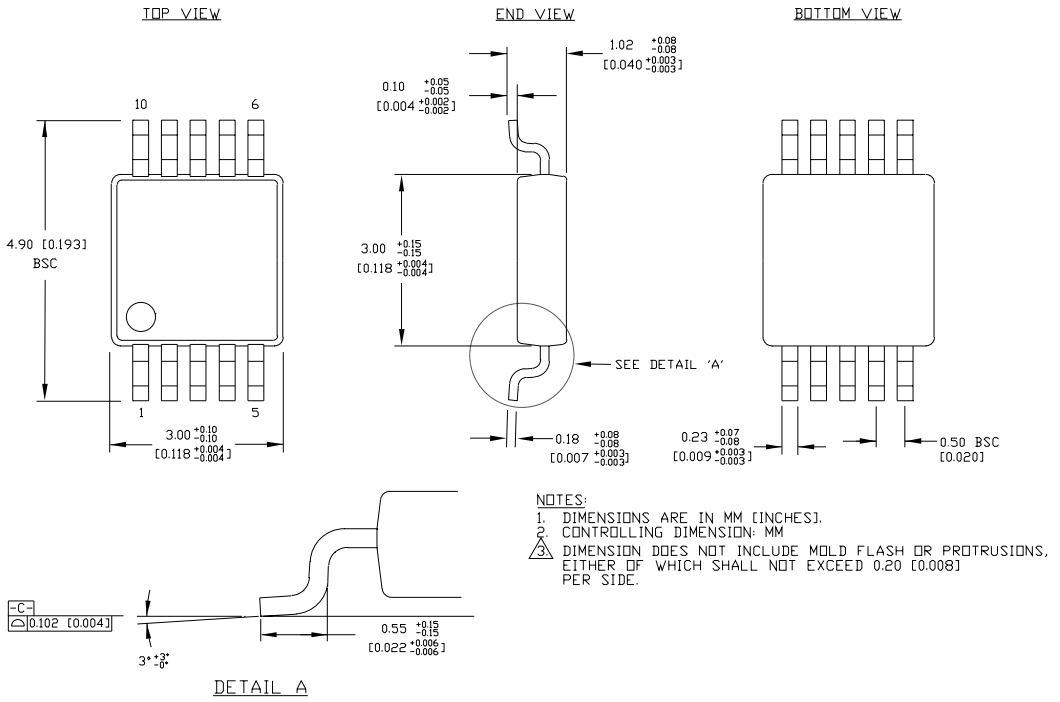
1.25Gbps
3.3V CML-to-LVDS



1.5Gbps
3.3V CML-to-LVDS

Note 1. 2^{23}–1 pattern.

10 LEAD MSOP (K10-1)



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