FAIRCHILD
SEMICONDUCTOR™

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74VCX163245
Low Voltage 16-Bit Dual Supply Translating Transceiver with 3-STATE Outputs

General Description

The VCX163245 is a dual supply, 16-bit translating transceiver that is designed for 2 way asynchronous communication between busses at different supply voltages by providing true signal translation. The supply rails consist of V_{CCA}, which is a higher potential rail operating at 2.3 to 3.6V and V_{CCB}, which is the lower potential rail operating at 1.65 to 2.7V. (V_{CCB} must be less than or equal to V_{CCA} for proper device operation). This dual supply design allows for translation from 1.8V to 2.5V busses to busses at a higher potential, up to 3.3V.

The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow. Transmit (active-HIGH) enables data from A Ports to B Ports; Receive (active-LOW) enables data from B Ports to A Ports. The Output Enable ($\overline{OE}$) input, when HIGH, disables both A and B Ports by placing them in a High-Z condition. The A Port interfaces with the higher voltage bus (2.7 – 3.3V); The B Port interfaces with the lower voltage bus (1.8 – 2.5V). Also the VCX163245 is designed so that the control pins ($T/\overline{R}_n$, $\overline{OE}_n$) are supplied by V_{CCB}.

The 74VCX163245 is suitable for mixed voltage applications such as notebook computers using a 1.8V CPU and 3.3V peripheral components. It is fabricated with an Advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

Features

- Bidirectional interface between busses ranging from 1.65V to 3.6V
- Supports Live Insertion and Withdrawal (Note 1)
- Static Drive (I_{OH}/I_{OL})
  - ±24 mA @ 3.0V V_{CC}
  - ±18 mA @ 2.3V V_{CC}
  - ±6 mA @ 1.65V V_{CC}
- Uses patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 16245
- Latchup performance exceeds 300 mA
- ESD performance:
  - Human Body Model >2000V
  - Machine model >200V

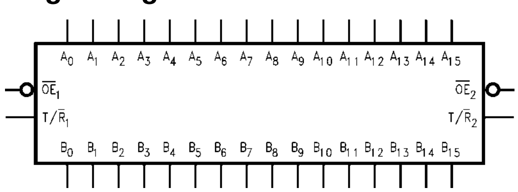
Note 1: To ensure the high impedance state during power up or power down, OE_n should be tied to V_{CCB} through a pull up resistor. The minimum value of the resistor is determined by the current sourcing capability of the driver.

Ordering Code:

Order Number	Package Number	Package Description
74VCX163245MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Device also available in Tape and Reel. Specify by appending the suffix letter “X” to the ordering code.

Logic Diagram

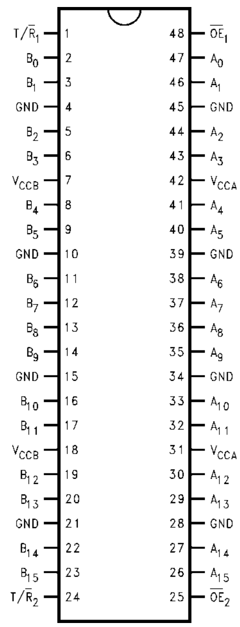


Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
$T/\overline{R}_n$	Transmit/Receive Input
A_0–A_{15}	Side A Inputs or 3-STATE Outputs
B_0–B_{15}	Side B Inputs or 3-STATE Outputs

Quiet Series™ is a trademark of Fairchild Semiconductor Corporation.

Connection Diagram



Truth Tables

Inputs		Outputs
$\overline{OE_1}$	$T/\overline{R_1}$	
L	L	Bus B_0–B_7 Data to Bus A_0–A_7
L	H	Bus A_0–A_7 Data to Bus B_0–B_7
H	X	HIGH Z State on A_0–A_7, B_0–B_7

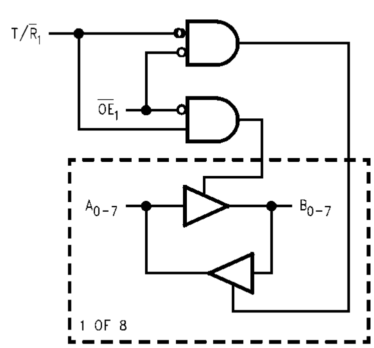
Inputs		Outputs
$\overline{OE_2}$	$T/\overline{R_2}$	
L	L	Bus B_8–B_{15} Data to Bus A_8–A_{15}
L	H	Bus A_8–A_{15} Data to Bus B_8–B_{15}
H	X	HIGH-Z State on A_8–A_{15}, B_8–B_{15}

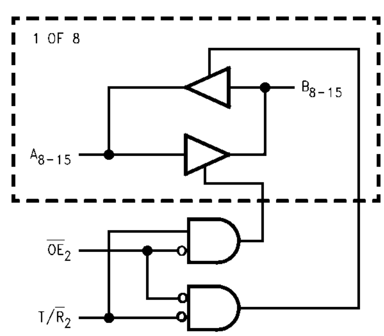
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial (HIGH or LOW, inputs may not float)
Z = High Impedance

VCX163245 Translator Power Up Sequence Recommendations

To guard against power up problems, some simple guidelines need to be adhered to. The VCX163245 is designed so that the control pins ($T/\overline{R}_n$, $\overline{OE}_n$) are supplied by V_{CCB}. Therefore the first recommendation is to begin by powering up the control side of the device, V_{CCB}. The $\overline{OE}_n$ control pins should be ramped with or ahead of V_{CCB}, this will guard against bus contentions and oscillations as all A Port and B Port outputs will be disabled. To ensure the high impedance state during power up or power down, $\overline{OE}_n$ should be tied to V_{CCB} through a pull up resistor. The minimum value of the resistor is determined by the current sourcing capability of the driver. Second, the $T/\overline{R}_n$ control pins should be placed at logic LOW (0V) level, this will ensure that the B-side bus pins are configured as inputs to help guard against bus contention and oscillations. B-side Data Inputs should be driven to a valid logic level (0V or V_{CCB}), this will prevent excessive current draw and oscillations. V_{CCA} can then be powered up after V_{CCB}, however V_{CCA} must be greater than or equal to V_{CCB} to ensure proper device operation. Upon completion of these steps the device can then be configured for the users desired operation. Following these steps will help to prevent possible damage to the translator device as well as other system components.

Logic Diagrams





Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 2)

Supply Voltage	
V_{CCA}	−0.5V to +4.6V
V_{CCB}	−0.5V to V_{CCA}
DC Input Voltage (V_I)	−0.5V to +4.6V
DC Output Voltage ($V_{I/O}$)	
Outputs 3-STATE	−0.5V to +4.6V
Outputs Active (Note 3)	
A_n	−0.5V to V_{CCA} + 0.5V
B_n	−0.5V to V_{CCB} + 0.5V
DC Input Diode Current (I_{IK})	
$V_I < 0V$	−50 mA
DC Output Diode Current (I_{OK})	
$V_O < 0V$	−50 mA
$V_O > V_{CC}$	+50 mA
DC Output Source/Sink Current	
(I_{OH}/I_{OL})	±50 mA
DC V_{CC} or Ground Current	±100 mA
Supply Pin (I_{CC} or Ground)	
Storage Temperature (T_{STG})	−65°C to +150°C

Recommended Operating Conditions (Note 4)

Power Supply (Note 5)	
V_{CCA}	2.3V to 3.6V
V_{CCB}	1.65V to 2.7V
Input Voltage (V_I) @ $\overline{OE}$, T/$\overline{R}$	0V to V_{CCB}
Input/Output Voltage ($V_{I/O}$)	
A_n	0V to V_{CCA}
B_n	0V to V_{CCB}
Output Current in I_{OH}/I_{OL}	
V_{CCA} = 3.0V to 3.6V	±24 mA
V_{CCA} = 2.3V to 2.7V	±18 mA
V_{CCB} = 2.3V to 2.7V	±18 mA
V_{CCB} = 1.65V to 1.95V	±6 mA
Free Air Operating Temperature (T_A	−40°C to +85°C
Minimum Input Edge Rate (Δt/ΔV)	
V_{IN} = 0.8V to 2.0V, V_{CC} = 3.0V	10 ns/V

Note 2: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 3: I_O Absolute Maximum Rating must be observed.

Note 4: Unused inputs or I/O pins must be held HIGH or LOW. They may not float.

Note 5: Operation requires: $V_{CCB} \le V_{CCA}$

DC Electrical Characteristics (1.65V < V_{CCB} ≤ 1.95V, 2.3V < V_{CCA} ≤ 2.7V)

Symbol	Parameter		Conditions	V_{CCB} (V)	V_{CCA} (V)	Min	Max	Units
V_{IHA}	HIGH Level Input Voltage	A_n		1.65–1.95	2.3–2.7	1.6		V
V_{IHB}		B_n, T/$\overline{R}$, $\overline{OE}$		1.65–1.95	2.3–2.7	0.65 x V_{CC}		V
V_{ILA}	LOW Level Input Voltage	A_n		1.65–1.95	2.3–2.7		0.7	V
V_{ILB}		B_n, T/$\overline{R}$, $\overline{OE}$		1.65–1.95	2.3–2.7		0.35 x V_{CC}	V
V_{OHA}	HIGH Level Output Voltage		I_{OH} = −100 μA	1.65–1.95	2.3–2.7	V_{CCA}–0.2		V
			I_{OH} = −18 mA	1.65	2.3–2.7	1.7		
V_{OHB}	HIGH Level Output Voltage		I_{OH} = −100 μA	1.65–1.95	2.3–2.7	V_{CCB}–0.2		V
			I_{OH} = −6 mA	1.65–1.95	2.3	1.25		
V_{OLA}	Low Level Output Voltage		I_{OL} = 100 μA	1.65–1.95	2.3–2.7		0.2	V
			I_{OL} = 18 mA	1.65	2.3–2.7		0.6	
V_{OLB}	Low Level Output Voltage		I_{OL} = 100 μA	1.65–1.95	2.3–2.7		0.2	V
			I_{OL} = 6 mA	1.65–1.95	2.3		0.3	
I_I	Input Leakage Current @ $\overline{OE}$, T/$\overline{R}$		0V ≤ V_I ≤ 3.6V	1.65–1.95	2.3–2.7		±5.0	μA
I_{OZ}	3-STATE Output Leakage		0V ≤ V_O ≤ 3.6V $\overline{OE}$ = V_{CCB} V_I = V_{IH} or V_{IL}	1.65–1.95	2.3–2.7		±10	μA
I_{OFF}	Power Off Leakage Current		0≤ (V_I, V_O) ≤ 3.6V	0	0		10	μA
I_{CCA}/I_{CCB}	Quiescent Supply Current, per supply, V_{CCA} / V_{CCB}		A_n = V_{CCA} or GND B_n, $\overline{OE}$, & T/$\overline{R}$ = V_{CCB} or GND	1.65–1.95	2.3–2.7		20	μA
			V_{CCA} ≤ An ≤ 3.6V V_{CCB} ≤ B_n, $\overline{OE}$, T/$\overline{R}$ ≤ 3.6V	1.65–1.95	2.3–2.7		±20	μA
ΔI_{CC}	Increase in I_{CC} per Input, B_n, T/$\overline{R}$, $\overline{OE}$		V_I = V_{CCB} – 0.6V	1.65–1.95	2.3–2.7		750	μA
	Increase in I_{CC} per Input, A_n		V_I = V_{CCA} – 0.6V	1.65–1.95	2.3–2.7		750	μA

DC Electrical Characteristics (1.65V < V_{CCB} ≤ 1.95V, 3.0V < V_{CCA} ≤ 3.6V)

Symbol	Parameter		Conditions	V_{CCB} (V)	V_{CCA} (V)	Min	Max	Units
V_{IHA}	HIGH Level Input Voltage	A_n		1.65–1.95	3.0–3.6	2.0		V
V_{IHB}		B_n, T/$\overline{R}$, $\overline{OE}$		1.65–1.95	3.0–3.6	0.65 x V_{CC}		V
V_{ILA}	LOW Level Input Voltage	A_n		1.65–1.95	3.0–3.6		0.8	V
V_{ILB}		B_n, T/$\overline{R}$, $\overline{OE}$		1.65–1.95	3.0–3.6		0.35 x V_{CC}	V
V_{OHA}	HIGH Level Output Voltage		I_{OH} = −100 μA	1.65–1.95	3.0–3.6	V_{CCA}–0.2		V
			I_{OH} = −24 mA	1.65	3.0–3.6	2.2		
V_{OHB}	HIGH Level Output Voltage		I_{OH} = −100 μA	1.65–1.95	3.0–3.6	V_{CCA}–0.2		V
			I_{OH} = −6 mA	1.65–1.95	3.0	1.25		
V_{OLA}	LOW Level Output Voltage		I_{OL} = 100 μA	1.65–1.95	3.0–3.6		0.2	V
			I_{OL} = 24 mA	1.65	3.0–3.6		0.55	
V_{OLB}	LOW Level Output Voltage		I_{OL} = 100 μA	1.65–1.95	3.0–3.6		0.2	V
			I_{OL} = 6 mA	1.65–1.95	3.0		0.3	
I_I	Input Leakage Current @ $\overline{OE}$, T/$\overline{R}$		0V ≤ V_I ≤ 3.6V	1.65–1.95	3.0–3.6		±5.0	μA
I_{OZ}	3-STATE Output Leakage		0V ≤ V_O ≤ 3.6V OE* = V_{CCB} V_I = V_{IH} or V_{IL}	1.65–1.95	3.0–3.6		±10	μA
I_{OFF}	Power OFF Leakage Current		0 ≤ (V_I, V_O) ≤ 3.6V	0	0		10	μA
I_{CCA}/I_{CCB}	Quiescent Supply Current, per supply, V_{CCA}/V_{CCB}		A_n = V_{CCA} or GND B_n, $\overline{OE}$, & T/$\overline{R}$ = V_{CCB} or GND	1.65–1.95	3.0–3.6		20	μA
			V_{CCA} ≤ A_n ≤ 3.6V V_{CCB} ≤ B_n, $\overline{OE}$, T/$\overline{R}$ ≤ 3.6V	1.65–1.95	3.0–3.6		±20	μA
ΔI_{CC}	Increase in I_{CC} per Input, B_n, T/$\overline{R}$, $\overline{OE}$		V_I = V_{CCB} − 0.6V	1.65–1.95	3.0–3.6		750	μA
	Increase in I_{CC} per Input, A_n		V_I = V_{CCA} − 0.6V	1.65–1.95	3.0–3.6		750	μA

DC Electrical Characteristics (2.3V < V_{CCB} ≤ 2.7V, 3.0V ≤ V_{CCA} ≤ 3.6V)

Symbol	Parameter		Conditions	V_{CCB} (V)	V_{CCA} (V)	Min	Max	Units
V_{IHA}	HIGH Level Input Voltage	A_n		2.3–2.7	3.0–3.6	2.0		V
V_{IHB}		B_n, T/$\overline{R}$, $\overline{OE}$		2.3–2.7	3.0–3.6	1.6		V
V_{ILA}	LOW Level Input Voltage	A_n		2.3–2.7	3.0–3.6		0.8	V
V_{ILB}		B_n, T/$\overline{R}$, $\overline{OE}$		2.3–2.7	3.0–3.6		0.7	V
V_{OHA}	HIGH Level Output Voltage		I_{OH} = −100 μA	2.3–2.7	3.0–3.6	V_{CCA}–0.2		V
			I_{OH} = −24 mA	2.3	3.0–3.6	2.2		
V_{OHB}	HIGH Level Output Voltage		I_{OH} = −100 μA	2.3–2.7	3.0–3.6	V_{CCB}–0.2		V
			I_{OH} = −18 mA	2.3–2.7	3.0	1.7		
V_{OLA}	LOW Level Output Voltage		I_{OL} = 100 μA	2.3–2.7	3.0–3.6		0.2	V
			I_{OL} = 24 mA	2.3	3.0–3.6		0.55	
V_{OLB}	LOW Level Output Voltage		I_{OL} = 100 μA	2.3–2.7	3.0–3.6		0.2	V
			I_{OL} = 18 mA	2.3–2.7	3.0		0.6	
I_I	Input Leakage Current @ $\overline{OE}$, T/$\overline{R}$		0V ≤ V_I ≤ 3.6V	2.3–2.7	3.0–3.6		±5.0	μA
I_{OZ}	3-STATE Output Leakage @ A_n		0V ≤ V_O ≤ 3.6V $\overline{OE}$ = V_{CCA} V_I = V_{IH} or V_{IL}	2.3–2.7	3.0–3.6		±10	μA
I_{OFF}	Power OFF Leakage Current		0 ≤ (V_I, V_O) ≤ 3.6V	0	0		10	μA
I_{CCA}/I_{CCB}	Quiescent Supply Current, per supply, V_{CCA}/V_{CCB}		A_n = V_{CCA} or GND B_n, $\overline{OE}$, & T/$\overline{R}$ = V_{CCB} or GND	2.3–2.7	3.0–3.6		20	μA
			V_{CCA} ≤ A_n ≤ 3.6V V_{CCB} ≤ B_n, $\overline{OE}$, T/$\overline{R}$ ≤ 3.6V	2.3–2.7	3.0–3.6		±20	μA
ΔI_{CC}	Increase in I_{CC} per Input, B_n, T/$\overline{R}$, $\overline{OE}$		V_I = V_{CCB} − 0.6V	2.3–2.7	3.0–3.6		750	μA
	Increase in I_{CC} per Input, A_n		V_I = V_{CCA} − 0.6V	2.3–2.7	3.0–3.6		750	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $C_L = 30$ pF, $R_L = 500\Omega$						Units
		$V_{CCB} = 1.65V$ to $1.95V$ $V_{CCA} = 2.3V$ to $2.7V$		$V_{CCB} = 1.65V$ to $1.95V$ $V_{CCA} = 3.0V$ to $3.6V$		$V_{CCB} = 2.3V$ to $2.7V$ $V_{CCA} = 3.0V$ to $3.6V$		
		Min	Max	Min	Max	Min	Max	
t_{PHL}, t_{PLH}	Prop Delay, A to B	1.5	5.8	1.5	6.2	0.8	4.4	ns
t_{PHL}, t_{PLH}	Prop Delay, B to A	0.8	5.5	0.6	5.1	0.6	4.0	ns
t_{PZL}, t_{PZH}	Output Enable Time, OE to B	1.5	8.3	1.5	8.2	0.8	4.6	ns
t_{PZL}, t_{PZH}	Output Enable Time, OE to A	0.8	5.3	0.6	5.1	0.6	4.0	ns
t_{PLZ}, t_{PHZ}	Output Disable Time, OE to B	0.8	4.6	0.8	4.5	0.8	4.4	ns
t_{PLZ}, t_{PHZ}	Output Disable Time, OE to A	0.8	5.2	0.6	5.6	0.6	4.8	ns
t_{osHL} t_{osLH}	Output to Output Skew (Note 6)		5.0		0.5		0.75	ns

Note 6: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{osHL}) or LOW-to-HIGH (t_{osLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CCB} (V)	V_{CCA} (V)	$T_A = +25°C$ Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}, A to B	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0V$	1.8	2.5	0.25	V
			1.8	3.3	0.25	
			2.5	3.3	0.6	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}, B to A	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0V$	1.8	2.5	0.6	V
			1.8	3.3	0.8	
			2.5	3.3	0.8	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}, A to B	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0V$	1.8	2.5	−0.25	V
			1.8	3.3	−0.25	
			2.5	3.3	−0.6	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}, B to A	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0V$	1.8	2.5	−0.6	V
			1.8	3.3	−0.8	
			2.5	3.3	−0.8	
V_{OHV}	Quiet Output Dynamic Valley V_{OH}, A to B	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0V$	1.8	2.5	1.3	V
			1.8	3.3	1.3	
			2.5	3.3	1.7	
V_{OHV}	Quiet Output Dynamic Valley V_{OH}, B to A	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0V$	1.8	2.5	1.7	V
			1.8	3.3	2.0	
			2.5	3.3	2.0	

Capacitance

Symbol	Parameter	Conditions	$T_A = +25°C$	Units
C_{IN}	Input Capacitance	$V_{CCB} = 2.5V$, $V_{CCA} = 3.3V$, $V_I = 0V$ or $V_{CCA/B}$	5	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CCB} = 2.5V$, $V_{CCA} = 3.3V$, $V_I = 0V$ or $V_{CCA/B}$	6	pF
C_{PD}	Power Dissipation Capacitance	$V_{CCB} = 2.5V$, $V_{CCA} = 3.3V$, $V_I = 0V$ or $V_{CCA/B}$ f = 10MHz	20	pF

AC Loading and Waveforms

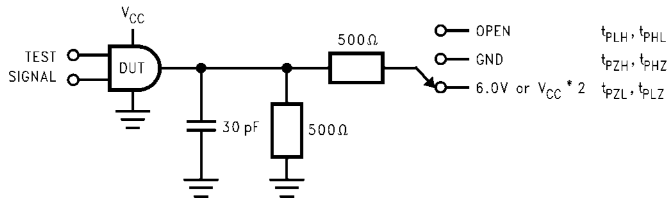


FIGURE 1. AC Test Circuit

TEST	SWITCH
t_{PLH}, t_{PHL}	OPEN
t_{PZL}, t_{PLZ}	6V at V_{CC} = 3.3 ±0.3V; V_{CC} x 2 at V_{CC} = 2.5 ± 0.2V; 1.8V ± 0.15V
t_{PZH}, t_{PHZ}	GND

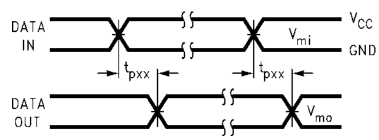


FIGURE 2. Waveform for Inverting and Non-inverting Functions
$t_R = t_F \leq$ 2.0 ns, 10% to 90%

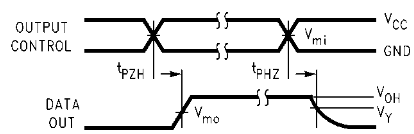


FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic
$t_R = t_F \leq$ 2.0 ns, 10% to 90%

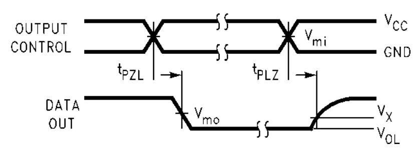
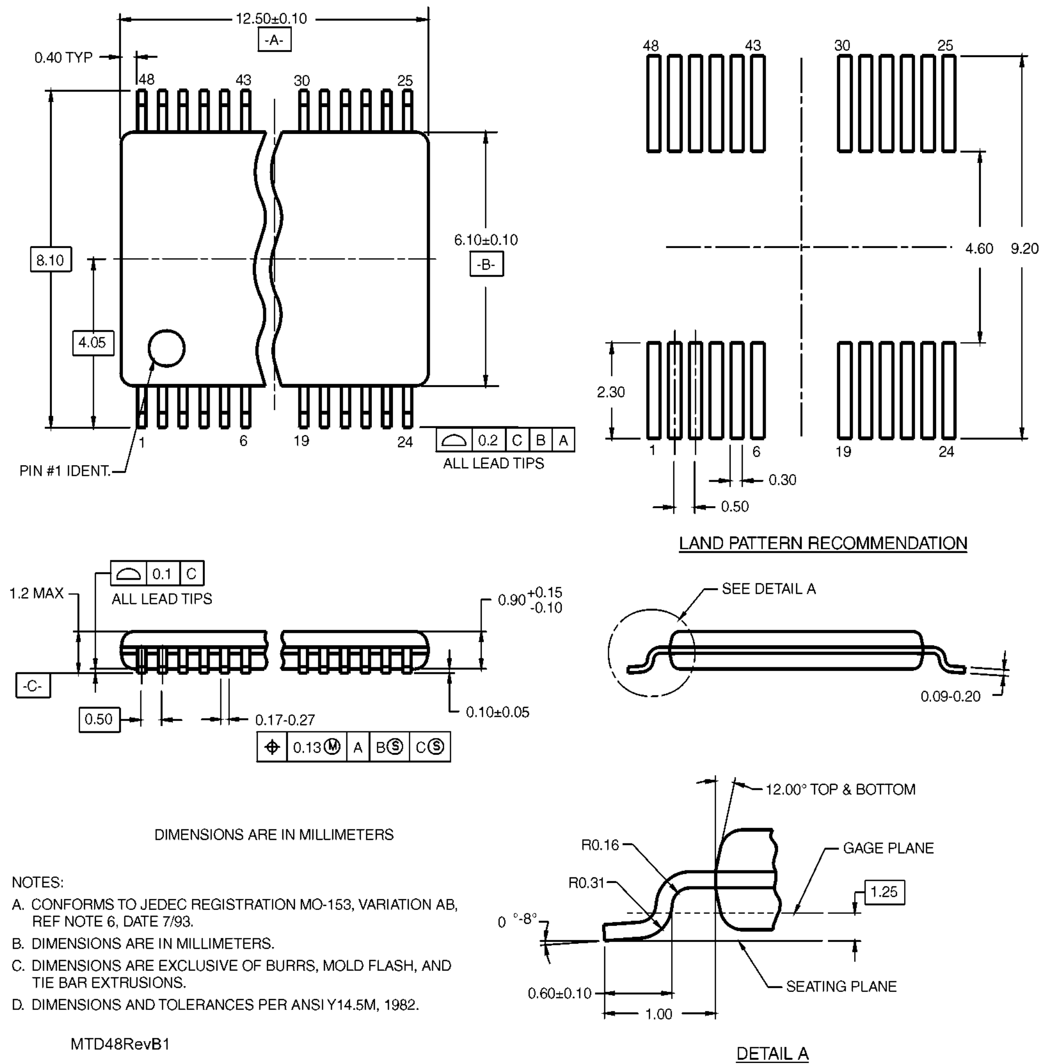


FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic
$t_R = t_F \leq$ 2.0 ns, 10% to 90%

Symbol	V_{CC}		
	3.3V ± 0.3V	**2.5V ± 0.2V**	**1.8V ± 0.15V**
V_{mi}	1.5V	V_{CC}/2	V_{CC}/2
V_{mo}	1.5V	V_{CC}/2	V_{CC}/2
V_X	V_{OL} + 0.3V	V_{OL} + 0.15V	V_{OL} + 0.15V
V_Y	V_{OH} – 0.3V	V_{OH} – 0.15V	V_{OH} – 0.15V

Physical Dimensions inches (millimeters) unless otherwise noted



48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48