

# MOS FIELD EFFECT TRANSISTOR $\mu$ PA2700GR

# SWITCHING N-CHANNEL POWER MOS FET

#### DESCRIPTION

The  $\mu$ PA2700GR is N-Channel MOS Field Effect Transistor designed for DC/DC converters and power management applications of notebook computers.

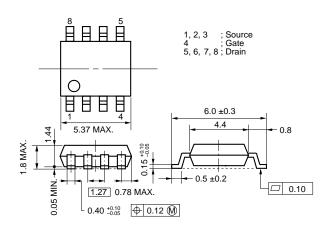
#### **FEATURES**

- Low on-state resistance RDS(on)1 = 5.3 m $\Omega$  MAX. (VGS = 10 V, ID = 9.0 A) RDS(on)2 = 7.3 m $\Omega$  MAX. (VGS = 4.5 V, ID = 9.0 A)
- Low Ciss: Ciss = 2600 pF TYP. (VDS = 10 V, VGS = 0 V)
- Small and surface mount package (Power SOP8)

### ORDERING INFORMATION

| PART NUMBER | PACKAGE    |
|-------------|------------|
| μPA2700GR   | Power SOP8 |

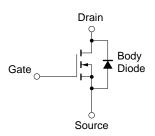
### **PACKAGE DRAWING (Unit: mm)**



### ABSOLUTE MAXIMUM RATINGS (TA = 25°C, All terminals are connected.)

| Drain to Source Voltage (Vgs = 0 V)                   | VDSS                  | 30           | V  |  |
|---|-----------------------|--------------|----|--|
| Gate to Source Voltage (Vps = 0 V)                    | Vgss                  | ±20          | V  |  |
| Drain Current (DC)                                    | ID(DC)                | ±17          | Α  |  |
| Drain Current (pulse) Note1                           | I <sub>D(pulse)</sub> | ±68          | Α  |  |
| Total Power Dissipation (T <sub>A</sub> = 25°C) Note2 | Рт                    | 2.0          | W  |  |
| Channel Temperature                                   | Tch                   | 150          | °C |  |
| Storage Temperature                                   | $T_{stg}$             | -55 to + 150 | °C |  |
| Single Avalanche Current Note3                        | las                   | 17           | Α  |  |
| Single Avalanche Energy Note3                         | Eas                   | 28.9         | mJ |  |

### **EQUIVALENT CIRCUIT**



- **Notes 1.** PW  $\leq$  10  $\mu$ s, Duty Cycle  $\leq$  1%
  - 2. Mounted on ceramic substrate of 1200 mm<sup>2</sup> x 2.2 mm
  - 3. Starting Tch = 25°C, VDD = 15 V, Rg = 25  $\Omega$ , L = 100  $\mu$ H, Vgs = 20  $\rightarrow$  0 V

**Remark** Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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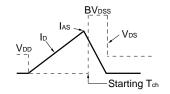


### **ELECTRICAL CHARACTERISTICS (TA = 25°C, All terminals are connected.)**

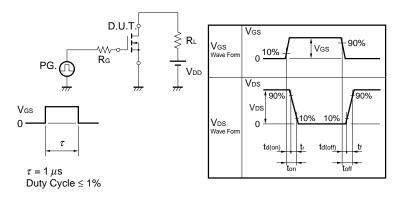
| CHARACTERISTICS                     | SYMBOL               | TEST CONDITIONS                                | MIN. | TYP. | MAX. | UNIT |
|-------------------------------------|----------------------|--|------|------|------|------|
| Zero Gate Voltage Drain Current     | Ipss                 | V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V  |      |      | 10   | μΑ   |
| Gate Leakage Current                | Igss                 | Vgs = ±20 V, Vps = 0 V                         |      |      | ±100 | nA   |
| Gate Cut-off Voltage                | V <sub>GS(off)</sub> | V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA  | 1.5  | 2.0  | 2.5  | V    |
| Forward Transfer Admittance         | yfs                  | V <sub>DS</sub> = 10 V, I <sub>D</sub> = 9.0 A | 11   | 21.5 |      | S    |
| Drain to Source On-state Resistance | RDS(on)1             | Vgs = 10 V, ID = 9.0 A                         |      | 4.2  | 5.3  | mΩ   |
|                                     | RDS(on)2             | VGS = 4.5 V, ID = 9.0 A                        |      | 5.5  | 7.3  | mΩ   |
|                                     | RDS(on)3             | VGS = 4.0 V, ID = 9.0 A                        |      | 6.3  | 8.4  | mΩ   |
| Input Capacitance                   | Ciss                 | V <sub>DS</sub> = 10 V                         |      | 2600 |      | pF   |
| Output Capacitance                  | Coss                 | VGS = 0 V                                      |      | 1000 |      | pF   |
| Reverse Transfer Capacitance        | Crss                 | f = 1 MHz                                      |      | 340  |      | pF   |
| Turn-on Delay Time                  | <b>t</b> d(on)       | V <sub>DD</sub> = 15 V, I <sub>D</sub> = 9.0 A |      | 20   |      | ns   |
| Rise Time                           | tr                   | V <sub>G</sub> S = 10 V                        |      | 24   |      | ns   |
| Turn-off Delay Time                 | td(off)              | R <sub>G</sub> = 10 Ω                          |      | 75   |      | ns   |
| Fall Time                           | tf                   |  |      | 22   |      | ns   |
| Total Gate Charge                   | Q <sub>G</sub>       | V <sub>DD</sub> = 15 V                         |      | 26   |      | nC   |
| Gate to Source Charge               | Qgs                  | V <sub>GS</sub> = 5 V                          |      | 7    |      | nC   |
| Gate to Drain Charge                | Q <sub>GD</sub>      | ID = 17 A                                      |      | 11   |      | nC   |
| Body Diode Forward Voltage          | V <sub>F(S-D)</sub>  | IF = 17 A, VGS = 0 V                           |      | 0.8  | 1.2  | V    |
| Reverse Recovery Time               | trr                  | I <sub>F</sub> = 17 A, V <sub>G</sub> s = 0 V  |      | 50   |      | ns   |
| Reverse Recovery Charge             | Qrr                  | di/dt = 100 A/ μs                              |      | 51   |      | nC   |

### **TEST CIRCUIT 1 AVALANCHE CAPABILITY**

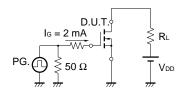
# $V_{GS} = 20 \rightarrow 0 \text{ V}$ $V_{GS} = 20 \rightarrow 0 \text{ V}$ $V_{DS} = 20 \rightarrow 0 \text{ V}$ $V_{DS} = 20 \rightarrow 0 \text{ V}$



### **TEST CIRCUIT 2 SWITCHING TIME**

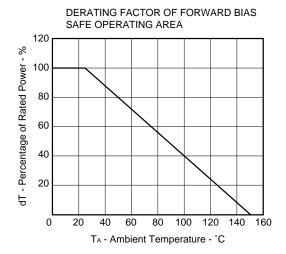


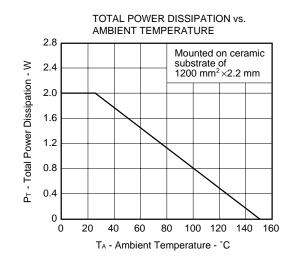
### **TEST CIRCUIT 3 GATE CHARGE**



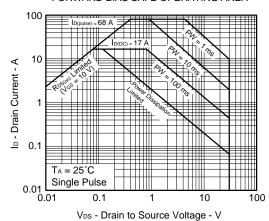
### TYPICAL CHARACTERISTICS (TA = 25°C)

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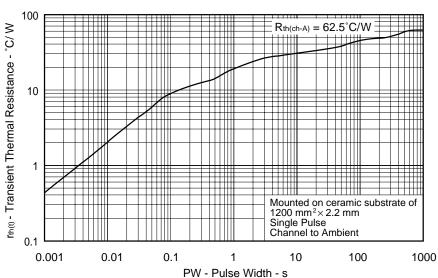


FORWARD BIAS SAFE OPERATING AREA



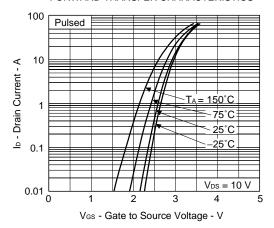
**Remark** Mounted on ceramic substrate of 1200 mm<sup>2</sup> x 2.2 mm

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

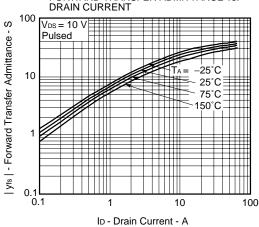


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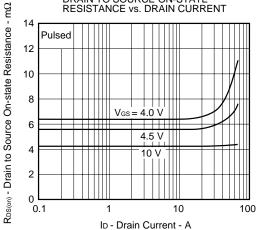
### FORWARD TRANSFER CHARACTERISTICS



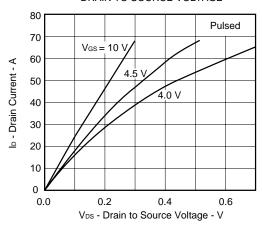
### FORWARD TRANSFER ADMITTANCE vs.



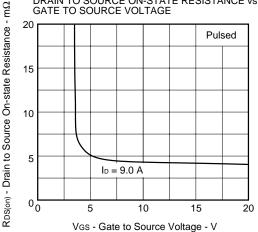
### DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



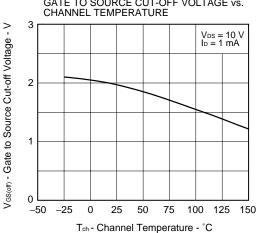
## DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

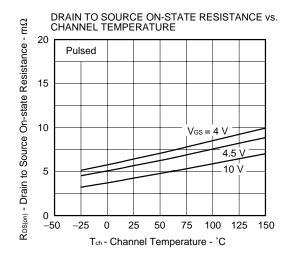


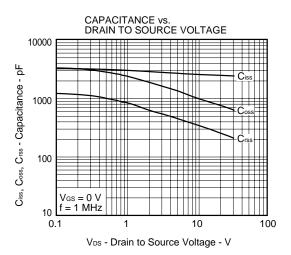
### DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

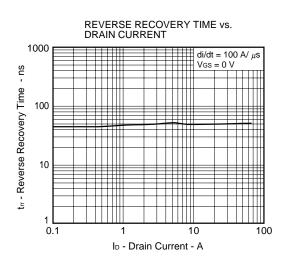


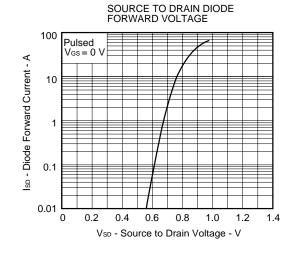
### GATE TO SOURCE CUT-OFF VOLTAGE vs.

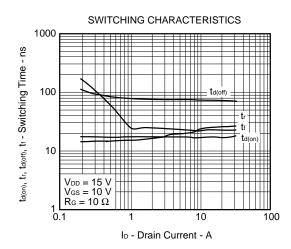


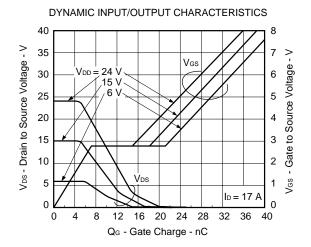












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