

STS5N150

N-CHANNEL 150V - 0.045 Ω - 5A SO-8 LOW GATE CHARGE STripFETTM POWER MOSFET

TARGET DATA

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TYPE	V _{DSS}	R _{DS(on)}	I _D
STS5N150	150 V	<0.06 Ω	5 A

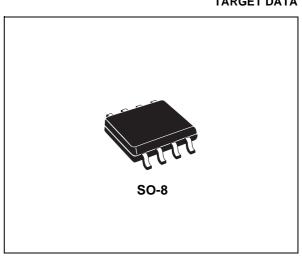
- TYPICAL $R_{DS}(on) = 0.045 \Omega$
- EXTREMELY HIGH dv/dt CAPABILITY
- EXTREMELY LOW GATE CHARGE

DESCRIPTION

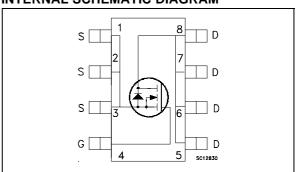
This MOSFET series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced highefficiency, high-frequency isolated DC-DC converters for Telecom and Computer applications. It is also intended for any applications with low gate drive requirements.

APPLICATIONS

- HIGH-EFFICIENCY DC-DC CONVERTERS
- UPS AND MOTOR CONTROL



INTERNAL SCHEMATIC DIAGRAM



Ordering Information

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SALES TYPE	MARKING	PACKAGE	PACKAGING
STS5N150	S5N150	SO-8	TAPE & REEL

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	150	V
V _{DGR}	Drain-gate Voltage ($R_{GS} = 20 \text{ k}\Omega$)	150	V
V _{GS}	Gate- source Voltage	± 20	V
I _D	Drain Current (continuous) at T _C = 25°C	5	Α
I _D	Drain Current (continuous) at T _C = 100°C	3	Α
I _{DM} (●)	Drain Current (pulsed)	20	Α
P _{tot}	Total Dissipation at T _C = 25°C	2.5	W
T _{stg}	Storage Temperature	-55 to 150	°C
Tj	Operating Junction Temperature	-55 to 150	

^(•) Pulse width limited by safe operating area.

June 2003

STS5N150

THERMAL DATA

Rthj-amb	(*)Thermal Resistance Junction-ambient	Max	50	°C/W
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^(*) When Mounted on 1 inch² FR-4 board, 2 oz of Cu and t \leq 10 sec.

ELECTRICAL CHARACTERISTICS ($T_{case} = 25 \, ^{\circ}\text{C}$ unless otherwise specified) OFF

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V _(BR) DSS	Drain-source Breakdown Voltage	$I_D = 250 \ \mu\text{A}, \ V_{GS} = 0$	150			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	$V_{DS} = Max Rating$ $V_{DS} = Max Rating T_C = 125$ °C			1 10	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 20 V			±100	nA

ON (*)

Symbol	Parameter	Test Conditions		Min.	Тур.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}$	$I_D = 250 \mu A$	2			V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V	I _D = 2.5 A		0.045	0.06	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
g _{fs} (*)	Forward Transconductance	$V_{DS} = 75 \text{ V}$ $I_{D} = 5 \text{ A}$		TBD		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25V$, $f = 1 MHz$, $V_{GS} = 0$		TBD TBD TBD		pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t _{d(on)} t _r	Turn-on Delay Time Rise Time	$\begin{array}{ccc} V_{DD} = 75 \text{ V} & I_D = 2.5 \text{ A} \\ R_G = 4.7 \; \Omega & V_{GS} = 10 \text{ V} \\ \text{(Resistive Load, Figure 1)} \end{array}$		TBD TBD		ns ns
Q _g Q _{gs} Q _{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V _{DD} = 120V I _D = 5A V _{GS} = 10V (see test circuit, Figure 2)		TBD TBD TBD	28	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t _{d(Off)} t _f	Turn-off Delay Time Fall Time	$\begin{array}{lll} V_{DD} = 75 \text{ V} & I_D = 2.5 \text{ A} \\ R_G = 4.7\Omega, & V_{GS} = 10 \text{ V} \\ \text{(Resistive Load, Figure 1)} \end{array}$		TBD TBD		ns ns

SOURCE DRAIN DIODE

Symbol	ymbol Parameter Test Conditions		Min.	Тур.	Max.	Unit
I _{SD} I _{SDM} (•)	Source-drain Current Source-drain Current (pulsed)				5 20	A A
V _{SD} (*)	Forward On Voltage	I _{SD} = 5 A V _{GS} = 0			1.2	V
t _{rr} Q _{rr} I _{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 5 \text{ A}$ di/dt = 100A/ μ s $V_{DD} = 50 \text{ V}$ $T_j = 150^{\circ}\text{C}$ (see test circuit, Figure 3)		TBD TBD TBD		ns nC A

^(*)Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %.
(•)Pulse width limited by safe operating area.

Fig. 1: Switching Times Test Circuits For Resistive Load

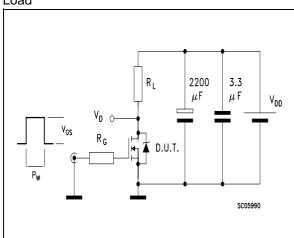


Fig. 2: Gate Charge test Circuit

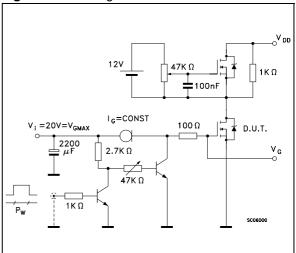
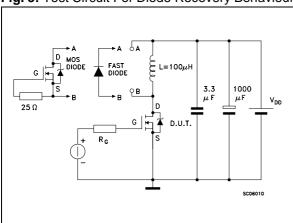
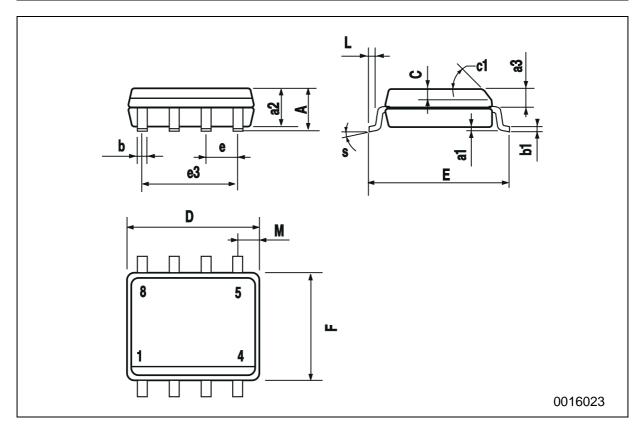


Fig. 3: Test Circuit For Diode Recovery Behaviour



SO-8 MECHANICAL DATA

DIM.		mm			inch	
DIWI.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
А			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
С	0.25		0.5	0.010		0.019
c1			45	(typ.)		
D	4.8		5.0	0.188		0.196
Е	5.8		6.2	0.228		0.244
е		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
М			0.6			0.023
S			8 (r	nax.)		



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