NIPPON PRECISION CIRCUITS INC.

QS7777PF/CF

QSurround™ 3D Virtual Audio Processor
for Dolby AC-3 and ProLogic

OVERVIEW

The QS7777PF/CF is an audio processor IC which implements the QSurround™ technology developed and licensed by QSound Labs, Inc. It processes Dolby Digital (AC-3) and Dolby Surround audio signals to produce enhanced virtual 3D sounds, even for 2-speaker systems. It can generate 2, 3, 4, and 5-channel speaker configurations, all with enhanced surround signal outputs.

FEATURES

- Enhanced surround signal from Dolby Digital (AC-3) and Dolby Surround (ProLogic) input signals
- 2-step adjustable sound enhancement
- Supported speaker configurations
  - Dolby Digital (AC-3) 6-channel signals to 2, 3, 4, 5-channel speaker QSurround signal configurations
  - Dolby Surround (ProLogic) 4-channel signals to 2, 3, 4-channel speaker QSurround signal configurations
- Monaural to virtual stereo conversion
- Parallel and 2 serial interface control modes selectable
  - QS7777CF: I²C bus 2-wire serial interface[1]
  - QS7777PF: 3-wire serial interface (Data, Clock, Strobe)
- 5 to 13V analog supply
- 4.5 to 5.5V digital supply
- 48-pin QFP package

1. NPC employs I²C bus serial interface components under license from Philips, and conforms to the Philips I²C bus specifications.

APPLICATIONS

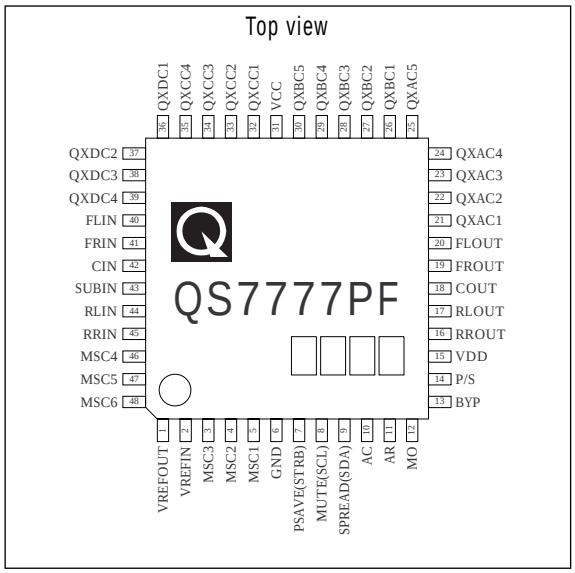
- DVD and laser disk players
- TV and AV equipment
- Multimedia products (including sound cards)
- Car audio

ORDERING INFORMATION

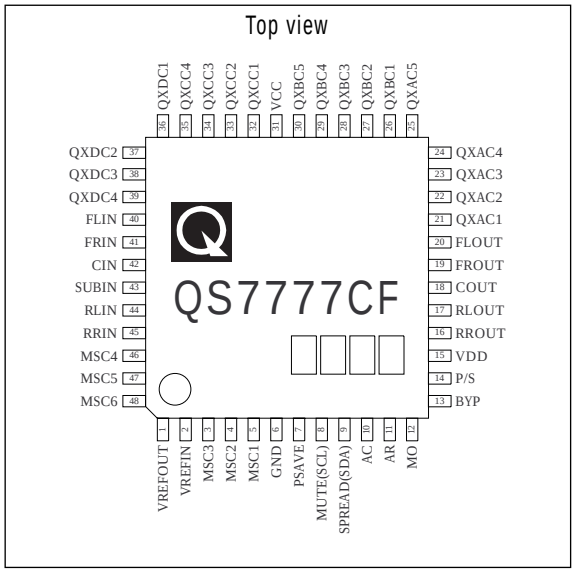
Device	Package
QS7777PF	48-pin QFP
QS7777CF	48-pin QFP

PINOUT

QS7777PF



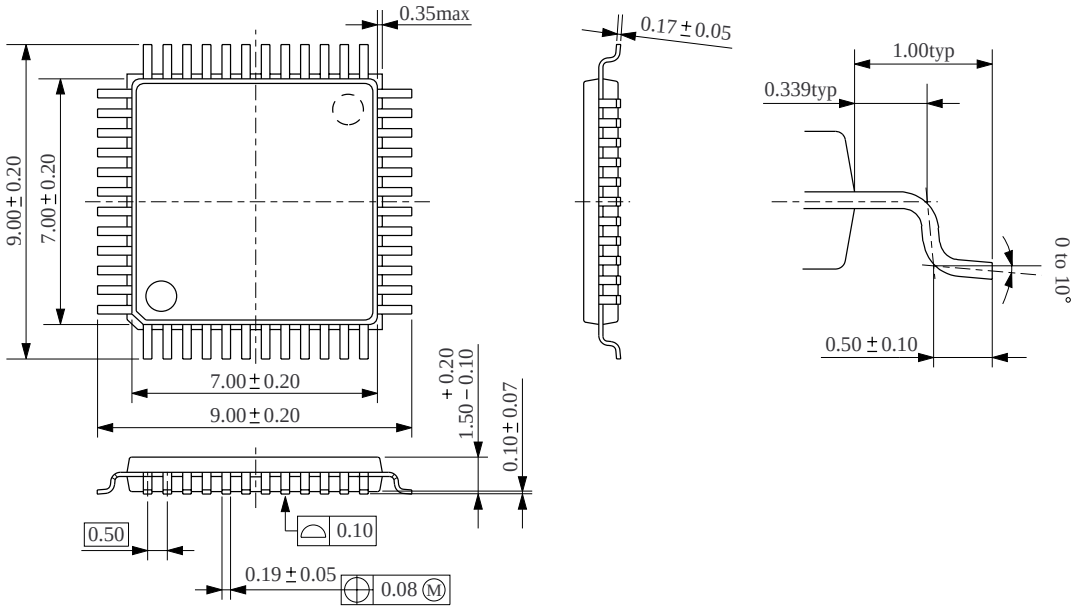
QS7777CF



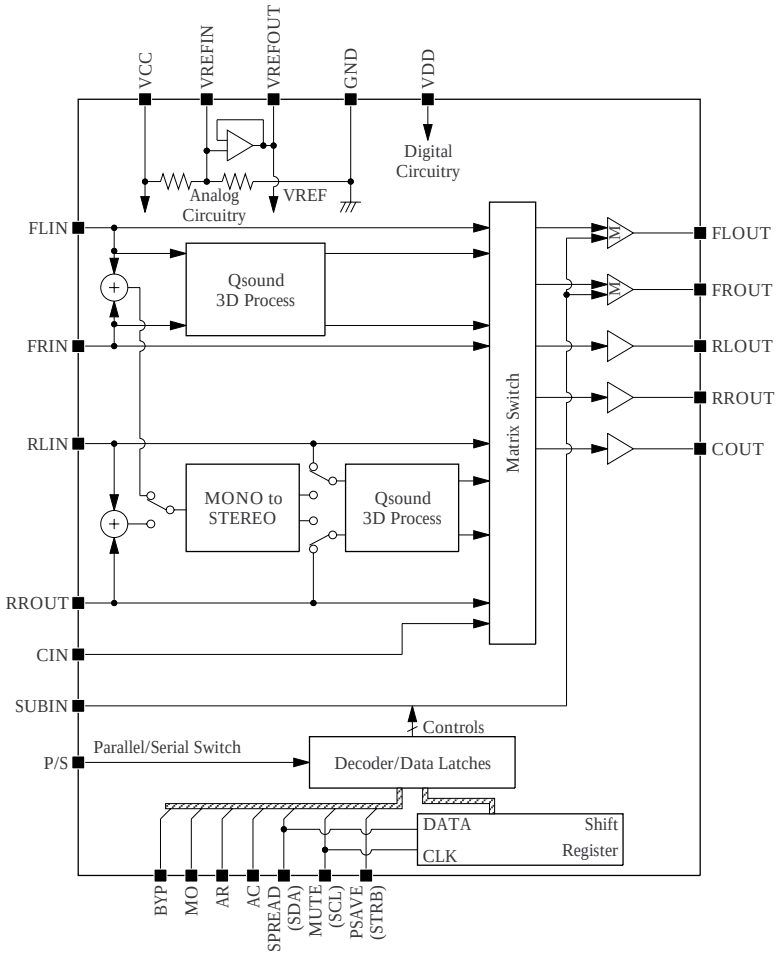
I²C bus is a registered trademark of Philips Electronics N.V.
Dolby and the double-D symbol are registered trademarks of Dolby Laboratories Licensing Corporation.

PACKAGE DIMENSIONS

Unit: mm



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name		I/O	Description
	Parallel	Serial		
1	VREFOUT		O	$V_{CC}/2$ reference voltage output
2	VREFIN		I	$V_{CC}/2$ reference voltage input (biased internally to $V_{CC}/2$)
3	MSC3		I	Mono/stereo conversion filter capacitor 3
4	MSC2		I	Mono/stereo conversion filter capacitor 2
5	MSC1		I	Mono/stereo conversion filter capacitor 1
6	GND		–	Ground
7	PSAVE	–	I	Power save control (HIGH: power save on, LOW: power save off)
	–	STRB	I	Serial data strobe (not used on I^2C bus device QS7777CF)
8	MUTE	–	I	Mute signal control (HIGH: mute on, LOW: mute off)
	–	SCL	I	Serial data shift clock input (QS7777CF: CMOS input, no protection diode connected between this pin and VDD)
9	SPREAD	–	I	Enhancement control (HIGH: maximum spread, LOW: minimum spread)
	–	SDA	I/O	Serial data input (and ACK signal output for I^2C bus device QS7777CF: n-channel open-drain pin, no protection diode connected between this pin and VDD).
10	AC		I	Center speaker control (HIGH: actual center, LOW: virtual center)
11	AR		I	Rear speaker control (HIGH: actual rear, LOW: virtual rear)
12	MO		I	Mono-to-stereo convert select (HIGH: ON, LOW: OFF)
13	BYP		I	Bypass/QSurround select control (HIGH: bypass, LOW: QSurround)
14	P/S		I	Interface method select (HIGH: parallel input, LOW: serial input)
15	VDD		–	4.5 to 5.5V DC digital supply
16	RROUT		O	Rear right-channel signal output
17	RLOUT		O	Rear left-channel signal output
18	COUT		O	Center signal output
19	FROUT		O	Front right-channel signal output
20	FLOUT		O	Front left-channel signal output
21	QXAC1		I	QExpander filter A capacitor 1
22	QXAC2		I	QExpander filter A capacitor 2
23	QXAC3		I	QExpander filter A capacitor 3
24	QXAC4		I	QExpander filter A capacitor 4
25	QXAC5		I	QExpander filter B capacitor 5
26	QXBC1		I	QExpander filter B capacitor 1
27	QXBC2		I	QExpander filter B capacitor 2
28	QXBC3		I	QExpander filter B capacitor 3
29	QXBC4		I	QExpander filter B capacitor 4
30	QXBC5		I	QExpander filter B capacitor 5
31	VCC		–	5 to 13V DC analog supply
32	QXCC1		I	QExpander filter C capacitor 1
33	QXCC2		I	QExpander filter C capacitor 2
34	QXCC3		I	QExpander filter C capacitor 3
35	QXCC4		I	QExpander filter C capacitor 4
36	QXDC1		I	QExpander filter D capacitor 1
37	QXDC2		I	QExpander filter D capacitor 2
38	QXDC3		I	QExpander filter D capacitor 3
39	QXDC4		I	QExpander filter D capacitor 4
40	FLIN		I	Front left-channel signal input
41	FRIN		I	Front right-channel signal input
42	CIN		I	Center-channel signal input
43	SUBIN		I	Sub-woofer signal input
44	RLIN		I	Rear left-channel signal input
45	RRIN		I	Rear right-channel signal input
46	MSC4		I	Mono/stereo conversion filter capacitor 4
47	MSC5		I	Mono/stereo conversion filter capacitor 5
48	MSC6		I	Mono/stereo conversion filter capacitor 6

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range (analog)	V_{CC}	–0.3 to 15	V
Supply voltage range (digital)	V_{DD}	–0.3 to 7	V
Input voltage range (analog)	V_{IANA}	–0.3 to V_{CC} + 0.3	V
Input voltage range (digital)	V_{IDIG}	–0.3 to V_{DD} + 0.3	V
I^2C signal input voltage (SDA, SCL)	V_{IOPEN}	10	V
Power dissipation	P_D	250	mW
Storage temperature range	T_{stg}	–40 to 125	°C
Soldering temperature	T_{sld}	255	°C
Soldering time	t_{sld}	10	s

Recommended Operating Conditions

Parameter	Symbol	Rating	Unit
Supply voltage range (analog)	V_{CC}	5 to 13	V
Supply voltage range (digital)	V_{DD}	4.5 to 5.5	V
Operating temperature range	T_{opr}	–20 to 70	°C

DC Characteristics

V_{CC} = 9V, V_{DD} = 5V, T_a = 25°C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Analog input impedance	Z_{AIN}	FLIN, FRIN, RLIN, RRIN, CIN, COUT	16	20	24	kΩ
Reference voltage output	V_{REFOUT}		–	V_{CC}/2	–	V
HIGH-level input voltage	V_{IH}		0.7V_{DD}	–	–	V
LOW-level input voltage	V_{IL}		–	–	0.3V_{DD}	V
Input leakage current	I_{LEAK}		–3	–	3	µA
Input leakage current (I^2C input)	I_{LOPEN}	SDA, SCL, 10V input voltage	–3	–	3	µA
LOW-level output voltage	V_{OL}	ACK signal output on SDA, 3mA sink current	0	–	0.4	V
Supply voltage (analog)	V_{CC}		5	–	13	V
Supply voltage (digital)	V_{DD}		4.5	–	5.5	V
Current consumption (analog)	I_{CC}	Quiescent input signal	–	10	13	mA
Current consumption (digital)	I_{DD}		–	0.3	0.5	mA
Standby current (analog)	I_{CCSAVE}		–	0.1	0.2	mA

Noise and THD Characteristics

V_{CC} = 9V, V_{DD} = 5V, T_a = 25°C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Bypass noise voltage	N_{BYP}	BYP = AR = AC = HIGH, MO = SPREAD = LOW, "A"-wgt, FLOUT, RLOUT, FROUT, RROUT, COUT	–	11	22	μV_{RMS}
QSurround noise voltage (front)	N_{QSF}	BYP = MO = SPREAD = LOW, AR = AC = HIGH, "A"-wgt, FLOUT, FROUT	–	16	32	μV_{RMS}
QSurround noise voltage (rear)	N_{QSR}	BYP = MO = SPREAD = LOW, AR = AC = HIGH, "A"-wgt, RLOUT, RROUT	–	14	28	μV_{RMS}
QSurround mono total harmonic distortion (front)	THD_F	MO = HIGH, all other excluding MO = LOW, all inputs $1V_{RMS}$, f = 1kHz, FROUT, FLOUT	–	–	0.1	%
QSurround mono total harmonic distortion (rear)	THD_R	MO = AR = AC = HIGH, BYP = SPREAD = AE = LOW, all inputs $1V_{RMS}$, f = 1kHz, RROUT, RLOUT, COUT	–	–	0.1	%

AC Characteristics

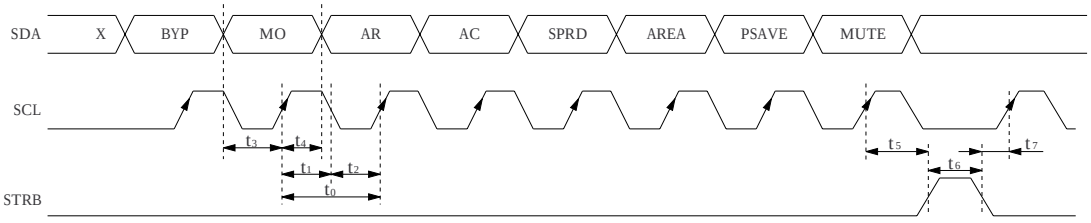
V_{CC} = 9V, V_{DD} = 5V, T_a = 25°C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Front maximum input voltage 1	V_{FIN1}	FLIN = FRIN, RLIN = RRIN = CIN = SUBIN = 0V, BYP = LOW, f = 1kHz	1.4	–	–	V_{RMS}
Front maximum input voltage 2	V_{FIN2}	FLIN = –FRIN, RLIN = RRIN = CIN = SUBIN = 0V, BYP = LOW, f = 1kHz	0.5	–	–	V_{RMS}
Rear maximum input voltage 1	V_{RIN1}	RLIN = RRIN, FLIN = FRIN = CIN = SUBIN = 0V, BYP = LOW, AR = LOW, f = 1kHz	1.4	–	–	V_{RMS}
Rear maximum input voltage 2	V_{RIN2}	RLIN = –RRIN, FLIN = FRIN = CIN = SUBIN = 0V, BYP = LOW, AR = LOW, f = 1kHz	0.3	–	–	V_{RMS}
Center maximum input voltage	V_{CIN}	FLIN = FRIN = RLIN = RRIN = SUBIN = 0V, BYP = LOW, AC = LOW, f = 1kHz	1.7	–	–	V_{RMS}
Sub-woofer maximum input voltage	V_{SUBIN}	FLIN = FRIN = RLIN = RRIN = CIN = 0V, f = 1kHz	2.2	–	–	V_{RMS}
FIN to FOUT bypass gain	G_{FFBYP}	BYP = HIGH, f = 1kHz, FLIN to FLOUT, FRIN to FROUT	–2	0	2	dB
RIN to ROUT bypass gain	G_{RRBYP}	BYP = HIGH, AR = HIGH, f = 1kHz, RLIN to RLOUT, RRIN to RROUT	–2	0	2	dB
RIN to FOUT bypass gain	G_{RFBYP}	BYP = HIGH, AR = LOW, f = 1kHz, RLIN to FLOUT, RRIN to FROUT	–2	0	2	dB
CIN to COUT gain	G_{CC}	AC = HIGH, f = 1kHz, CIN to COUT	–2	0	2	dB
CIN to FOUT gain	G_{CF}	AC = LOW, f = 1kHz, CIN to FLOUT, CIN to FROUT	–2.8	–0.8	1.2	dB
SUBIN to FOUT gain	G_{SUBF}	f = 1kHz, SUBIN to FLOUT, SUBIN to FROUT	–8	–6	–4	dB
FIN to FOUT gain	G_{FF}	SPREAD = HIGH, BYP = LOW, f = 1kHz, FLIN to FLOUT, FRIN to FROUT	5.7	7.5	9.5	dB
FIN to FOUT crosstalk gain	G_{FXF}	SPREAD = HIGH, BYP = LOW, f = 1kHz, FLIN to FROUT, FRIN to FLOUT	3.7	5.7	7.7	dB
RIN to ROUT gain	G_{RR}	BYP = LOW, AR = HIGH, f = 1kHz, RLIN to RLOUT, RRIN to RROUT	2.7	4.7	6.7	dB
RIN to ROUT crosstalk gain	G_{RXR}	BYP = LOW, AR = HIGH, f = 1kHz, RLIN to RROUT, RRIN to RLOUT	–1.2	0.8	2.8	dB

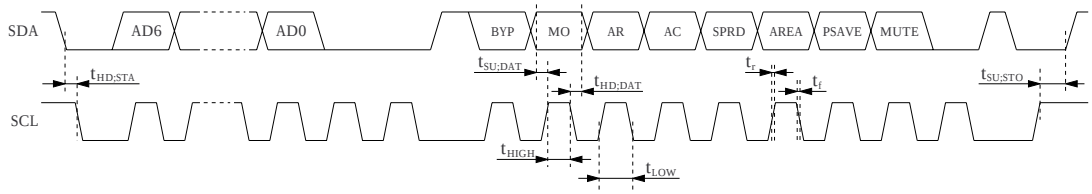
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
RIN to FOUT gain	G_{RF}	SPREAD = HIGH, BYP = LOW, AR = LOW, f = 1kHz, RLIN to FLOUT, RRIN to FROUT	8	10	12	dB
RIN to FOUT crosstalk gain	G_{RXF}	SPREAD = HIGH, BYP = LOW, AR = LOW, f = 1kHz, RLIN to FROUT, RRIN to FLOUT	8.5	10.5	12.5	dB
SCL clock pulse period	t_0	QS7777PF	100	–	–	ns
SCL clock HIGH-level pulsewidth	t_1	QS7777PF	40	–	–	ns
SCL clock LOW-level pulsewidth	t_2	QS7777PF	40	–	–	ns
SDA setup time	t_3	QS7777PF	15	–	–	ns
SDA hold time	t_4	QS7777PF	30	–	–	ns
STRB setup time	t_5	QS7777PF	50	–	–	ns
STRB clock pulsewidth	t_6	QS7777PF	100	–	–	ns
STRB hold time	t_7	QS7777PF	50	–	–	ns
SCL hold time	$t_{HD;STA}$	QS7777CF (I^2C)	4.0	–	–	µs
SCL setup time	$t_{SU;STO}$	QS7777CF (I^2C)	4.0	–	–	µs
SDA hold time	$t_{HD;DAT}$	QS7777CF (I^2C)	5.0	–	–	µs
SDA setup time	$t_{SU;DAT}$	QS7777CF (I^2C)	250	–	–	ns
SCL clock HIGH-level pulsewidth	t_{HIGH}	QS7777CF (I^2C)	4.0	–	–	µs
SCL clock LOW-level pulsewidth	t_{LOW}	QS7777CF (I^2C)	4.7	–	–	µs
SCL rise time	t_r	QS7777CF (I^2C)	–	–	1000	ns
SCL fall time	t_f	QS7777CF (I^2C)	–	–	300	ns

Serial Interface Timing

3-wire (QS7777PF) timing



I^2C 2-wire (QS7777CF) timing



AD6:0 represents the QS7777CF I^2C slave address 0011110.

FUNCTIONAL DESCRIPTION

Operating Modes (BYP, MO, AR, AC)

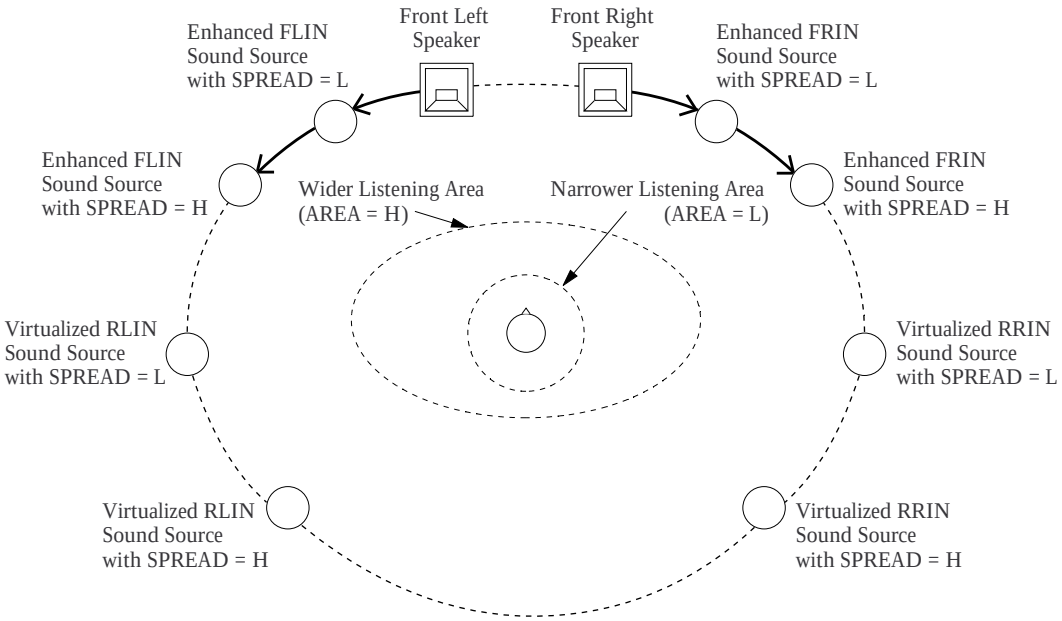
The control pins BYP, MO, AR, and AC select the operating mode bypass/QSurround signal processing of the FLIN, FRIN, RLIN, RRIN, CIN, and SUBIN input signals and determine the outputs on FLOUT, FROUT, RLOUT, RROUT, and COUT. The relationship between the inputs and outputs as selected by the control pins is shown in the following table.

Control pins				Output signals[1]								
BYP	MO	AR	AC	FLOUT			FROUT			RLOUT	RROUT	COUT
0	0	0	0	Qx(FLIN)	+Q1(RLIN)	+CIN	Qx(FRIN)	+Q1(RRIN)	+CIN			
0	0	0	1	Qx(FLIN)	+Q1(RLIN)		Qx(FRIN)	+Q1(RRIN)				CIN
0	0	1	0	Qx(FLIN)		+CIN	Qx(FRIN)		+CIN	q(RLIN)	q(RRIN)	
0	0	1	1	Qx(FLIN)			Qx(FRIN)			q(RLIN)	q(RRIN)	CIN
0	1	0	0	Qx(FLIN)	+Q1(M(R))	+CIN	Qx(FRIN)	+Q1(M(R))	+CIN			
0	1	0	1	Qx(FLIN)	+Q1(M(R))		Qx(FRIN)	+Q1(M(R))				CIN
0	1	1	0	Qx(FLIN)		+CIN	Qx(FRIN)		+CIN	q(M(R))	q(M(R))	
0	1	1	1	Qx(FLIN)			Qx(FRIN)			q(M(R))	q(M(R))	CIN
1	0	0	0	FLIN	+RLIN	+CIN	FRIN	+RRIN	+CIN			
1	0	0	1	FLIN	+RLIN		FRIN	+RRIN				CIN
1	0	1	0	FLIN		+CIN	FRIN		+CIN	RLIN	RRIN	
1	0	1	1	FLIN			FRIN			RLIN	RRIN	CIN
1	1	0	0	Q1(M(F))			Q1(M(F))					
1	1	0	1	Q1(M(F))			Q1(M(F))			q(M(F))	q(M(F))	
1	1	1	0	Qx(FLIN)			Qx(FRIN)			q(FLIN)	q(FRIN)	
1	1	1	1	FLIN			FRIN			FLIN	FRIN	

1. Qx( ), Q1( ), and q( ) = QSurround processed signals. For example, Qx(FLIN) indicates a QSurround-processed signal derived from FLIN input.
   R = RLIN + RRIN signal, and F = FLIN + FRIN signal.
   M( ) = monaural to stereo converted signal. For example, M(R) indicates monaural to stereo conversion of the RLIN+RRIN signal.
   The SUBIN signal is normally output on both FLOUT and FROUT.

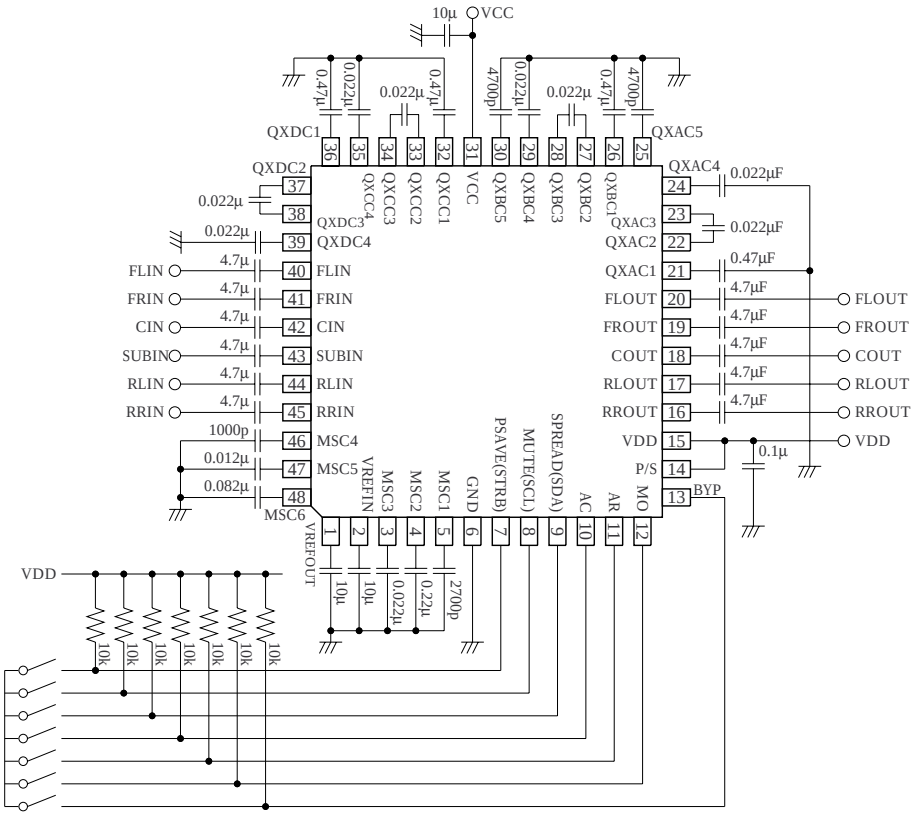
Controls (SPREAD, AREA)

The SPREAD input and AREA flag are used to control the FLOUT and FROUT signals in QSurround mode. In QSurround mode, the total sound heard is an enhanced version (virtual sound source) of the actual sound sources (speaker). When SPREAD is HIGH, the virtual sound source is widened, strengthening the surround enhancement effect. The AREA flag is used to widen the surround sound effect sweet-spot. This can be used for a larger listening audience. Note that AREA is set by serial input data only, and is therefore not available in parallel interface mode. The SPREAD and AREA control functions are shown in the following figure.

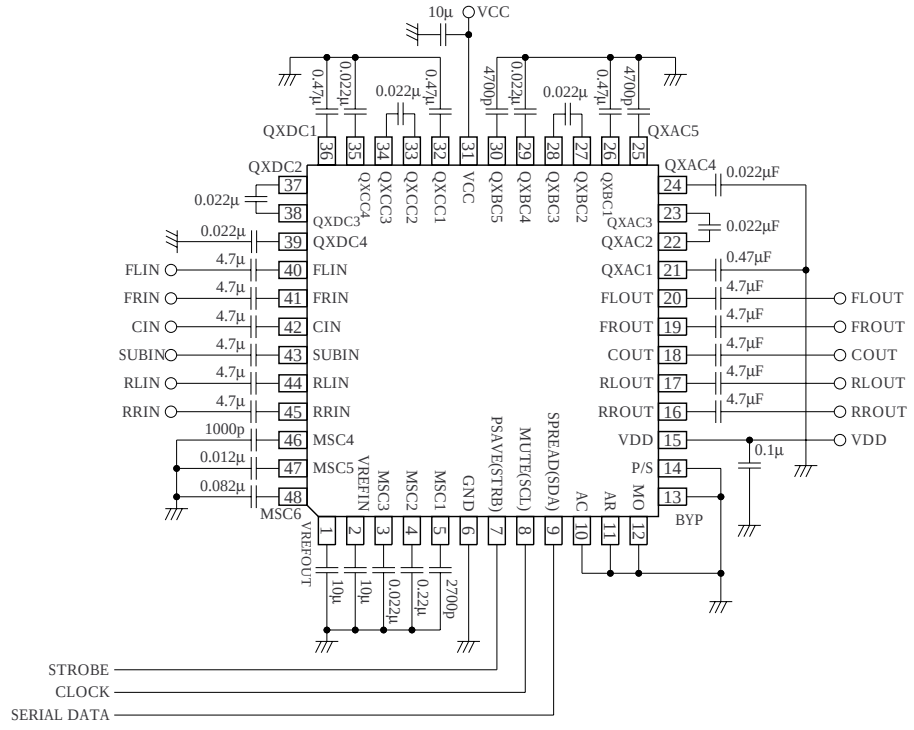


TYPICAL APPLICATION CIRCUITS

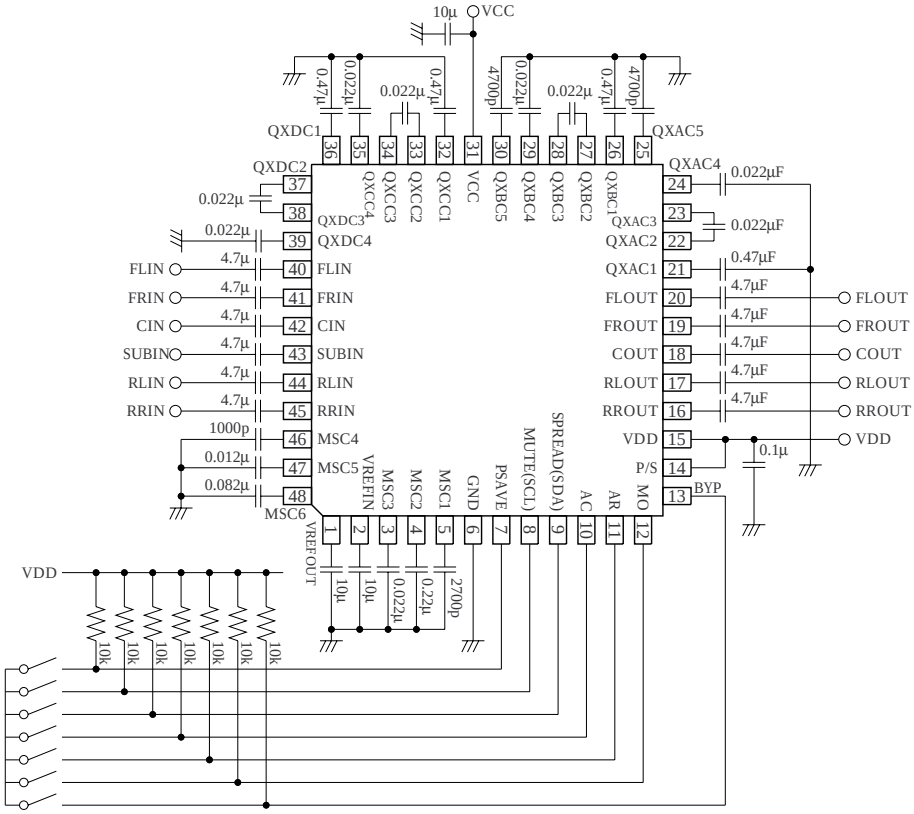
QS7777PF Parallel Interface



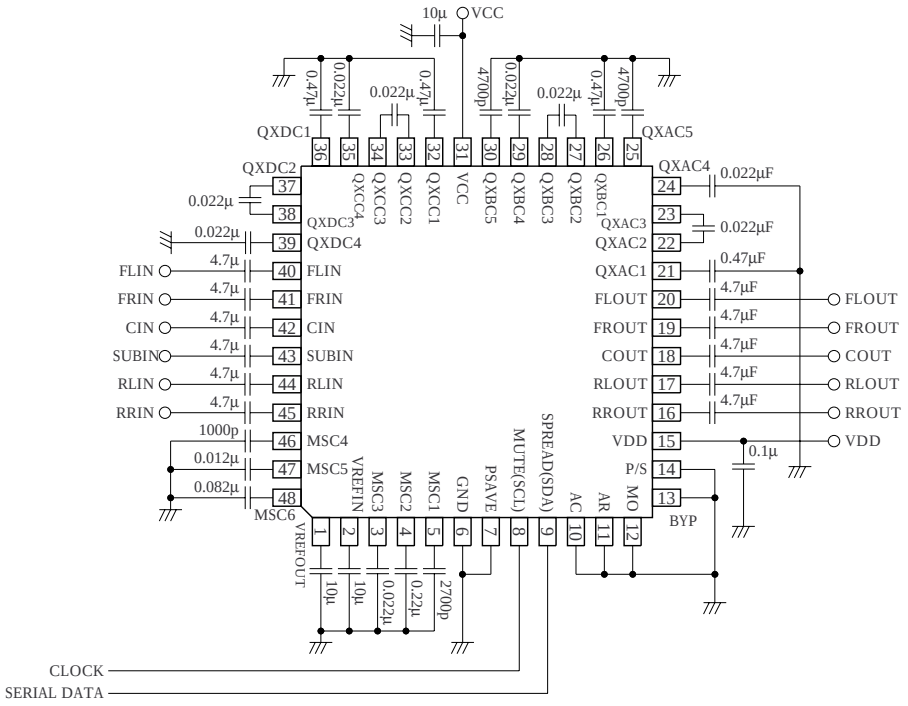
QS7777PF Serial Interface



QS7777CF Parallel Interface



QS7777CF Serial Interface



NPC
NIPPON PRECISION CIRCUITS INC.

NIPPON PRECISION CIRCUITS INC.

4-3, Fukuzumi 2-chome
Koto-ku, Tokyo 135-8430, Japan
Telephone: 03-3642-6661
Facsimile: 03-3642-6698

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