

M5M44258BP, J, L-7, -8, -10

STATIC COLUMN MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

DESCRIPTION

This is a family of 262144-word by 4-bit dynamic RAMs, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of triple-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage cell provide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

In addition to the $\overline{\text{RAS}}$ -only refresh mode, the hidden refresh mode and $\overline{\text{CS}}$ before $\overline{\text{RAS}}$ refresh mode are available.

FEATURES

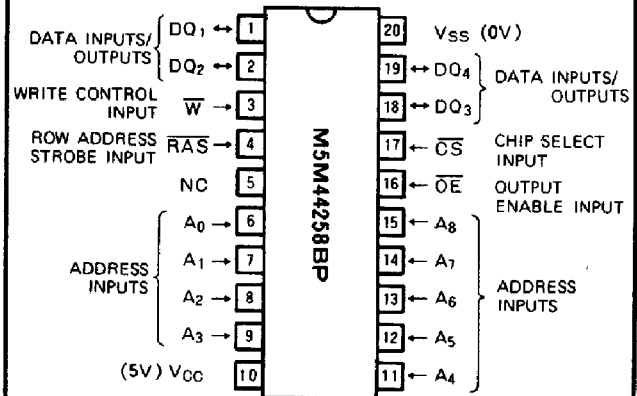
Type name	RAS access time (max ns)	CS access time (max ns)	Address access time (max ns)	OE access time (max ns)	Cycle time (min ns)	Power dissipation (typ mW)
M5M44258B-7	70	20	35	20	140	230
M5M44258B-8	80	20	40	20	160	200
M5M44258B-10	100	25	50	25	190	175

- High performance CMOS technology
- Standard 20 pin DIP, 26 pin SOJ, 20 pin ZIP
- Single 5V±10% supply
- Low stand-by power dissipation
2.75mW (max) CMOS Input level
- Low operating power dissipation
M5M44258BP, J, L-7 440mW (max)
M5M44258BP, J, L-8 385mW (max)
M5M44258BP, J, L-10 330mW (max)
- All inputs, outputs TTL compatible and low capacitance
- Tri-state unlatched output
- 512 refresh cycles/8ms
- Early write mode and $\overline{\text{OE}}$ control output buffer impedance
- Read-Modify-write, $\overline{\text{RAS}}$ -only refresh, Static column mode capabilities
- $\overline{\text{CS}}$ before $\overline{\text{RAS}}$ refresh mode capability
- $\overline{\text{CS}}$ controlled output allows hidden refresh
- Wide $\overline{\text{RAS}}$ pulse width for Static column mode 50µs (max)

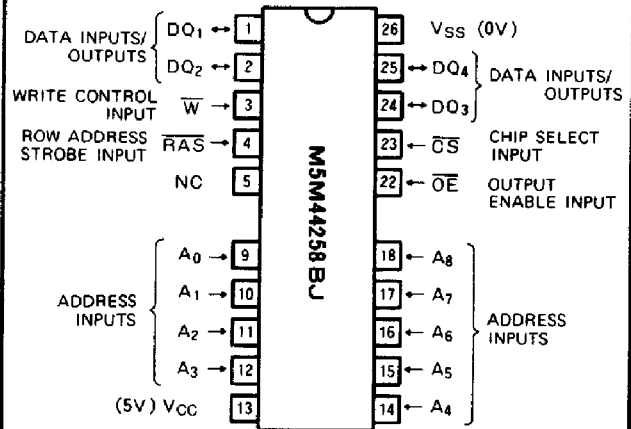
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

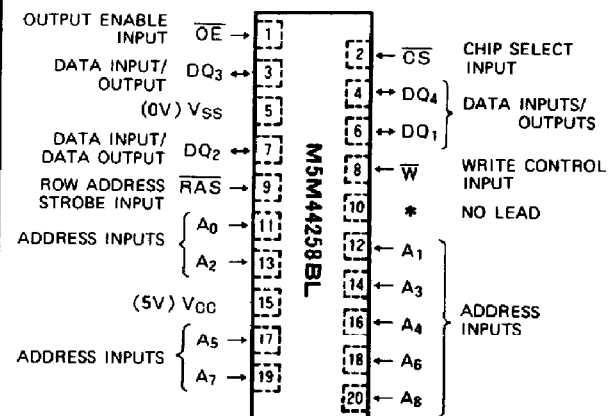
PIN CONFIGURATION (TOP VIEW)



Outline 20P4Y (DIP)



Outline 26P0J (SOJ)



Outline 20P5L-A(ZIP)

NC: NO CONNECTION

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FUNCTION

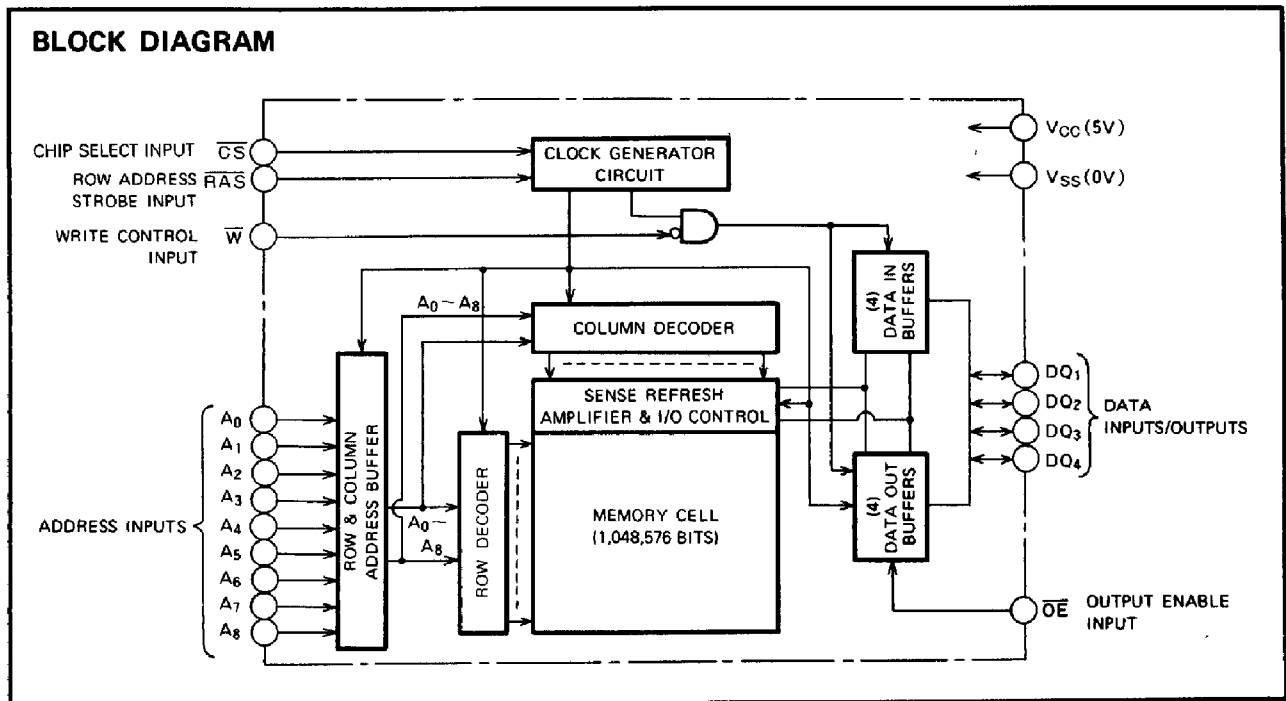
The M5M44258BP, J, L provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., static column mode, $\overline{\text{RAS}}$ -only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{\text{RAS}}$	$\overline{\text{CS}}$	$\overline{\text{W}}$	$\overline{\text{OE}}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Note
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Read-Modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
$\overline{\text{RAS}}$ -only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	ACT	APD	DNC	OPN	VLD	YES	
$\overline{\text{CS}}$ before $\overline{\text{RAS}}$ refresh	ACT	ACT	DNC	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note ACT active, NAC nonactive, DNC don't care, VLD valid, APD applied, OPN open
 Static column mode is identical except early write

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage	With respect to V _{SS}	-1~7	V
V _I	Input voltage		-1~7	V
V _O	Output voltage		-1~7	V
I _O	Output current		50	mA
P _d	Power dissipation	T _a = 25°C	1000	mW
T _{opr}	Operating temperature		0~70	°C
T _{stg}	Storage temperature		-65~150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = 0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V _{CC}	Supply voltage	4.5	5	5.5	V
V _{SS}	Supply voltage	0	0	0	V
V _{IH}	High-level input voltage, all inputs	2.4		6.5	V
V _{IL}	Low level input voltage, all inputs	-1.0		0.8	V

Note 1 All voltage values are with respect to V_{SS}

ELECTRICAL CHARACTERISTICS (T_a = 0~70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Note 2)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{OH}	High-level output voltage	I _{OH} = -5mA	2.4		V _{CC}	V
V _{OL}	Low level output voltage	I _{OL} = 4.2mA	0		0.4	V
I _{OZ}	Off state output current	Q floating 0V ≤ V _{OUT} ≤ 5.5V	-10		10	μA
I _I	Input current	0V ≤ V _{IH} ≤ 6.5V, Other inputs pins = 0V	-10		10	μA
I _{CC1(AV)}	Average supply current from V _{CC} , operating (Note 3, 4)	M5M44258B-7	R _{AS} , C _S cycling t _{RC} = t _{WC} = min, output open		80	mA
		M5M44258B-8			70	
		M5M44258B-10			60	
I _{CC2(AV)}	Average supply current from V _{CC} , stand-by (Note 6)	R _{AS} = C _S = V _{IH} , output open		2	mA	
		R _{AS} = C _S = 0E ≥ V _{CC} -0.5V, output open		0.5		
I _{CC3(AV)}	Average supply current from V _{CC} , refreshing (Note 3)	M5M44258B-7	R _{AS} cycling, C _S = V _{IH} t _{RC} = min, output open		80	mA
		M5M44258B-8			70	
		M5M44258B-10			60	
I _{CC6(AV)}	Average supply current from V _{CC} , C _S before R _{AS} refresh mode (Note 3)	M5M44258B-7	C _S before R _{AS} refresh cycling t _{RC} = min, output open		80	mA
		M5M44258B-8			70	
		M5M44258B-10			60	
I _{CC7(AV)}	Average supply current from V _{CC} , Static Column mode (Note 3, 4)	M5M44258B-7	R _{AS} = V _{IL} , Column address cycling t _{WSC} , t _{RSC} = min, output open		70	mA
		M5M44258B-8			60	
		M5M44258B-10			50	

Note 2 Current flowing into an IC is positive, out is negative

3 I_{CC1(AV)}, I_{CC3(AV)}, I_{CC6(AV)} and I_{CC7(AV)} are dependent on cycle rate, maximum current is measured at the fastest cycle rate

4 I_{CC1(AV)} and I_{CC7(AV)} are dependent on output loading. Specified values are obtained with the output open

CAPACITANCE (T_a = 0~70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C _{I(A)}	Input capacitance, address inputs (Note 5)	V _I = V _{SS} f = 1MHz Vi = 25mVrms			5	pF
C _{I(OE)}	Input capacitance, OE input				7	pF
C _{I(W)}	Input capacitance, write control input				7	pF
C _{I(RAS)}	Input capacitance, R _{AS} input				7	pF
C _{I(CS)}	Input capacitance, C _S input				7	pF
C _{I/O}	Input/Output capacitance, data ports				7	pF

Note 5 C_{I(A)} of ZIP is 6pF (max)

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SWITCHING CHARACTERISTICS (Ta = 0 ~ 70°C, VCC = 5V ± 10%, VSS = 0V, unless otherwise noted) (Note 6)

Symbol	Parameter	Limits						Unit
		M5M44258B-7		M5M44258B-8		M5M44258B-10		
		Min	Max	Min	Max	Min	Max	
t _{CAC}	Access time from \overline{CS} (Note 7, 8)		20		20		25	ns
t _{RAC}	Access time from \overline{RAS} (Note 7, 9)		70		80		100	ns
t _{CAA}	Column Address access time (Note 7, 10)		35		40		50	ns
t _{OE}	Access time from \overline{OE} (Note 7)		20		20		25	ns
t _{PWA}	Access time from previous \overline{W} low (Note 7)		65		70		85	ns
t _{WRA}	Access time from \overline{W} high (Note 7)		35		40		50	ns
t _{GLZ}	Output low impedance time from \overline{CS} low (Note 7)	5		5		5		ns
t _{OFF}	Output disable time after \overline{CS} high (Note 11)	0	20	0	20	0	25	ns
t _{dis(OE)}	Output disable time after \overline{OE} high (Note 11)	0	20	0	20	0	25	ns

- Note 6 An initial pause of 500μs is required after power up followed by any 8 \overline{RAS} or $\overline{RAS}/\overline{CS}$ cycles before proper device operation is achieved
 Note that \overline{RAS} may be cycled during the initial pause. And any 8 \overline{RAS} or $\overline{RAS}/\overline{CS}$ cycles are required after prolonged periods of \overline{RAS} inactivity before proper device operation is achieved
- 7 Measured with a load circuit equivalent to 2TTL loads and 100pF
- 8 Assume that $t_{RCD} \geq t_{RCD(max)}$, $t_{RAD} \leq t_{RAD(max)}$
- 9 Assume that $t_{RCD} \leq t_{RCD(max)}$, $t_{RAD} \leq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than $t_{RCD(max)}$ or $t_{RAD(max)}$ then t_{RAC} will increase by the amount that t_{RCD} or t_{RAD} exceeds $t_{RCD(max)}$ or $t_{RAD(max)}$
- 10 Assume that $t_{RCD} - t_{RAD} \leq t_{CAA(max)} - t_{CAC(max)}$ and $t_{RCD} \geq t_{RCD(max)}$
- 11 $t_{OFF(max)}$ and $t_{dis(OE)(max)}$ define the time at which the output achieves the high impedance state ($I_{OUT} \leq \pm 10\mu A$) and are not reference to $V_{OH(min)}$ or $V_{OL(max)}$

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Static Column Mode Cycles) (Ta = 0 ~ 70°C, VCC = 5V ± 10%, VSS = 0V, unless otherwise noted, See notes 12, 13)

Symbol	Parameter	Limits						Unit
		M5M44258B-7		M5M44258B-8		M5M44258B-10		
		Min	Max	Min	Max	Min	Max	
t _{REF}	Refresh cycle time		8		8		8	ms
t _{RP}	\overline{RAS} high pulse width	60		70		80		ns
t _{RCD}	Delay time, \overline{RAS} low to \overline{CS} low (Note 14)	20	50	25	60	25	75	ns
t _{CRP}	Delay time, \overline{CS} high to \overline{RAS} low (Note 15)	10		10		10		ns
t _{CPN}	\overline{CS} high pulse width	10		10		10		ns
t _{RAD}	Column address delay time from \overline{RAS} low (Note 16)	15	35	20	40	20	50	ns
t _{ASR}	Row address setup time before \overline{RAS} low	0		0		0		ns
t _{ASC}	Column address setup time before \overline{CS} low or \overline{W} low	0		0		0		ns
t _{RAH}	Row address hold time after \overline{RAS} low	10		15		15		ns
t _{CAH}	Column address hold time after \overline{CS} low or \overline{W} low	15		20		20		ns
t _T	Transition time (Note 17)	3	50	3	50	3	50	ns

- Note 12 The timing requirements are assumed $t_T = 5ns$
- 13 $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals
- 14 $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC} . If t_{RCD} is greater than $t_{RCD(max)}$, access time is controlled by exclusively t_{CAC} , $t_{RCD(min)}$ is specified as $t_{RCD(min)} = t_{RAH(min)} + 2t_T + t_{ASC(min)}$
- 15 t_{CRP} requirement is applicable for all $\overline{RAS}/\overline{CS}$ cycles
- 16 $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \geq t_{RAD(max)}$, access time is assumed by t_{CAA} for read cycle
- 17 t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$

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Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		M5M44258B-7		M5M44258B-8		M5M44258B-10		
		Min	Max	Min	Max	Min	Max	
t _{RC}	Read cycle time	140		160		190		ns
t _{RAS}	\overline{RAS} low pulse width	70	10000	80	10000	100	10000	ns
t _{CS}	\overline{CS} low pulse width	20	10000	20	10000	25	10000	ns
t _{CSH}	\overline{CS} hold time after \overline{RAS} low	70		80		100		ns
t _{RSH}	\overline{RAS} hold time after \overline{CS} low	20		20		25		ns
t _{RCS}	Read setup time before \overline{CS} low	0		0		0		ns
t _{RCH}	Read hold time after \overline{CS} high (Note 18)	0		0		0		ns
t _{RRH}	Read hold time after \overline{RAS} high (Note 18)	10		10		10		ns
t _{RAL}	Column address to \overline{RAS} setup time	35		40		50		ns
t _{AH}	Column address hold time after \overline{RAS} high	10		10		10		ns
t _{RPC}	Precharge to \overline{CS} active time	0		0		0		ns
t _{h(CLOE)}	\overline{OE} hold time after \overline{CS} low	20		20		25		ns
t _{h(RLOE)}	\overline{OE} hold time after \overline{RAS} low	70		80		100		ns
t _{DOEL}	Delay time, Data to \overline{OE} low	0		0		0		ns
t _{OEHD}	Delay time, \overline{OE} high to Data	15		15		20		ns
t _{h(OECH)}	\overline{CS} hold time after \overline{OE} low	20		20		25		ns
t _{h(OERH)}	\overline{RAS} hold time after \overline{OE} low	20		20		25		ns

Note 18 Either t_{RCH} or t_{RRH} must be satisfied for a read cycle

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits						Unit
		M5M44258B-7		M5M44258B-8		M5M44258B-10		
		Min	Max	Min	Max	Min	Max	
t _{WC}	Write cycle time	140		160		190		ns
t _{RAS}	\overline{RAS} low pulse width	70	10000	80	10000	100	10000	ns
t _{CS}	\overline{CS} low pulse width	20	10000	20	10000	25	10000	ns
t _{CSH}	\overline{CS} hold time after \overline{RAS} low	70		80		100		ns
t _{RSH}	\overline{RAS} hold time after \overline{CS} low	20		20		25		ns
t _{CWL}	\overline{CS} hold time after write low	20		20		25		ns
t _{RWL}	\overline{RAS} hold time after write low	20		20		25		ns
t _{WH}	Write command hold time for output disable	0		0		0		ns
t _{WCS}	Write setup time before \overline{CS} low (Note 20)	0		0		0		ns
t _{WCH}	Write hold time after \overline{CS} low	15		15		20		ns
t _{AH}	Column address hold time after \overline{RAS} high	10		10		10		ns
t _{WP}	Write pulse width	15		15		20		ns
t _{DS}	Data setup time	0		0		0		ns
t _{DH}	Data hold time after \overline{CS} low	15		15		20		ns
t _{OEHD}	Delay time, \overline{OE} high to Data	15		15		20		ns
t _{h(WOE)}	\overline{OE} hold time after write low	15		15		20		ns

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Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits						Unit
		M5M44258B-7		M5M44258B-8		M5M44258B-10		
		Min	Max	Min	Max	Min	Max	
t _{RWC}	Read-write/read-modify-write cycle time (Note 19)	185		205		245		ns
t _{RAS}	$\overline{\text{RAS}}$ low pulse width	115	10000	125	10000	155	10000	ns
t _{CS}	$\overline{\text{CS}}$ low pulse width	65	10000	65	10000	80	10000	ns
t _{CSH}	$\overline{\text{CS}}$ hold time after $\overline{\text{RAS}}$ low	115		125		155		ns
t _{RSH}	$\overline{\text{RAS}}$ hold time after $\overline{\text{CS}}$ low	65		65		80		ns
t _{RCS}	Read setup time before $\overline{\text{CS}}$ low	0		0		0		ns
t _{CWD}	Delay time, $\overline{\text{CS}}$ low to write low (Note 20)	40		40		50		ns
t _{RWD}	Delay time, $\overline{\text{RAS}}$ low to write low (Note 20)	90		100		125		ns
t _{CWL}	$\overline{\text{CS}}$ hold time after write low	20		20		25		ns
t _{RWL}	$\overline{\text{RAS}}$ hold time after write low	20		20		25		ns
t _{WP}	Write pulse width	15		15		20		ns
t _{DS}	Data setup time	0		0		0		ns
t _{DH}	Data hold time after write low	15		15		20		ns
t _{AWD}	Delay time, address to write low (Note 20)	55		60		75		ns
t _{h(CLOE)}	$\overline{\text{OE}}$ hold time after $\overline{\text{CS}}$ low	20		20		25		ns
t _{h(RLOE)}	$\overline{\text{OE}}$ hold time after $\overline{\text{RAS}}$ low	70		80		100		ns
t _{DOEL}	Delay time, Data to $\overline{\text{OE}}$ low	0		0		0		ns
t _{OEHD}	Delay time, $\overline{\text{OE}}$ high to Data	15		15		20		ns
t _{h(WOE)}	$\overline{\text{OE}}$ hold time after write low	15		15		20		ns

Note 19 t_{RWC} is specified as t_{RWC}(min) = t_{RAC}(max) + t_{OEHD}(min) + t_{RWL}(min) + t_{RP}(min) + 4t_τ

20 t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are specified as reference points only. If t_{WCS} ≥ t_{WCS}(min), the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If t_{CWD} ≥ t_{CWD}(min), t_{RWD} ≥ t_{RWD}(min) and t_{AWD} ≥ t_{AWD}(min), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the DQ (at access time and until $\overline{\text{CS}}$ or $\overline{\text{OE}}$ goes back to V_{IH}) is indeterminate.

Static Column Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycles)

Symbol	Parameter	Limits						Unit
		M5M44258B-7		M5M44258B-8		M5M44258B-10		
		Min	Max	Min	Max	Min	Max	
t _{RSC}	SC read cycle time	40		45		55		ns
t _{WSC}	SC write cycle time	40		45		55		ns
t _{RWSC}	SC R/W, R/M/W, cycle time	90		95		115		ns
t _{RAS}	$\overline{\text{RAS}}$ low pulse width	110	50000	125	50000	155	50000	ns
t _{CS}	$\overline{\text{CS}}$ low pulse width	20	10000	20	10000	25	10000	ns
t _{CP}	$\overline{\text{CS}}$ high pulse width	10		10		10		ns
t _{RSW}	Delay time, $\overline{\text{RAS}}$ to 2nd Write low	80		90		110		ns
t _{WI}	Write invalid time	10		10		10		ns
t _{PWH}	Column address hold time to previous $\overline{\text{W}}$ low	65		70		85		ns
t _{WH}	Write command hold time for output disable	0		0		0		ns
t _{AOH}	Data hold time from address change	10		10		10		ns
t _{WAD}	Delay time write to address change (Note 21)	20	30	20	30	25	35	ns
t _{RSH}	$\overline{\text{RAS}}$ hold time after $\overline{\text{CS}}$ low	20		20		25		ns
t _{h(WHOE)}	$\overline{\text{OE}}$ hold time after write high	45		50		60		ns

Note 21 t_{WAD}(max) is specified as a reference point only. If t_{WAD} ≥ t_{WAD}(max), access time is assumed by t_{CAA}.

$\overline{\text{CS}}$ before $\overline{\text{RAS}}$ Refresh Cycle (Note 22)

Symbol	Parameter	Limits						Unit
		M5M44258B-7		M5M44258B-8		M5M44258B-10		
		Min	Max	Min	Max	Min	Max	
t _{CSR}	$\overline{\text{CS}}$ setup time for $\overline{\text{CS}}$ before $\overline{\text{RAS}}$ refresh	10		10		10		ns
t _{CHR}	$\overline{\text{CS}}$ hold time for $\overline{\text{CS}}$ before $\overline{\text{RAS}}$ refresh	15		15		20		ns
t _{RPC}	Precharge to $\overline{\text{CS}}$ active time	0		0		0		ns

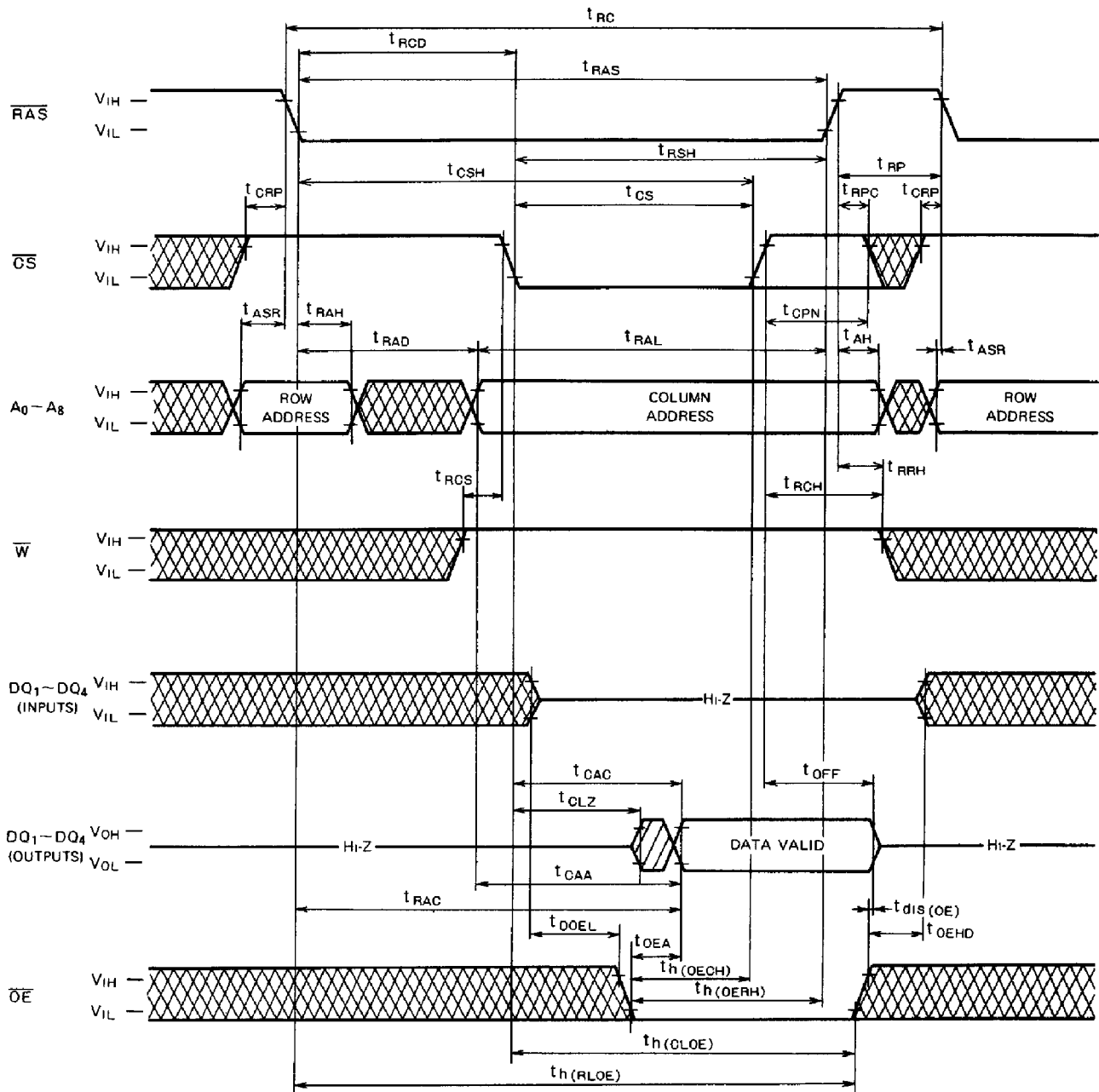
Note 22 Eight or more $\overline{\text{CS}}$ before $\overline{\text{RAS}}$ cycles instead of eight $\overline{\text{RAS}}$ cycles are necessary for proper operation of $\overline{\text{CS}}$ before $\overline{\text{RAS}}$ refresh mode.

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Timing Diagrams (Note 23)

Read Cycle



Note 23



Indicates the invalid output.
 $V_{IH(min)} \leq V_{IN} \leq V_{IH(max)}$ or $V_{IL(min)} \leq V_{IN} \leq V_{IL(max)}$

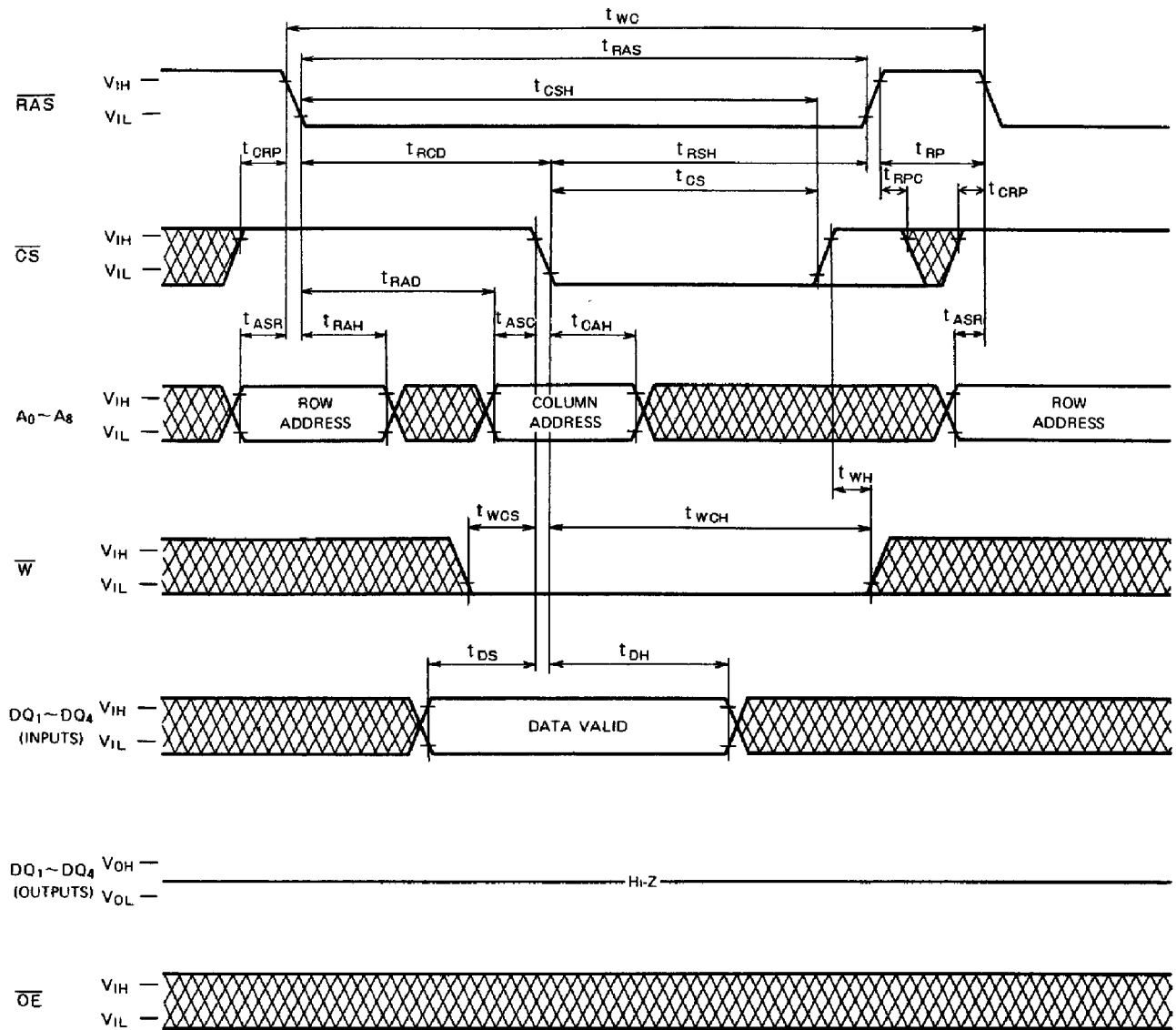


Indicates the invalid output

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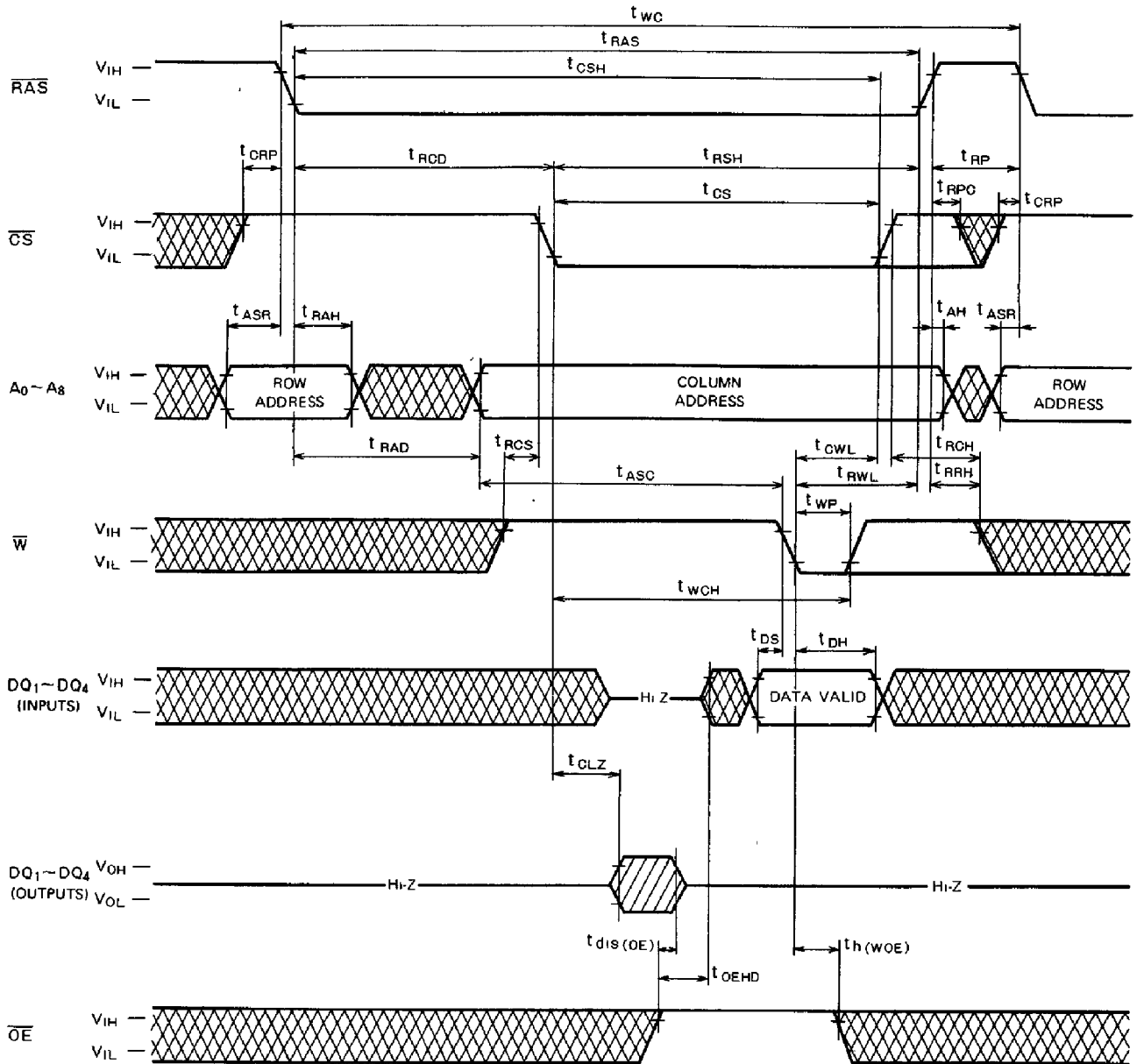
Write Cycle (Early write)



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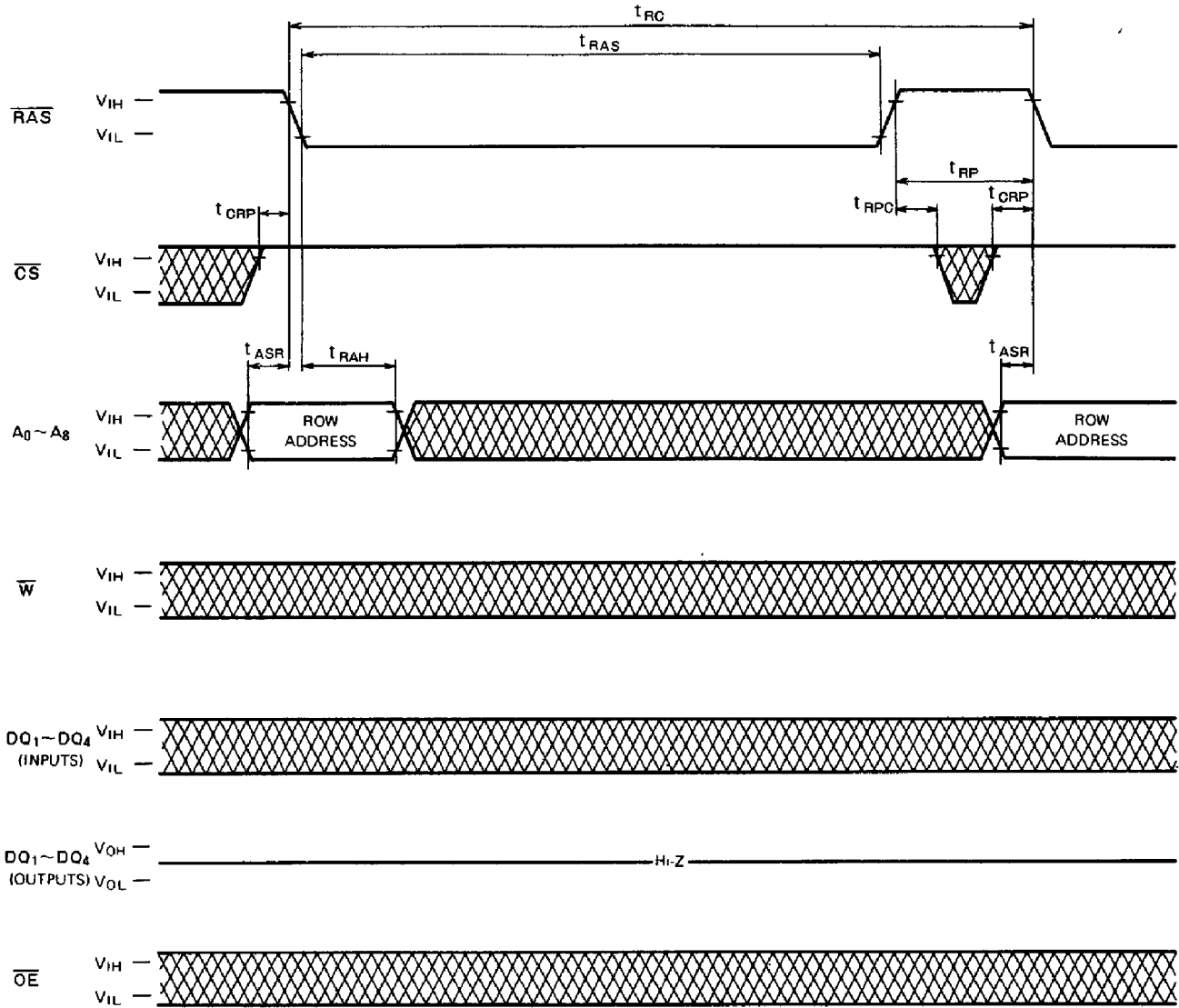
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Write Cycle (Delayed Write)



STATIC COLUMN MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

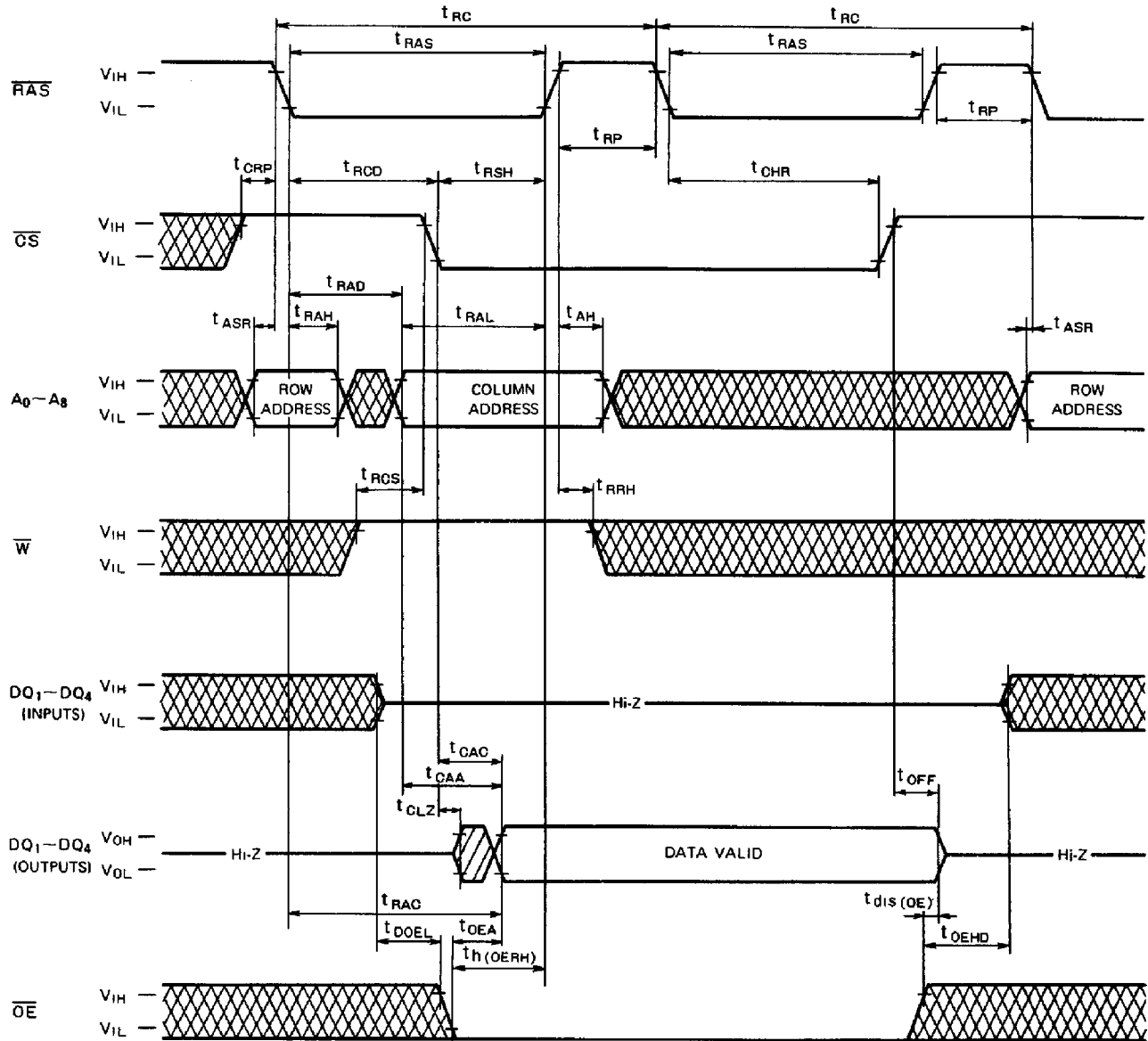
RAS-only Refresh Cycle



MITSUBISHI LSIs
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STATIC COLUMN MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

Hidden Refresh Cycle (Read) (Note 24)

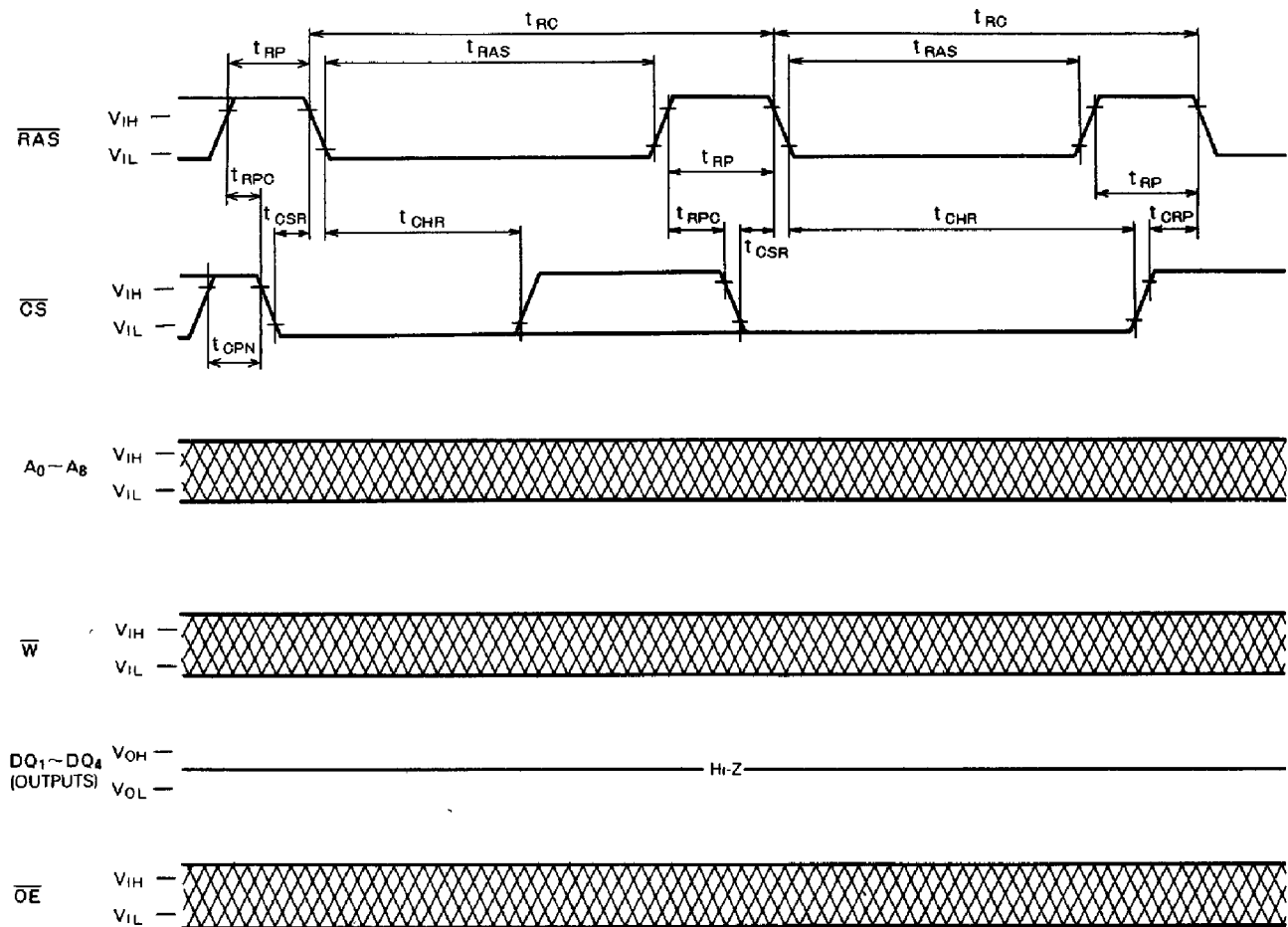


Note 24. Early write, delayed write, read-write or read-modify-write cycle is applicable instead of read cycle. Timing requirements and output state are the same as that of each cycle shown before.

M5M44258BP, J, L-7, -8, -10

STATIC COLUMN MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

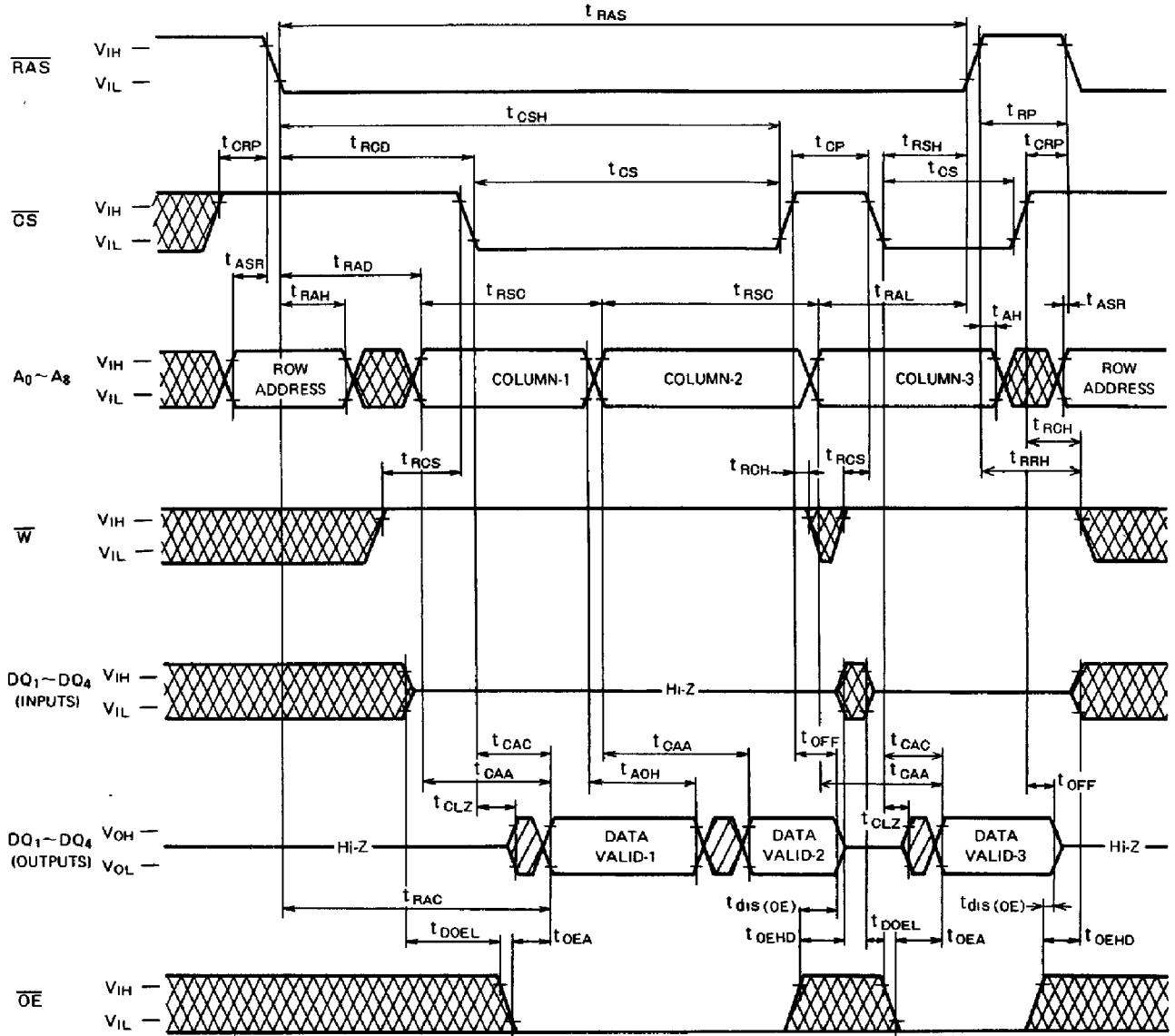
$\overline{\text{CS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle



M5M44258BP, J, L-7, -8, -10

STATIC COLUMN MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

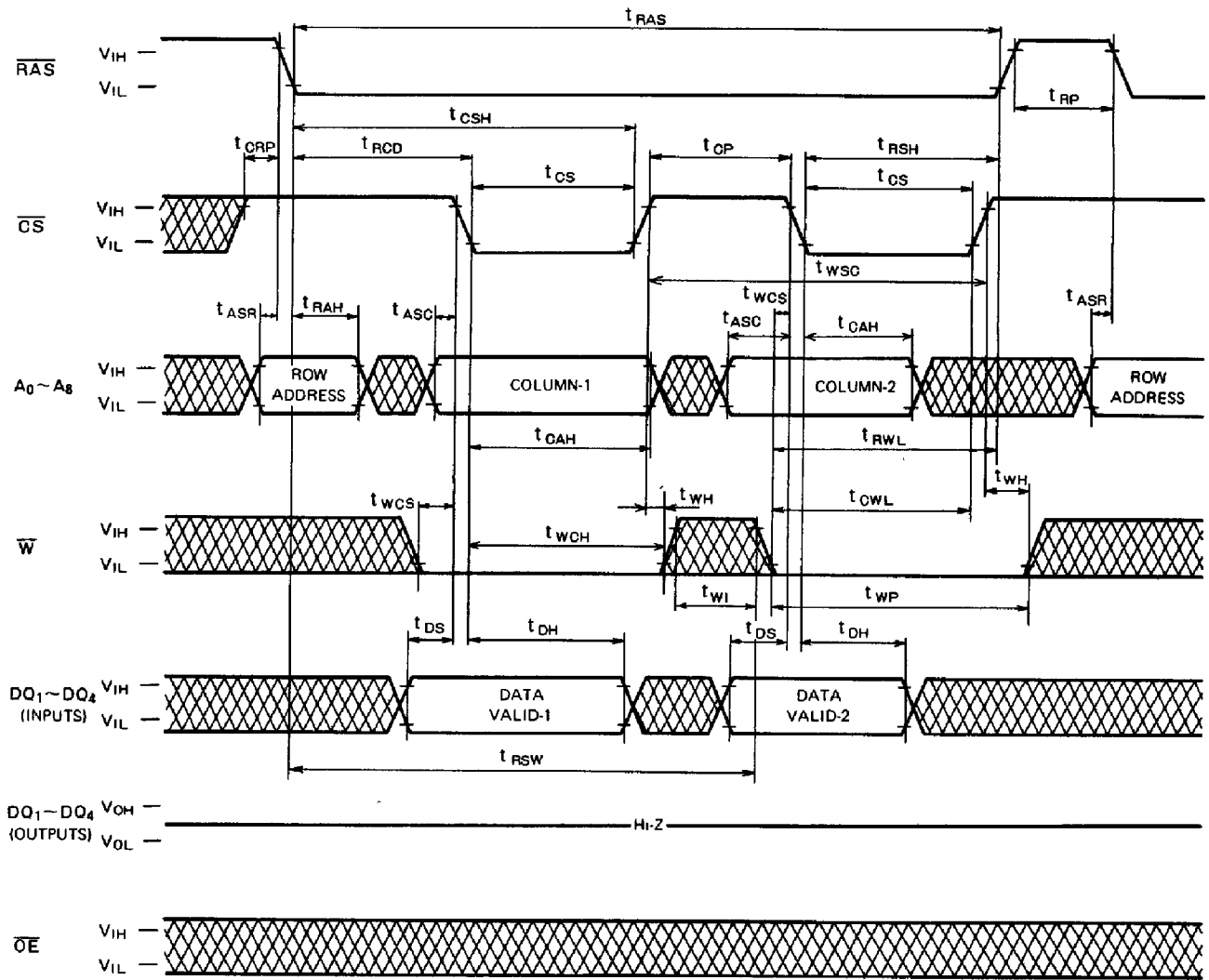
Static Column Mode Read Cycle



MITSUBISHI LSIs
M5M44258BP, J, L-7, -8, -10

STATIC COLUMN MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

Static Column Mode Write Cycle (Early Write)



MITSUBISHI LSIs
M5M44258BP, J, L-7, -8, -10

STATIC COLUMN MODE 1048576-BIT (262144-WORD BY 4-BIT) DYNAMIC RAM

Static Column Mode Write Cycle (Delayed Write)

