

ASSP

Dual Serial Input PLL Frequency Synthesizer

MB15F73SP

■ DESCRIPTION

The Fujitsu MB15F73SP is a serial input Phase Locked Loop (PLL) frequency synthesizer with a 2000 MHz prescaler and a 600 MHz prescaler. A 64/65 or a 128/129 for the 2000 MHz prescaler, and a 8/9 or a 16/17 for the 600 MHz prescaler can be selected for the prescaler that enables pulse swallow operation.

MB15F73SP has the same configuration with MB15F03 or MB15F03L. The BiCMOS process is used, as a result a supply current is typically 3.5 mA at 2.7 V. The supply voltage range is from 2.4 V to 3.6 V. A refined charge pump supplies well-balanced output current with 1.5 mA and 6 mA selectable by serial data.

The new package (BCC20) decreases an area of MB15F73SP more than 30 % comparing with the former BCC16 (for dual PLL).

MB15F73SP is ideally suited for wireless mobile communications, such as PDC.

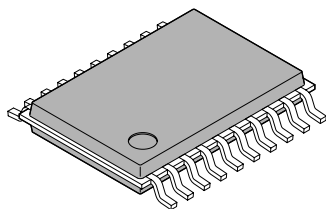
■ FEATURES

- High frequency operation : RF synthesizer : 2000 MHz max
: IF synthesizer : 600 MHz max
- Low power supply voltage : $V_{CC} = 2.4$ to 3.6 V
- Ultra Low power supply current : $I_{CC} = 3.5$ mA typ.
($V_{CC} = V_p = 2.7$ V, $T_a = +25^\circ\text{C}$, $SW_{IF} = SW_{RF} = 0$ in IF/RF locking state)

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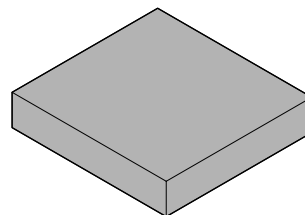
■ PACKAGES

20-pin plastic TSSOP



(FPT-20P-M06)

20-pad plastic BCC



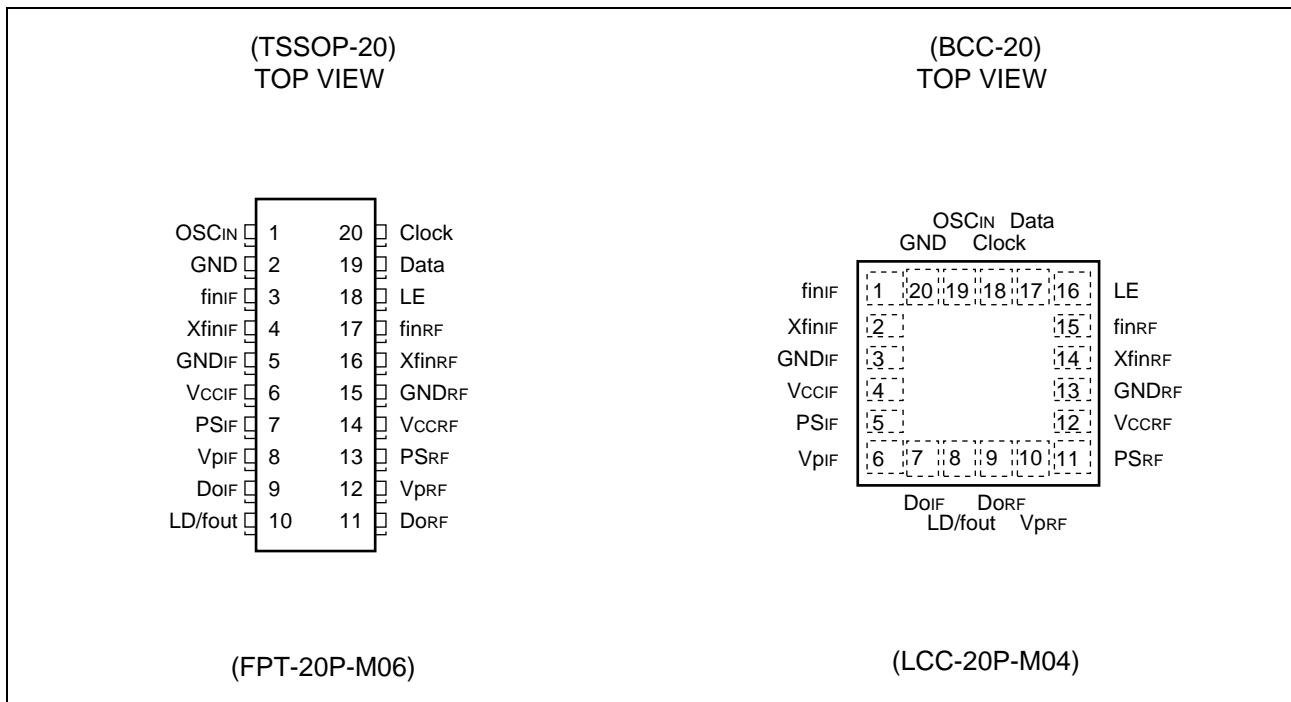
(LCC-20P-M04)

MB15F73SP

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- Direct power saving function: Power supply current in power saving mode
 Typ. 0.1 μ A ($V_{CC} = V_p = 2.7$ V, $T_a = +25^\circ\text{C}$)
 Max. 10 μ A ($V_{CC} = V_p = 2.7$ V)
- Software selectable charge pump current: 1.5 mA/6.0 mA typ.
- Dual modulus prescaler: 2000 MHz prescaler (64/65 or 128/129)/600 MHz prescaler (8/9 or 16/17)
- 23 bit shift register
- Serial input binary 14-bit programmable reference divider: R = 3 to 16,383
- Serial input programmable divider consisting of:
 - Binary 7-bit swallow counter: 0 to 127
 - Binary 11-bit programmable counter: 3 to 2,047
- Built-in high-speed tuning, low-noise phase comparator, current-switching type constant current circuit
- On-chip phase control for phase comparator
- Built-in digital locking detector circuit to detect PLL locking and unlocking
- Operating temperature: $T_a = -40$ to $+85^\circ\text{C}$
- Sireal data format compatible with MB15F02SL

■ PIN ASSIGNMENTS

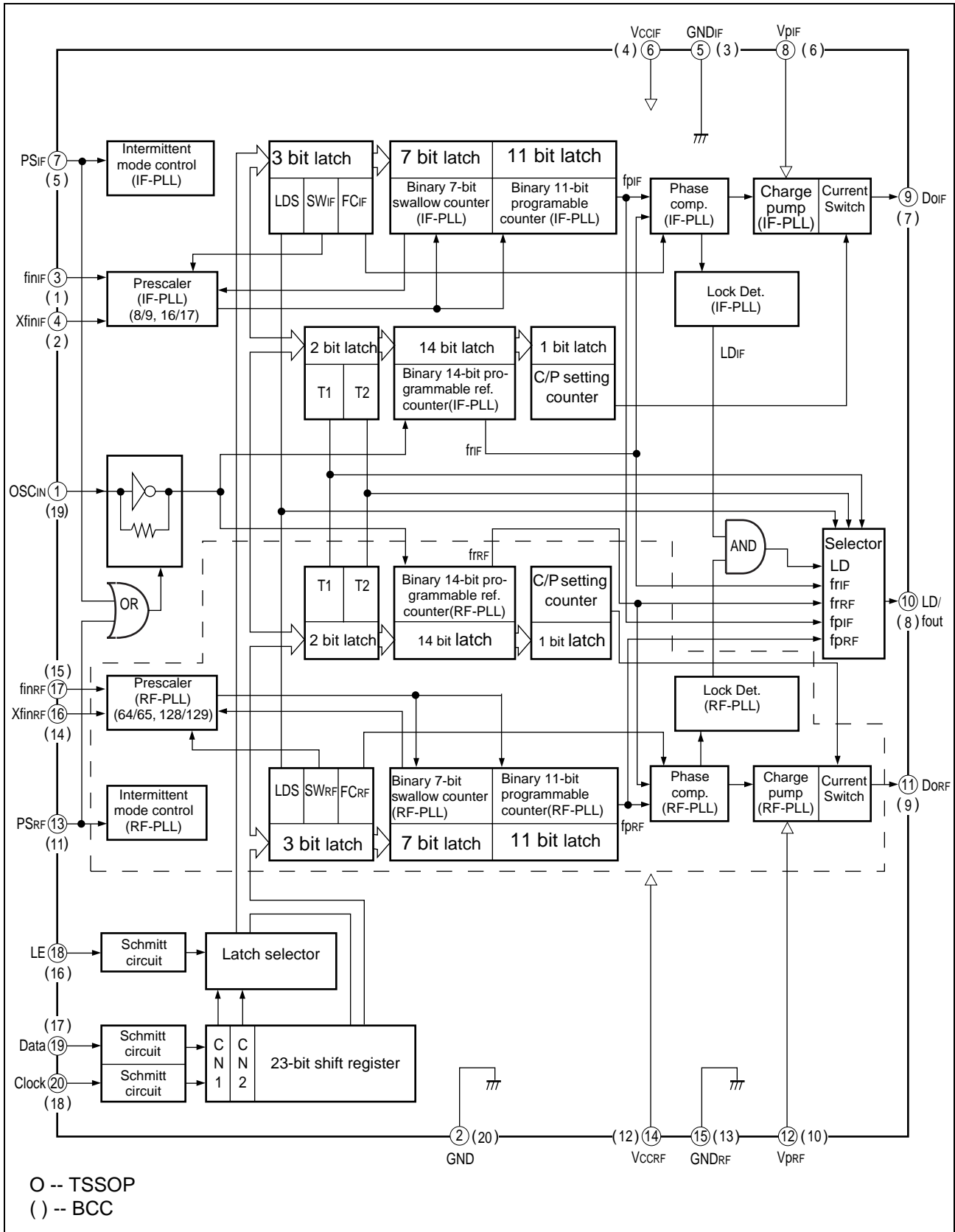


■ PIN DESCRIPTION

Pin no.		Pin name	I/O	Descriptions
TSSOP	BCC			
1	19	OSC _{IN}	I	The programmable reference divider input. TCXO should be connected with a AC coupling capacitor.
2	20	GND	—	Ground for OSC input buffer and the shift register circuit.
3	1	fin _{IF}	I	Prescaler input pin for the IF-PLL. Connection to an external VCO should be AC coupling.
4	2	Xfin _{IF}	I	Prescaler complimentary input for the IF-PLL section. This pin should be grounded via a capacitor.
5	3	GND _{IF}	—	Ground for the IF-PLL section.
6	4	V _{CCIF}	—	Power supply voltage input pin for the IF-PLL section (except for the charge pump circuit), the shift register and the oscillator input buffer.
7	5	PS _{IF}	I	Power saving mode control for the IF-PLL section. This pin must be set at "L" Power-On. (Open is prohibited.) PS _{IF} = "H" ; Normal mode / PS _{IF} = "L" ; Power saving mode
8	6	V _{pIF}	—	Power supply voltage input pin for the IF-PLL charge pump.
9	7	Do _{IF}	O	Charge pump output for the IF-PLL section.
10	8	LD/fout	O	Look detect signal output (LD)/ phase comparator monitoring output (fout). The output signal is selected by a LDS bit in a serial data. LDS bit = "H" ; outputs fout signal / LDS bit = "L" ; outputs LD signal
11	9	Do _{RF}	O	Charge pump output for the RF-PLL section.
12	10	V _{pRF}	—	Power supply voltage input pin for the RF-PLL charge pump.
13	11	PS _{RF}	I	Power saving mode control for the RF-PLL section. This pin must be set at "L" Power-ON. (Open is prohibited.) PS _{RF} = "H" ; Normal mode / PS _{RF} = "L" ; Power saving mode
14	12	V _{CCRF}	—	Power supply voltage input pin for the RF-PLL section (except for the charge pump circuit).
15	13	GND _{RF}	—	Ground for the RF-PLL section.
16	14	Xfin _{RF}	I	Prescaler complimentary input for the RF-PLL section. This pin should be grounded via a capacitor.
17	15	fin _{RF}	I	Prescaler input pin for the RF-PLL. Connection to an external VCO should be AC coupling.
18	16	LE	I	Load enable signal input (with the schmitt trigger circuit.) When LE is set "H", data in the shift register is transferred to the corresponding latch according to the control bit in a serial data.
19	17	Data	I	Serial data input (with the schmitt trigger circuit.) A data is transferred to the corresponding latch (IF-ref. counter, IF-prog. counter, RF-ref. counter, RF-prog. counter) according to the control bit in a serial data.
20	18	Clock	I	Clock input for the 23-bit shift register (with the schmitt trigger circuit.) One bit data is shifted into the shift register on a rising edge of the clock.

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■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating		Unit
			Min.	Max.	
Power supply voltage		V_{CC}	-0.5	4.0	V
		V_p	V_{CC}	4.0	V
Input voltage		V_i	-0.5	$V_{CC} + 0.5$	V
Output voltage	LD/fout	V_o	GND	V_{CC}	V
	Do	V_{Do}	GND	V_p	V
Storage temperature		T_{stg}	-55	+125	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Value			Unit
			Min.	Typ.	Max.	
Power supply voltage		V_{CC}	2.4	2.7	3.6	V
		V_p	V_{CC}	2.7	3.6	V
Input voltage		V_i	GND	—	V_{CC}	V
Operating temperature		T_a	-40	—	+85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

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■ ELECTRICAL CHARACTERISTICS

($V_{CC} = 2.4 \text{ V to } 3.6 \text{ V}$, $T_a = -40 \text{ }^\circ\text{C to } +85 \text{ }^\circ\text{C}$)

Parameter	Symbol	Condition	Value			Unit	
			Min.	Typ.	Max.		
Power supply current	I_{CCIF}^{*1}	IF PLL	—	1.3	—	mA	
	I_{CCRF}^{*2}	RF PLL	—	2.2	—	mA	
Power saving current	I_{PSIF}	$PS_{IF} = PS_{RF} = \text{“L”}$	—	0.1^{*8}	10	μA	
	I_{PSRF}	$PS_{IF} = PS_{RF} = \text{“L”}$	—	0.1^{*8}	10	μA	
Operating frequency	fin_{IF}^{*3}	fin_{IF}	IF PLL	50	—	600	MHz
	fin_{RF}^{*3}	fin_{RF}	RF PLL	100	—	2000	MHz
	OSC_{IN}	f_{OSC}	—	3	—	40	MHz
Input sensitivity	fin_{IF}	$P_{fin_{IF}}$	IF PLL, 50Ω system	-15	—	+2	dBm
	fin_{RF}	$P_{fin_{RF}}$	RF PLL, 50Ω system	-15	—	+2	dBm
Input available voltage	OSC_{IN}	V_{OSC}	—	0.5	—	V_{CC}	V_{P-P}
“H” level input voltage	Data LE	V_{IH}	Schmitt trigger input	$0.7 V_{CC} + 0.4$	—	—	V
“L” level input voltage	Clock	V_{IL}	Schmitt trigger input	—	—	$0.3 V_{CC} - 0.4$	V
“H” level input voltage	PS_{IF}	V_{IH}	—	$0.7 V_{CC}$	—	—	V
“L” level input voltage	PS_{RF}	V_{IL}	—	—	—	$0.3 V_{CC}$	V
“H” level input current	Data LE	I_{IH}^{*4}	—	-1.0	—	+1.0	μA
“L” level input current	Clock PS	I_{IL}^{*4}	—	-1.0	—	+1.0	μA
“H” level input current	OSC_{IN}	I_{IH}	—	0	—	+100	μA
“L” level input current		I_{IL}^{*4}	—	-100	—	0	μA
“H” level output voltage	LD/ f_{out}	V_{OH}	$V_{CC} = V_p = 2.7 \text{ V}$, $I_{OH} = -1 \text{ mA}$	$V_{CC} - 0.4$	—	—	V
“L” level output voltage		V_{OL}	$V_{CC} = V_p = 2.7 \text{ V}$, $I_{OL} = 1 \text{ mA}$	—	—	0.4	V
“H” level output voltage	DO_{IF}	V_{DOH}	$V_{CC} = V_p = 2.7 \text{ V}$, $I_{DOH} = -0.5 \text{ mA}$	$V_p - 0.4$	—	—	V
“L” level output voltage	DO_{RF}	V_{DOL}	$V_{CC} = V_p = 2.7 \text{ V}$, $I_{DOL} = 0.5 \text{ mA}$	—	—	0.4	V
High impedance cutoff current	DO_{IF} DO_{RF}	I_{OFF}	$V_{CC} = V_p = 2.7 \text{ V}$ $V_{OFF} = 0.5 \text{ V to } V_p - 0.5 \text{ V}$	—	—	2.5	nA
“H” level output current	LD/ f_{out}	I_{OH}^{*4}	$V_{CC} = V_p = 2.7 \text{ V}$	—	—	-1.0	mA
“L” level output current		I_{OL}	$V_{CC} = V_p = 2.7 \text{ V}$	1.0	—	—	mA

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($V_{CC} = 2.4\text{ V to }3.6\text{ V}$, $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$)

Parameter	Symbol	Condition	Value			Unit	
			Min.	Typ.	Max.		
“H” level output current	DoIF DoRF	IDOH *4 $V_{CC} = V_p = 2.7\text{ V}$, $V_{DOH} = V_p / 2$, $T_a = +25\text{ }^\circ\text{C}$	CS bit = “H”	—	-6.0	—	mA
			CS bit = “L”	—	-1.5	—	mA
“L” level output current	DoIF DoRF	IDOL $V_{CC} = V_p = 2.7\text{ V}$, $V_{DOL} = V_p / 2$, $T_a = +25\text{ }^\circ\text{C}$	CS bit = “H”	—	6.0	—	mA
			CS bit = “L”	—	1.5	—	mA
Charge pump current rate	IDOL/IDOH	IDOMT *5 $V_{DO} = V_p / 2$	—	3	—	%	
	vs VDO	IDOVD *6 $0.5\text{ V} \leq V_{DO} \leq V_p - 0.5\text{ V}$	—	10	—	%	
	vs Ta	IDOTA *7 $-40\text{ }^\circ\text{C} \leq T_a \leq 85\text{ }^\circ\text{C}$, $V_{DO} = V_p / 2$	—	10	—	%	

*1 : $f_{inIF} = 480\text{ MHz}$, $f_{osc} = 12.8\text{ MHz}$, $V_{CCIF} = V_{pIF} = 2.7\text{ V}$, $SW_{IF} = 0$, $T_a = +25\text{ }^\circ\text{C}$, in locking state.

*2 : $f_{inRF} = 2000\text{ MHz}$, $f_{osc} = 12.8\text{ MHz}$, $V_{CCRF} = V_{pRF} = 2.7\text{ V}$, $SW_{RF} = 0$, $T_a = +25\text{ }^\circ\text{C}$, in locking state.

*3 : AC coupling. 1000 pF capacitor is connected under the condition of minimum operating frequency.

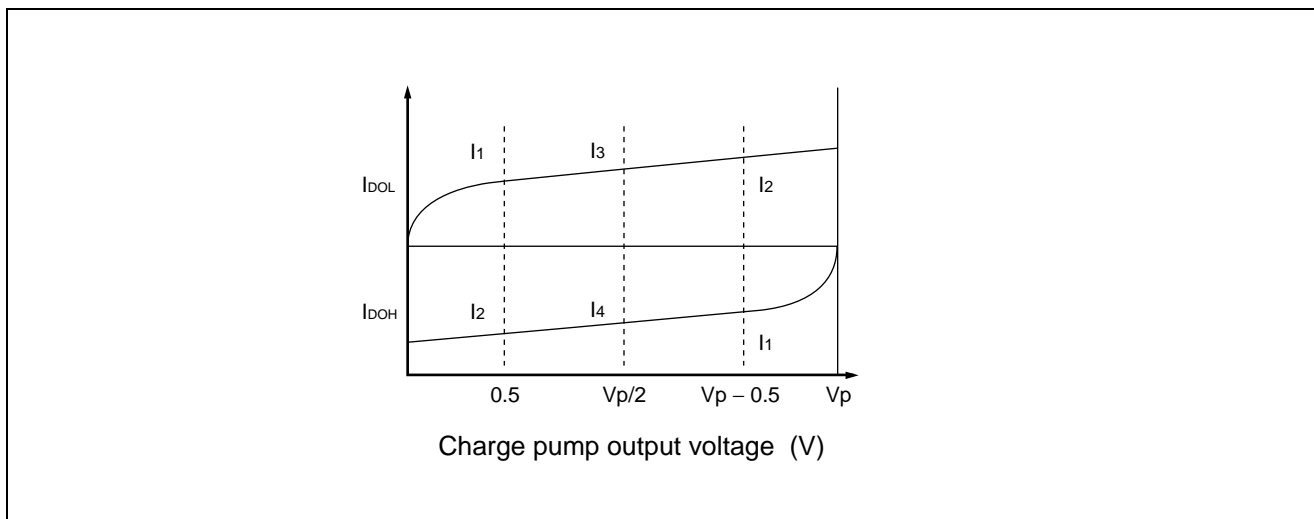
*4 : The symbol “-” (minus) means direction of current flow.

*5 : $V_{CC} = V_p = 2.7\text{ V}$, $T_a = +25\text{ }^\circ\text{C}$
 $(|I_3| - |I_4|) / [(|I_3| + |I_4|) / 2] \times 100\text{ }(\%)$

*6 : $V_{CC} = V_p = 2.7\text{ V}$, $T_a = +25\text{ }^\circ\text{C}$ (Applied to each I_{DOL} , I_{DOH})
 $[(|I_2| - |I_1|) / 2] / [(|I_1| + |I_2|) / 2] \times 100\text{ }(\%)$

*7 : $V_{CC} = V_p = 2.7\text{ V}$, $T_a = +25\text{ }^\circ\text{C}$ (Applied to each I_{DOL} , I_{DOH})
 $[|I_{DO(85^\circ\text{C})}| - |I_{DO(-40^\circ\text{C})}|] / 2] / [|I_{DO(85^\circ\text{C})}| + |I_{DO(-40^\circ\text{C})}|] \times 100\text{ }(\%)$

*8 : $f_{osc} = 12.8\text{ MHz}$, $V_{CCRF} = V_{pRF} = V_{CCIF} = V_{pIF} = 2.7\text{ V}$, $T_a = +25\text{ }^\circ\text{C}$



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FUNCTIONAL DESCRIPTION

1. Pulse swallow function

$$f_{VCO} = [(P \times N) + A] \times f_{osc} \div R$$

f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)

P : Preset divide ratio of dual modulus prescaler (8 or 16 for IF-PLL, 64 or 128 for RF-PLL)

N : Preset divide ratio of binary 11-bit programmable counter (3 to 2,047)

A : Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$, $A < N$)

f_{osc} : Reference oscillation frequency (OSC_{IN} input frequency)

R : Preset divide ratio of binary 14-bit programmable reference counter (3 to 16,383)

2. Serial Data Input

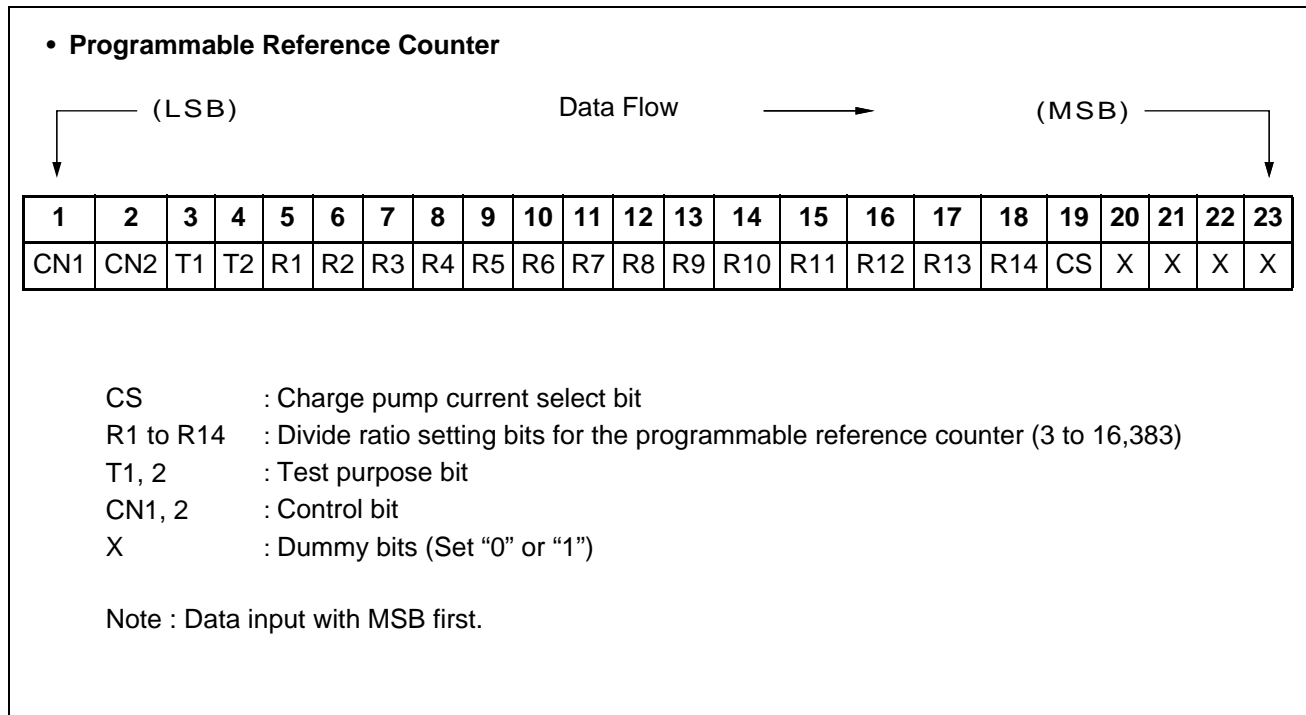
Serial data is entered using three pins, Data pin, Clock pin, and LE pin. Programmable dividers of IF/RF-PLL sections, programmable reference dividers of IF/RF-PLL sections are controlled individually.

Serial data of binary data is entered through Data pin.

On rising edge of Clock, one bit of serial data is transferred into the shift register. On a rising edge of load enable signal, the data stored in the shift register is transferred to one of latch of them depending upon the control bit data setting.

	The programmable reference counter for the IF-PLL	The programmable reference counter for the RF-PLL	The programmable counter and the swallow counter for the IF-PLL	The programmable counter and the swallow counter for the RF-PLL
CN1	0	1	0	1
CN2	0	0	1	1

(1) Shift Register Configuration



MB15F73SP

- Prescaler Data Setting

Divide ratio	SW = "H"	SW = "L"
Prescaler divide ratio IF-PLL	8/9	16/17
Prescaler divide ratio RF-PLL	64/65	128/129

- Charge Pump Current Setting

Current value	CS
±6.0 mA	1
±1.5 mA	0

- LD/fout Output Select Data Setting

LD/fout output signal	LDS
fout signals	1
LD signal	0

- Test Purpose Bit Setting

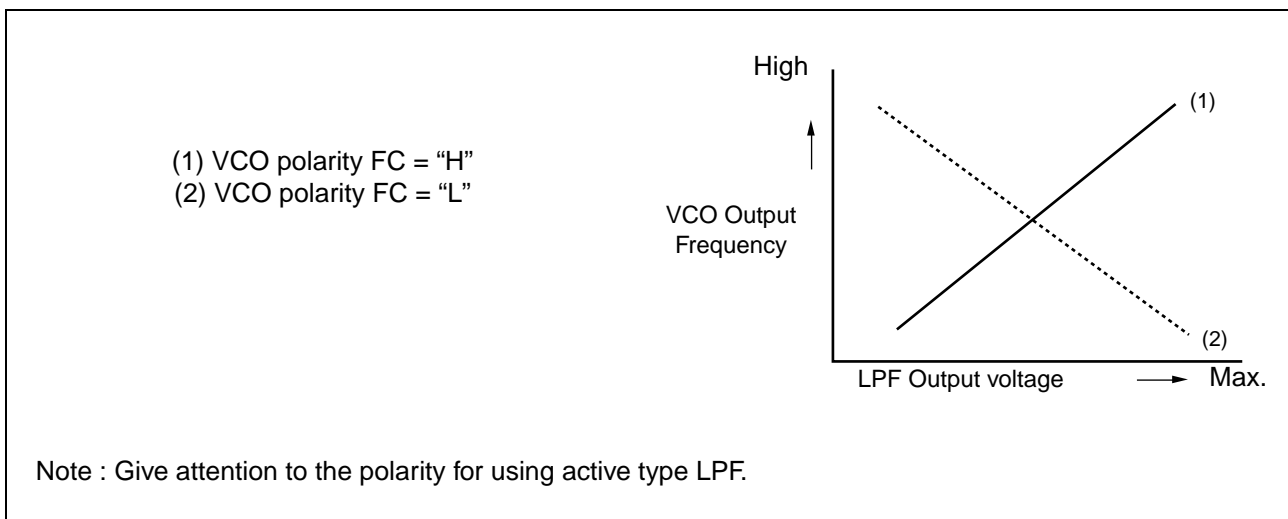
LD/fout pin state	T1	T2
Outputs fr _{IF} .	0	0
Outputs fr _{RF} .	1	0
Outputs fp _{IF} .	0	1
Outputs fp _{RF} .	1	1

- Phase Comparator Phase Switching Data Setting

Phase comparator input	FC _{IF, RF} = "H"	FC _{IF, RF} = "L"
	Do _{IF, RF}	Do _{IF, RF}
fr > fp	H	L
fr < fp	L	H
fr = fp	Z	Z

Z : High-impedance

Depending upon the VCO and LPF polarity, FC bit should be set.



3. Power Saving Mode (Intermittent Mode Control Circuit)

Status	PS pin
Normal mode	H
Power saving mode	L

The intermittent mode control circuit reduces the PLL power consumption.

By setting the PS pin low, the device enters into the power saving mode, reducing the current consumption. See the Electrical Characteristics chart for the specific value.

The phase detector output, Do, becomes high impedance.

For the single PLL, the lock detector, LD, remains high, indicating a locked condition.

For the dual PLL, the lock detector, LD, is as shown in the LD Output Logic table.

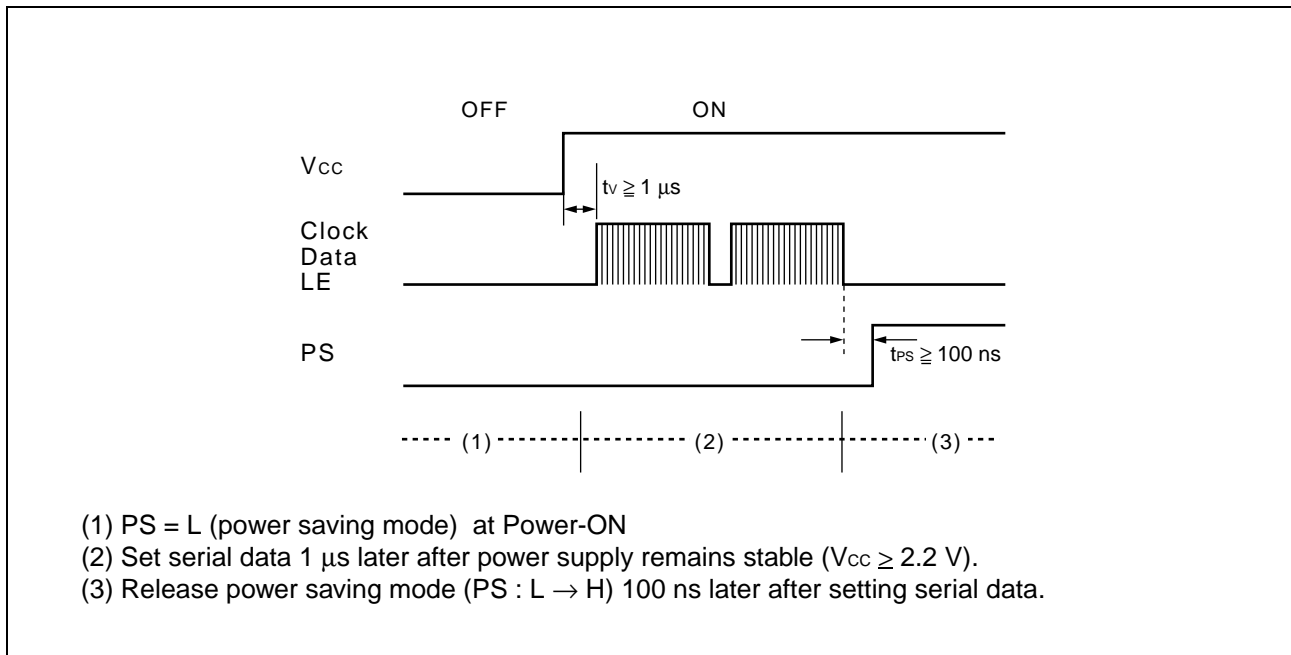
Setting the PS pin high, releases the power saving mode, and the device works normally.

The intermittent mode control circuit also ensures a smooth startup when the device returns to normal operation. When the PLL is returned to normal operation, the phase comparator output signal is unpredictable. This is because of the unknown relationship between the comparison frequency (f_p) and the reference frequency (f_r) which can cause a major change in the comparaoor output, resulting in a VCO frequency jump and an increase in lockup time.

To prevent a major VCO frequency jump, the intermittent mode control circuit limits the magnitude of the error signal from the phase detector when it returns to normal operation.

Note : When power (V_{CC}) is first applied, the device must be in standby mode, PS = Low, for at least 1 μ s.

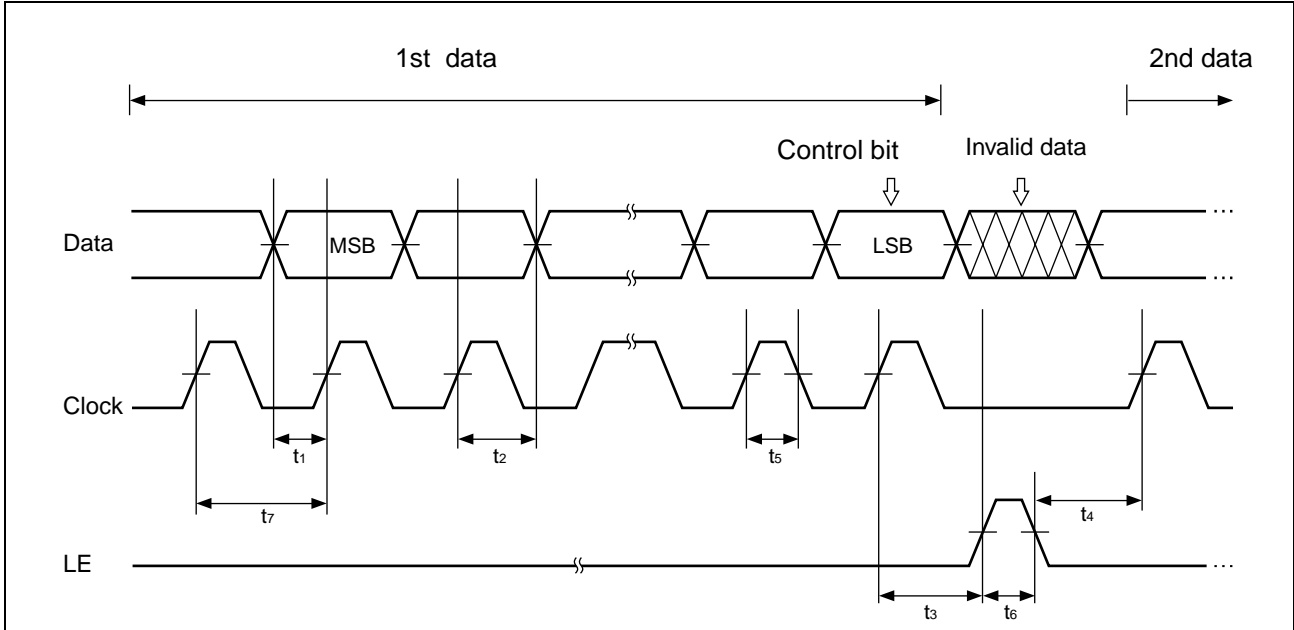
Note : PS pin must be set "L" for Power-ON.



- (1) PS = L (power saving mode) at Power-ON
- (2) Set serial data 1 μs later after power supply remains stable ($V_{CC} \geq 2.2 V$).
- (3) Release power saving mode (PS : L \rightarrow H) 100 ns later after setting serial data.

4. SERIAL DATA INPUT TIMING

Frequency multiplier setting is performed through a serial interface using the Data pin, Clock pin, and LE pin. Setting data is read into the shift register at the rise of the clock signal, and transferred to a latch at the rise of the LE signal. The following diagram shows the data input timing.

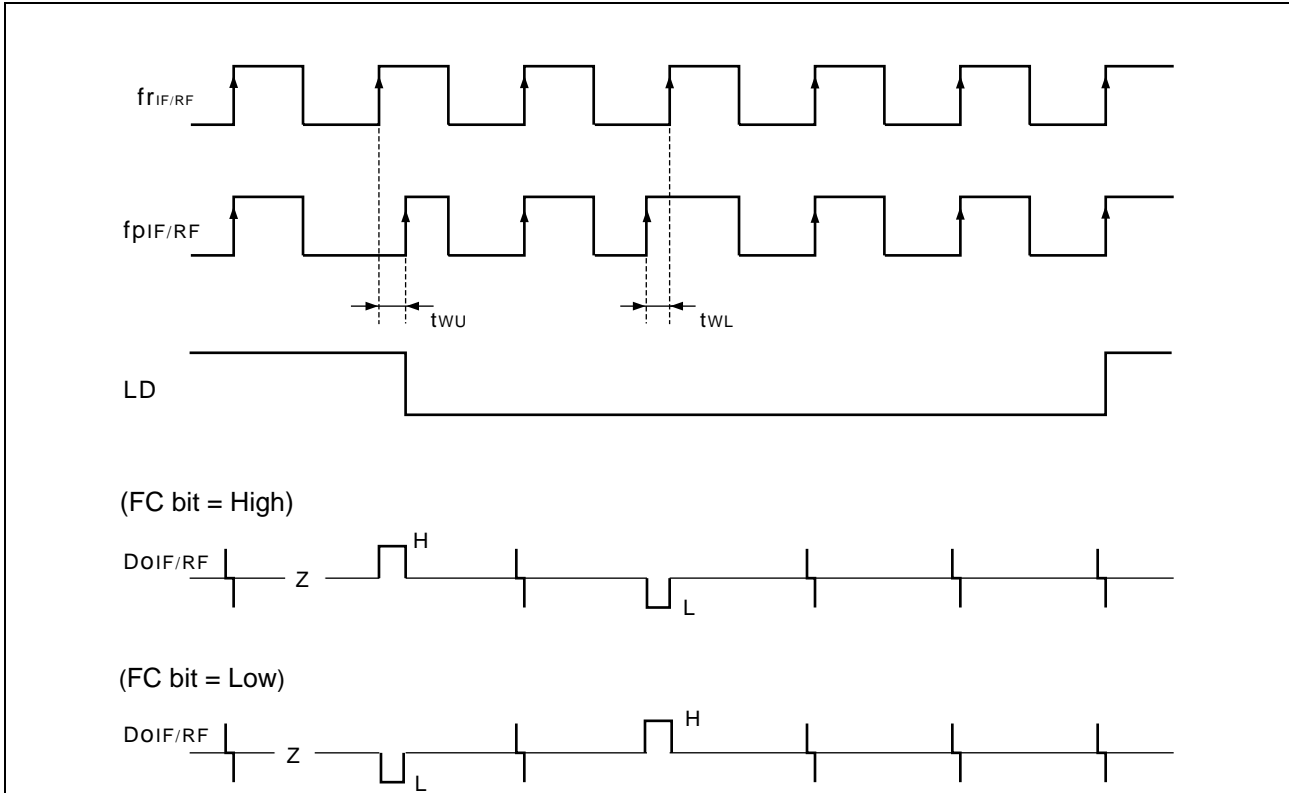


Parameter	Min.	Typ.	Max.	Unit
t_1	20	—	—	ns
t_2	20	—	—	ns
t_3	30	—	—	ns
t_4	20	—	—	ns

Parameter	Min.	Typ.	Max.	Unit
t_5	30	—	—	ns
t_6	100	—	—	ns
t_7	100	—	—	ns

Note : LE should be "L" when the data is transferred into the shift register.

■ PHASE COMPARATOR OUTPUT WAVEFORM



• LD Output Logic

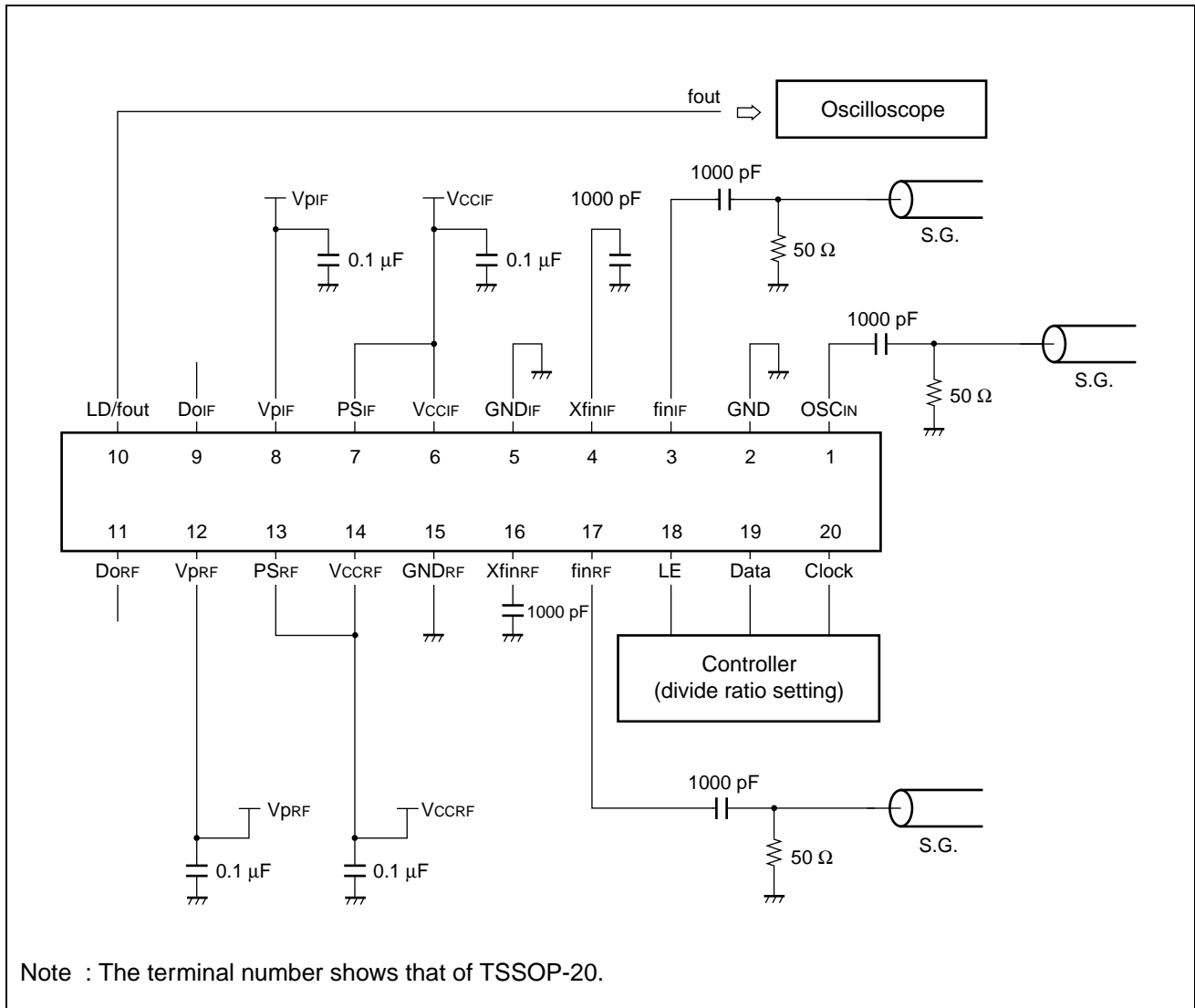
IF-PLL section	RF-PLL section	LD output
Locking state/Power saving state	Locking state/Power saving state	H
Locking state/Power saving state	Unlocking state	L
Unlocking state	Locking state/Power saving state	L
Unlocking state	Unlocking state	L

Notes :• Phase error detection range = -2π to $+2\pi$

- Pulses on $Do_{IIF/RF}$ signals during locking state are output to prevent dead zone.
- LD output becomes low when phase error is t_{WU} or more.
- LD output becomes high when phase error is t_{WL} or less and continues to be so for three cycles or more.
- t_{WU} and t_{WL} depend on OSC_{IN} input frequency as follows.
 - $t_{WU} \geq 2/f_{osc}$: e.g. $t_{WU} \geq 156.3$ ns when $f_{osc} = 12.8$ MHz
 - $t_{WL} \leq 4/f_{osc}$: e.g. $t_{WL} \leq 312.5$ ns when $f_{osc} = 12.8$ MHz

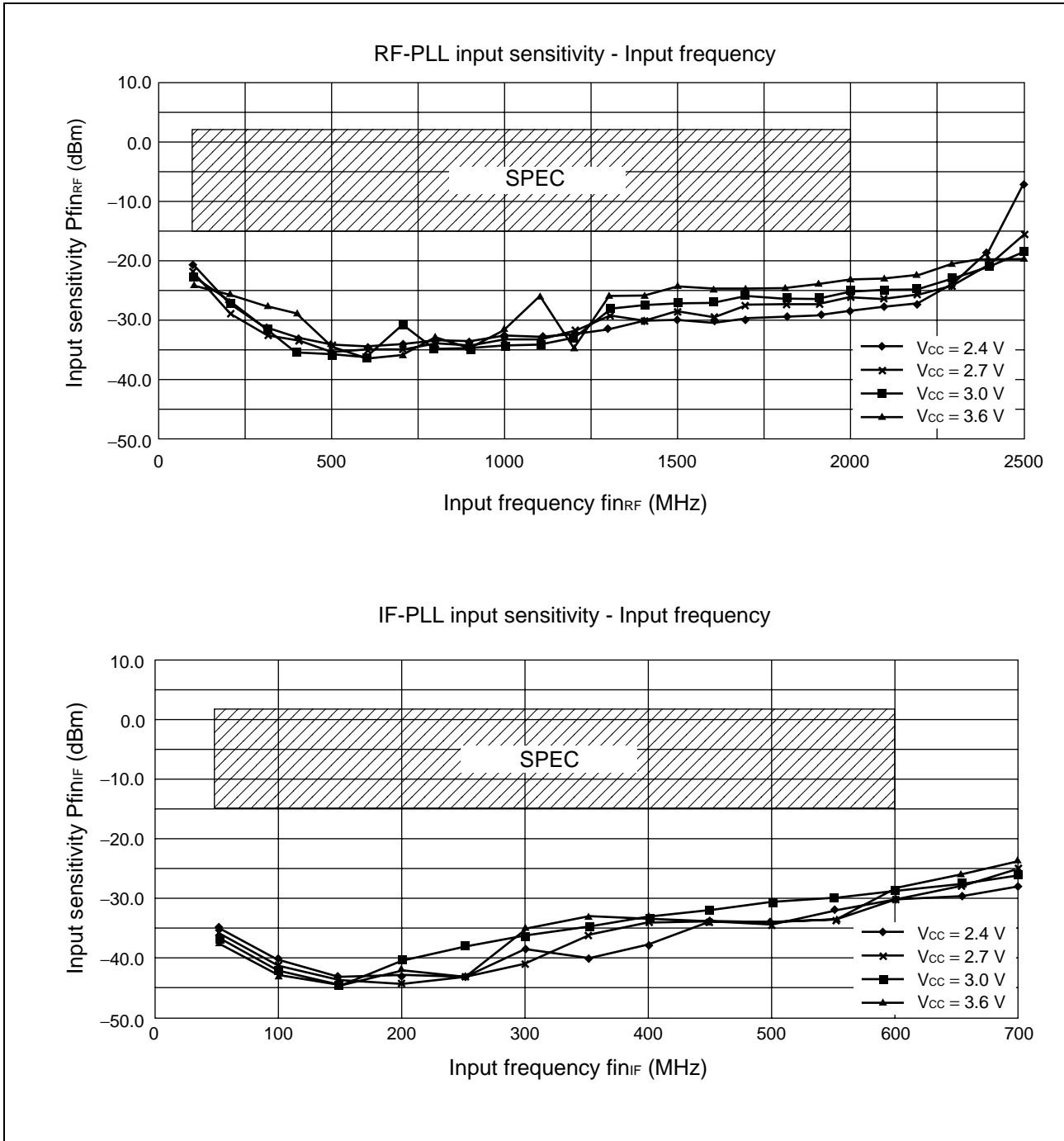
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■ TEST CIRCUIT (for Measuring Input Sensitivity f_{in}/OSC_{IN})



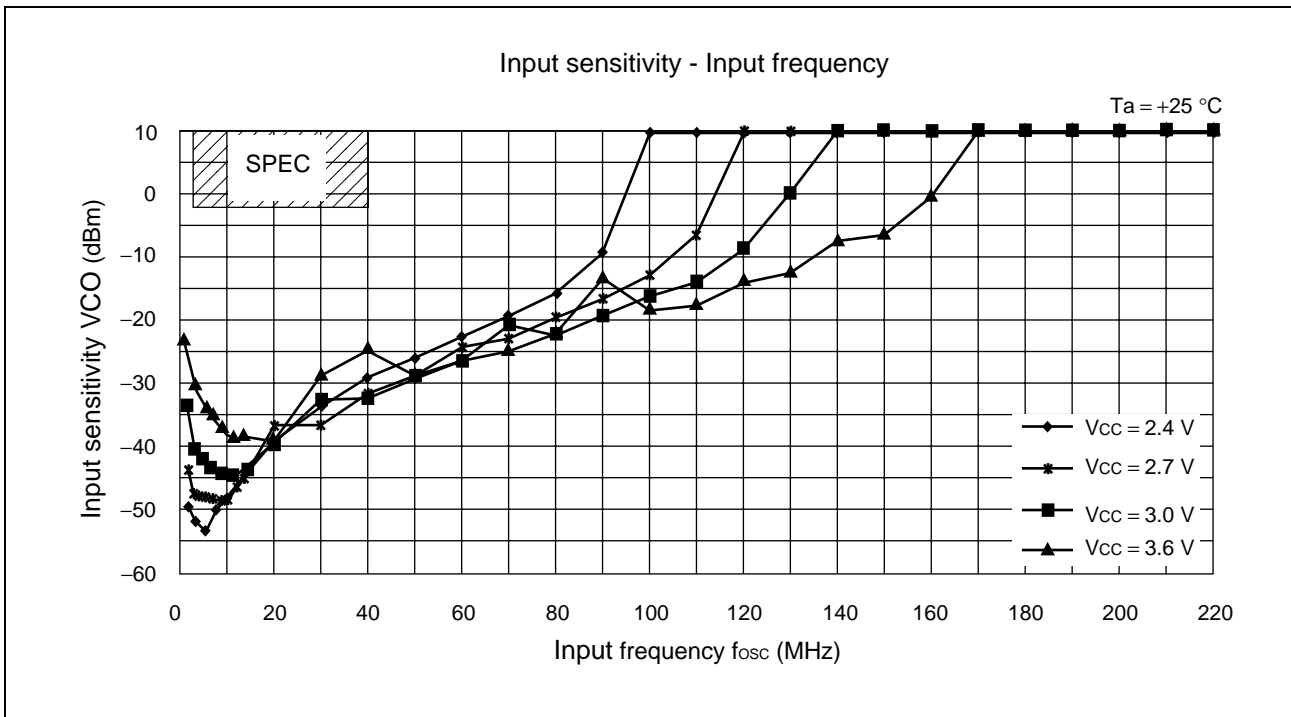
■ TYPICAL CHARACTERISTICS

1. f_{in} input sensitivity



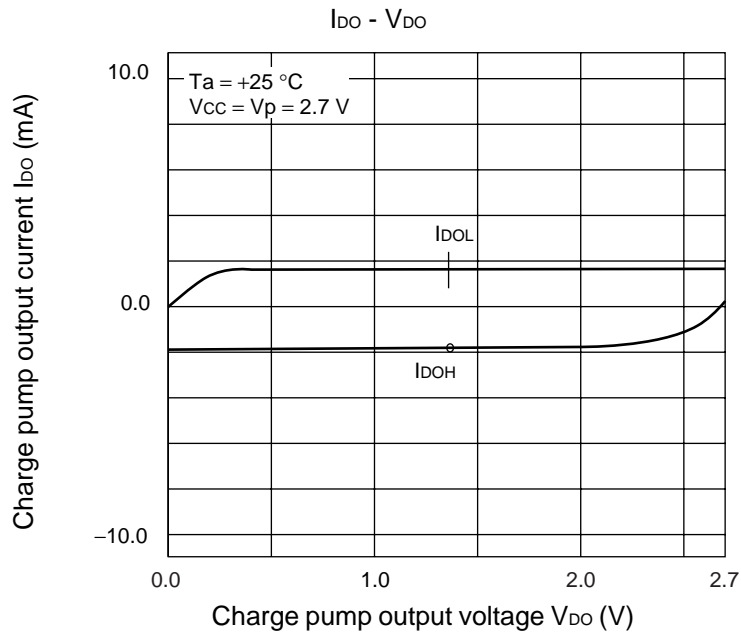
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2. OSC_{IN} input sensitivity

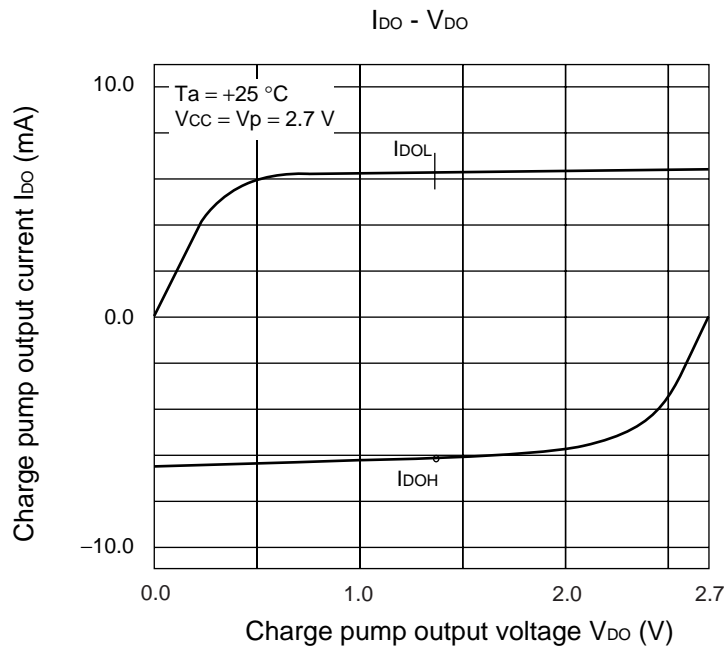


3. RF-PLL Do output current

- 1.5 mA mode

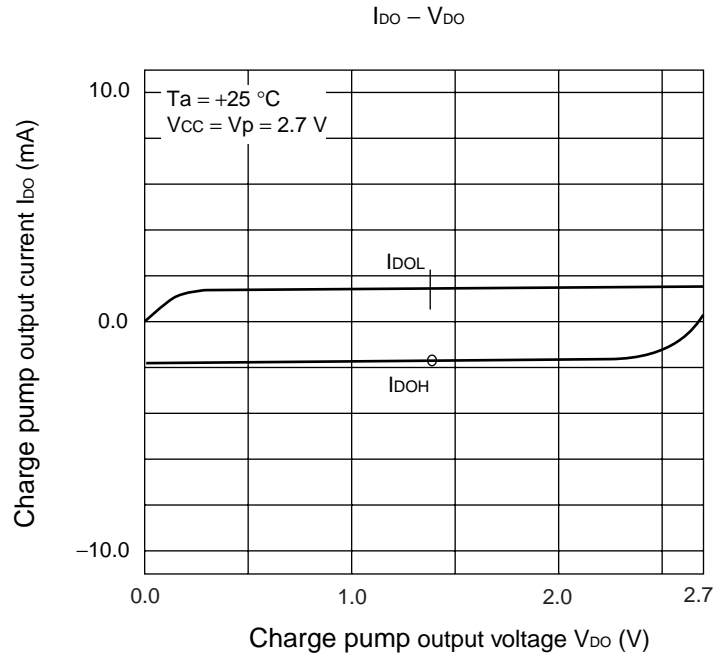


- 6.0 mA mode

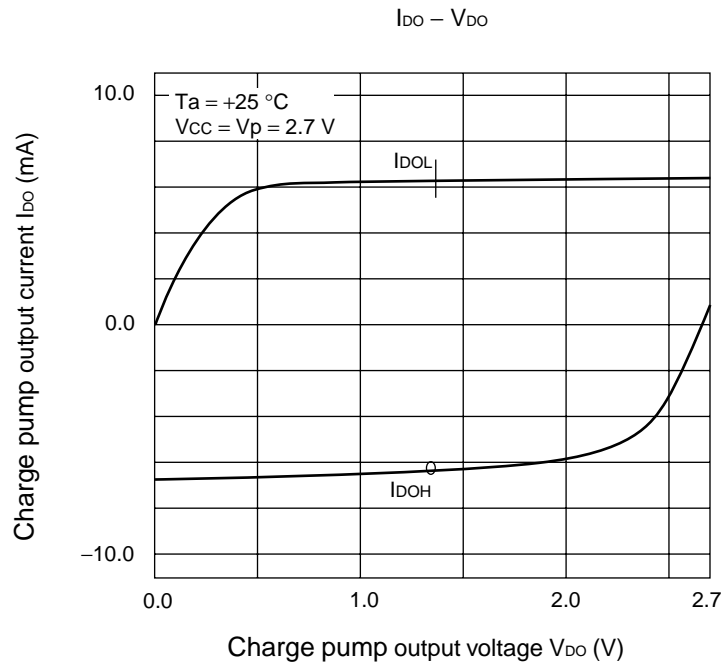


4. IF-PLL Do output current

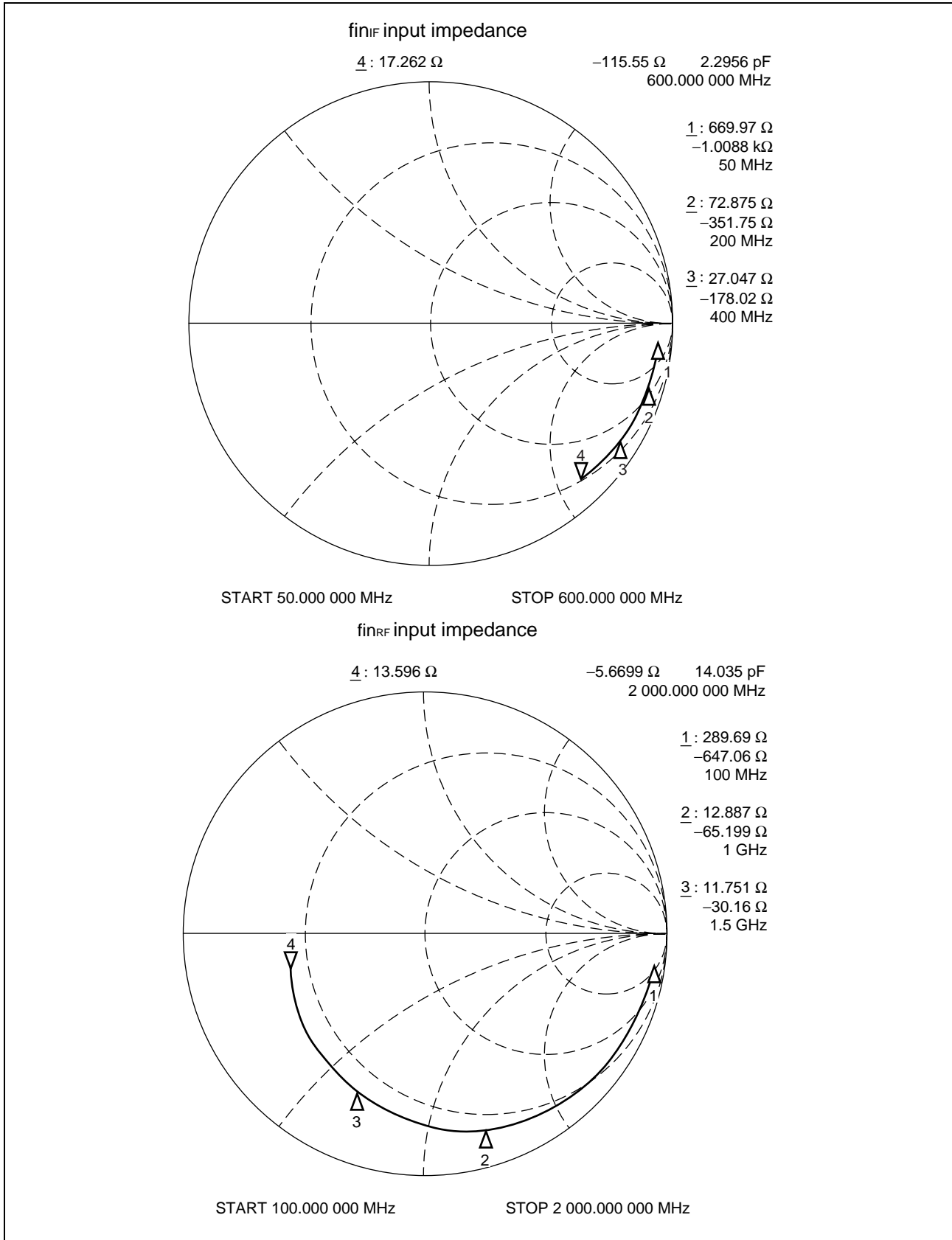
- 1.5 mA mode



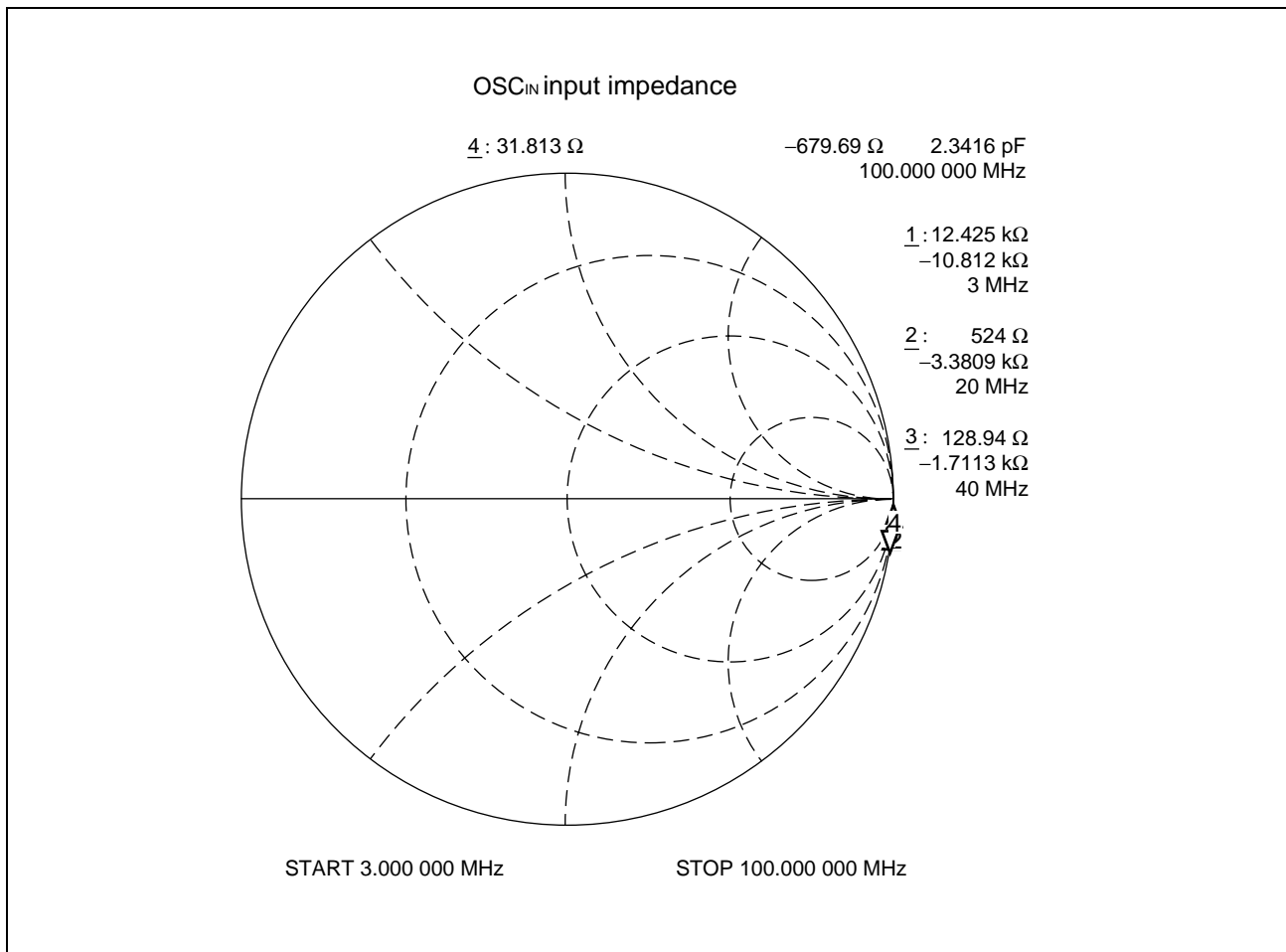
- 6.0 mA mode



5. fin input impedance

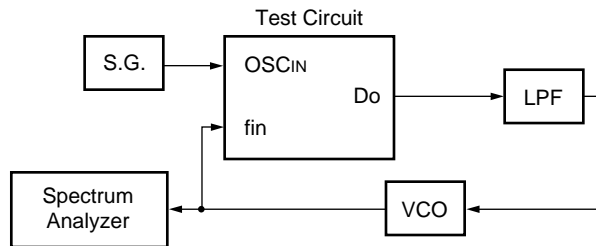


6. OSC_{IN} input impedance

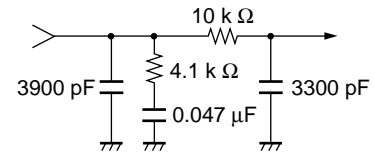


■ REFERENCE INFORMATION

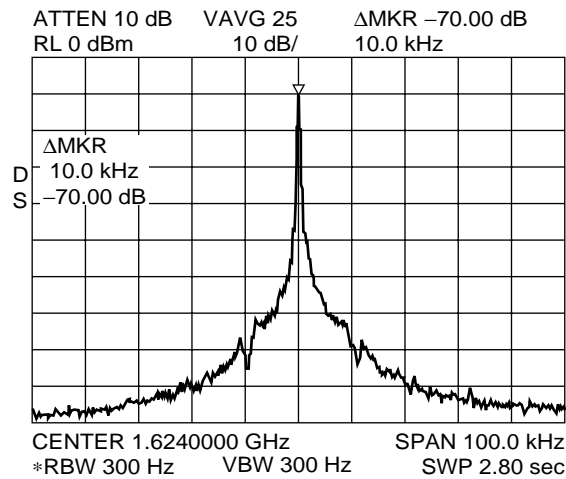
(for Lock-up Time, Phase Noise and Reference Leakage)



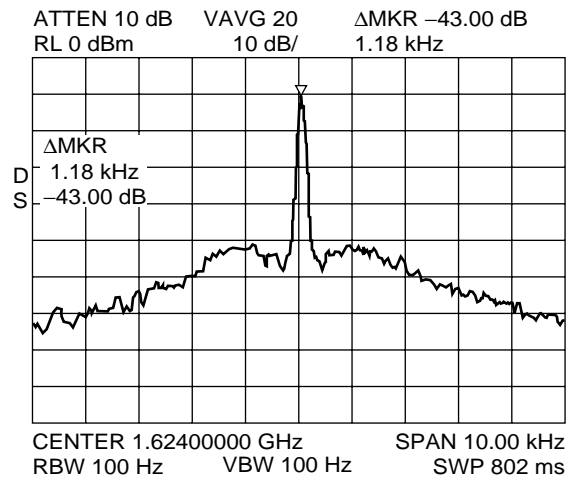
$f_{vco} = 1624 \text{ MHz}$ $V_{cc} = 3.0 \text{ V}$
 $K_v = 22 \text{ MHz/V}$ $V_{vco} = 3.0 \text{ V}$
 $f_r = 10 \text{ kHz}$ $T_a = +25 \text{ }^\circ\text{C}$
 $f_{osc} = 19.68 \text{ MHz}$ $CP : 6 \text{ mA mode}$
 LPF



• PLL Reference Leakage



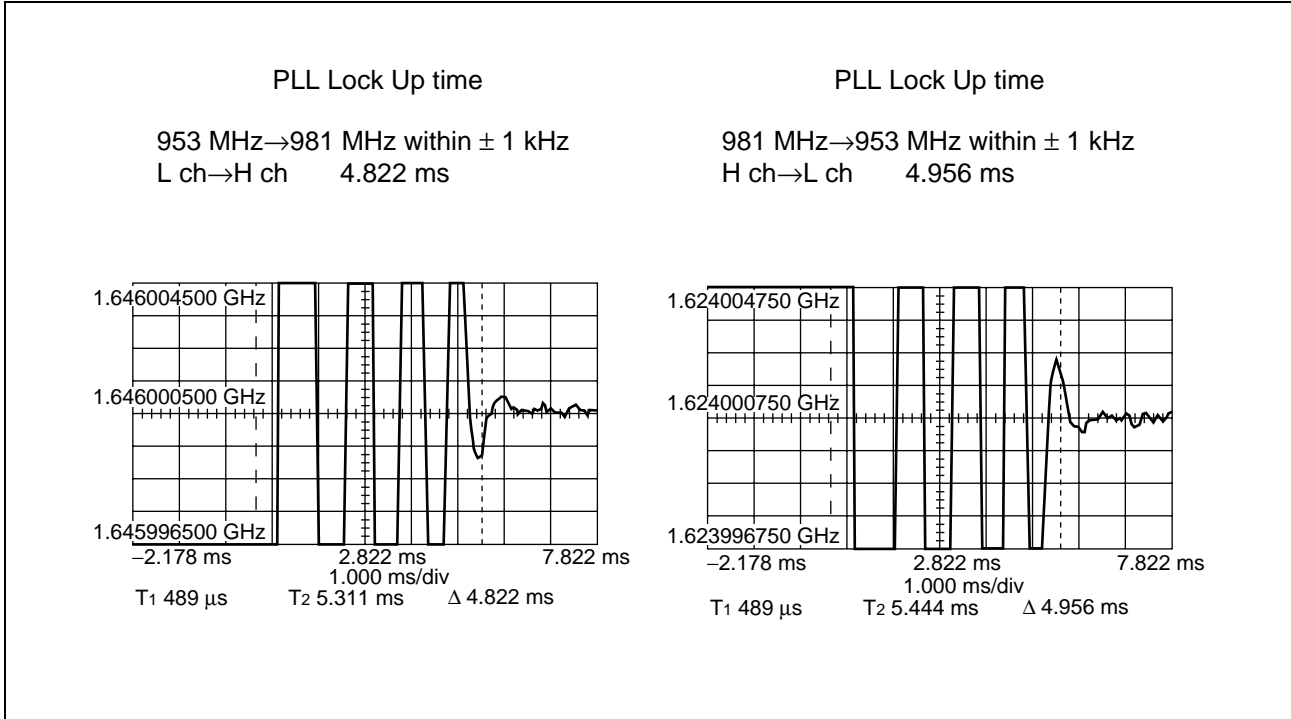
• PLL Phase Noise



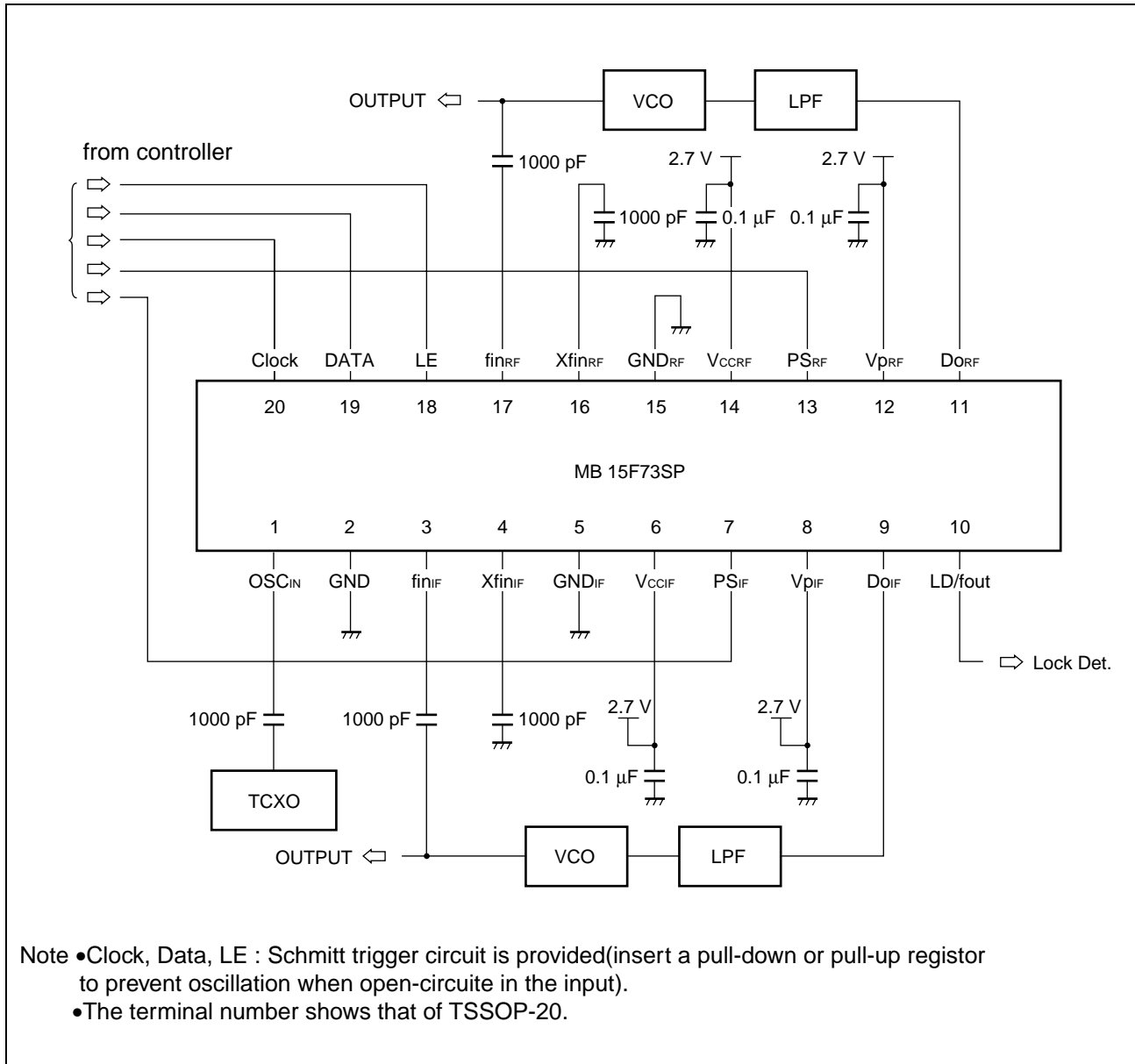
(Continued)

MB15F73SP

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APPLICATION EXAMPLE



MB15F73SP

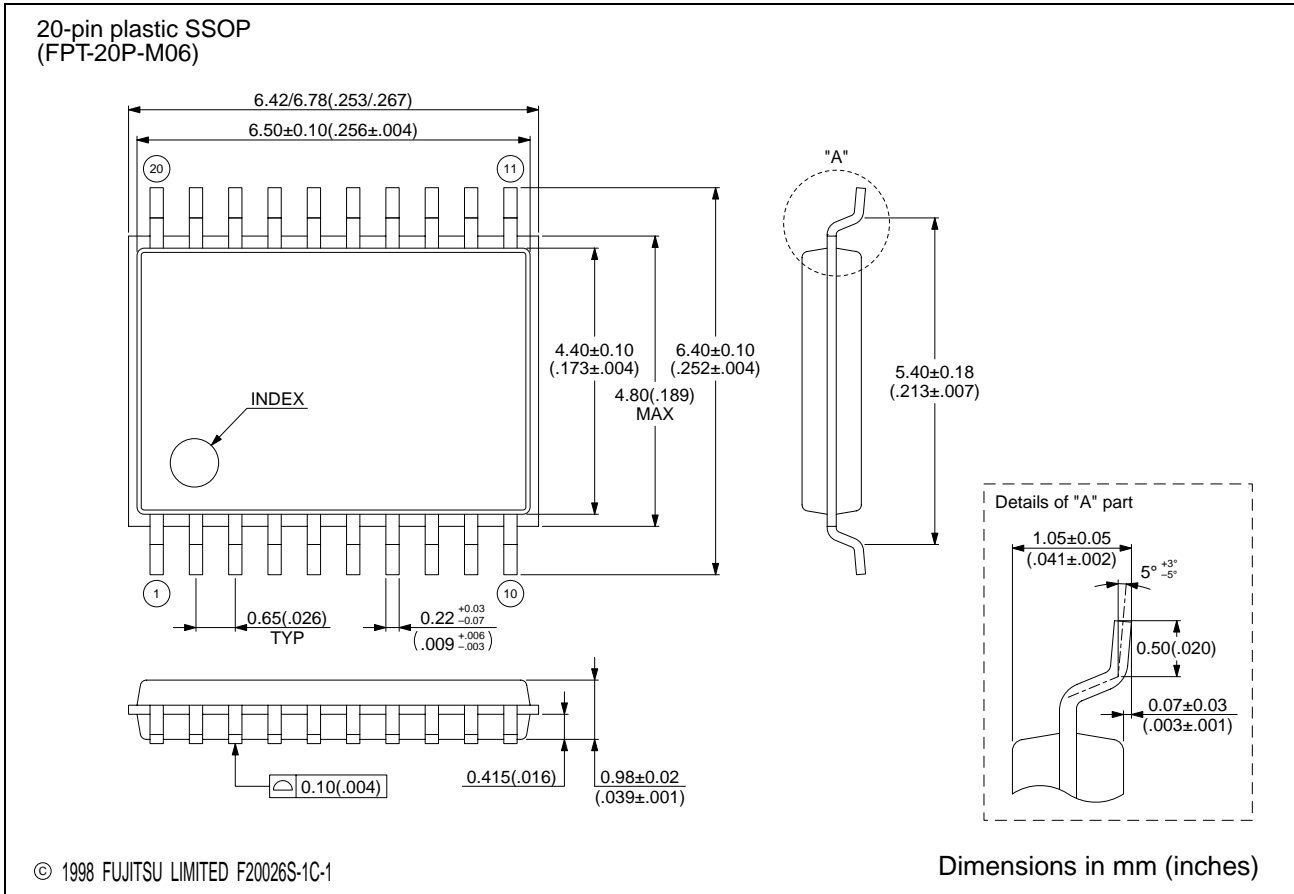
■ USAGE PRECAUTIONS

- (1) V_{CCRF} , V_{PRF} , V_{CCIF} and V_{PIF} must equal equal voltage.
Even if either RF-PLL or IF-PLL is not used, power must be supplied to both V_{CCRF} , V_{PRF} , V_{CCIF} and V_{PIF} to keep them equal. It is recommended that the non-use PLL is controlled by power saving function.
- (2) To protect against damage by electrostatic discharge, note the following handling precautions:
 - Store and transport devices in conductive containers.
 - Use properly grounded workstations, tools, and equipment.
 - Turn off power before inserting or removing this device into or from a socket.
 - Protect leads with conductive sheet, when transporting a board mounted device

■ ORDERING INFORMATION

Part number	Package	Remarks
MB15F73SPPFT	20-pin plastic TSSOP (FPT-20P-M06)	
MB15F73SPPV	20-pad plastic BCC (LCC-20P-M04)	

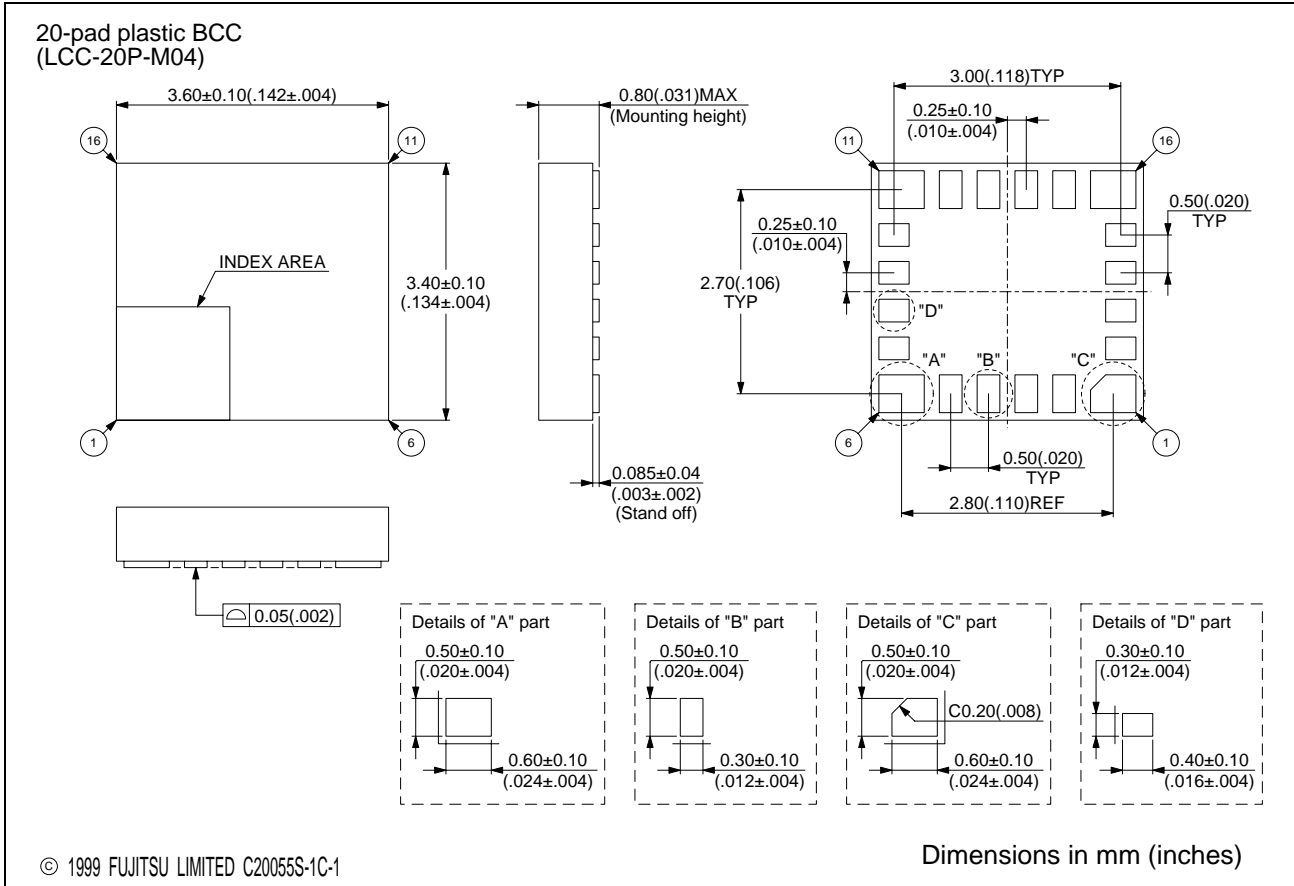
■ PACKAGE DIMENSIONS



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MB15F73SP

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FUJITSU LIMITED

For further information please contact:

Japan

FUJITSU LIMITED
Corporate Global Business Support Division
Electronic Devices
KAWASAKI PLANT, 4-1-1, Kamikodanaka
Nakahara-ku, Kawasaki-shi
Kanagawa 211-8588, Japan
Tel: 81(44) 754-3763
Fax: 81(44) 754-3329

<http://www.fujitsu.co.jp/>

North and South America

FUJITSU MICROELECTRONICS, INC.
Semiconductor Division
3545 North First Street
San Jose, CA 95134-1804, USA
Tel: (408) 922-9000
Fax: (408) 922-9179

Customer Response Center
Mon. - Fri.: 7 am - 5 pm (PST)
Tel: (800) 866-8608
Fax: (408) 922-9179

<http://www.fujitsumicro.com/>

Europe

FUJITSU MICROELECTRONICS EUROPE GmbH
Am Siebenstein 6-10
D-63303 Dreieich-Buchsschlag
Germany
Tel: (06103) 690-0
Fax: (06103) 690-122

<http://www.fujitsu-edo.com/>

Asia Pacific

FUJITSU MICROELECTRONICS ASIA PTE LTD
#05-08, 151 Lorong Chuan
New Tech Park
Singapore 556741
Tel: (65) 281-0770
Fax: (65) 281-0220

<http://www.fmap.com.sg/>

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