

# HAT2064R

Silicon N Channel Power MOS FET  
Power Switching

# HITACHI

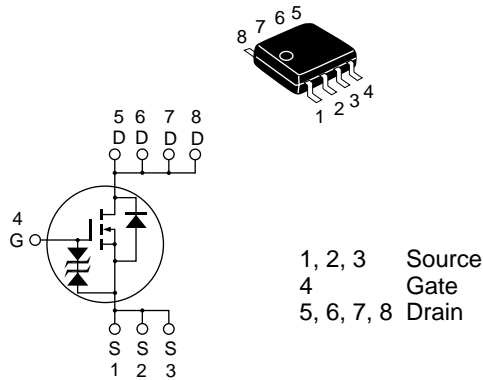
ADE-208-930G (Z)  
8th. Edition  
May 2000

## Features

- Capable of 4.5 V gate drive
- Low drive current
- High density mounting
- Low on-resistance  
 $R_{DS(on)} = 5.0 \text{ m}\Omega$  typ (at  $V_{GS} = 10\text{V}$ )

## Outline

SOP-8



## Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V <sub>DSS</sub>	30	V
Gate to source voltage	V <sub>GSS</sub>	± 20	V
Drain current	I <sub>D</sub>	16	A
Drain peak current	I <sub>D(pulse)</sub> <sup>Note1</sup>	128	A
Body-drain diode reverse drain current	I <sub>DR</sub>	16	A
Channel dissipation	Pch <sup>Note2</sup>	2.5	W
Channel to Ambient Thermal Impedance	θch-a <sup>Note2</sup>	50	°C/W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	- 55 to + 150	°C

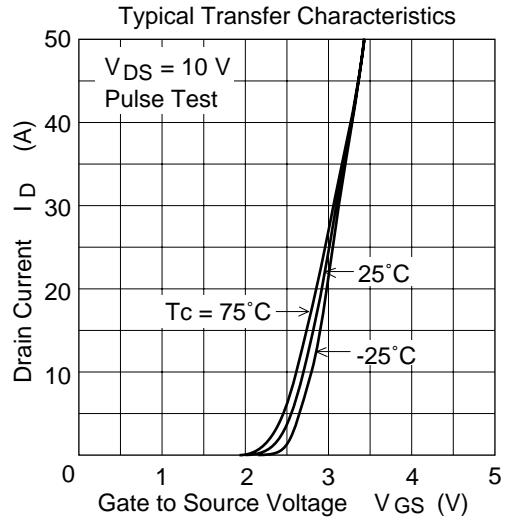
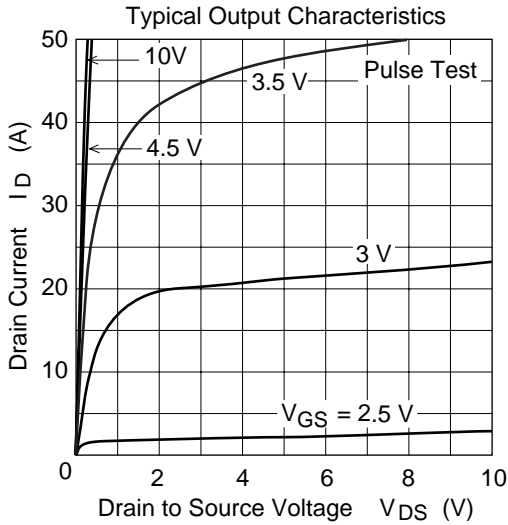
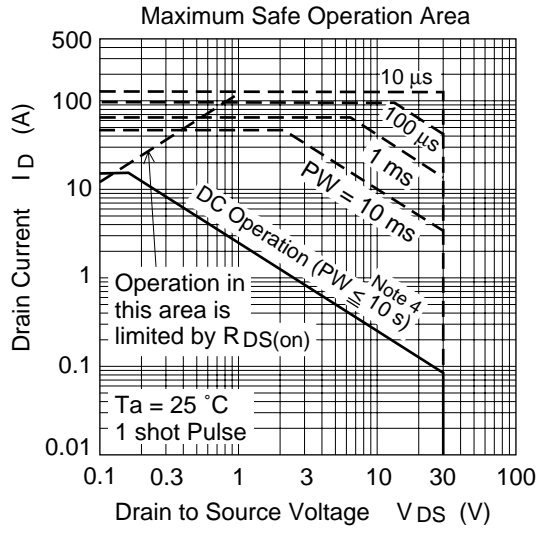
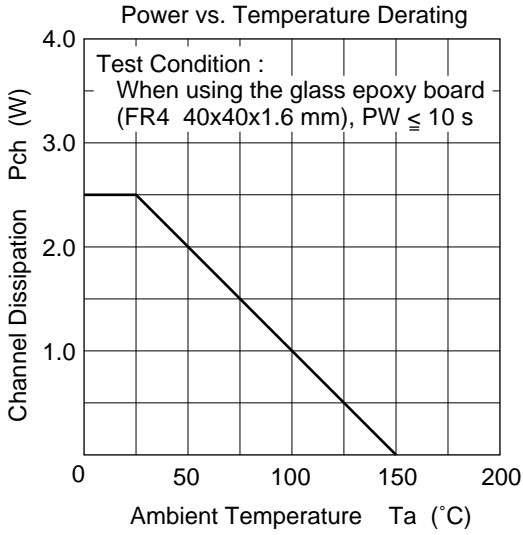
- Note: 1. PW ≤ 10 μs, duty cycle ≤ 1%  
2. When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW ≤ 10s

## Electrical Characteristics (Ta = 25°C)

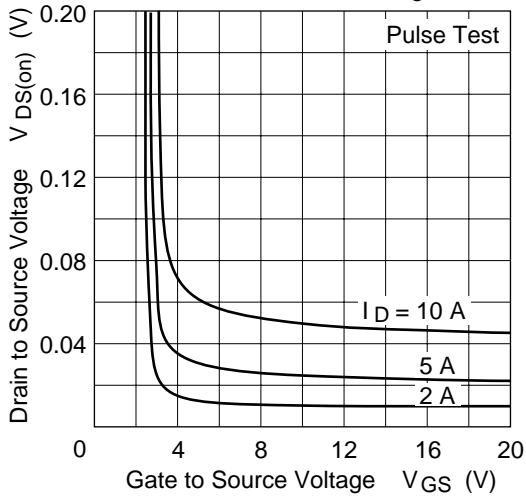
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	$\pm 20$	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}, V_{DS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 10$	$\mu\text{A}$	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	1	$\mu\text{A}$	$V_{DS} = 30 \text{ V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	$V_{DS} = 10 \text{ V}, I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	5.0	6.3	$\text{m}\Omega$	$I_D = 8 \text{ A}, V_{GS} = 10 \text{ V}$ <sup>Note3</sup>
	$R_{DS(on)}$	—	7.0	10	$\text{m}\Omega$	$I_D = 8 \text{ A}, V_{GS} = 4.5 \text{ V}$ <sup>Note3</sup>
Forward transfer admittance	$ y_{fs} $	18	30	—	S	$I_D = 8 \text{ A}, V_{DS} = 10 \text{ V}$ <sup>Note3</sup>
Input capacitance	$C_{iss}$	—	2200	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	$C_{oss}$	—	600	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	$C_{rss}$	—	330	—	pF	$f = 1 \text{ MHz}$
Total gate charge	$Q_g$	—	40	—	nc	$V_{DD} = 10 \text{ V}$
Gate to source charge	$Q_{gs}$	—	6	—	nc	$V_{GS} = 10 \text{ V}$
Gate to drain charge	$Q_{gd}$	—	8	—	nc	$I_D = 16 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	20	—	ns	$V_{GS} = 10 \text{ V}, I_D = 8 \text{ A}$
Rise time	$t_r$	—	35	—	ns	$V_{DD} \approx 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	60	—	ns	$R_L = 1.25 \text{ }\Omega$
Fall time	$t_f$	—	16	—	ns	$R_g = 4.7 \text{ }\Omega$
Body-drain diode forward voltage	$V_{DF}$	—	0.9	1.17	V	$I_F = 16 \text{ A}, V_{GS} = 0$ <sup>Note3</sup>
Body-drain diode reverse recovery time	$t_{rr}$	—	50	—	ns	$I_F = 16 \text{ A}, V_{GS} = 0$ $diF/dt = 50 \text{ A}/\mu\text{s}$

Note: 3. Pulse test

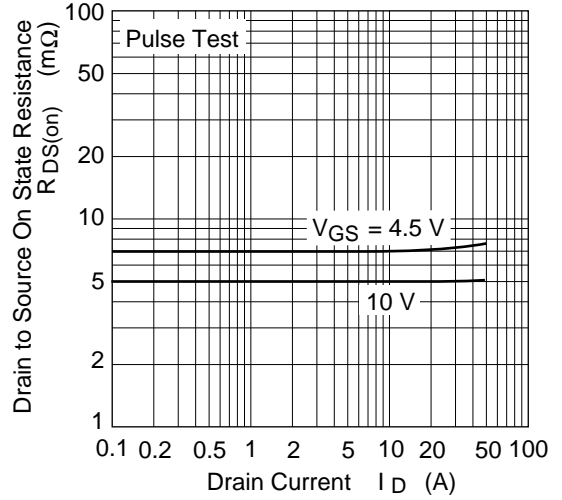
## Main Characteristics



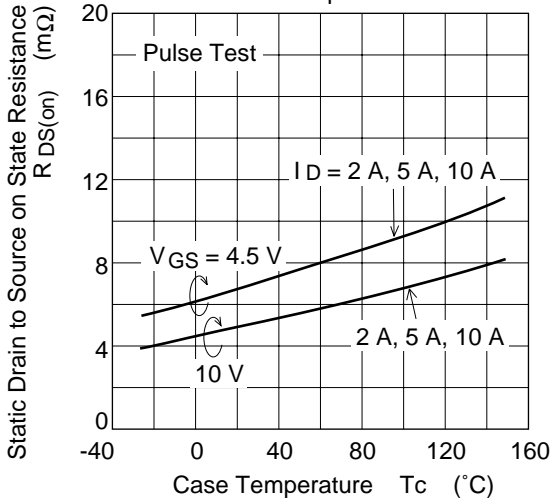
Drain to Source Saturation Voltage vs. Gate to Source Voltage



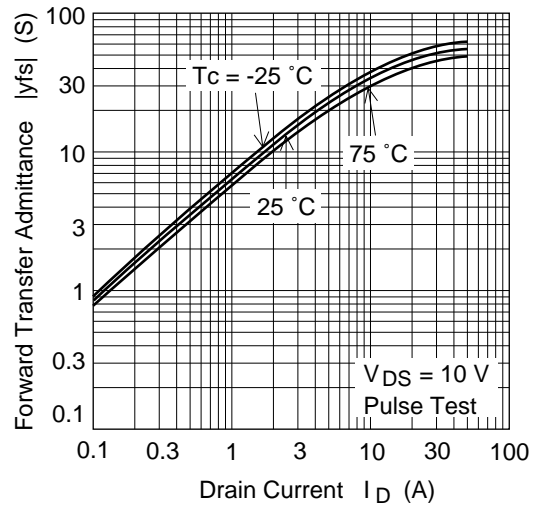
Static Drain to Source on State Resistance vs. Drain Current



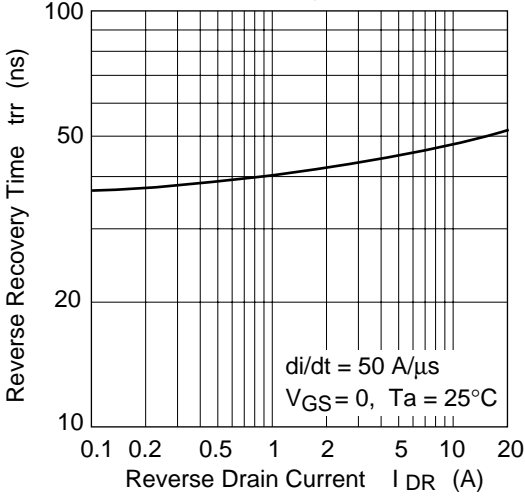
Static Drain to Source on State Resistance vs. Temperature



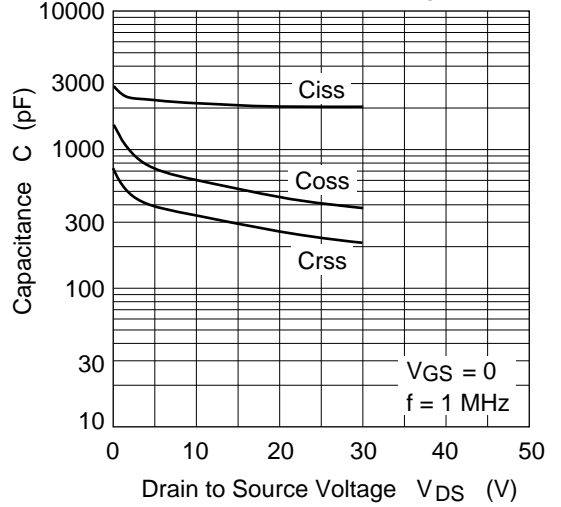
Forward Transfer Admittance vs. Drain Current



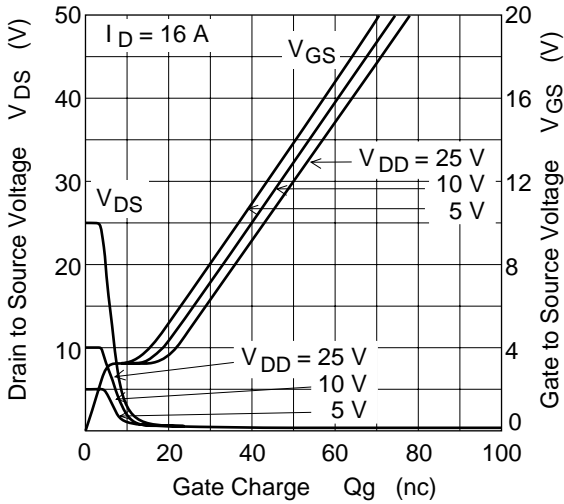
Body Drain Diode Reverse Recovery Time



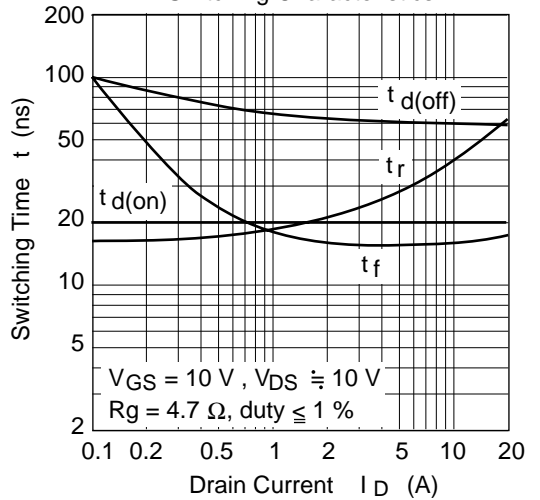
Typical Capacitance vs. Drain to Source Voltage

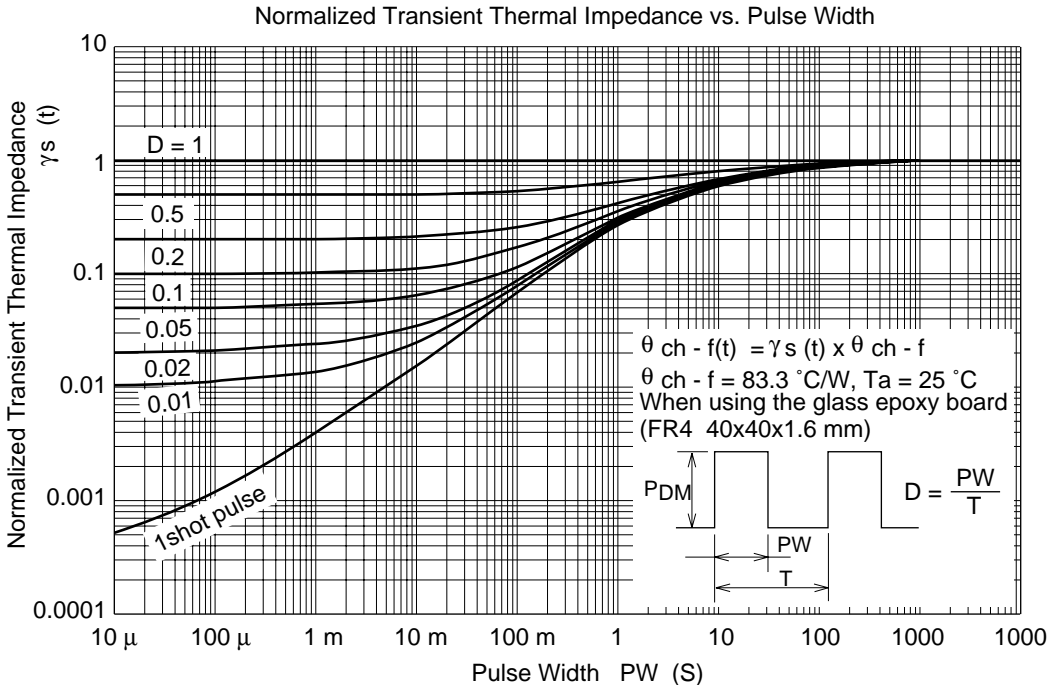
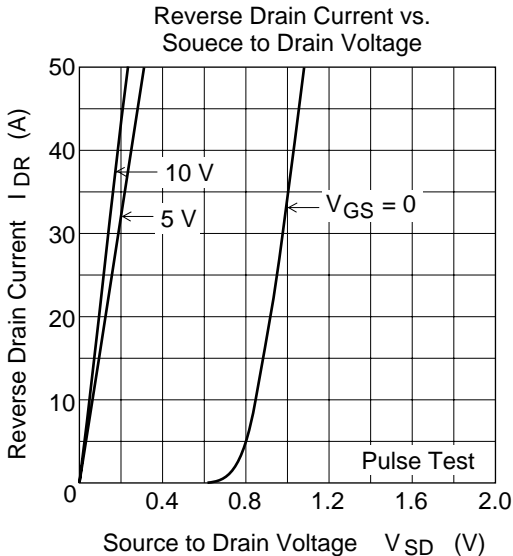


Dynamic Input Characteristics

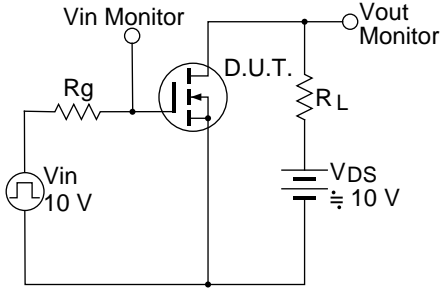


Switching Characteristics

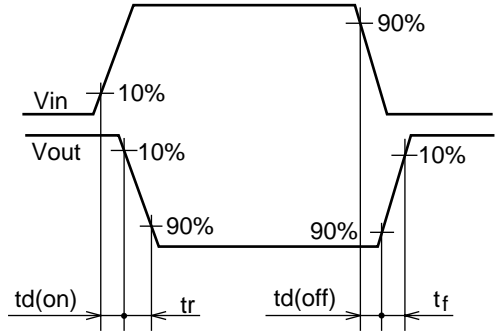




Switching Time Test Circuit



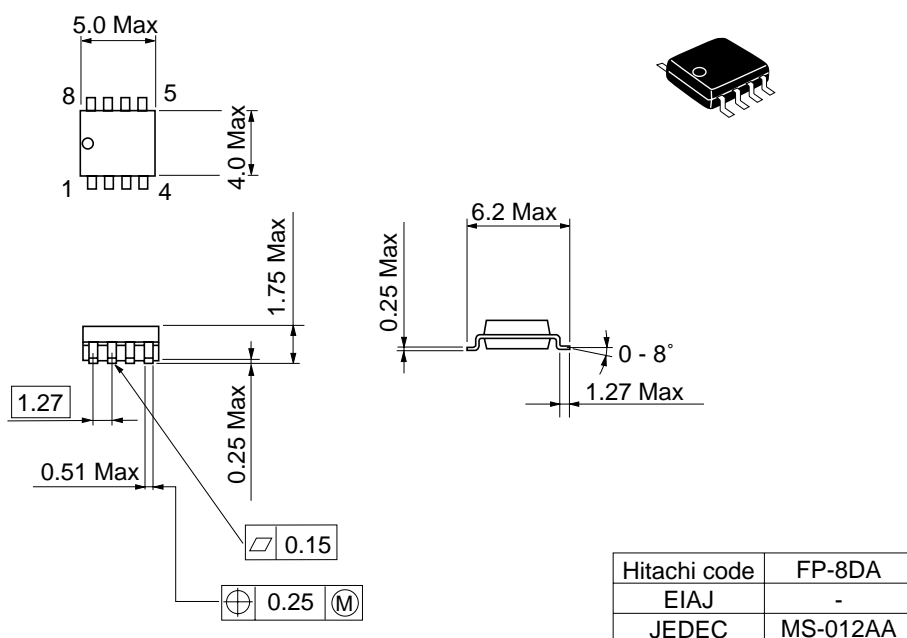
Switching Time Waveform





Package Dimensions

Unit: mm



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