Type	Ordering Code	Package
SFZH 211 S	Q67000-H639-S1	P-DIP-16
SFZH 215 S	Q67000-H2431	

Four NAND drivers with open collector outputs, 2 inputs, and N input for delay circuits. The input threshold can be switched to LSL, TTL, or CMOS level, depending on the supply voltage used.

Typical Application

Driver up to 30 V/150 mA, relay driver, and level converter.

Calculation of the load resistance for wired AND connection is carried out as described for FZH 161/181 (refer to LSL data book). In the case of wired AND connection and N wiring, the capacitors C_N must have identical values.

Maximum Ratings

Description	Symbol	Test conditions	min	max	Unit
Supply voltage	V_S		0	30	V
Input voltage	V_I		−0.5	30	V
Voltage between 2 inputs	V_{II}			30	V
Voltage at output, output transistor cut off	$V_{Q\,H}$			30	V
Voltage at output, output transistor conducting	$V_{Q\,L}$		0		V
Output current	$I_{Q\,L}$			150	mA
Capacitance at Q	C_L			5	nF
Capacitance between N and Q	C_N			0.1	µF
Voltage at N			−1	0.6	V
Current at N			−10	2	mA
Storage temperature	T_{stg}		−65	125	°C
Thermal resistance system – air	$R_{th\,SA}$			60	K/W

Operating Range

Supply voltage range 1	V_S	TTL threshold at A, B	4	7	V
Supply voltage range 2	V_S	LSL threshold at A, B	9	30	V
Supply voltage	V_S	Switching of threshold at A, B at $V_S = 8$ V, typical	4	30	V
Ambient temperature					
FZH 211 S (range 1)	T_A		0	70	°C
FZH 215 S (range 5)	T_A		−25	85	°C

Characteristics in the 5 V Range

Temperature range 1 and 5

Description	Symbol	Test conditions	min	typ	max	Unit
Supply voltage	V_S		4		7	V
H-input voltage	V_{IH}	$V_S = V_{SB}$	2			V
L-input voltage	V_{IL}	$V_S = V_{SA}$ and V_{SB}			0.8	V
Static noise immunity	V_{sn}		0.4	1.0		V
L-output voltage	V_{QL}	$I_{QL} = 1.6$ mA | $V_{IH} = 8$ V		0.7	0.8	V
L-output voltage	V_{QL}	$I_{QL} = 100$ mA | $V_S = V_{SB}$			1.3	V
L-output voltage[1])	V_{QL}	$I_{QL} = 150$ mA			1.5	V
H-input current	I_{IH}	$U_{IH} = 30$ V | $V_{IH} = V_{SA}$			1	µA
L-input current	$-I_{IL}$	$V_{IL} = 0$ V		5	50	µA
H-output current	I_{QL}	$V_{IL} = 0.8$ V, $V_{QH} = 30$ V, $V_S = V_{SB}$			50	µA
Supply current per package	I_S	$V_S = 7$ V, $V_I = 0$ V	1.5	3	5	mA

Characteristics in the 12 V, 15 V, 24 V Ranges

Temperature range 1 and 5

Supply voltage	V_S		9		30	V
H-input voltage	V_{IH}	$V_S = V_{SB}$	8			V
L-input voltage	V_{IL}	$V_S = V_{SA}$ and V_{SB}			6	V
Static noise immunity	V_{sn}		2.5	5.0		V
L-output voltage	V_{QL}	$I_{QL} = 100$ mA | $V_{IH} = 8$ V		1	1.3	V
L-output voltage[1])	V_{QL}	$I_{QL} = 150$ mA | $V_S = V_{SB}$			1.5	V
H-Input current	I_{IH}	$V_{IH} = 30$ V | $V_S = V_{SA}$			1	µA
L-Input current	$-I_{IL}$	$V_{IL} = 0$ V		5	50	µA
H-output current	I_{QH}	$V_{IL} = 6$ V, $V_{QH} = 30$ V, $V_S = V_{SB}$			50	µA
Supply current per package	I_S	$V_S = 30$ V, $V_I = 0$ V	1.5	3	5	mA

Switching Characteristics at $V_S = 12$ V, $T_A = 25$ °C

Signal propagation time	t_{PLH}	$V_{SC} = 12$ V $R_C = 760\ \Omega$ $C_L = 15$ pF		550		ns
	t_{PHL}			200		ns
Signal transition time	t_{TLH}			90		ns
	t_{THL}			25		ns

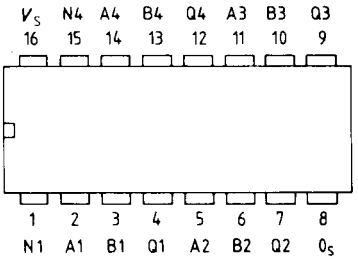
Signal transition times at Q
with C_N wiring between N and Q:

$$\left.\begin{aligned} t_{THL} &= 6 \cdot C_N \cdot (V_{QH} - V_{QL}) \\ t_{TLH} &= 15 \cdot C_N \cdot (V_{QH} - V_{QL}) \end{aligned}\right\} \ (\mu s, \mu F, V)$$

typical values for $C_N > 0.02$ µF

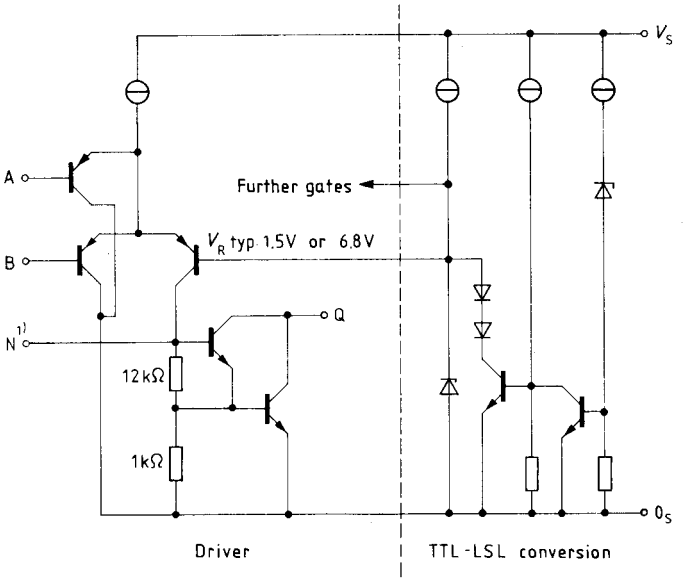
[1]) The sum of all output currents per package may not exceed 400 mA for the FZH 211 S and 350 mA for the FZH 215 S.

Pin Configuration
top view



A, B = inputs
Q = output

Schematic (one gate)



Logic function $Q = \overline{A \wedge B}$

1) only in case of gate 1 and 4