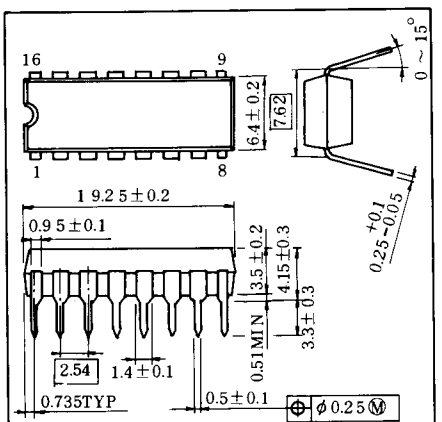
TC9142P

QUARTZ PLL MOTOR CONTROL

The TC9142P is a C^2-MOS LSI developed for controlling the motor of a quartz-lock D.D. record player. Since an 8-bit D/A converter system has been employed for each of the speed control system (AFC) and the phase control system (APC), a wide reduction of external parts can be made in comparison with conventional capacitor-type S/H systems, thus having realized adjustment free operation.



Package width and length do not include mold protrusion.
Allowable mold protrusion is 0.15mm.

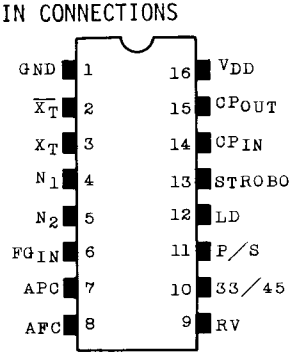
JEDEC	—
TOSHIBA	DIP16-P-300A

- Has built-in AFC and APC, for each of which 8-bit D/A converter system has been employed.
- Speed-changeover positions are available at 33 1/3 and 45-rpm.
- Crystal can be used up to 12 MHz, and crystal reference dividing frequency is selectable from three positions of 1/4, 1/32 and 1/128 to increase the degree of freedom in the number of FG pulses of motor or crystal frequency, which allows a wide range of design to be made.
- External oscillator makes possible fine adjustment of speed.
- Provided with strobe reference output and reverse signal output.

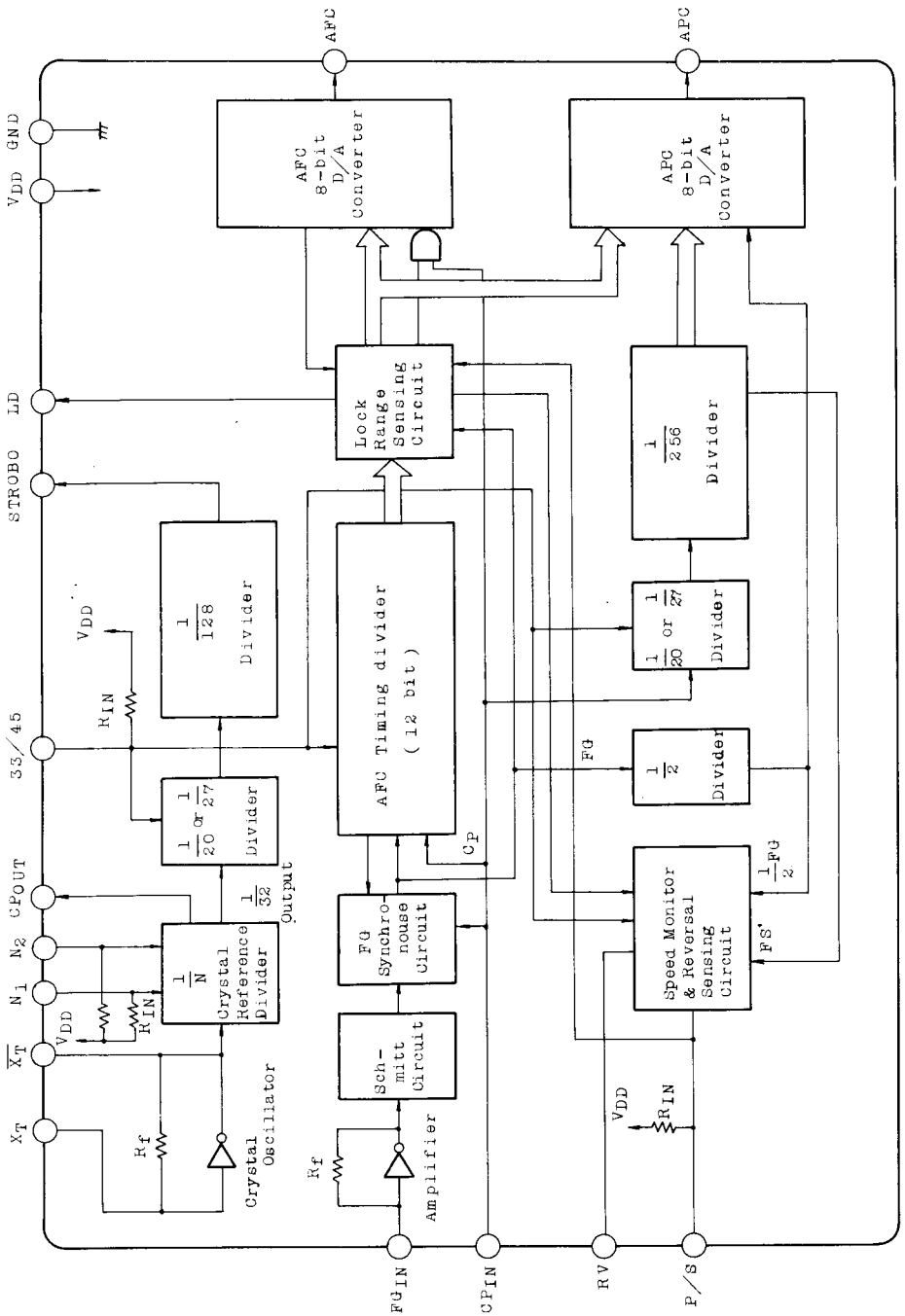
MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	-0.3 ∿ 10.0	V
Input Voltage	V_{IN}	-0.3 ∿ VDD + 0.3	V
Power Dissipation	P_D	300	mW
Operating Temperature	Topr	-30 ∿ 75	°C
Storage Temperature	Tstg	-55 ∿ 125	°C

PIN CONNECTIONS



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (Unless otherwise specified VDD=7.5V, Ta=25°C)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage		$V_{DD}(1)$		X'tal=6MHz, CP_{IN}=1.5MHz, *	5.0	∿	9.5	V
		$V_{DD}(2)$		X'tal=12MHz, CP_{IN}=3.0MHz, *	7.5	∿	9.5	V
Operating Supply Current		I_{DD}	1	X'tal=12MHz, CP_{IN}=3.0MHz, *	-	5.5	12	mA
Operating Frequency Range	X_T	$f_{MAX}(1)$	2	V_{DD}=5.0∿7.5V, *	1.0	∿	6.0	MHz
		$f_{MAX}(2)$		V_{DD}=7.5∿9.5V, *	1.0	∿	12.0	MHz
	CP_{IN}	$f_{MAX}(3)$	3	V_{DD}=5.0∿7.5V, *	-	∿	1.5	MHz
		$f_{MAX}(4)$		V_{DD}=7.5∿9.5V, *	-	∿	3.0	MHz
FG_{IN} Operating Frequency Range		f_{FG}		V_{DD}=5.0∿9.5V, V_{IN}=0.5V_{pp}, *	-	∿	10	kHz
FG_{IN} Input Amplitude Voltage	Operation	$V_{IN}(1)$	4	V_{DD}=5.0∿9.5V, f_{FG}∿10kHz Sine Wave *	0.5	∿	V_{DD} -0.5	V_{pp}
	Non-Operation	$V_{IN}(2)$		f_{FG}∿10kHz, Sine Wave *	0	∿	30	mV_{pp}
FG_{IN} Threshold Voltage Range		$V_{TH}(FG)$		V_{DD}=5.0∿9.5V, At time of DC connection	0.2 × V_{DD}	-	0.8 × V_{DD}	V
AFC, APC D/A Converter	Max. Deviation			V_{DD}=5.0∿9.5V, I_{OUT}=0	-	±2.5	±6.5	LSB
	Resolution				-	V_{DD} /256	-	V
	Ladder Resistor	$\overline{R_L}$	7		35	55	80	kΩ
	Temperature Drift			V_{DD}=5.0∿9.5V, *	-	±1	-	LSB
Ladder Resistor Temperature Factor				*	-	+0.55	+0.8	% /deg.
Amplifier Feedback Resistor		R_f	5		100	200	500	kΩ

N1, N2, 33/45, P/S, CP_{IN}

Pullup Resistor		R_{IN}	6	Except CP_{IN} Terminal	15	35	70	kΩ
Input Voltage	"H" Level	V_{IH}		V_{DD}=5.0∿9.5V Except N_1 and N_2 Terminal	0.7 × V_{DD}	-	V_{DD} +0.3	V
	"L" Level	V_{IL}			-0.3	-	0.3 × V_{DD}	V

RV, LD, STROBE, CP_{OUT}

Output Current	"H" Level	I_{OH}	8	V_{OH}=6.5V	-0.5	-	-	mA
	"L" Level	I_{OL}	9	V_{OL}=1.0V	0.5	-	-	mA

* : Ta=Range of -30∿+75°C

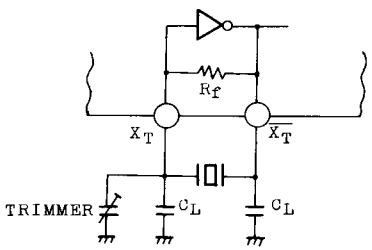
FUNCTIONAL EXPLANATION OF EACH TERMINAL

PIN NO.	SYMBOL	TERMINAL NAME	FUNCTIONAL & OPERATION EXPLANATION	REMARKS
16	V_{DD}	Power Termianl	V_{DD}=5-9.5V is applied	
1	GND	Ground Terminal	Ground.	
2 3	$\overline{X_T}$ X_T	Crystal Oscillation Terminal	Crystal Oscillator is connected.	With a built-in feedback resistor
6	FG_{IN}	FG Pulse Input Terminal	Input terminal for pulse showing motor speed.	With a built-in amplifier.
10	$33/45$	Speed Switching Terminal	Terminal for switching motor speed. L=33 1/3rpm, H or NC=45rpm.	With a built-in pull-up resistor.
11	P/S	PLAY/STOP Input Terminal	Motor PLAY/STOP signal input terminal L=PLAY, H or NC=STOP	With a built-in pull-up resistor.
14	CP_{IN}	Reference Frequency Input Terminal	Normally connected to CPOUT. For external fine adjustment input from an external oscillator.	
15	CPOUT	Reference Frequency Output Terminal	Terminal for divided output from the crystal reference frequency divider. Normally connected to CPIN.	
13	STROBE	Strobe Output Terminal	Reference frequency output termianl for strobe. Duty is 1/8.	
12	LD	Lock Detecting Terminal	This termianl becomes H when the motor speed is within the lock range and otherwise L.	
8	AFC	AFC Output Terminal	Output terminal for motor speed control system. Output of 8bit D/A converter.	
7	APC	APC Output Terminal	Output terminal for motor phase control system. Output of 8bit D/A converter.	
9	RV	Reverse Signal Output Treminal	Terminal for motor reverse signal Output.	
4 5	N_1 N_2	Reference Divided Frequency Switching Terminal	Switching of divided frequency from the crystal reference frequency divider into 1/4, 1/32 and 1/128 is possible.	With a built-in pull-up resistor.

EXPLANATION OF OPERATION

(1) Crystal oscillation terminals (X_T, $\overline{X_T}$)

. The crystal oscillator is used by connecting as shown below.



* C_L OF 10~30pF is appropriate.

. Crystal oscillation frequency is calculated by the following equation according to number of FG pulses of a motor to be used.

$$f_X = 3/4\ FG' \times 128 \times 20 \times N = 5/9\ FG' \times 128 \times 27 \times N = 1920\ FG' \cdot N \quad (Hz)$$

(Note) 3/4 FG' : FG_{IN} frequency at 45rpm.
5/9 FG' : FG_{IN} frequency at 33 1/3rpm.

Further, f_X: Crystal oscillation frequency, FG': No. of FG pulses generated per revolution of motor.

N : Ratio of frequency division of the crystal reference frequency divider. (Refer to Item (10).)

. Maximum operating frequency is above 12MHz and crystals up to 12MHz can be used.

(2) Reference frequency input/output terminals (CP_{OUT}, CP_{IN})

. Divided output $\frac{f_X}{N}$ from the crystal reference frequency divider is available at CP_{OUT}, which is normally connected to CP_{IN}.

. When an external oscillator (CR oscillator, etc.) is connected to CP_{IN}, motor speed can be finally adjusted.

(3) Strobe reference frequency output terminal (STROBE)

. This is the reference output terminal for strobe and $\frac{1}{32 \times (20 \text{ or } 27) \times 128}$ of crystal oscillation frequency is available at this terminal.

. Duty is 1/8 and suited to a single stripe strobe.

(4) FG pulse input terminal (FG_{IN})

. This is the input terminal of FG pulse that shows the motor speed. This FG pulse becomes comparison frequency.

. This terminal has built-in Amplifier and Schmitt circuit. FG pulses are applied through capacitor coupling and small amplitude is enough for proper operation.

(5) Speed switching terminal (33/45)

. This terminal is for switching the motor speed 33 1/3 and 45rpm, with a pull-up resistor and chattering preventive circuit.

(TRUTH TABLE)

33/45	DIVIDED FREQUENCY	SPEED
L	$\frac{1}{27}$	$33\frac{1}{3}$ rpm
H or NC	$\frac{1}{20}$	45rpm

(6) APC, AFC output terminal (APC, AFC)

. AFC (speed control output) is a F-V converter for FG frequency, and is consisting of a 8bit D/A converter.

. APC (phase control output) is a phase comparator (ϕ-V converter) that compares phase difference ϕ between 1/2 FG and reference frequency FS' , and is also consisting of a 8bit D/A converter.

. Both APC and AFC perform the following 3 operations according to FG_{IN} frequency.

a. When FG_{IN} frequency is within the lock range:

Both APC and AFC perform the normal operation for FG_{IN}.

Further, the Lock range is,

$$\begin{cases} \text{at 45rpm.....Reference cycle } \frac{1}{FS}\begin{cases} +4.6 \\ -5.3 \end{cases} \% \\ \text{at 33 1/3rpm .....Reference cycle } \frac{1}{FS}\begin{cases} +3.4 \\ -3.9 \end{cases} \% \end{cases}$$

(Note)

Reference frequency $FS = \frac{f_X}{N\ (20 \text{ or } 27)\ 128}$ (Hz), $FS' = \frac{1}{2}$ FS

b. When FG_{IN} frequency is below the lock range (under speed):

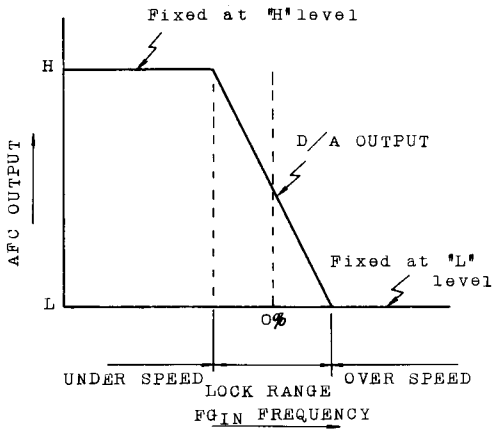
APC and AFC outputs are both fixed at "H" level.

c. When FG_{IN} frequency is above the lock range (over speed):

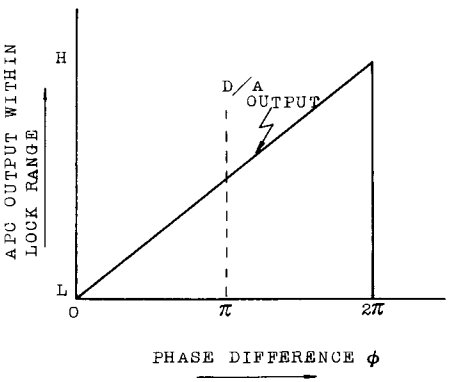
APC and AFC outputs are both fixed at "L" level.

. When a motor is in STOP state (P/S=H or NC), both AFC and APC are fixed "L" level.

AFC Output change status for FG_{IN} frequency

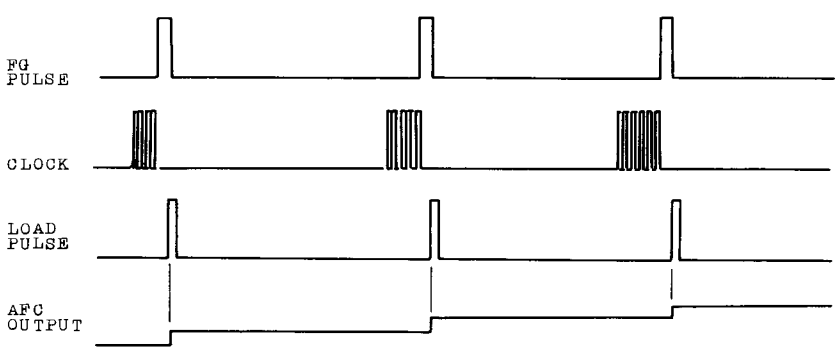


APC Output change status for phase difference ϕ.

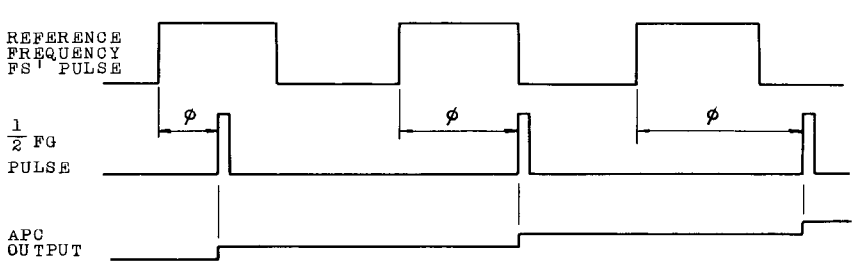


. AFC and APC timing chart within lock range.

a. AFC (SPEED CONTROL SYSTEM)



b. APC (PHASE CONTROL SYSTEM)



(7) Lock detecting terminal (LD)

. This terminal is the lock detecting output and is placed at "H" level when FG_{IN} frequency is within the lock range and otherwise, placed at "L" level.

(8) PLAY/STOP input terminal (P/S)

. PLAY/STOP signals of the motor are input to this terminal.
PLAY=L, STOP=H or NC.
. This terminal has a pull-up resistor and a chattering proventive circuit.
. During PLAY (P/S=L), AFC, APC and LD perform the above-mentioned operations for FG_{IN} frequency, and during STOP (P/S=H or NC), AFC, APC and LD are all fixed at "L" level.

(9) Reverse signal output terminal (RV)

. Reverse signal for braking the motor at time of switching of motor speed from 45rpm to 33 1/3rpm or the operation from PLAY to STOP is output through this terminal.
. Change of RV output status

PREVIOUS STATUS ⇨	RV OUTPUT CHANGE TO "H" LEVEL	⇨ RV OUTPUT CHANGE TO "L" LEVEL
During normal rotation (during lock) at 45rpm.	When the motor speed is switched from 45rpm to 33 1/3rpm.	When the motor speed is locked at 33 1/3rpm, or When $FG_{IN} \leqq 1/8$ FS, or When the motor speed is switched from 33 1/3rpm to 45rpm
During normal rotation (during lock) at 33 1/3 rpm or 45rpm.	When the operation is switched from PLAY to STOP.	When $FG_{IN} \leqq 1/8$ FS or When the operation is switched from STOP to PLAY.

. In other cases than above, RV output is not changed and fixed at "L" level.
. Further, if FG frequency rises up to 1.5 times of normal rotation at 45rpm. (2 times of normal rotation at 33rpm), RV output is reset.

(10) Reference divided frequency switching terminal (N1, N2)

. Divided frequency 1/N of the crystal reference frequency divider can be switched to 1/4, 1/32 or 1/128 by number of FG pulses or a crystal used.

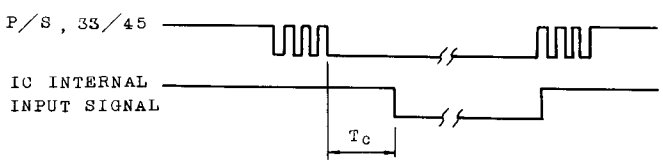
. This terminal has a built-in pull-up resistor.

(TRUTH TABLE)

N_1	N_2	$\frac{1}{N}$	STROBE OUTPUT FREQUENCY
H	H	$\frac{1}{32}$	$\frac{f_X\ [Hz]}{32 \times (20 \text{ or } 27) \times 128}$
L	H	$\frac{1}{128}$	$\frac{f_X\ [Hz]}{32 \times (20 \text{ or } 27) \times 128}$
H	L	$\frac{1}{4}$	$\frac{f_X\ [Hz]}{32 \times (20 \text{ or } 27) \times 128}$

$\frac{1}{N}$: CRISTAL REFERENCE DIVIDED FREQUENCY

(11) Chattering preventing time of P/S, 33/45 terminal: Tc

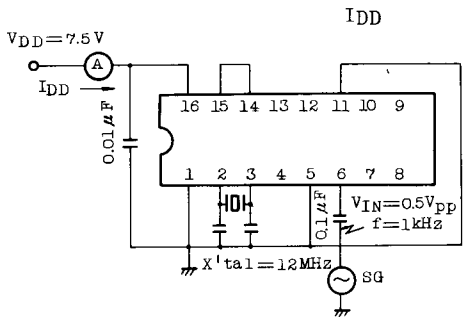


N_1	N_2	CHATTERING PREVENTING TIME Tc (S)	
		At 33rpm	At 45rpm
H	H	$\frac{1728}{f_{CP_{IN}}} \times (1 \sim 2)$	$\frac{1280}{f_{CP_{IN}}} \times (1 \sim 2)$
L	H	$\frac{432}{f_{CP_{IN}}} \times (1 \sim 2)$	$\frac{320}{f_{CP_{IN}}} \times (1 \sim 2)$
H	L	$\frac{6912}{f_{CP_{IN}}} \times (1 \sim 2)$	$\frac{5120}{f_{CP_{IN}}} \times (1 \sim 2)$

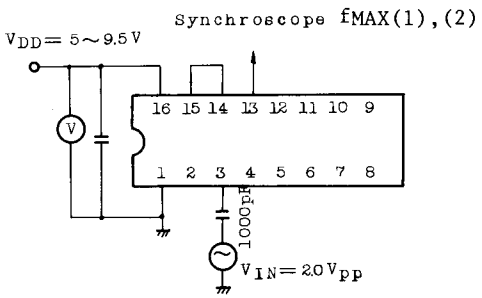
$f_{CP_{IN}}$: CP_{IN} INPUT FREQUENCY (Hz)

CHARACTERISTIC TEST CIRCUIT

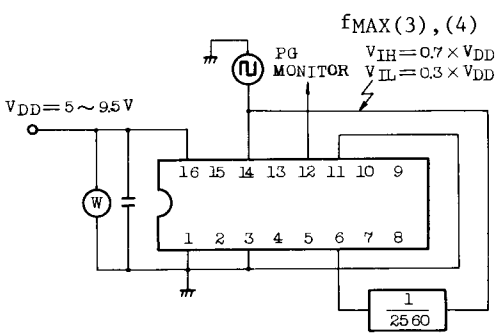
(1) Operating supply current



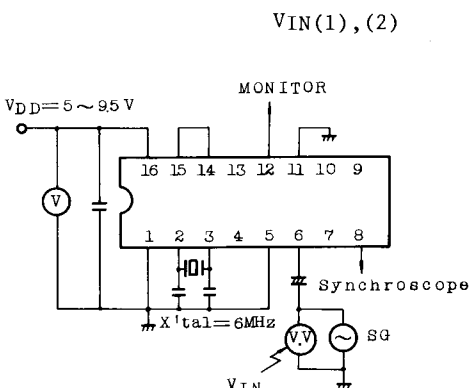
(2) X_T Operating frequency range



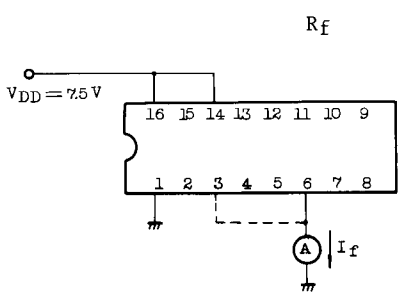
(3) CP_{IN} Operating frequency range



(4) FG_{IN} Input sensitivity

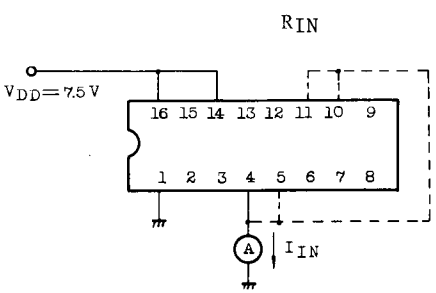


(5) Amplifier feedback resistor



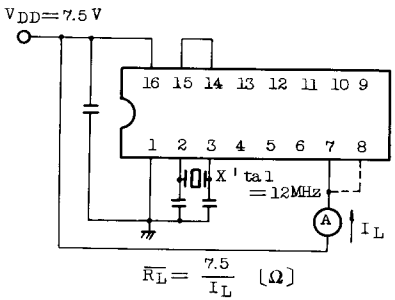
$$R_f = \frac{7.5}{I_f} \ [\Omega]$$

(6) Pullup resistor

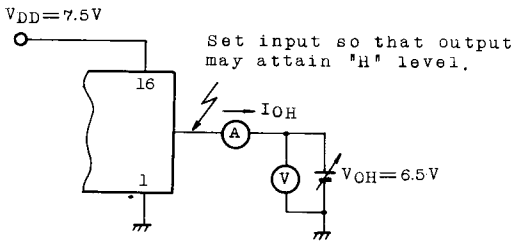


$$R_{IN} = \frac{7.5}{I_{IN}} \ [\Omega]$$

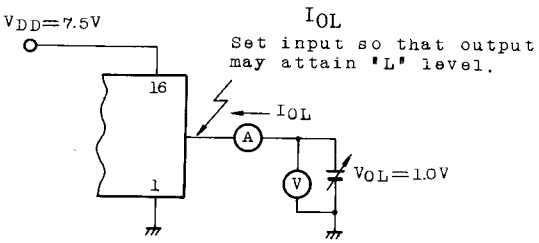
(7) D/A Converter ladder resistor $\overline{R_L}$



(8) Output current ("H" level) I_{OH}

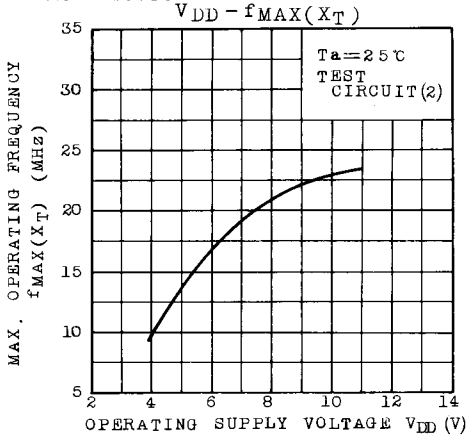


(9) Output current ("L" level) I_{OL}

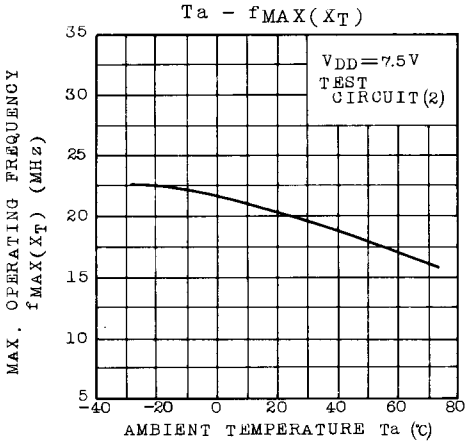


CHARACTERISTIC DATA

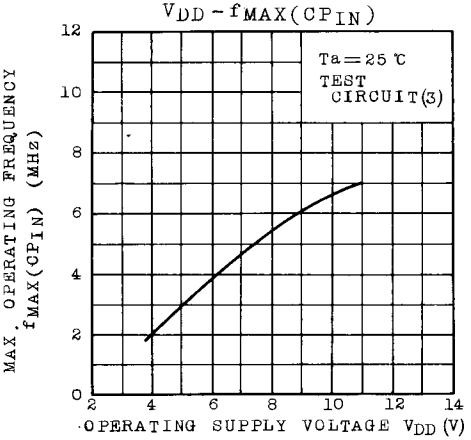
$V_{DD} - f_{MAX}(X_T)$



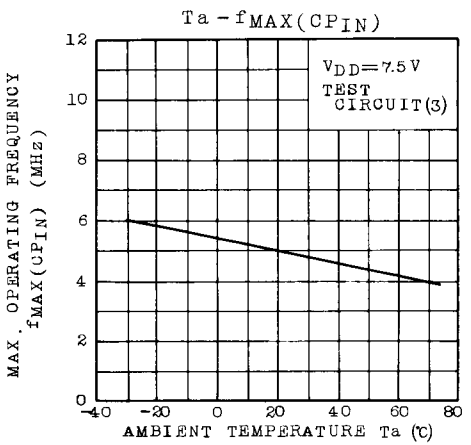
$Ta - f_{MAX}(X_T)$



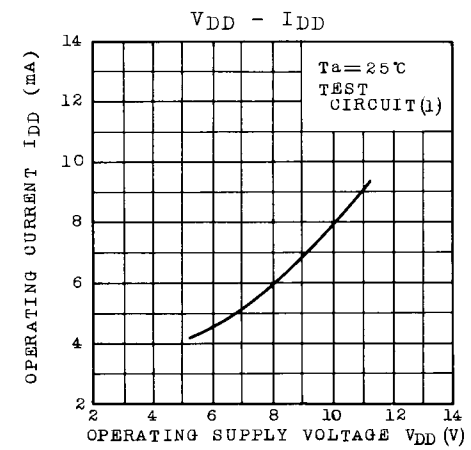
$V_{DD} - f_{MAX}(CP_{IN})$



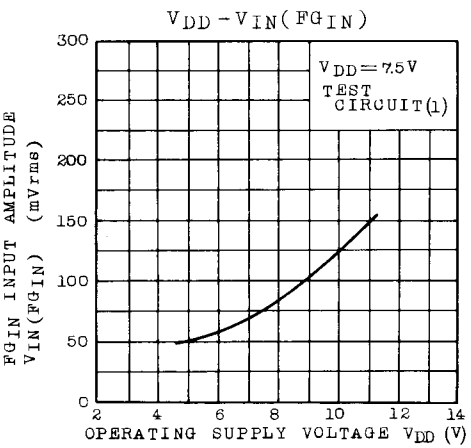
$Ta - f_{MAX}(CP_{IN})$



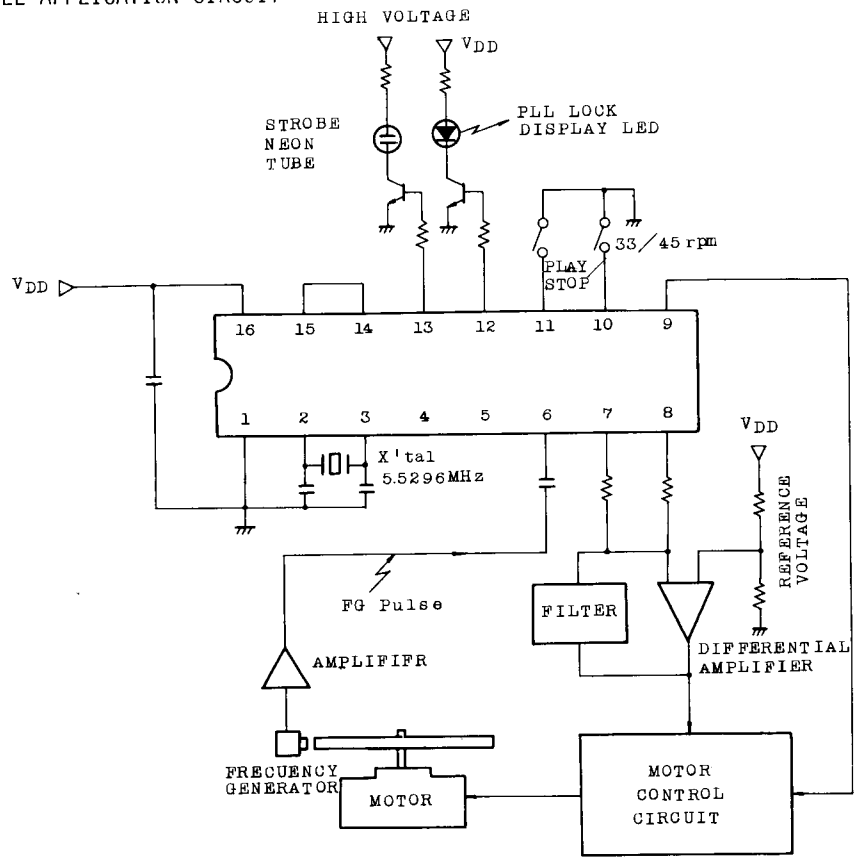
$V_{DD} - I_{DD}$



$V_{DD} - V_{IN}(FG_{IN})$



EXAMPLE APPLICATION CIRCUIT



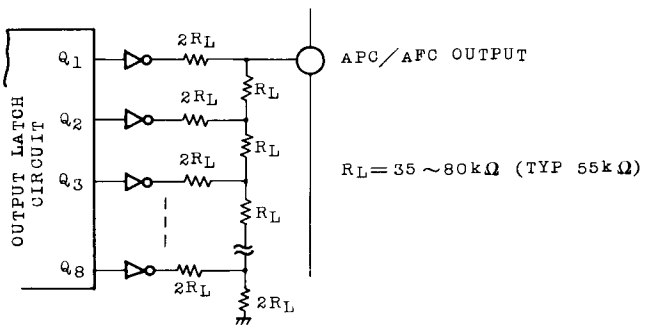
Example of crystal oscillation frequency calculation

When FG' (number of FG pulse)=90 pulses, if the dividing frequency of reference divider is set at N=32 dividing frequency, the crystal oscillation frequency f_X is as follows :

$$f_X = 1920.FG'N = 1920 \times 90 \times 32 = 5,5296MHz$$

CAUTION IN APPLICATION

. APC and AFC terminals are for the 8-bit D/A converter outputs, which are directly output from the R-2R ladder type resistor network as shown in the following diagram. Impedance of these outputs becomes equal to the ladder resistor value R_L. Terefore, input impedance at the receiving side of these terminals shall be designed accordingly.



. A filter for an externally mounted differential amplifier on an application circuit shall be selected to meet the response characteristic of a motor to be used.