SHARP

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To ;

SPECIFICATIONS

Product Type 80 Output LCD Segment Driver

Model No. LH1514AF

※This tentative specifications contains 20 pages including the cover and appendix.
If you have any objections, please contact us before issuing purchasing order.

CUSTOMERS ACCEPTANCE

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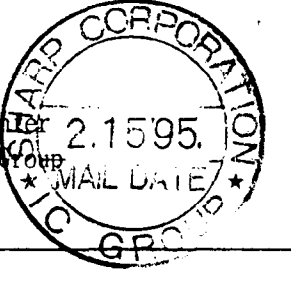

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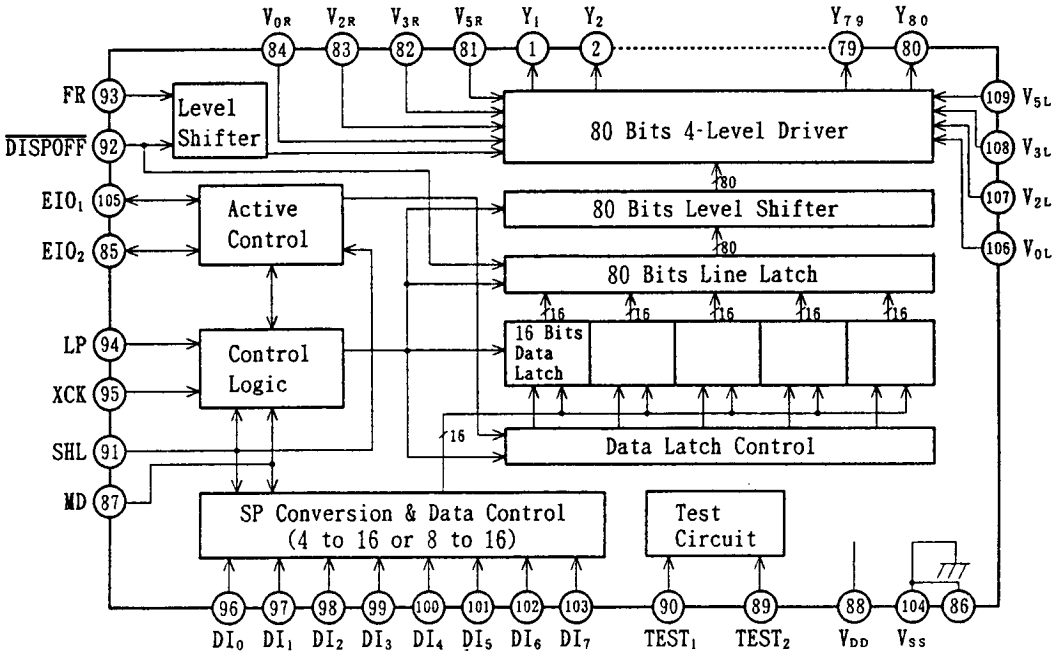
1. Summary

The LH1514AF is a 80 output segment driver LSI suitable for driving black and white dot matrix LC panels.
Through the use of SST (Super Slim TCP) technology, it is ideal for substantially decreasing the size of the frame section of the LC module.
The LH1514AF is particularly well suited to driving black and white LC panels used for palmtop personal computers because of its low-voltage operation (Supply voltage for logic system : -5.5 to -2.5 V).
When combined with the LH1513A Common Driver, a low power consuming, high-precision LC panel display can be assembled.

2. Features

- Supply voltage for the logic system : -5.5 to -2.5 V
- Supply voltage for LC drive : -28.0 to -10.0 V
  (absolute maximum rating -30.0 V)
- Number of LC drive outputs : 80
- Low output impedance : 1.5 kΩ (Typ.)
- Shift Clock frequency : 6.5 MHz (Max.)
- Low power consumption
- Adopts a data bus system
- 4-bit/8-bit parallel input modes are selectable with a mode (MD) pin
- Automatic transfer function of an enable signal
- Automatic counting function which, in the chip select mode, causes the internal clock to be stopped by automatically counting 80 of input data
- Line latch circuit reset function when DISPOFF active
- Supports high capacity LC panel display when combined with the LH1513A Common Driver
- CMOS process (N-type Silicon Substrate)
- Package : 109 pin TCP (Tape Carrier Package)
- Not designed or rated as radiation hardened

3. Block Diagram

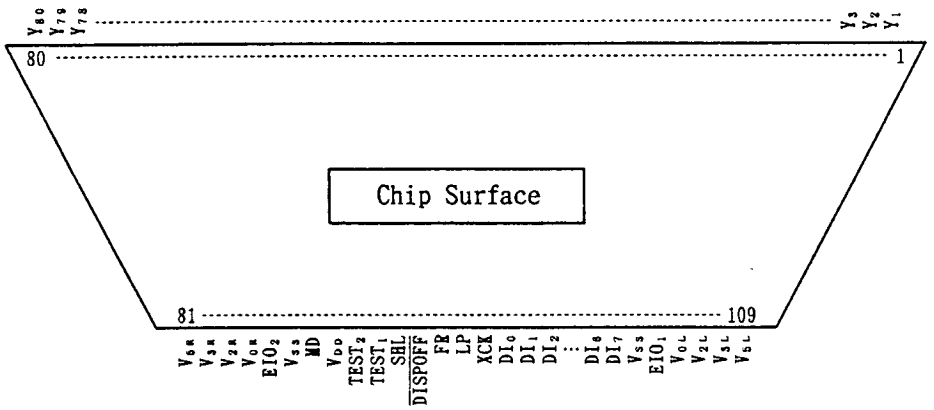


4. Functional Operations of Each Block

Block	Function
Active Control	Controls the selection or deselection of the chip. Following a LP signal input, and after the chip select signal is input, a select signal is generated internally until 80 bits of data have been read in. Once data input has been completed, a select signal for cascade connection is output, and the chip is deselected.
SP Conversion & Data Control	Keep input data which are 4 clocks of XCK at 4-bit parallel mode into latch circuit,or keep input data which are 2 clocks of XCK at 8-bit parallel mode into latch circuit,after that they are put on the internal data bus 16 bits at a time.
Data Latch Control	Selects the state of the data latch which reads in the data bus signals. The shift direction is controlled by the control logic, for every 16 bits of data read in, the selection signal shifts one bit based on the state of the control circuit.
Data Latch	Latches the data on the data bus. The latched state of each LC driver output pin is controlled by the control logic and the data latch control, 80 bits of data are read in five sets of 16 bits.
Line Latch	All 80 bits which have been read into the data latch are simultaneously latched on the falling edge of the LP signal, and output to the level shifter block.

Block	Function
Level Shifter	The logic voltage signal is level-shifted to the LC drive voltage level, and output to the driver block.
4-Level Driver	Drives the LC driver output pins from the latch data, selecting one of 4 levels (V_0, V_2, V_3, V_5) based on the FR and $\overline{\text{DISPOFF}}$ signals.
Control Logic	Controls the operation of each block. When a LP signal has been input, all blocks are reset and the control logic waits for the selection signal output from the active control block. Once the selection signal has been output, operation of the data latch and data transmission are controlled, 80 bits of data are read in, and the chip is deselected.

5. Pin Configuration

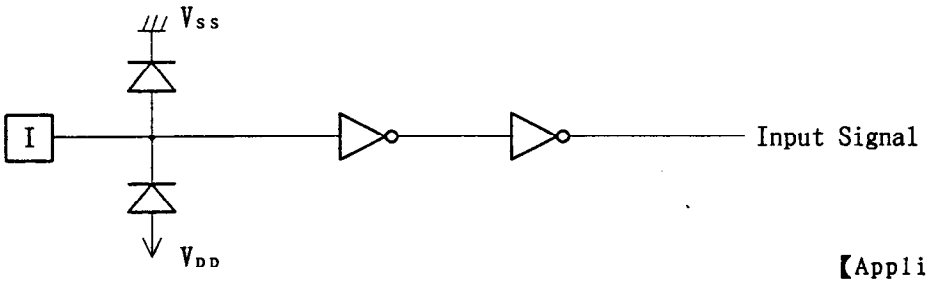


6. Pin Descriptions

6-1. Pin Designations

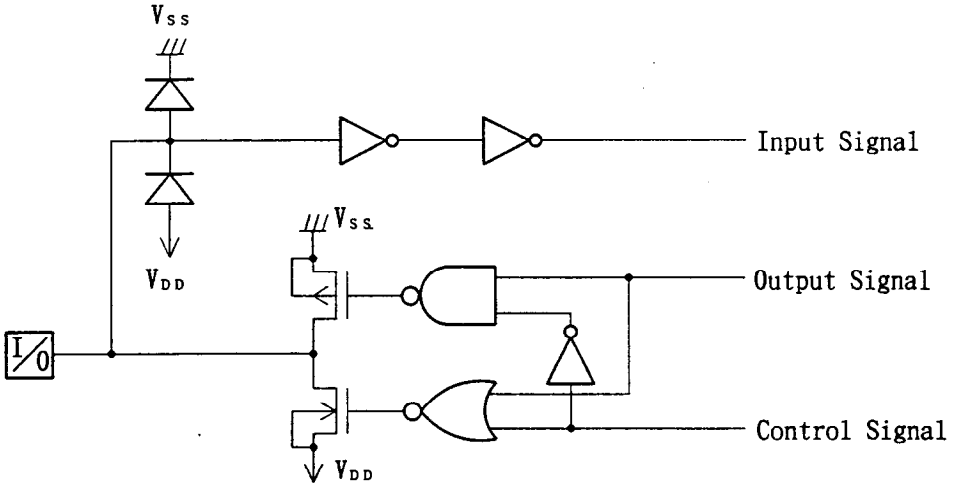
Pin No.	Symbol	I/O	Designation
1 to 80	Y_1-Y_{80}	O	LC drive output
81, 109	V_{5R}, V_{5L}	-	Power supply for LC drive
82, 108	V_{3R}, V_{3L}	-	Power supply for LC drive
83, 107	V_{2R}, V_{2L}	-	Power supply for LC drive
84, 106	V_{0R}, V_{0L}	-	Power supply for LC drive
85, 105	EIO_2, EIO_1	I/O	Input/Output for chip select
86, 104	V_{SS}	-	Ground (0 V)
87	MD	I	Mode selection input
88	V_{DD}	-	Power supply for logic system (-5.5 to -2.5 V)
89	$TEST_2$	I	Test mode selection input
90	$TEST_1$	I	Test mode selection input
91	SHL	I	Display data shift direction selection
92	$\overline{DISPOFF}$	I	Control input for deselect output level
93	FR	I	AC-converting signal input for LC drive waveform
94	LP	I	Display data latch pulse input
95	XCK	I	Display data shift clock input
96 to 103	DI_0-DI_7	I	Display data input

6-2. Input/Output Circuits



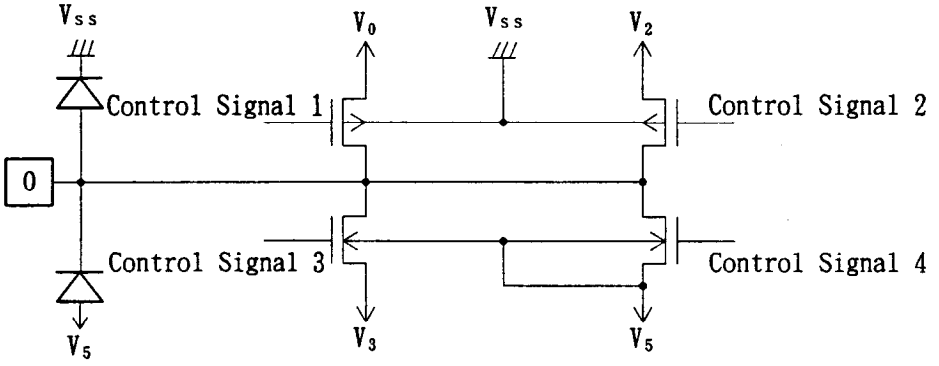
【Applicable pins】
DI_{0-7}, XCK, LP, FR
SHL, MD, $\overline{DISPOFF}$

Fig.1 Input Circuit



【Applicable pins】
EIO_1, EIO_2

Fig.2 Input/Output Circuit



【Applicable pins】
Y_1-Y_{80}

Fig.3 LC Drive Output Circuit

7. Description of Functional Operations

7-1. Pin Functions

Symbol	Function
V_{DD}	Logic system power supply pin connects to -5.5 to -2.5 V
V_{SS}	Ground pin connects to 0 V
V_{0R}, V_{0L} V_{2R}, V_{2L} V_{3R}, V_{3L} V_{5R}, V_{5L}	Power supply pin for LC driver voltage bias. •Normally, the bias voltage used is set by a resistor divider. •Ensure that voltages are set such that $V_{SS} \geqq V_0 > V_2 > V_3 > V_5$. •To further reduce the difference between the output waveforms of LC driver output pins Y_1 and Y_{80}, externally connect V_{iR} and V_{iL} (i=0, 2, 3, 5).
DI_0-DI_7	Input Pin for display data •In 4-bit parallel input mode, input data into the 4 pins DI_0-DI_3. Connect DI_4-DI_7 to V_{SS} or V_{DD}. •In 8-bit parallel input mode, input data into the 8 pins DI_0-DI_7.
XCK	Clock input pin for taking display data •Data is read on the falling edge of the clock pulse.
LP	Latch pulse input pin for display data •Data is latched on the falling edge of the clock pulse.
SHL	Direction selection pin for reading display data •When set to V_{DD} level "L", data is read sequentially from Y_{80} to Y_1. •When set to V_{SS} level "H", data is read sequentially from Y_1 to Y_{80}.
$\overline{DISPOFF}$	Control input pin for output deselect level •The input signal is level-shifted from logic voltage level to LC drive voltage level,and controls LC drive circuit. •When set to V_{DD} level "L",the LC drive output pins (Y_1-Y_{80}) are set to level V_0. •While set to "L",the contents of the line latch are reset,but read the display data in the data latch regardless of condition of $\overline{DISPOFF}$. When the $\overline{DISPOFF}$ function is canceled,the driver outputs deselect level (V_2 or V_3),then outputs the contents of the date latch on the next falling edge of the LP. That time,if $\overline{DISPOFF}$ removal time can not keep regulation what is shown AC characteristics(Page 14),can not output the reading data correctly.
FR	AC signal input for LC driving waveform •The input signal is level-shifted from logic voltage level to LC drive voltage level,and controls LC drive circuit. •Normally,inputs a frame inversion signal. •The LC driver output pin's output voltage level can be set using the line latch output signal and the FR signal.Table of truth values is shown in 7-2-1.

Symbol	Function
MD	Mode selection pin •When set to V_{DD} level "L", 4-bit parallel input mode is set. •When set to V_{SS} level "H", 8-bit parallel input mode is set. •The relationship between the display data and driver output pins is shown in 7-2-2.
EIO_1 EIO_2	Input/Output pin for chip selection •When SHL input is at V_{DD} level "L", EIO_1 is set for output, and EIO_2 is set for input. •When SHL input is at V_{SS} level "H", EIO_1 is set for input, and EIO_2 is set for output. •During output, set to "H" while LP*$\overline{XCK}$ is "H" and after 80 bits of data have been read set to "L" for one cycle (from falling edge to falling edge of the XCK),after which it return to "H". •During input, after the LP signal is input, the chip is selected while EI is set to "L". After 80-bits of data have been read, the chip is deselected.
$TEST_1$ $TEST_2$	Test mode select pin •During normal operation, tie to V_{DD} level "L".
Y_1-Y_{80}	LC driver output pins •Corresponding directly to each bit of the data latch, one level (V_0, V_2, V_3, or V_5) is selected and output.

7-2. Functional Operations

7-2-1. Truth Table

FR	Latch Data	$\overline{DISPOFF}$	Driver Output Voltage Level (Y_1-Y_{80})
L	L	H	V_2
L	H	H	V_0
H	L	H	V_3
H	H	H	V_5
x	x	L	V_0

Here, $V_{SS} \geq V_0 > V_2 > V_3 > V_5$, L : V_{DD}(-5.5 to -2.5 V), H : V_{SS}(0 V), x : Don't care

【Note】 "Don't care" should be fixed to "H" or "L", avoiding floating.

There are two kinds of power supply (logic level voltage,LC drive voltage) for LCD driver, please supply regular voltage which assigned by specification for each power pin.

7-2-2. Relationship between the Display Data and Driver Output pins

(a) 4-Bit Parallel Mode

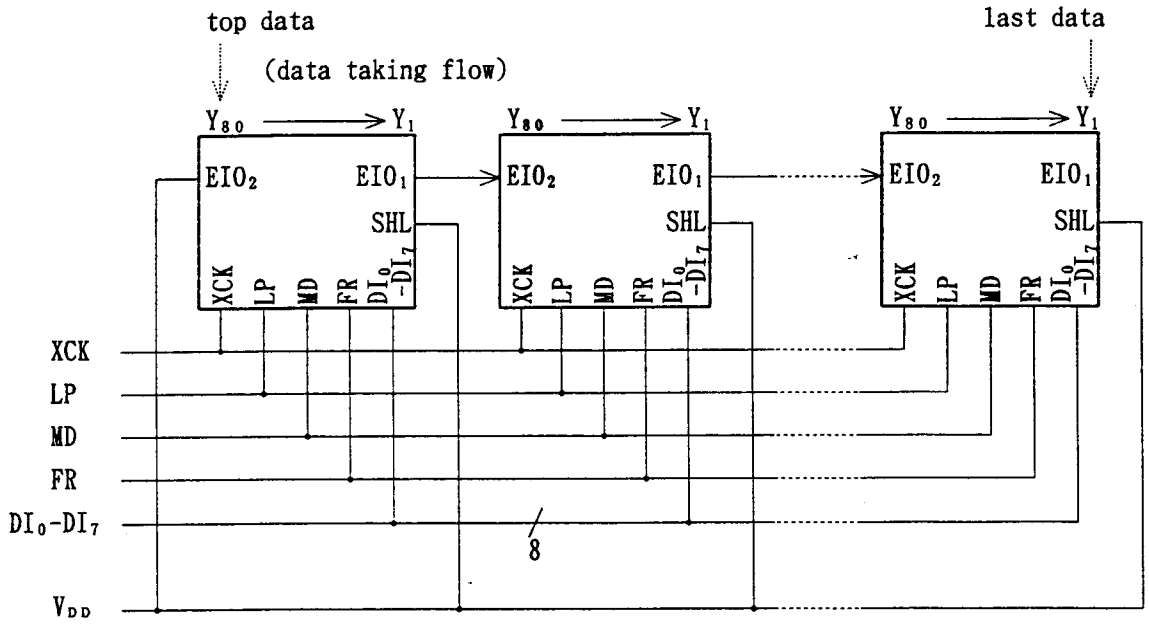
MD	SHL	EIO_1	EIO_2	Data Input	Figure of Clock						
					20clock	19clock	18clock	···	3clock	2clock	1clock
L	L	Output	Input	DI_0	Y_1	Y_5	Y_9	···	Y_{69}	Y_{73}	Y_{77}
				DI_1	Y_2	Y_6	Y_{10}	···	Y_{70}	Y_{74}	Y_{78}
				DI_2	Y_3	Y_7	Y_{11}	···	Y_{71}	Y_{75}	Y_{79}
				DI_3	Y_4	Y_8	Y_{12}	···	Y_{72}	Y_{76}	Y_{80}
L	H	Input	Output	DI_0	Y_{80}	Y_{76}	Y_{72}	···	Y_{12}	Y_8	Y_4
				DI_1	Y_{79}	Y_{75}	Y_{71}	···	Y_{11}	Y_7	Y_3
				DI_2	Y_{78}	Y_{74}	Y_{70}	···	Y_{10}	Y_6	Y_2
				DI_3	Y_{77}	Y_{73}	Y_{69}	···	Y_9	Y_5	Y_1

(b) 8-Bit Parallel Mode

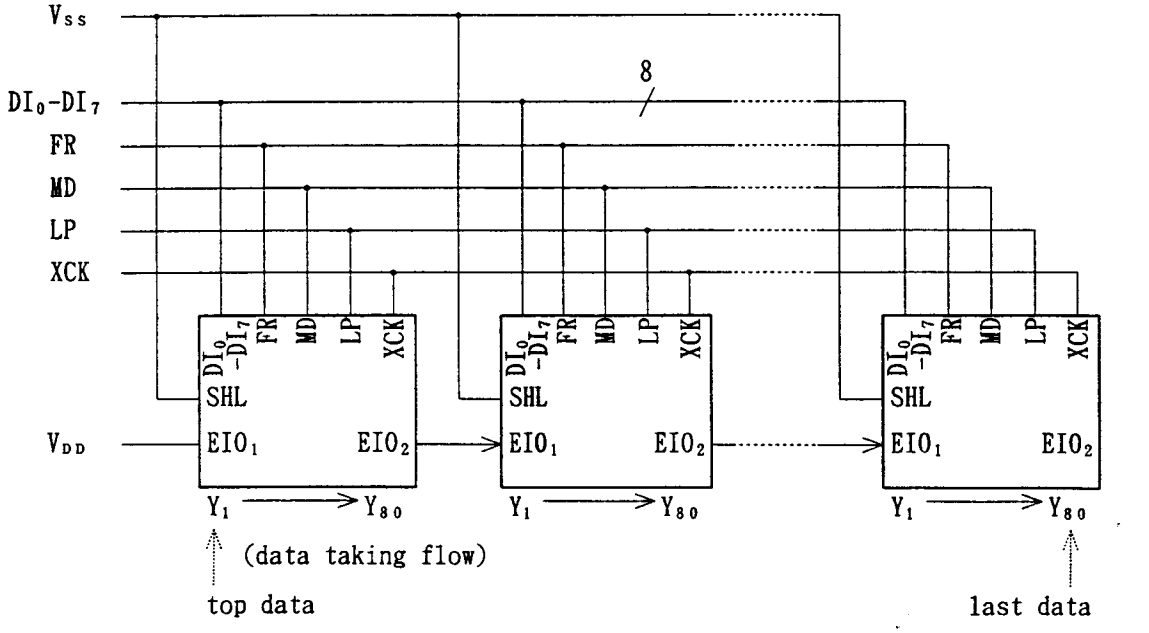
MD	SHL	EIO_1	EIO_2	Data Input	Figure of Clock						
					20clock	19clock	18clock	···	3clock	2clock	1clock
H	L	Output	Input	DI_0	Y_1	Y_9	Y_{17}	···	Y_{57}	Y_{65}	Y_{73}
				DI_1	Y_2	Y_{10}	Y_{18}	···	Y_{58}	Y_{66}	Y_{74}
				DI_2	Y_3	Y_{11}	Y_{19}	···	Y_{59}	Y_{67}	Y_{75}
				DI_3	Y_4	Y_{12}	Y_{20}	···	Y_{60}	Y_{68}	Y_{76}
				DI_4	Y_5	Y_{13}	Y_{21}	···	Y_{61}	Y_{69}	Y_{77}
				DI_5	Y_6	Y_{14}	Y_{22}	···	Y_{62}	Y_{70}	Y_{78}
				DI_6	Y_7	Y_{15}	Y_{23}	···	Y_{63}	Y_{71}	Y_{79}
				DI_7	Y_8	Y_{16}	Y_{24}	···	Y_{64}	Y_{72}	Y_{80}
H	H	Input	Output	DI_0	Y_{80}	Y_{72}	Y_{64}	···	Y_{24}	Y_{16}	Y_8
				DI_1	Y_{79}	Y_{71}	Y_{63}	···	Y_{23}	Y_{15}	Y_7
				DI_2	Y_{78}	Y_{70}	Y_{62}	···	Y_{22}	Y_{14}	Y_6
				DI_3	Y_{77}	Y_{69}	Y_{61}	···	Y_{21}	Y_{13}	Y_5
				DI_4	Y_{76}	Y_{68}	Y_{60}	···	Y_{20}	Y_{12}	Y_4
				DI_5	Y_{75}	Y_{67}	Y_{59}	···	Y_{19}	Y_{11}	Y_3
				DI_6	Y_{74}	Y_{66}	Y_{58}	···	Y_{18}	Y_{10}	Y_2
				DI_7	Y_{73}	Y_{65}	Y_{57}	···	Y_{17}	Y_9	Y_1

7-2-3. Connection Examples of Plural Segment Drivers

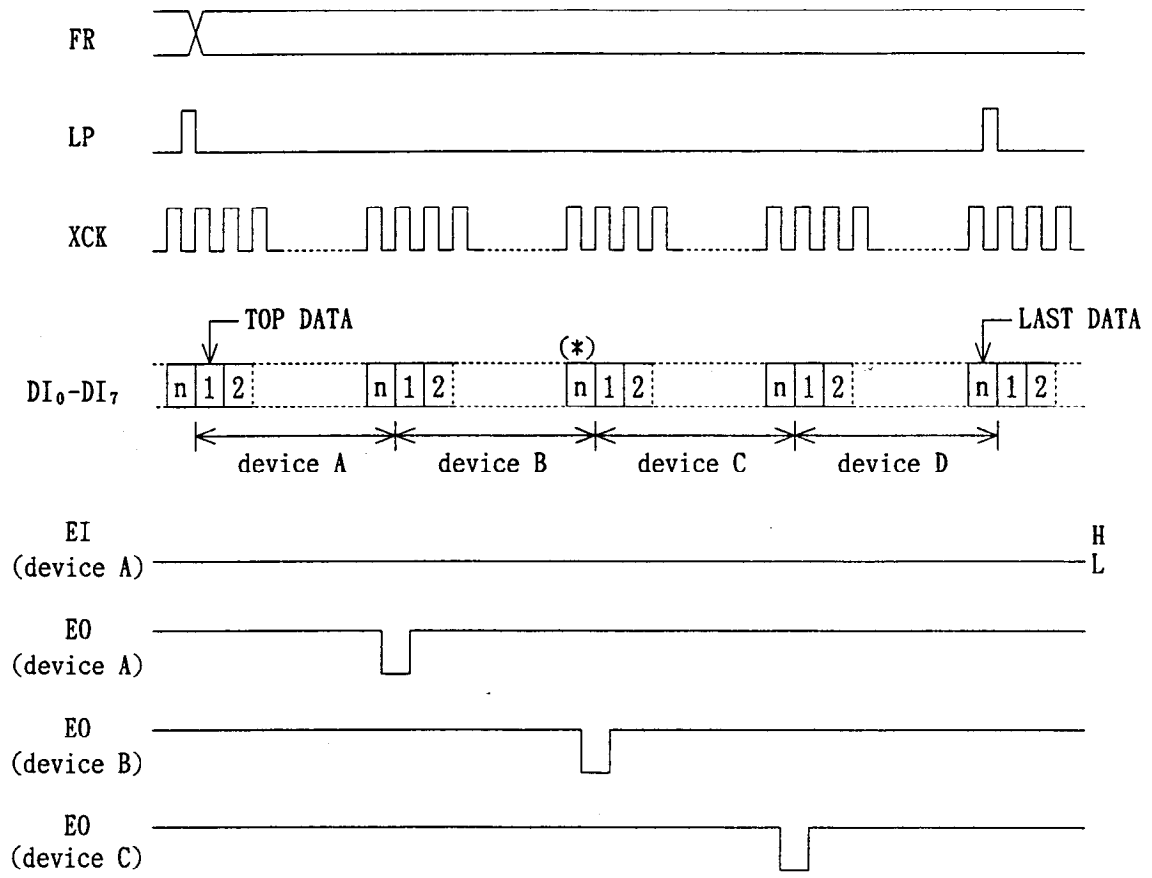
(a) Case of SHL="L"



(b) Case of SHL="H"



7-2-4. Timing Chart of 4-Device cascade Connection



(*) n : 4-bit parallel mode 20
8-bit parallel mode 10

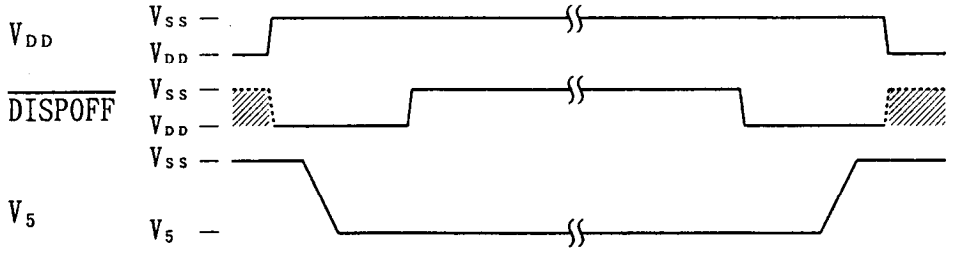
8. Precaution

○Precaution when connecting or disconnecting the power

This LSI has a high-voltage LCD driver, so it may be permanently damaged by a high current which may flow if a voltage is supplied to the LC drive power supply while the logic system power supply is floating.
The detail is as follows.

- When connecting the power supply, connect the LC drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LC drive power.
- We recommend you connecting the serial resistor (50 to 100 Ω) to the LC drive power V_5 of the system as a current limitter resistor. And set up the suitable value of the resistor in consideration of LC display grade.

And when connecting the logic power supply, the logic condition of this LSI inside is insecurity. Therefore connecting the LC drive power supply after resetting logic condition of this LSI inside on $\overline{DISPOFF}$ function. After that, cancel the $\overline{DISPOFF}$ function after the LC drive power supply has become stable. Furthermore, when disconnecting the power, set the LC driver output pins to level V_0 on $\overline{DISPOFF}$ function. After that, disconnect the logic system power after disconnecting the LC drive power.
When connecting the power supply, show the following recommend sequence.



9. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Applicable pins	Ratings	Unit
Supply voltage (1)	V_{DD}	Ta=25 ℃	V_{DD}	-7.0 to +0.3	V
Supply voltage (2)	V_0	Referenced	V_{0L}, V_{0R}	V_5-0.3 to +0.3	V
	V_2	to V_{SS}(0 V)	V_{2L}, V_{2R}	V_5-0.3 to +0.3	V
	V_3		V_{3L}, V_{3R}	V_5-0.3 to +0.3	V
	V_5		V_{5L}, V_{5R}	-30.0 to +0.3	V
Input voltage	V_I		DI_{0-7}, XCK, LP, $\overline{SHL}$, FR, MD, EIO_1, EIO_2, $\overline{DISPOFF}$	V_{DD}-0.3 to +0.3	V
Storage temperature	T_{stg}			-45 to +125	℃

10. Recommended Operating Conditions

Parameter	Symbol	Conditions	Applicable pins	Min.	Typ.	Max.	Unit
Supply voltage (1)	V_{DD}	Referenced	V_{DD}	-5.5		-2.5	V
Supply voltage (2)	V_5	to V_{SS}(0 V)	V_{5L}, V_{5R}	-28.0		-10.0	V
Operating temperature	T_{opr}			-20		+85	℃

11. Electrical Characteristics

11-1. DC Characteristics

(V_{SS}=V_0=0 V, V_{DD}=-5.5 to -2.5 V, V_5=-28.0 to -10.0 V, Ta=-20 to +85 ℃)

Parameter	Symbol	Conditions	Applicable pins	Min.	Typ.	Max.	Unit
Input voltage	V_{IH}		DI_{0-7}, XCK, LP, $\overline{SHL}$, FR	0.2V_{DD}			V
	V_{IL}		MD, EIO_1, EIO_2, $\overline{DISPOFF}$			0.8V_{DD}	V
Output voltage	V_{OH}	I_{OH}=-0.4 mA	EIO_1, EIO_2	-0.4			V
	V_{OL}	I_{OL}=+0.4 mA				V_{DD}+0.4	V
Input leakage current	I_{LI}	V_{SS}≦V_I≦V_{DD}	DI_{0-7}, XCK, LP, SHL, FR, MD, $\overline{DISPOFF}$			±10.0	μA
I/O leakage current	$I_{LI/O}$	V_{SS}≦V_I≦V_{DD}	EIO_1, EIO_2			±10.0	μA
Output resistance	R_{ON}	*1	Y_1-Y_{80}		1.5	3.0	kΩ
Stand-by current	I_{STB}	*2	V_{SS}			50.0	μA
Consumed current (1) (Deselection)	I_{DD1}	V_{DD}=-3 V,*3	V_{DD}			0.6	mA
		V_{DD}=-5 V,*3				1.0	mA
Consumed current (2) (Selection)	I_{DD2}	V_{DD}=-3 V,*3	V_{DD}			3.0	mA
		V_{DD}=-5 V,*3				5.0	mA
Consumed current (3)	I_5	V_{DD}=-3 V,*4	V_{5L}, V_{5R}			1.0	mA
		V_{DD}=-5 V,*4				1.0	mA

【Note】

*1 : $|\Delta V_{ON}|$=0.5 V

*2 : V_{DD}=-5.0 V, V_5=-28.0 V, V_{IH}=V_{SS}, V_{IL}=V_{DD}, $TEST_1$=$TEST_2$=V_{DD}

*3 : V_5=-28.0 V, f_{XCK}=6.15 MHz, No-load
The input data is turned over by data taking clock(4-bit parallel input mode)

*4 : V_5=-28.0 V, f_{XCK}=6.15 MHz, f_{LP}=19.2 kHz, f_{FR}=80 Hz, No-load
The input data is turned over by data taking clock(4-bit parallel input mode)

11-2. AC Characteristics

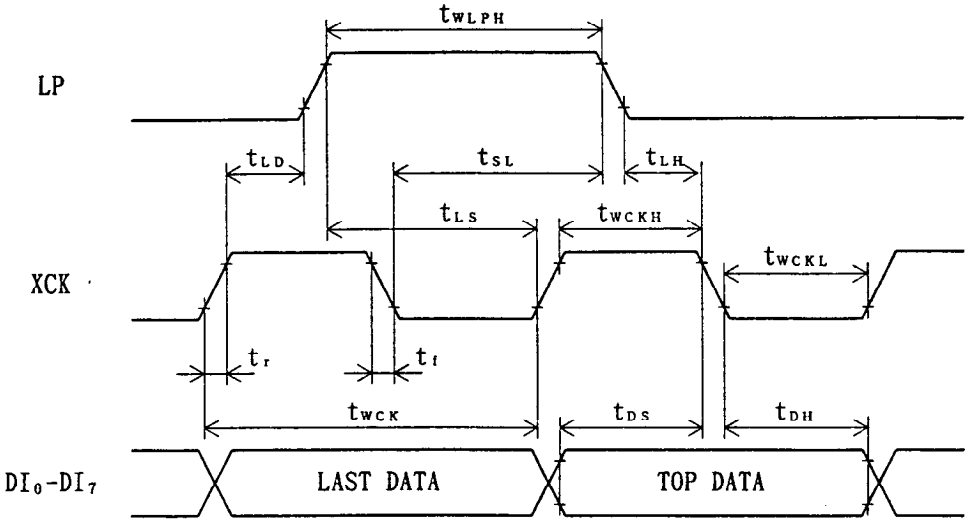
(V_{SS}=V_0=0 V, V_{DD}=-5.5 to -2.5 V, V_5=-28.0 to -10.0 V, Ta=-20 to +85 ℃)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Shift clock period	t_{WCK}	t_r, t_f≦11 ns	152			ns
Shift clock "H" pulse width	t_{WCKH}		65			ns
Shift clock "L" pulse width	t_{WCKL}		65			ns
Data setup time	t_{DS}		50			ns
Data hold time	t_{DH}		40			ns
Latch pulse "H" pulse width	t_{WLPH}		65			ns
Shift clock rise to Latch pulse rise time	t_{LD}		0			ns
Shift clock fall to Latch pulse fall time	t_{SL}		65			ns
Latch pulse rise to Shift clock rise time	t_{LS}		65			ns
Latch pulse fall to Shift clock fall time	t_{LH}		65			ns
Enable setup time	t_S		45			ns
$\overline{\text{DISPOFF}}$ "L" pulse width	t_{WDL}		1.2			μs
$\overline{\text{DISPOFF}}$ removal time	t_{rem}		100			ns
Input signal rise time	t_r	Note			50	ns
Input signal fall time	t_f				50	ns
Output delay time (1) XCK to EIO_1, EIO_2	t_D	C_L=15 pF			95	ns
Output delay time (2) FR to Y_1-Y_{80}	tpd_1				1.2	μs
Output delay time (3) LP to Y_1-Y_{80}	tpd_2				1.2	μs
Output delay time (4) $\overline{\text{DISPOFF}}$ to Y_1-Y_{80}	tpd_3				1.2	μs

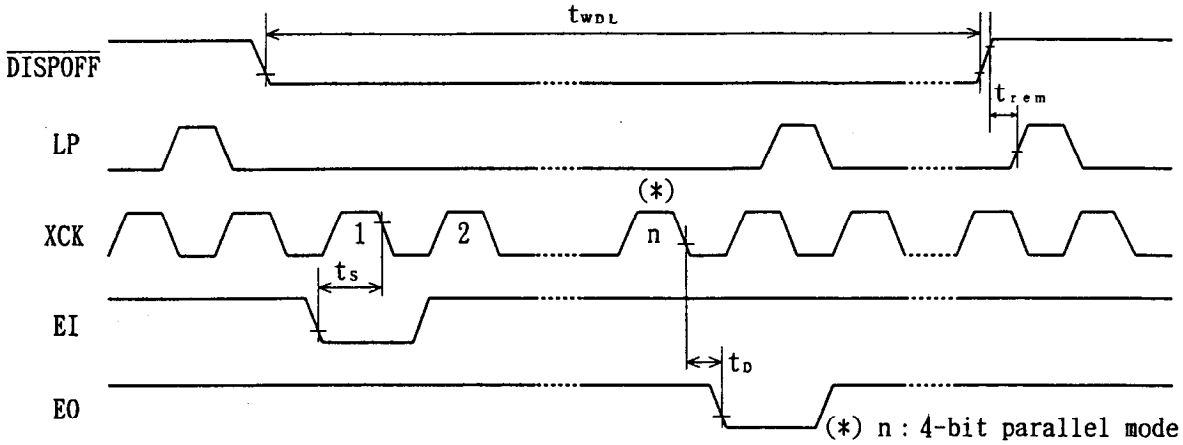
【Note】 (t_{CK}-t_{WCKH}-t_{WCKL})/2 is maximum in the case of high speed operation.

11-3. Timing Diagrams

Input Timing Characteristics

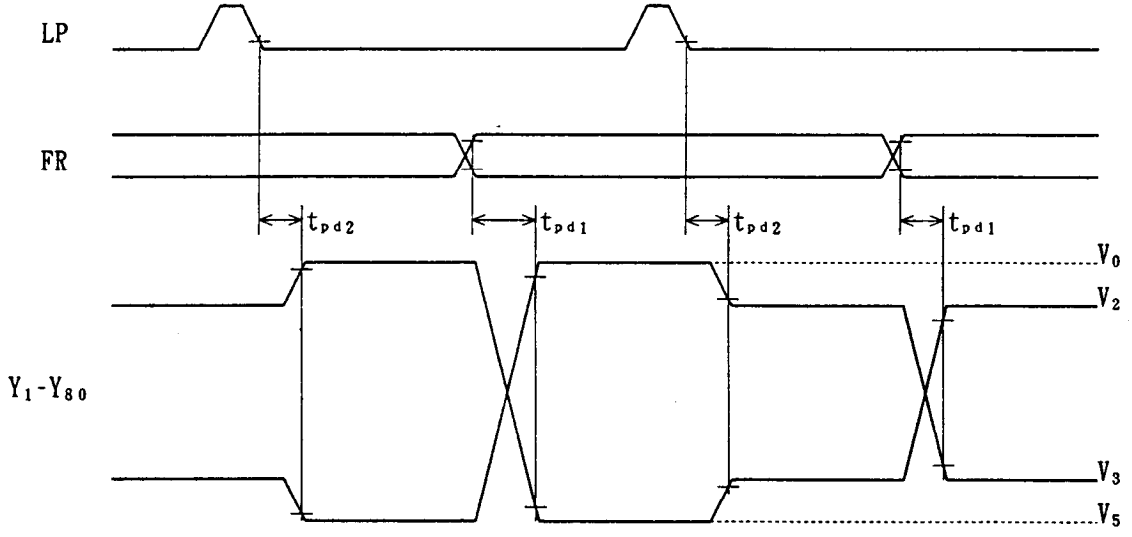


Input/Output Timing Characteristics

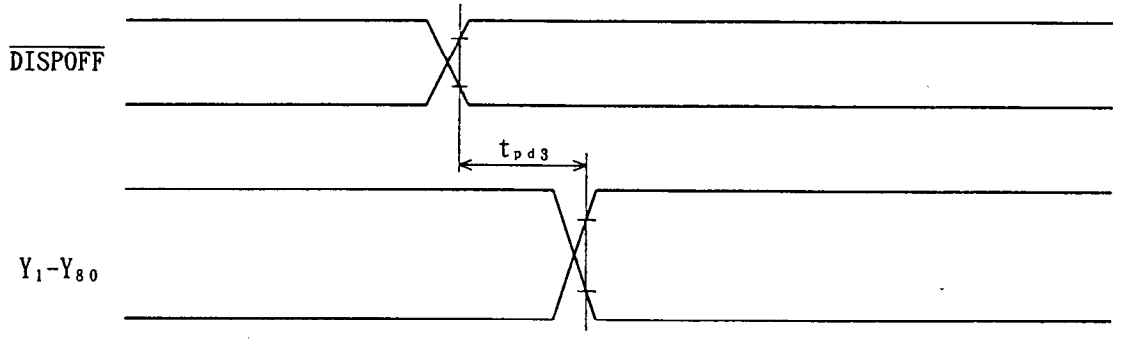


(*) n : 4-bit parallel mode 20
8-bit parallel mode 10

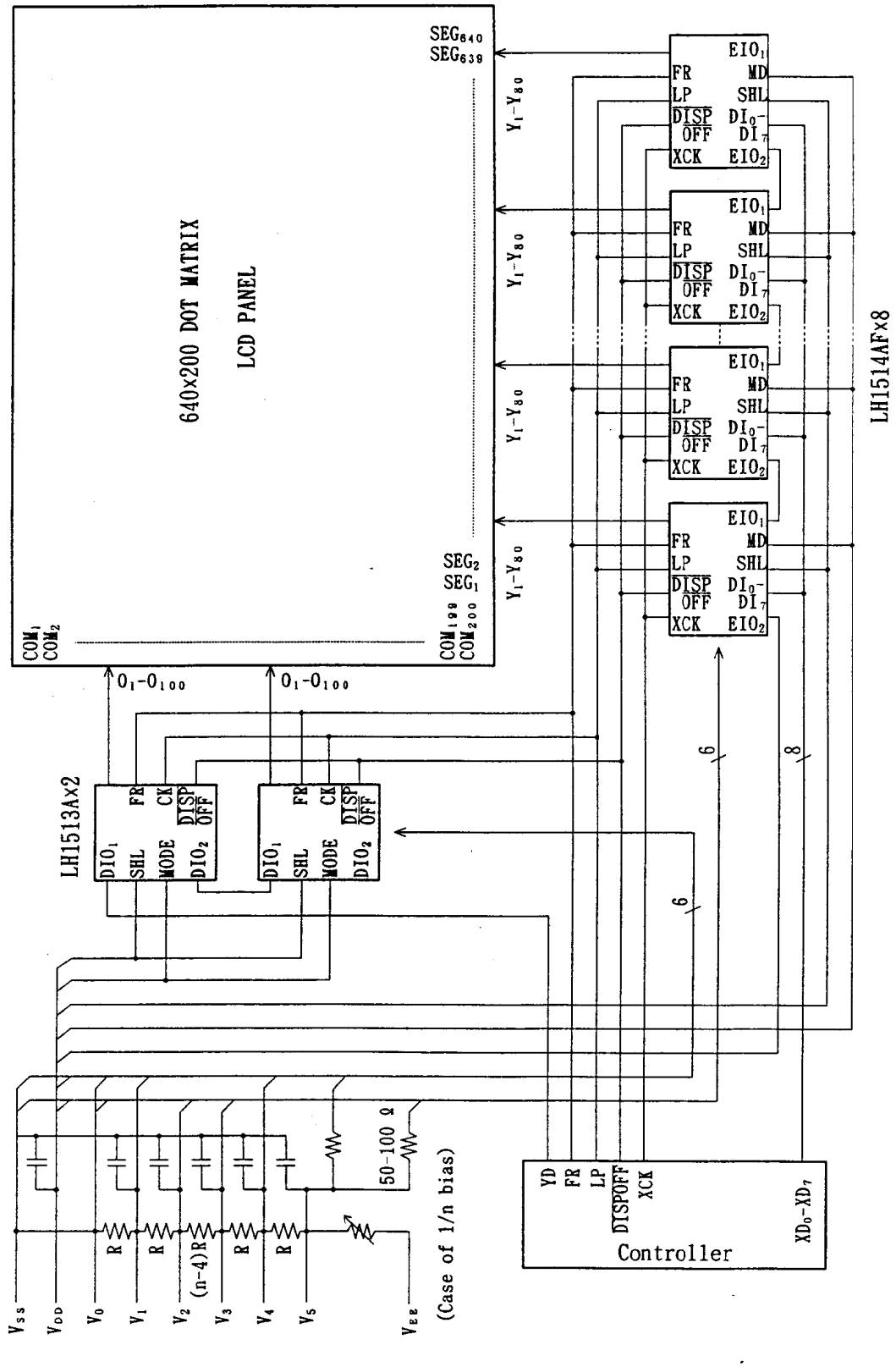
Output Timing Characteristics 1



Output Timing Characteristics 2



12. Example of System Configuration



13. Example of Typical Characteristic

Parameter	Conditions	Mim.	Typ.	Max.	Unit
Typical Fundamental Rating Propagation Delay Time	Ta=+25 ℃, V_{SS}=0 V, V_{DD}=-5.0 V		50		ns

14. PACKAGE AND PACKING SPECIFICATION

1. Package Outline Specification
   Refer to drawing No. SPN2171-00

2. Markings
   The meanings of the device code printed on each tape carrier package are as follows.

   (1) Date code (example) : 4 (a) 37 (b) 0 (c)

   a) denotes the last figure of Anno Domini (of production)
   b) denotes the week (of production)
   c) denotes the number of times of alteration

3. Packing Specifications

   (1) Packing Materials

Item	Material	Purpose
Reel	Anti-static treated plastic (405mm dia.)	Packing of tape carrier package.
Separator	Anti-static treated PET (188 μ mt)	Protects device and prevents ESD (Electro Static Discharge)
Laminated aluminium bag	(520 × 600mm)	Keeping dry.
Adhesive tape paper		Fixing of tape carrier package and sparator.
Carton	Cardboard(420x420x50mm)	Contains a reel.
Label	Paper	Indicates production name, lot.No., and quantity.
Desiccant	Silica gel	Drying of device

   (2) Packing Form

   a) Tape carrier package(TCP)is wound on a reel with separators 1 and 2 and the ends of them are fixed with adhesive tape.
   b) A label indicating production name, lot no. and quantity is stuck on one side of the reel.
   c) The reel and silica gel is put in a laminated aluminium bag. Nitrogen gas is enclosed in the bag and the bag is sealed. The same label(b) is affixed to the bag. The bag is put in a carton and the same label(b) is affixed to one side of the carton.

* Specification of label

TYPE	PRODUCTION NAME LOT NO.
QUANTITY	QUANTITY
LOT(DATE)	SHIPPING DATE

4. Miscellaneous

   (1) The length of the tape carrier is 34 ~ 46 meters maximum per reel, and depends on shipping quantity.

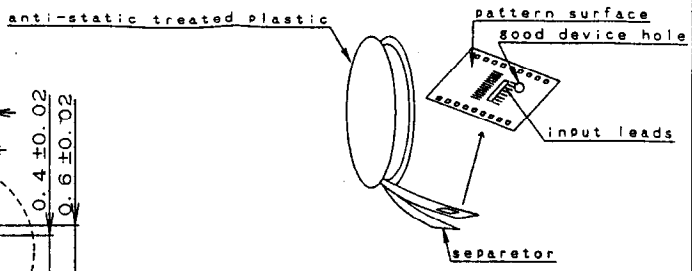
   (2) Before unpacking, prepare a work bench equipped with anti-static devices. Also, the operater shoud ware anti-static wrist bands.

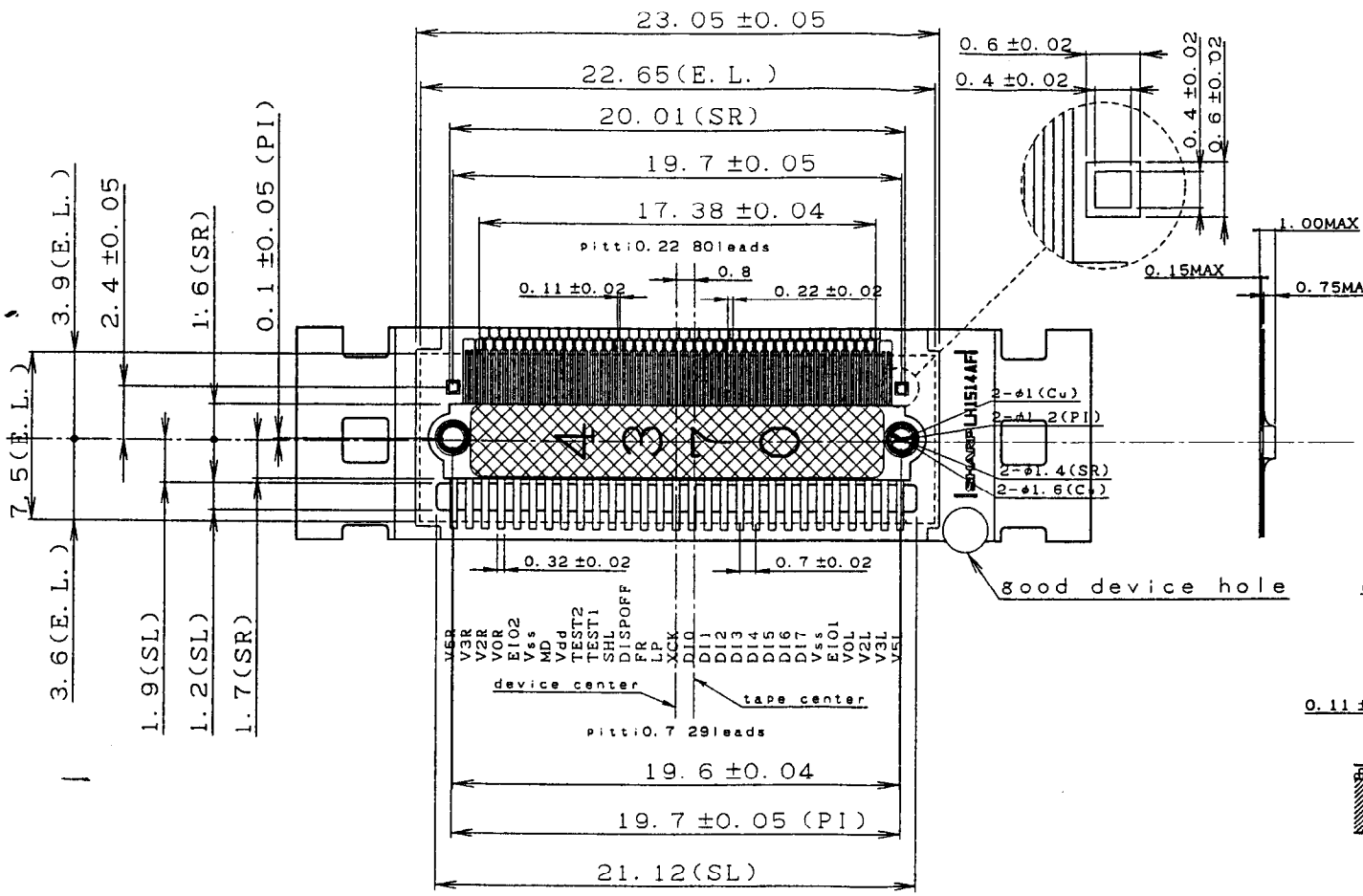
   (3) The device, once unpacked, should be stored in a nitrogen gas, room temperature atomosphere and used within 1 week.

ISSUE DATE	AUG.24.1994	APROVE	CHECK	DESIGN	(NOTE)
ISSUE NUMBER	H6805	A. Suzuki	Y. Honda	T. Kidoguchi	
S/C NUMBER					

SHARP

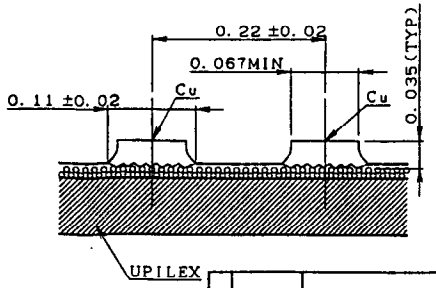
NOTES: 1. REEL WINDING





2. RESIN AREA OF FRONT AND BACK SURFACE IS 18.5X3.5mm(MAX).
3. E.L. MEANS ASSUMED EXCISING LINE.
4. SL MEANS DIMENSION OF PUNCHING HOLE AND ITS TOLERANCE IS ±0.05mm.
5. SR MEANS DIMENSION OF SOLDER RESIST AND ITS TOLERANCE IS ±0.3mm.

CROSS SECTION OF OUTPUT LEADS



APPLICATION		SCALE	UNIT	
	LH1514AF	5/1	mm	
TOLERANCE	TAPE FORMAT	TAPE MATERIALS	FINISH	
±0.1	35mmWIDE TYPE 2 PERFO-PITCH	UPILEX S75 ADHESIVE #5700 ED Cu(SLP) SOLDER RESIST	TIN PLATING	
DATE	AUG. 24. 1994			
DESIGN	T. KIDOGUCHI	ASSEMBLY ENGINEERINP DEPT.		
DRAWING	T. KIDOGUCHI	IC GROUP		
CHECK	A. Suzuki	SHARP CORPORATION		

DATE	REVISE	CHARGE

TITLE	OUT LINE DRAWING OF LH1514AF
CODE	
DRAWING NO.	SPN2171-00