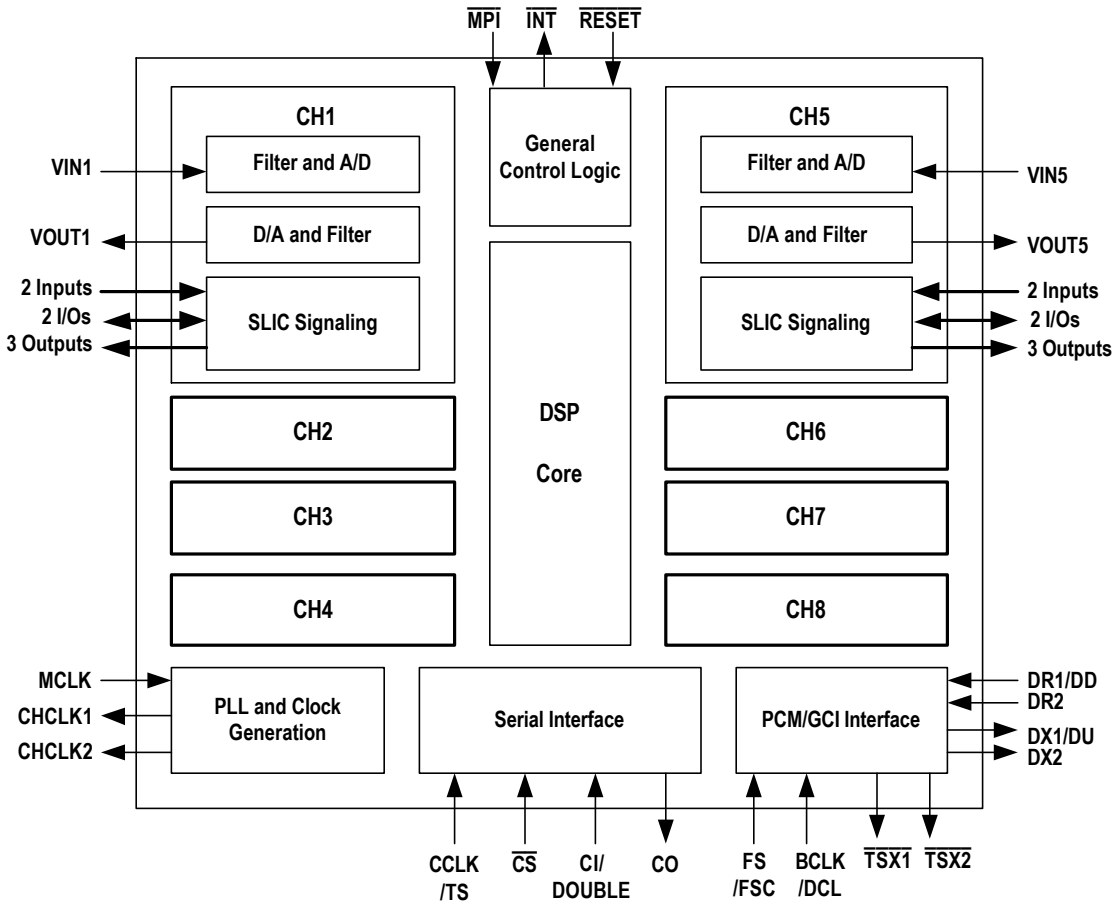
OCTAL PROGRAMMABLE PCM CODEC

IDT821068

FEATURES

- 8 channel CODEC with on-chip digital filters
- Programmable A/m-law compressed or linear code conversion
- Meets ITU-T G.711 - G.714 requirements
- Programmable digital filter adapting to system demands:
  - *AC impedance matching*
  - *Transhybrid balance*
  - *Frequency response correction*
  - *Gain setting*
- Supports two programmable PCM buses and one GCI bus
- Flexible PCM interface with up to 128 programmable time slots, data rate from 512 kbits/s to 8.192 Mbits/s
- Broadcast mode for coefficient setting
- 7 SLIC signaling pins (including 2 debounced pins) per channel
- Fast hardware ring trip mechanism
- Two programmable tone generators per channel for testing, ringing and DTMF generation
- Programmable teletax signal generation (12 kHz or 16 kHz)
- FSK generator
- Two programmable chopper clocks
- Master clock frequency selectable: 1.536 MHz, 1.544 MHz, 2.048 MHz, 3.072 MHz, 3.088 MHz, 4.096 MHz, 6.144 MHz, 6.176 MHz or 8.192 MHz
- Advanced test capabilities
  - *3 analog loopback tests*
  - *5 digital loopback tests*
  - *Level metering function*
- High analog driving capability (300 Ω AC)
- TTL and CMOS compatible digital I/O
- CODEC identification
- +5 V single power supply
- Operating temperature range: - 40°C to + 85°C
- Package available: 128 pin PQFP

FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION

The IDT821068 is a feature rich, single-chip, programmable 8 channel PCM CODEC with on-chip filters. Besides the A-Law/μ-Law companding and linear coding/decoding (16-bit 2's complement), IDT821068 provides 2 programmable Tone generators per channel (which can also generate ring signals), 1 FSK generator, 1 programmable Teletax Signal generator and 2 programmable chopper clocks for SLIC.

The digital filters in IDT821068 provide the necessary transmit and receive filtering for voice telephone circuit to interface with time-division multiplexed systems. An integrated programmable DSP realizes AC Impedance Matching, Transhybrid Balance, Frequency Response Correction and Gain Setting functions. The IDT821068 supports 2 PCM buses with programmable sampling edge, that allows an extra delay of up to 7 clocks. Once the delay is determined, it is effective to all eight channels of IDT821068. The device also provides 7 signaling pins to SLIC on per channel basis.

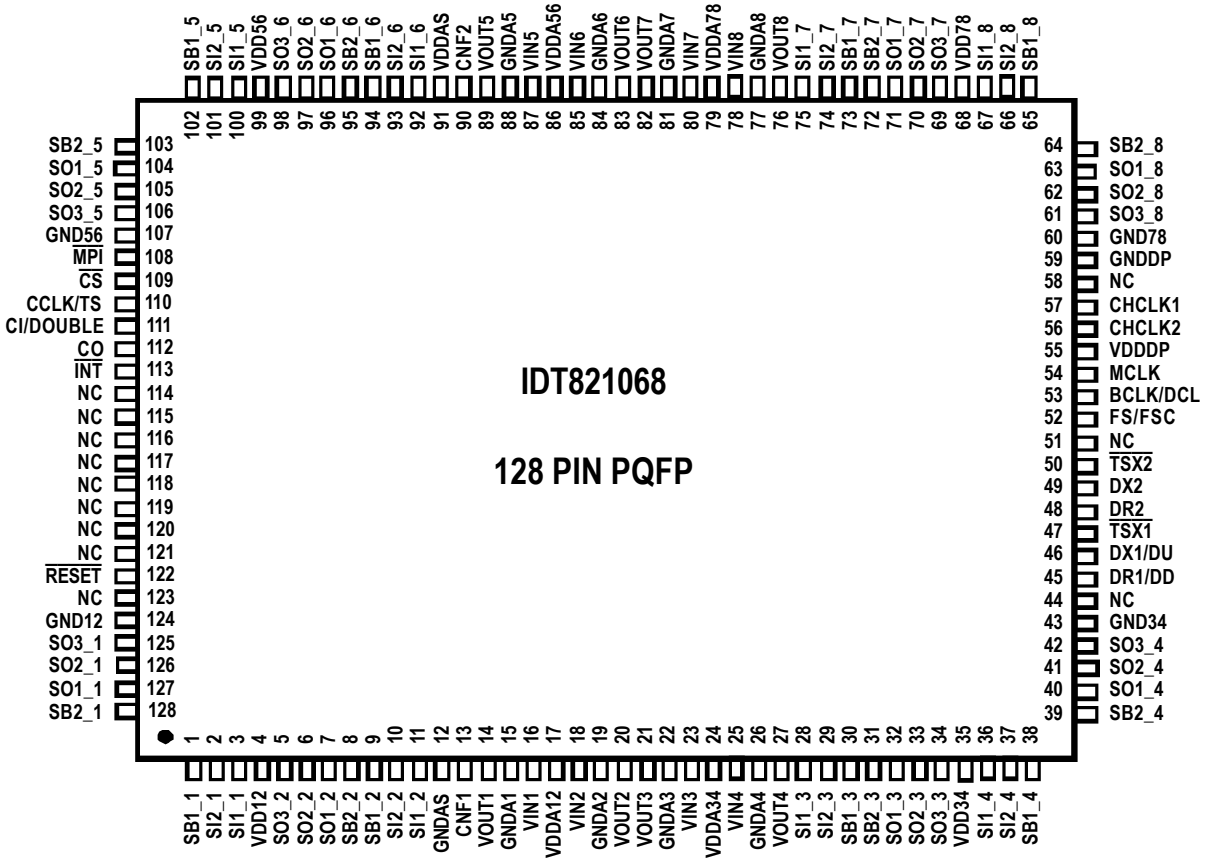
The IDT821068 provides 2 programming interfaces: Microprocessor Interface (MPI) and General Control Interface (GCI), which is also known as ISDN Oriented Module (IOM®-2). For both MPI and GCI programming, the device supports both compressed and linear data format.

The device also offers strong test capability with several analog/digital loopbacks and level metering function. It brings convenience to system maintenance and diagnosis.

A unique feature of 'Hardware Ring Trip' is implemented in IDT821068. When off-hook signal is detected, IDT821068 can reverse an output pin to stop ringing immediately.

The IDT821068 can be used in digital telecommunication applications such as Central Office Switch, PBX, DLC and Integrated Access Device (IAD), i.e. VoIP and VoDSL.

PIN CONFIGURATIONS



IOM®-2 is a registered trademark of Siemens AG.

PIN DESCRIPTION

Name	Type	Pin Number	Description
GNDA1 GNDA2 GNDA3 GNDA4 GNDA5 GNDA6 GNDA7 GNDA8	-	15 19 22 26 88 84 81 77	**Analog Ground.** All ground pins should be connected together.
GNDAS	-	12	**Analog Ground For Bias.** All ground pins should be connected together.
GND12 GND34 GND56 GND78	-	124 43 107 60	**Digital Ground.** All ground pins should be connected together.
GNDDP	-	59	**Digital Ground For PLL.** All ground pins should be connected together.
VDDA12 VDDA34 VDDA56 VDDA78	-	17 24 86 79	**+5V Analog Power Supply.** These pins should be connected to ground via a 0.1μF capacitor. All power supply pins should be connected together.
VDDAS	-	91	**+5V Analog Power Supply For Bias.** This pin should be connected to ground via a 0.1μF capacitor. All power supply pins should be connected together.
VDD12 VDD34 VDD56 VDD78	-	4 35 99 68	**+5V Digital Power Supply.** These pins should be connected to ground via a 0.1μF capacitor. All power supply pins should be connected together.
VDDDP	-	55	**+5V Digital Power Supply For PLL.** This pin should be connected to ground via a 0.1μF capacitance. All power supply pins should be connected together.
VIN1-8	I	16, 18, 23, 25 87, 85, 80, 78	**Analog Voice Inputs.** These pins should be connected with the SLIC via a capacitor (0.22 μF).
VOUT1-8	O	14, 20, 21, 27 89, 83, 82, 76	**Voice Frequency Receiver Outputs.** These pins can drive 300 Ω AC load. It allows the direct driving of transformer.
SI1_(1-8) SI2_(1-8)	I	3, 11, 28, 36 100, 92, 75,67 2, 10, 29, 37 101, 93, 74,66	**Debounced SLIC Signaling Inputs for Channel 1-8.**
SB1_(1-8) SB2_(1-8)	I/O	1, 9, 30, 38 102, 94, 73,65 128, 8, 31,39 103, 95,72, 64	**SLIC Signaling I/Os for Channel 1-8.**
SO1_(1-8) SO2_(1-8) SO3_(1-8)	O	127, 7, 32,40 104, 96,71, 63 126, 6, 33,41 105, 97,70, 62 125, 5, 34,42 106, 98,69, 61	**SLIC Signaling Outputs for Channel 1-8.**
DX1/DU	O	46	**Transmit PCM Data Output (For MPI)/GCI Data Upstream (For GCI).** In MPI mode, this pin remains high-impedance until a pulse appears on FS input. PCM data can output from DX1 or DX2 as selected by serial port, following the BCLK. In GCI mode, GCI data is serially transmitted on this pin for all 8 channels of IDT821068. Which part of the GCI data will be occupied is determined by CCLK/TS pin.
DX2	O	49	**Transmit PCM Data Output (For MPI).** This pin remains high-impedance until a pulse appears on FS input. PCM data can output from DX1 or DX2 as selected by serial port. This pin is not used in GCI mode.
DR1/DD	I	45	**Receive PCM Data Input (For MPI)/GCI Data Downstream (For GCI).** In MPI mode, PCM data is shifted into DR1 or DR2 following the BCLK. PCM data can input from DR1 and DR2 as selected by serial port. In GCI mode, GCI data is received serially on this pin for all 8 channels of IDT821068. Which part of the GCI data will be transmitted is determined by CCLK/TS pin.

PIN DESCRIPTION (CONTINUED)

Name	Type	Pin Number	Description
DR2	I	48	**Receive PCM Data Input (For MPI).** PCM data is shifted into DR1 or DR2 following the BCLK. PCM data can input from DR1 and DR2 as selected by serial port. This pin is not used in GCI mode
FS/FSC	I	52	**Frame Synchronization signal (For MPI)/Frame Sync signal (For GCI).** In MPI mode, FS is an 8 kHz synchronization clock that identifies the beginning of the PCM frame. In GCI mode, FSC is an 8 kHz signal that identifies the beginning of Timeslot 0 in the GCI frame.
BCLK/DCL	I	53	**Bit Clock (For MPI)/Data Clock (For GCI).** In MPI mode, BCLK pin clocks out the PCM data on DX1 or DX2 pin and clock in PCM data from DR1 or DR2 pin. It may vary from 512kHz to 8.192 MHz, and is required to be synchronous with FS. In GCI mode, DCL pin is either 2.048 MHz or 4.096 MHz. The frequency is selected by CI/DOUBLE pin. When CI/DOUBLE pin is low, DCL will be 2.048 MHz; when CI/DOUBLE pin is high, DCL will be 4.096 MHz. It is recommended to connect MCLK and DCL pin together.
$\overline{\text{TSX1}}$ $\overline{\text{TSX2}}$	O	47 50	**Timeslot Indicator Output (For MPI).** This pin pulses low during the receive timeslot. A low on this pin indicates DX1/DX2 output. These two open-drain pins are not used in GCI mode.
$\overline{\text{CS}}$	I	109	**Chip Selection.** In MPI mode, a low level on this pin enables the Serial Control Interface. In GCI mode, a low level on this pin configures a Compressed GCI operation, while a high level on this pin configures a Linear GCI operation.
CI/DOUBLE	I	111	**Serial Control Interface Data Input (For MPI)/Double DCL (For GCI).** In MPI mode, data input on this pin can control both CODEC and SLIC. In GCI mode, this pin is used to determine the frequency of DCL. When low, DCL will be 2.048 MHz; when high, DCL will be 4.096 MHz.
CO	O	112	**Serial Control Interface Data Output (For MPI).** This pin is used to monitor SLIC working status. It is in high impedance state when $\overline{\text{CS}}$ is high. This pin is not used in GCI mode.
CCLK/TS	I	110	**Serial Control Interface Clock (For MPI)/Timeslot Selection (For GCI).** In MPI mode, this is the clock for Serial Control Interface. It can be up to 8.192 MHz. In Compressed GCI mode, this pin indicates which half of 8 continuous GCI timeslots is used. When this pin is low, timeslots 0-3 are selected; when this pin is high, timeslots 4-7 are selected. In Linear GCI mode, this pin indicates which half of 8 continuous GCI timeslots is used for voice signal. When this pin is low, timeslots 0-3 are used as Monitor channel and C/I octet, timeslots 4-7 are used for linear voice; when this pin is high, timeslots 4-7 are used for linear voice, timeslots 0-3 are used as Monitor channel and C/I octet.
$\overline{\text{MPI}}$	I	108	**MPI/GCI Select.** This pin is used to determine which operation mode the IDT821068 works in. When this pin is low, MPI/PCM mode is selected; When this pin is high, GCI mode is selected.
$\overline{\text{RESET}}$	I	122	**Reset Input.** Forces the device to default mode. Active low.
$\overline{\text{INT}}$	O	113	**Interrupt Output Pin.** Active low interrupt signal for ch1-ch8, open-drain. It reflects the changes on SLIC pins.
MCLK	I	54	**Master Clock.** Master clock provides the clock for DSP. In MPI mode, it can be 1.536 MHz, 1.544 MHz, 2.048 MHz, 3.072 MHz, 3.088 MHZ, 4.096 MHz, 6.144 MHz, 6.176 MHz or 8.192 MHz. It can be asynchronous to BCLK. In GCI mode, it is recommended to connect MCLK and DCL pin together. The frequency of MCLK can be 2.048 MHz or 4.096 MHz. See BCLK/DCL pin description.
CHCLK1	O	57	**Chopper Clock Output.** Provides a programmable (2 -28 ms) output signal synchronous to MCLK.
CHCLK2	O	56	**Chopper Clock Output.** Provides a programmable 256 kHz, or 512 kHz or 16.384 MHz output signal synchronous to MCLK.
CNF1 CNF2	-	13 90	**Capacitor Noise Filter.**
NC	-	44, 51, 58, 114 115,116,117,118 119,120,121,123	**No Connection.**

FUNCTIONAL DESCRIPTION

The IDT821068 performs the CODEC/filter functions required for the subscribe line interface circuitry in telecommunications system. IDT821068 converts analog voice signals to digital PCM samples and digital PCM samples back to analog voice signals. High performance oversampling Analog-to-Digital Converters (ADC) and Digital-to-Analog Converters (DAC) in the IDT821068 provide the required conversion accuracy. The associated decimation and interpolation filters are realized with both dedicated hardware and Digital Signal Processor (DSP). The DSP also handles all other necessary functions such as PCM bandpass filtering, sample rate conversion and PCM companding. See the Functional Block Diagram for more detail.

MPI/PCM MODE AND GCI MODE

Microprocessor Interface (MPI) and General Control Interface (GCI) help the user to program and control the CODEC. $\overline{MPI}$ pin selects the interface: '0' selects MPI mode and '1' selects GCI mode.

MPI CONTROL MODE

In MPI mode, the internal configuration registers (local/global), the SLIC signaling interface and the Coefficient-RAM, FSK-RAM of the IDT821068 are programmed by microprocessor via the serial control interface, which consists of four lines (pins): CCLK, $\overline{CS}$, CI and CO. All the commands and data transmitted or received are aligned in byte (8 bits). CCLK is the Serial Control Interface Clock, it can be up to 8.192 MHz; $\overline{CS}$ is the Chip Select pin, a low level on it enables the serial control interface; CI and CO are the serial control interface data input and output, carrying the control commands and data bytes to/from the IDT821068.

The data transfer is synchronized to the CCLK input. The contents of CI is latched on the rising edges of CCLK, while CO changes on the falling edges of CCLK. When finishing a read or write command, the CLCK must last at least one cycle after the $\overline{CS}$ is set high. During the execution of commands that are followed by output data (read commands), the device will not accept any new commands from CI. The data transfer sequence can be interrupted by setting $\overline{CS}$ high. See Figure 1 and Figure 2.

CCLK is the only reference of CI and CO pins. Its duty and frequency may not necessarily be standard.

PCM BUS

In MPI mode, IDT821068 provides two flexible PCM buses for all 8 channels. The digital PCM data can be compressed (A/μ-law) or linear format, which is determined by the DMS bit in Global Command 7. The data rate can be configured as same as Bit Clock (BCLK) or half of it. The data can be transmitted or received either on BCLK rising edges or on falling edges. The data transmit and receive time slots can be offset from Frame Synchronization (FS) by 0 BCLK period to 7 BCLK periods. See Figure 3. All the selections are implemented by Global Command 7, which is configured for all 8 channels.

The PCM data of each channel can be assigned to any time slot of the PCM bus. The number of available time slots is determined by BCLK frequency. For example, when BCLK is 512 kHz, time slot 0-7 are available; when BCLK is 1.024 MHz, time slot 0-15 are available; when BCLK is 8.192 MHz, time slot 0-127 are available. The IDT821068 allows any BCLK frequency between 512 kHz and 8.192 MHz at increment of 64 kHz in a system.

When compressed format (8-bit) is selected, the voice data of one channel occupies one time slot. The TT[6:0] bits in Local Command 7 selects the transmit time slot for each channel, while the RT[6:0] bits in Local Command 8 selects the receive time slot for each channel.

When linear format is selected, the voice data is a 16-bit 2's complement number (b15 and b14 are the same as b13, which is the sign bit, b13 to b0 are effective bits). Then the voice data of one channel occupies a time slot group, which is consisted of 2 successive time slots. The TT[6:0] bits in Local Command 7 select the transmit time slot group for each channel, while the RT[6:0] bits in Local Command 8 select the receive time slot group for each channel.

PCM data for each individual channel can be clocked out of DX1 or DX2 pin on the programmed edges of BCLK according to time slot assignment. The transmit highway (DX1/2) is selected by the THS bit in Local Command 7. The frame sync (FS) pulse identifies the beginning of a transmit frame, or time slot 0. The PCM data is transmitted serially on DX1 or DX2 with MSB first.

PCM data for each channel can be clocked into DR1 or DR2 pin on the programmed edges of BCLK according to time slot assignment. The receive highway (DR1/2) is selected by the RHS bit in Local Command 8. The frame sync (FS) pulse identifies the beginning of a receive frame, or time slot 0. The PCM data is received serially from DR1 or DR2 with MSB first.

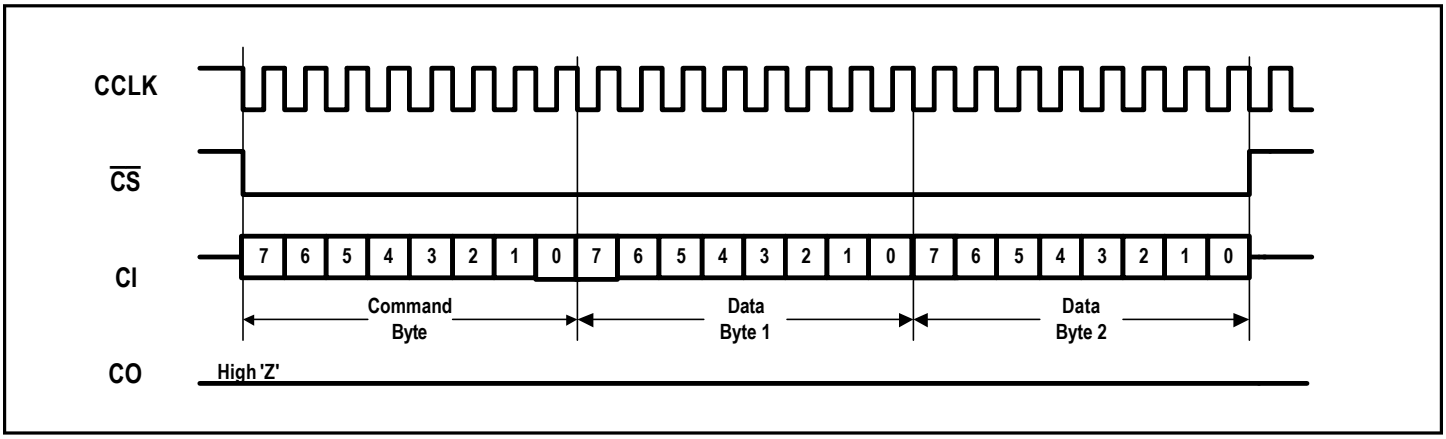


Figure 1. An Example of Serial Interface Write Mode

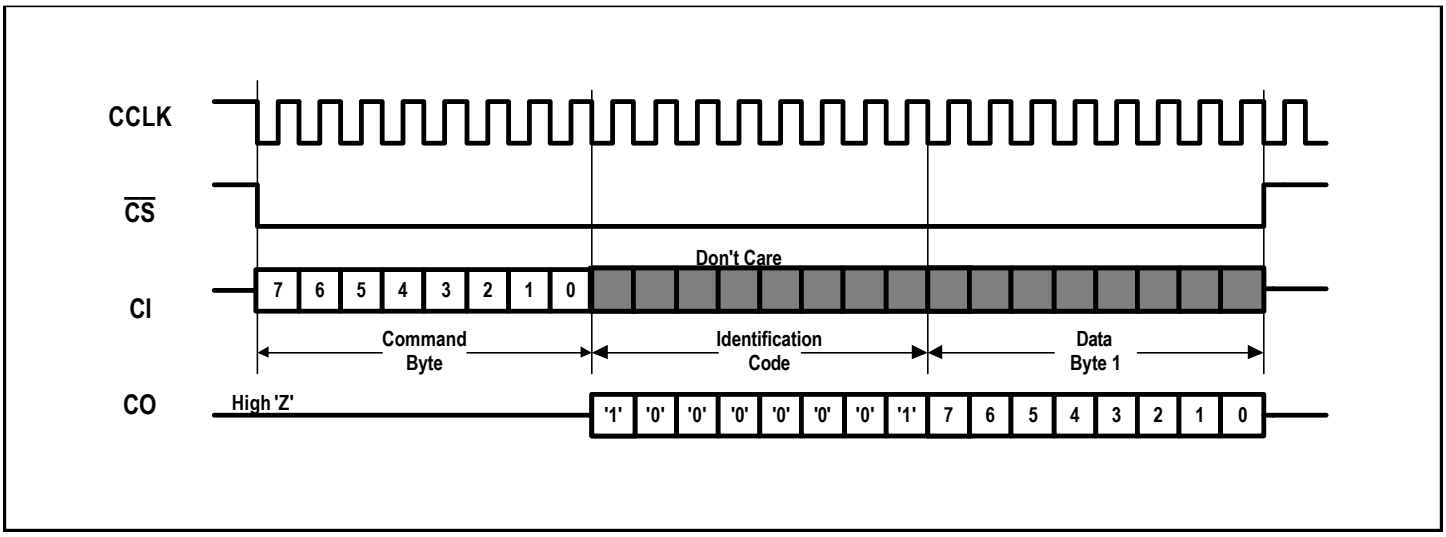


Figure 2. An Example of Serial Interface Read Mode (ID = 81h)

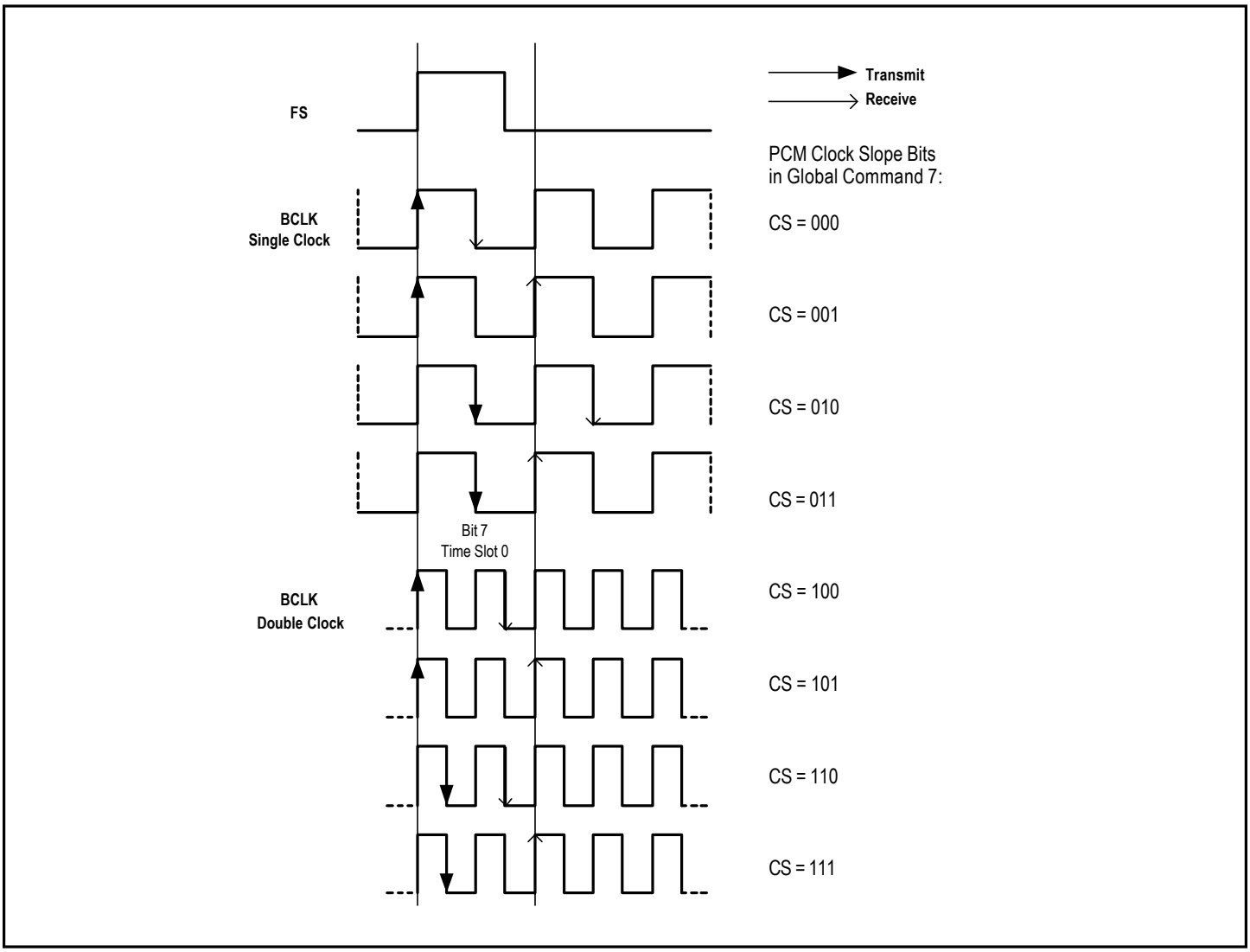


Figure 3. Sampling Edge Select Waveform

GCI MODE

In GCI mode, the GCI interface provides communication of both control and voice data between the GCI bus and SLIC over a pair of pins (DD and DU). The IDT821068 follows the GCI standard where voice and control data for eight channels are combined into one serial bit stream: Data Upstream is sent out of the DU pin and Data Downstream is received on the DD pin. The data transmission is controlled by the Data Clock (DCL) and Frame Synchronization (FSC) signals. The Frame Sync (FSC) pulse identifies the beginning of the Transmit and Receive frames and all GCI time slots refer to it. The DCL signal can be 2.048MHz or 4.096 MHz, decided by DOUBLE pin. The IDT821068 adjusts internal timing to accommodate signal (2.048 MHz) or double (4.096 MHz) clock rate. A complete GCI frame is sent upstream on DU pin and received downstream on DD pin every 125 μs.

In GCI mode, IDT821068 supports compressed and linear voice data format. To make the selection, users should set the $\overline{MPI}$ and $\overline{CS}$ pin to correct level as shown in the following table, and at the same time, set the DMS bit in Global Command accordingly.

$\overline{MPI}$	$\overline{CS}$	Voice Data Format
1	0	Compressed GCI
1	1	Linear GCI

Compressed GCI Structure

In GCI compressed mode, the Data Upstream Interface logic controls the transmission of data onto the GCI bus. One GCI frame consists of 8 GCI time slots, and one GCI time slot consists of four 8-bit bytes as described below:

- Two voice data bytes from the A-law or μ-law compressor for two different channels. For easy description, we name the two channels as channel A and channel B. The compressed voice data bytes for channel A and B are 8-bit wide;
- One monitor channel byte, which is used for reading control data from the device for channel A and B;
- One C/I channel byte, which contains a 6 bit width C/I channel sub-byte together with an MX bit and an MR bit. All real time signaling information is carried on the C/I channel sub-byte. The MX (Monitor Transmit) bit and MR (Monitor Receive) bits are used for handshaking functions for channel A and B. Both MX and MR are active low.

The data structure of the Data Downstream is as same as that of Upstream. The Data Downstream Interface logic controls the reception of data bytes from the GCI bus. The two compressed voice channel data bytes of the GCI time slot are transferred to the A-law or μ-law expansion logic circuit. The expanded data is passed to the receive path of the signal processor. The monitor channel and C/I channel bytes are transferred to the GCI control logic for processing.

Figure 4 shows the overall compressed GCI frame structure.

In compressed operation, four time slots are required to access the eight channels of IDT821068. The GCI time slot assignment is determined by the TS pin as shown in Table 1.

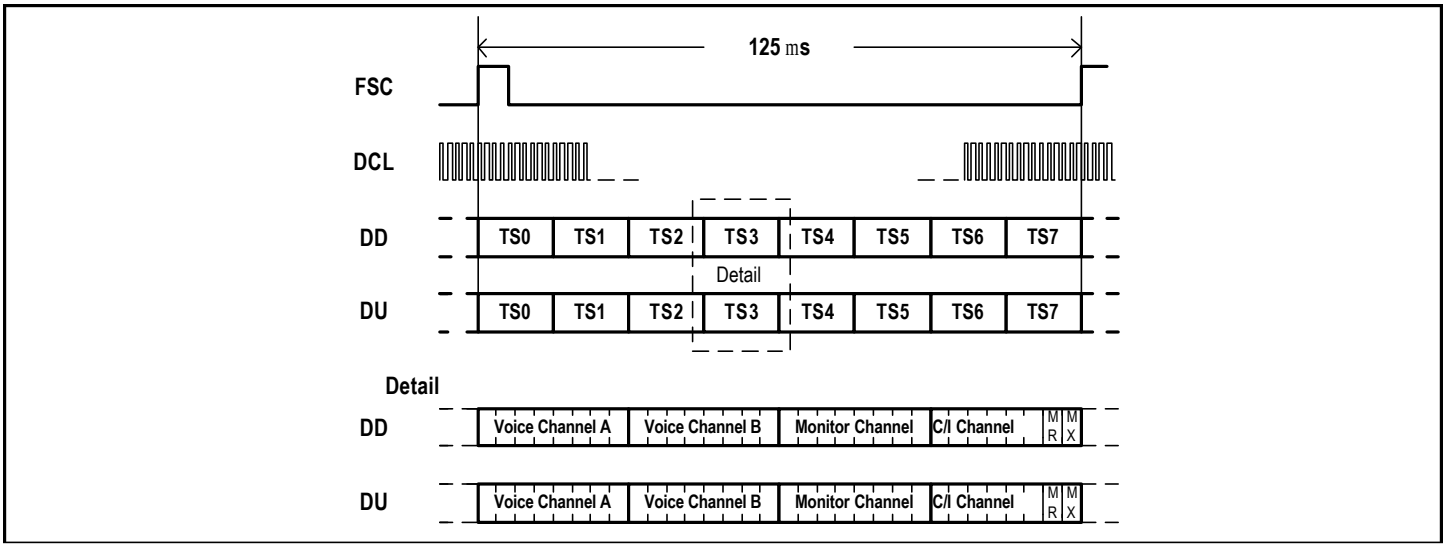


Figure 4. Compressed GCI Frame Structure

Table 1 - Time Slot Selection for compressed GCI

IDT821068 Channels	TS = 0		TS = 1	
	Timeslot	Voice Channel	Timeslot	Voice Channel
1	Timeslot0	A	Timeslot4	A
2	Timeslot0	B	Timeslot4	B
3	Timeslot1	A	Timeslot5	A
4	Timeslot1	B	Timeslot5	B
5	Timeslot2	A	Timeslot6	A
6	Timeslot2	B	Timeslot6	B
7	Timeslot3	A	Timeslot7	A
8	Timeslot3	B	Timeslot7	B

Linear GCI Structure

In GCI linear mode, one GCI frame consists of 8 GCI time slots, each GCI time slot consists of four 8-bit bytes. Four of the 8 time slots are used as Monitor Channel and C/I octet, they have a common data structure:

- Two Don't Care bytes.
- One monitor channel byte, which is used for reading/writing control data/coefficients from/to the device for channel A and B.
- One C/I byte, which contains a 6 bit width C/I channel sub-byte together with an MX bit and an MR bit. All real time signaling information is carried on the C/I channel sub-byte. The MX (Monitor Transmit) bit and MR (Monitor Receive) bits are used for handshaking functions for channel A and B. Both MX and MR bits are active low.

Other four GCI time slots are used for linear voice data (16-bit 2's complement). Each time slot consists of two 16-bit linear voice data bytes: one byte contains the linear voice data for channel A, the other byte contains the linear voice data for channel B.

The GCI time slot assignment is determined by the TS pin. When TS is low, the linear GCI Frame Structure is shown in Figure 5.

In linear operation, total eight GCI time slots are required to access the eight channels of IDT821068. See Table 2 for detailed information about time slot assignment for linear mode.

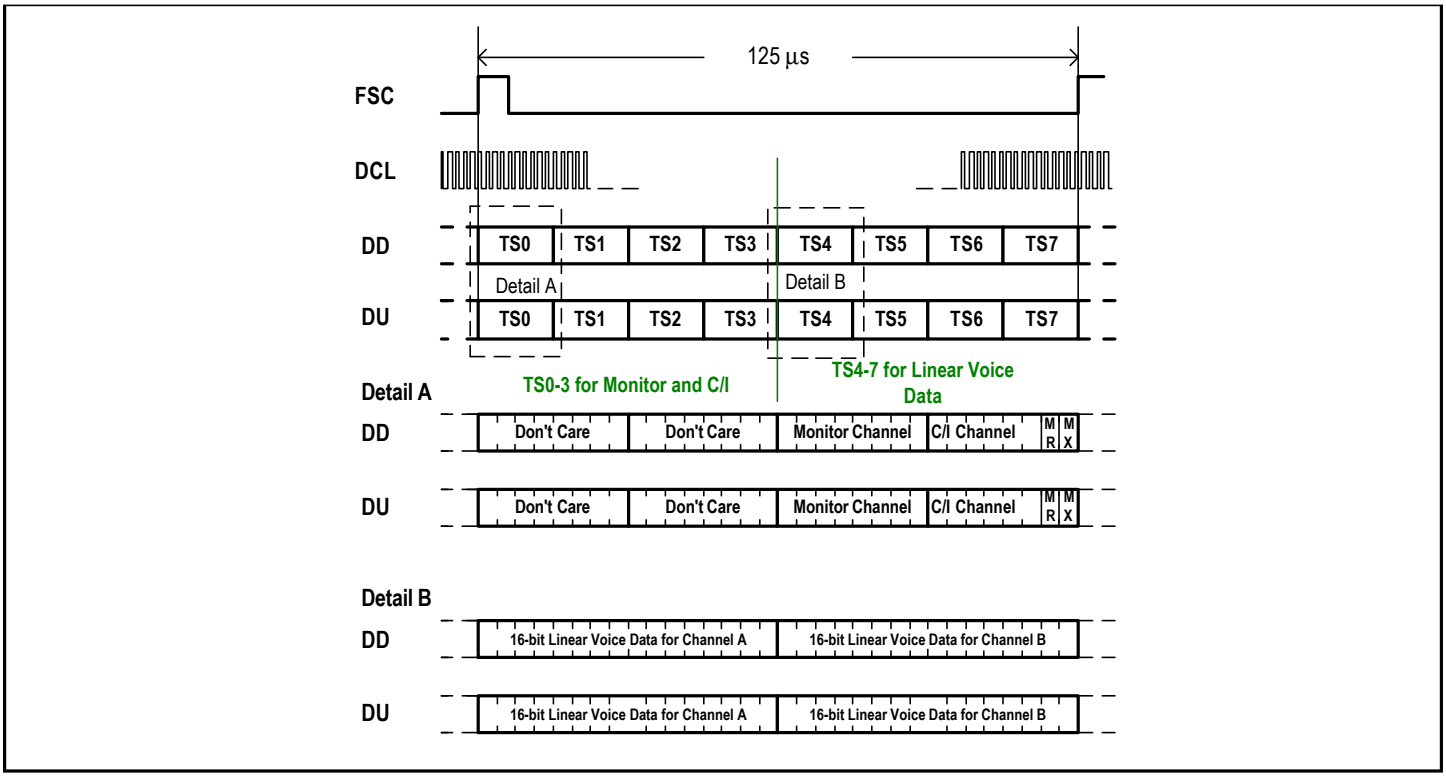


Figure 5. Linear GCI Frame Structure When TS Is Low

Table 2 - Time Slot Selection for linear GCI

IDT821068 Channels	TS = 0			
	Timeslot	Monitor and C/I	Timeslot	Voice Channel
1	Timeslot0	A	Timeslot4	A
2	Timeslot0	B	Timeslot4	B
3	Timeslot1	A	Timeslot5	A
4	Timeslot1	B	Timeslot5	B
5	Timeslot2	A	Timeslot6	A
6	Timeslot2	B	Timeslot6	B
7	Timeslot3	A	Timeslot7	A
8	Timeslot3	B	Timeslot7	B
	TS = 1			
1	Timeslot4	A	Timeslot0	A
2	Timeslot4	B	Timeslot0	B
3	Timeslot5	A	Timeslot1	A
4	Timeslot5	B	Timeslot1	B
5	Timeslot6	A	Timeslot2	A
6	Timeslot6	B	Timeslot2	B
7	Timeslot7	A	Timeslot3	A
8	Timeslot7	B	Timeslot3	B

C/I CHANNEL

In both compressed GCI and linear GCI mode, the upstream and downstream C/I channel bytes are continuously carrying I/O information every frame to and from the IDT821068. In this way, the upstream processor can have an immediate access to SLIC output data present on IDT821068's programmable I/O port on SLIC side through downstream C/I channel, as well as to SLIC input data through upstream C/I channel. The IDT821068 transmits or receives the C/I channel data with the Most Significant Bit first.

The MR and MX bits are used for handshaking during data exchanges on the monitor channel.

Upstream C/I Channel

The C/I channel which includes six C/I channel bits, is transmitted upstream by the IDT821068 every frame. The bit definitions for the upstream C/I channel are shown below.

Upstream C/I Octet

MSB LSB

b7	b6	b5	b4	b3	b2	b1	b0
SI1(A)	SI2(A)	SB1(A)	SI1(B)	SI2(B)	SB1(B)	MR	MX

The logic state of input ports SI1 and SI2 for channel A and channel B, as well as the bidirectional port SB1 for channel A and B if SB1 is programmed as an input, are read and transmitted in the upstream C/I channel. When SB2 is programmed as input, its data are not available in upstream C/I channel and can be read by Global Command 12 only.

Downstream C/I Channel

The downstream C/I octet is defined as:

Downstream C/I Octet

MSB LSB

b7	b6	b5	b4	b3	b2	b1	b0
$\overline{A}$/B	SO3	SO2	SO1	SB1	SB2	MR	MX

Herein, $\overline{A}$/B selects channel A or Channel B:

$\overline{A}$/B = 0: channel A is selected; $\overline{A}$/B = 1: channel B is selected.

The downstream C/I channel carries the SLIC output data bits of SO1, SO2 and SO2 for channel A or B, as well as SB1 and SB2 output bits when SB1 and SB2 are programmed as outputs.

MONITOR CHANNEL

The monitor channel is used to transfer of maintenance information between the upstream and downstream devices. The information includes reading/writing the global/local registers and coefficient/FSK RAM of the IDT821068 or providing SLIC signaling and so on. Using two monitor control bits (MR and MX) per direction, data is transferred in a complete handshake procedure. The MR and MX bits in the C/I Channel of the GCI frame are used for the handshake procedure of the monitor channel. See Figure 6.

The monitor channel transmission operates on a pseudo-asynchronous basis:

- Data transfer (bits) on the bus is synchronized to FSC;
- Data flow (bytes) are asynchronously controlled by the handshake procedure.

For example: Data is placed onto the DD Monitor Channel by the Monitor Transmitter of the master device (DD MX bit is activated and set to '0'). This data transfer will be repeated within each frame (125 μs rate) until it is acknowledged by the IDT821068 Monitor Receiver by setting the DU MR bit to '0', which is checked by the Monitor Transmitter of the master device. Thus, the data rate is not 8 kbytes/s.

Monitor Handshake

The monitor channel works in 3 states:

I. Idle state: A pair of inactive (set to '1') MR and MX bits during two or more consecutive frames shows an idle state on the monitor channel and the End of Message (EOM);

II. Sending state: MX bit is activated (set to '0') by the Monitor Transmitter, together with data-bytes (can be changed) on the monitor channel;

III. Acknowledging: MR bit is set to active (i.e. '0') by the Monitor Receiver, together with a data byte remaining in the monitor channel.

A start of transmission is initiated by a monitor transmitter by sending out an active MX bit together with the first byte of data to be transmitted in the monitor channel. This state remains until the addressed monitor receiver acknowledges the receipt by sending out an active low MR bit. The data transmission is repeated each 125 μs frame (minimum is one repetition). During this time the Monitor Transmitter keeps evaluating the MR bit.

Flow control, means in the form of transmission delay, can only take place when the transmitters MX and the receivers MR bit are in active state.

Since the receiver is able to receive the monitor data at least twice (in two consecutive frames), it is able to check for data errors. If two different bytes are received the receiver will wait for the receipt of two identical successive bytes (last look function).

A collision resolution mechanism (check if another device is trying to send data during the same time) is implemented in the transmitter. This is done by looking for the inactive ('1') phase of the MX bit and making a per bit collision check on the transmitted monitor data (check if transmitted '1's are on DU/DD line; DU/DD line are open drain lines).

Any abort leads to a reset of the IDT821068 command stack, the device is ready to receive new commands.

To obtain a maximum speed data transfer, the transmitter anticipates the falling edge of the receivers acknowledgment.

Due to the inherent programming structure, duplex operation is not possible. It is not allowed to send any data to the IDT821068, while transmission is active.

Refer to Figure 7 and 8 for more information about monitor handshake procedure.

The IDT821068 can be controlled very flexibly by commands operating on registers or RAMs via the GCI monitor channel, refer to "Programming Description" for further details.

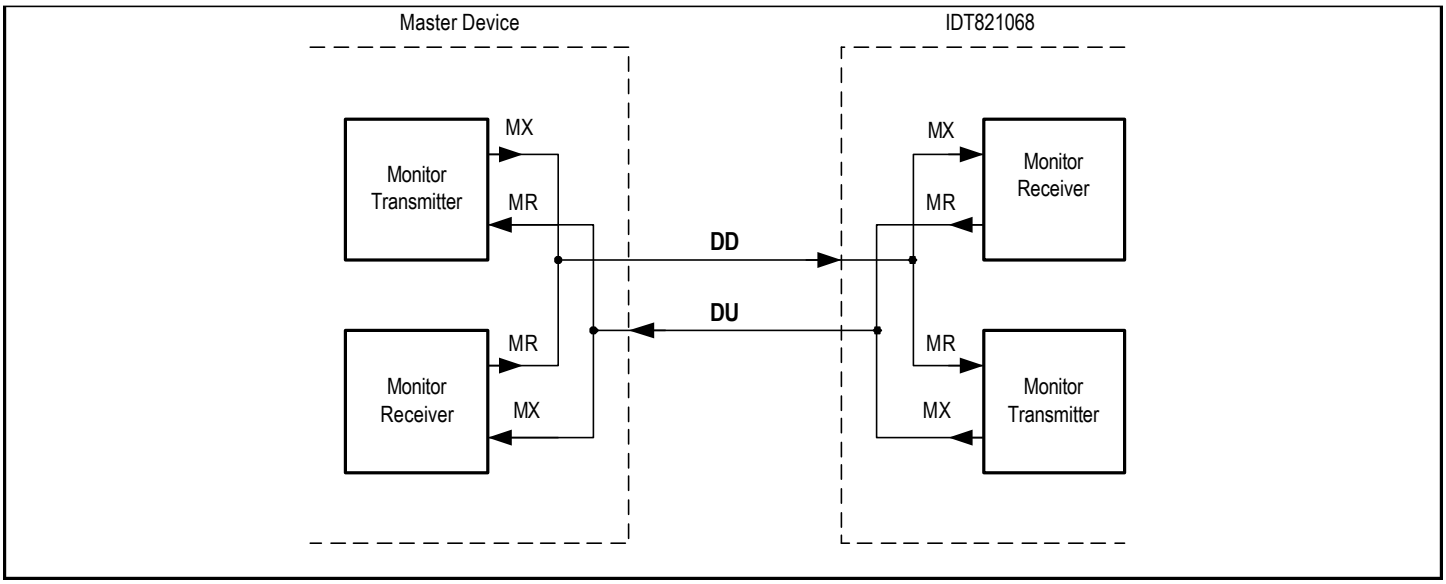


Figure 6. Monitor Channel Operation

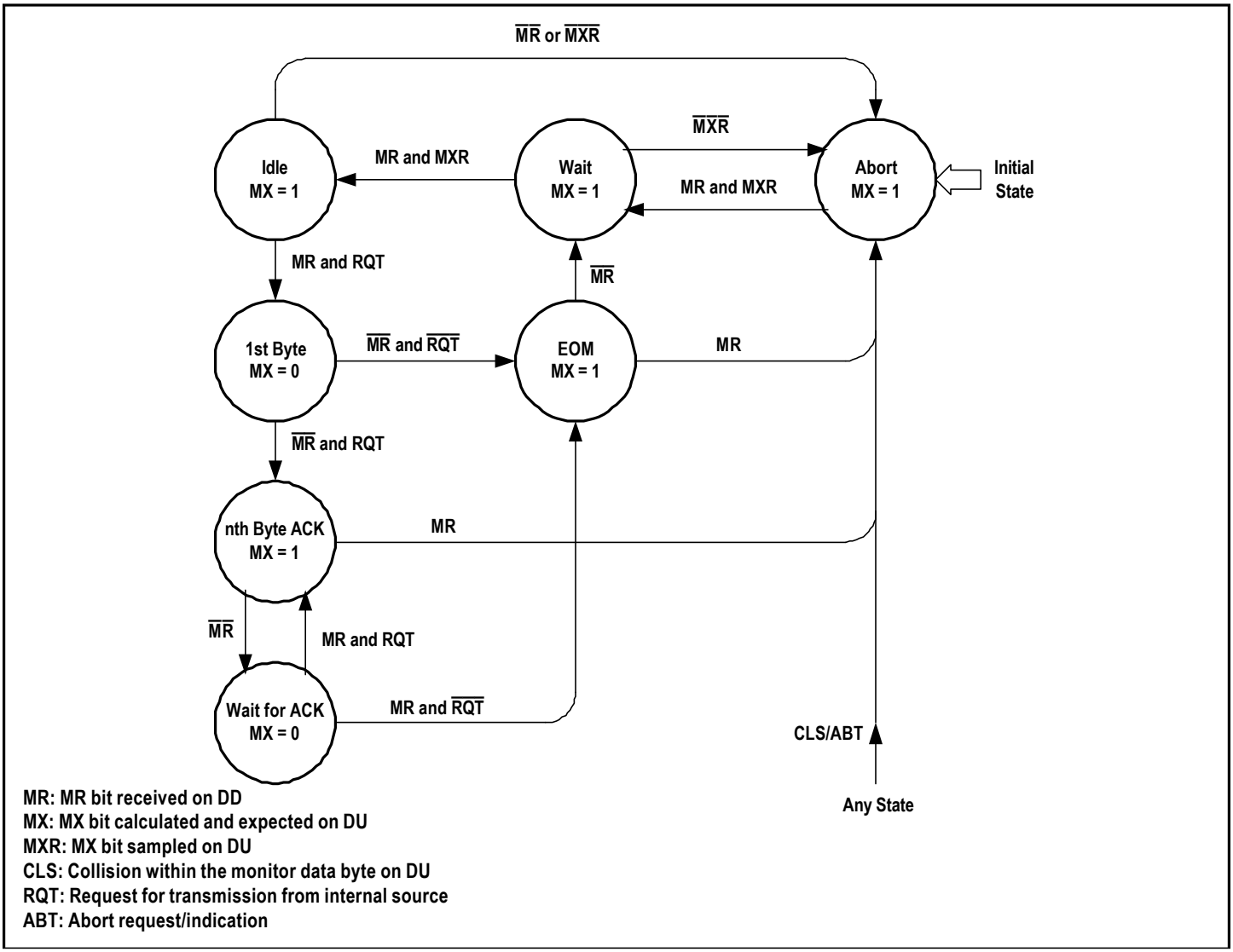
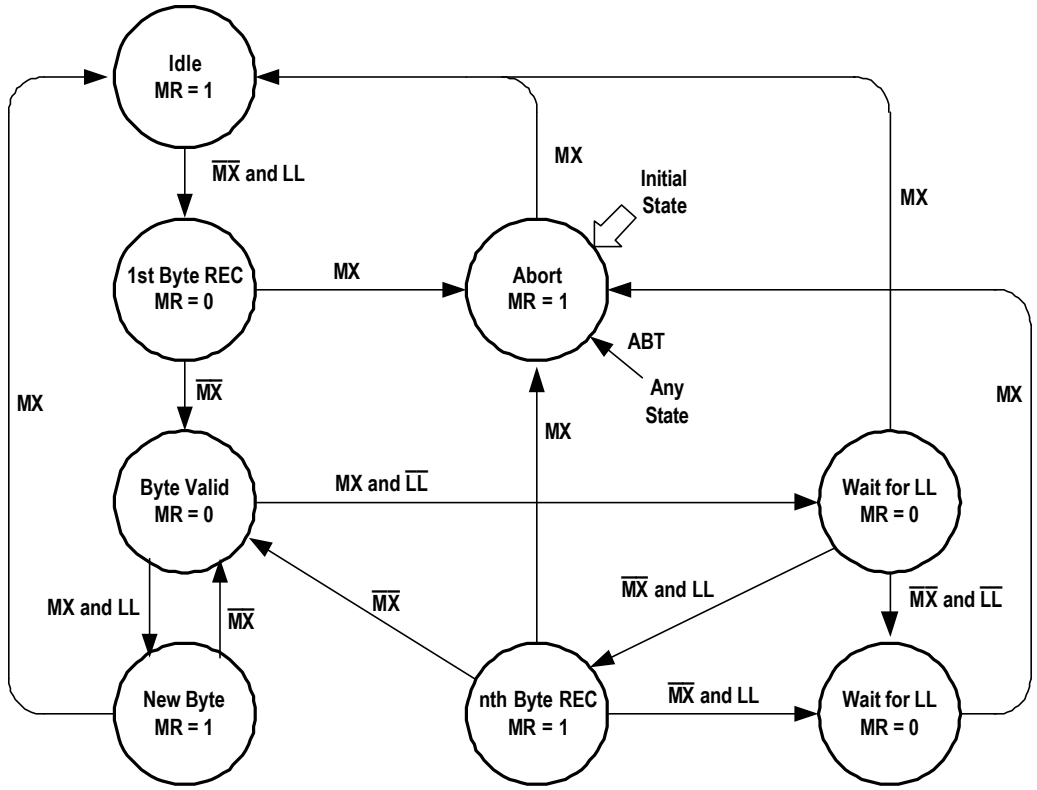


Figure 7. State Diagram of Monitor Transmitter



MR: MR bit calculated and transmitted on DU
MX: MX bit received data downstream (DD)
LL: Last look of monitor byte received on DD
ABT: Abort indication to internal source

Figure 8. State Diagram of Monitor Receiver

DSP PROGRAMMING

SIGNAL PROCESSING

Several blocks are programmable for signal processing. This allows users to optimize the performance of the IDT821068 for the system. Figure 9 shows the Signal Flow for each channel and indicate the programmable blocks.

The programmable digital filters can be adjusted for desired gain, impedance, transhybrid balance and frequency response. The coefficients of all digital filters can be calculated by a software (Cal48) provided by IDT. Users should provide accurate SLIC model, impedance and gain requirements, then the software (Cal48) will calculate all the coefficients. When these coefficients are written to the coefficient RAM of the IDT821068, the final AC characteristics of the line card (consists of SLIC and CODEC) will meet the ITU-T specifications.

GAIN ADJUSTMENT

The analog gain and digital gain of each channel can be adjusted separately in IDT821068.

For each individual channel, in transmit path, analog A/D gain can be selected as 0 dB or 6 dB. The selection is done by A/D Gain (GAD) bit in Local Command 10. The default analog gain for transmit path is 0 dB.

For each individual channel, in receive path, analog D/A gain can be selected as 0 dB or -6 dB. The selection is done by D/A Gain (GDA) bit in Local Command 10. The default analog gain for receive path is 0 dB.

Digital gain of transmit path (GTX) can be programmed from -3 dB to +12 dB with minimum 0.1 dB step. If CS[5] bit is '0' in Local Command 1, the digital gain in transmit path is set to be the default value. If CS[5] bit is '1' in Local Command 1, the digital gain in transmit path will be decided by the coefficient in GTX RAM.

Digital gain of receive path (GRX) can be programmed from -12 dB to +3 dB with minimum 0.1 dB step. If CS[7] bit is '0' in Local Command 1, the digital gain in receive path is set to be the default value. If CS[7] bit is '1' in Local Command 1, the digital gain in receive path will be decided by the coefficient in GRX RAM.

IMPEDANCE MATCHING

There is a programmable feedback path on each channel from VIN to VOUT in the IDT821068. It synthesizes the two-wire impedance of the SLIC. The Impedance Matching Filter (IMF) and the Gain of Impedance Scaling (GIS) are adjustable, they work together to realize impedance matching. If the CS[0] bit in Local Command 1 is '0', the IMF coefficient is set to be default value; if CS[0] is '1', the IMF coefficient is set by the IMF RAM. If the CS[2] bit in Local Command 1 is '0', the GIS coefficient is set to be default value; if CS[2] is '1', the GIS coefficient is set by the GIS RAM.

TRANSHYBRID BALANCE

Transhybrid balancing filter is used to adjust transhybrid balance to ensure the echo cancellation meets the ITU-T specifications. The coefficient for Echo Cancellation (ECF) can be programmed. If the CS[1] bit in Local Command 1 is '0', the coefficient of ECF is set to be default value; if CS[1] is '1', the coefficient of ECF is decided by the ECF RAM.

FREQUENCY RESPONSE CORRECTION

The IDT821068 provides two filters that can be programmed to correct any frequency distortion caused by the impedance matching filter, they are: Frequency Response Correction for Transmit path (FRX) filter and Frequency Response Correction for Receive path (FRR) filter. The coefficients of FRX filter and FRR filter can be programmed. If the CS[4] bit in Local Command 1 is '0', the FRX coefficient is set to be default value, while if CS[4] is '1', the FRX coefficient is decided by the FRX RAM. If the CS[6] bit in Local Command 1 is '0', the FRR coefficient is set to be default value, while if CS[6] is '1', the FRR coefficient is decided by the FRR RAM.

The address of the Coe-RAM including GTX, GRX, FRX, FRR, GIS, ECF and IMF RAM are listed in APPENDIX.

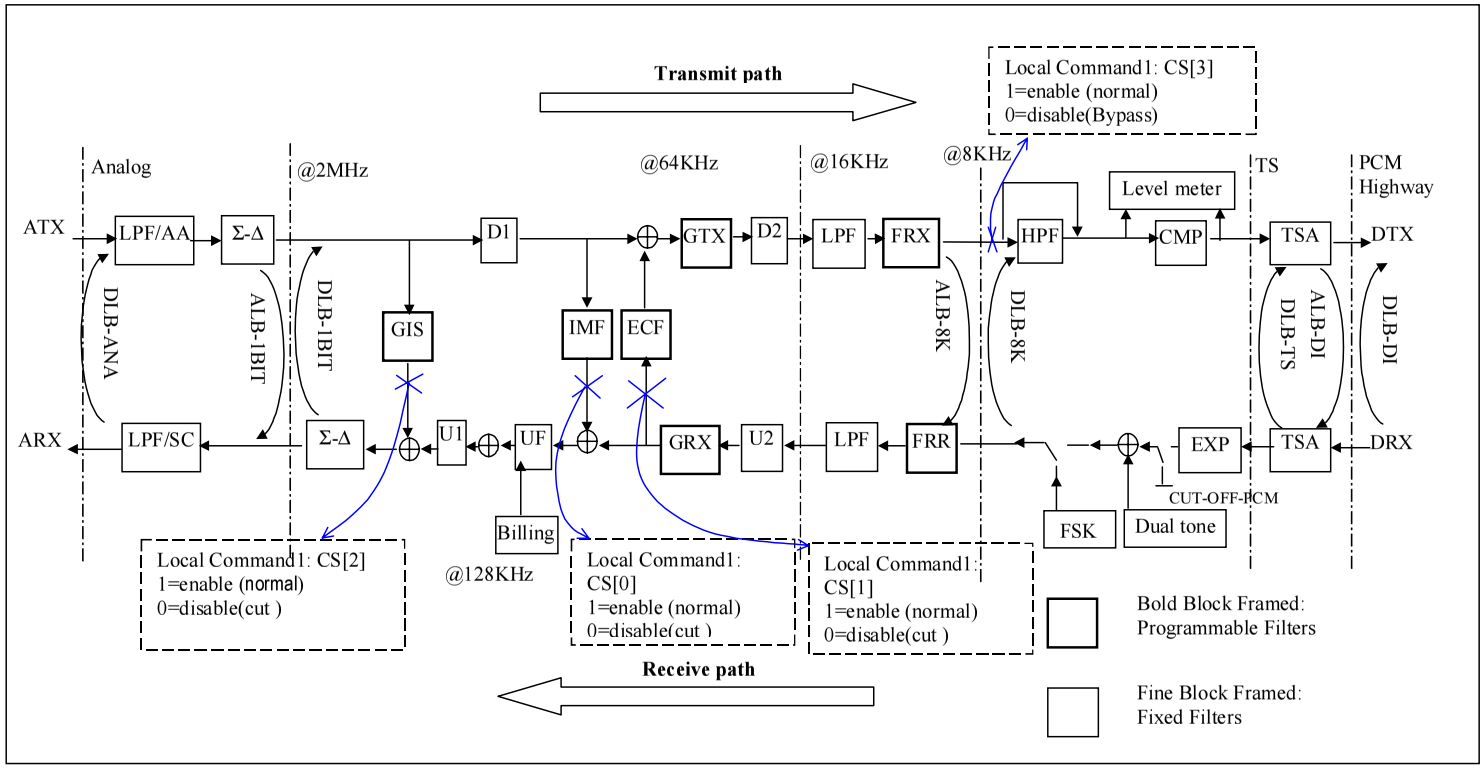


Figure 9. Signal Flow for Each Channel

Abbreviation List

LPF/AA: Anti-Alias Low-pass Filter
LPF/SC: Smoothing Low-pass Filter
LPF: Low-pass Filter
HPF: High-pass Filter
GIS: Gain for Impedance Scaling
D1: 1st Down Sample Stage
D2: 2nd Down Sample Stage
U1: 1st Up Sample Stage
U2: 2nd Up Sample Stage
UF: Up Sampling Filter (64k-128k)

IMF: Impedance Matching Filter
ECF: Echo Cancellation Filter
GTX: Gain for Transmit Path
GRX: Gain for Receive Path
FRX: Frequency Response Correction for Transmit
FRR: Frequency Response Correction for Receive
CMP: Compression
EXP: Expansion
TSA: Time slot Assignment

SLIC CONTROL

The SLIC interface of IDT821068 for each channel consists of 7 pins: 2 inputs SI1 and SI2, 2 I/O pins SB1 and SB2, together with 3 outputs SO1, SO2 and SO3.

SI1 AND SI2

In both MPI and GCI mode, SLIC inputs SI1 and SI2 can be read via Global Command 9 or 10 for all 8 channels. The eight SIA bits of Global Command 9 represent the eight debounced SI1 signals on corresponding channels, while the eight SIB bits of Global Command 10 represent the eight debounced SI2 signals on corresponding channels. In this way, information on SI1 or SI2 for eight channels can be obtained from IDT821068 with a read operation. Both SI1 and SI2 can be assigned to off-hook, ring trip, ground key signals or other signals. The 2 Global Commands allow the microprocessor a more efficient way of obtaining time-critical data such as on/off-hook and ring trip information.

In MPI operation, SI1 and SI2 data for each channel can also be read by Local Command 9.

In GCI operation, SI1 and SI2 data for each channel can be obtained in the field of upstream C/I octet. Refer to GCI Interface Description.

SB1 AND SB2

In both MPI and GCI mode, SLIC I/O pin SB1 for each channel can be configured as input or output separately (the default direction is input), by Global Command 13. Each bit in this command corresponds to one channel's SB1 direction. When a bit in this command is set to 0, the SB1 pin of its corresponding channel is configured as an input; when the bit is set to 1, the SB1 pin of its corresponding channel is configured as an output.

Global Command 14 determines the I/O direction of the SB2 pins for each channel in the same way.

In MPI mode, if SB1 and SB2 are selected as inputs, they can be read by Global Command 11 or 12, which provides SB1 or SB2 information for all 8 channels; or by Local Command 9, which provides SB1 and SB2 information for each individual channel.

In MPI mode, if SB1 and SB2 are selected as outputs, data can be written to them by Global Command 11 or 12 only.

In GCI mode, if SB1 and SB2 are selected as inputs, the information of them can be read by Global Command 11 or 12. For SB1, the information can also be read in the field of upstream C/I channel octet.

In GCI mode, if SB1 and SB2 are selected as outputs, data can only be written to them through downstream C/I channel octet. Refer to GCI Interface Description for detail.

SO1, SO2 AND SO3

SLIC output signals to SO1, SO2 and SO3 pins can only be written for each individual channel.

In MPI mode, Local Command 9 writes the 3 output pins for each channel. When Local Command 9 reads a channel's SLIC pins, the SO1-SO3 bits will be read out with the data written in at last write operation.

In GCI mode, data can only be written to SO1, SO2 and SO3 through downstream C/I channel octet.

HARDWARE RING TRIP

In order to prevent the damage caused by high voltage ring signal, the IDT821068 offers a hardware ring trip function to respond to the off-hook signal as fast as possible. This function can be enabled by setting RTE bit in Global Command 15.

The off-hook signal can be input via either SI1 or SI2, while the ring control signal can be output via any pin of SO1, SO2, SO3, SB1 and SB2 (when SB1 and SB2 are configured as outputs). In Global Command 15, IS bit determines which input is used and OS[2:0] bits determine which output is used.

When a valid off-hook signal arrives on SI1 or SI2, the IDT821068 will turn off the ring signal by inverting the selected output, regardless of the value in corresponding SLIC output control register (the content in the corresponding SLIC control register should be changed later). This function provides a much faster response to off-hook signal than the software ring trip which turns off the ring signal by changing the value of selected output in the corresponding register.

The IPI bit in Global Command 15 is used to indicate the valid polarity of input. If the off-hook signal is active low, the IPI bit should be set to 0; if the off-hook signal is active high, the IPI bit should be set to 1.

The OPI bit in Global Command 15 is used to indicate the valid polarity of output. If the ring control signal is required to be low in normal status and be high to activate a ring, the OPI bit should be set to 1; if it is required to be high in normal status and be low to activate a ring, the OPI bit should be set to 0.

For example, in a system where the off-hook signal is active low and ring control signal is active high, the IPI bit in Global Command 15 should be set to 0 and the OPI bit should be set to 1. In normal status, the selected input (off-hook signal) is high and the selected output (ring control signal) is low. When the ring is activated by setting the output (ring control signal) high, a low pulse appearing on the input (off-hook signal) will inform the device to invert the output to low and cut off the ring signal.

INTERRUPT AND INTERRUPT ENABLE

An interrupt mechanism is offered in IDT821068 for reading the SLIC input status. Each SLIC input generates interrupt respectively when it changes state.

Any of SI1, SI2, SB1 and SB2 (when SB1 and SB2 are configured as inputs) can be interrupt source. As SI1 and SI2 are debounced signals while SB1 and SB2 are not, users should be careful if they select SB1 and SB2 as interrupt sources.

The IDT821068 provides an Interrupt Enable Command (Local Command 2) for each interrupt source to enable its interrupt ability. This command contains 4 bits (IE[3:0]) for each channel. Each bit of the IE[3:0] corresponds to one interrupt source of the specific channel. The device will ignore the interrupt signal if its corresponding bit in Interrupt Enable Command is set to 0 (disable).

Multiple interrupt sources can be enabled at the same time. The interrupt sources can only be cleared by executing a read operation of Local Command 9, by which clear all the 7 interrupt sources for the corresponding channel.

CHOPPER CLOCK

IDT821068 offers two programmable chopper clock outputs: CHCLK1 and CHCLK2. Both CHCLK1 and CHCLK2 are synchronous to MCLK. CHCLK1 outputs signal with programmable 2-28 ms clock cycle, while the frequency of CHCLK2 can be any of 256 kHz, 512 kHz and 16.384 MHz. The frequency selection of chopper clocks can be implemented by Global Command 8. The chopper clocks can be used to drive the power supply switching regulators on SLICs.

DEBOUNCE FILTERS

For each channel, IDT821068 provides two debounce filter circuits: Debounced Switch Hook (DSH) Filter for SI1 and Ground Key (GK) Filter for SI2 as shown in Figure 10. They are used to buffer the input signals on SI1 and SI2 pins before changing the state of the SLIC Debounced Input SI1/SI2 Registers (Global Command 9 and 10), or, before changing the state of the GCI upstream C/I octet. Frame Sync (FS) is necessary for both DSH filter and GK filter.

DSH Debounce bits in Local Command 4 can program the debounce time of SI1 input from SLIC on individual channel. The DSH filter is initially clocked at half of the frame sync rate (250 μs), and any data changing at this sample rate resets a programmable counter. The counter clocks at the rate of 2 ms, and the count value can be varied from 0 to 30 which is determined by Local Command 4. The corresponding SIA bit in the SLIC Debounced Input SI1 Register (accessed by Global Command 9), and the corresponding channel's SI1 bit in GCI upstream C/I octet would not be updated with the SI1 input state until the count value is reached. SI1 bit usually contains SLIC switch hook status.

GK Debounce bits in Local Command 4 can program the debounce interval of SI2 input from SLIC on corresponding channel. The debounced signal will be output to SIB of SLIC Debounced Input SI2 Register (accessed by Global Command 10) and the corresponding channel's SI2 bit in GCI upstream C/I octet. The GK debounce filter consists of an up/down counter that ranges between 0 and 6. This six-state counter is clocked by the GK timer at the sampling period of 0-30 ms, as programmed by Local Command 4. When the sampled value is low, the counter is decremented by each clock pulse. When the sampled value is high, the counter is incremented by each clock pulse. When the counter increments to 6, it sets a latch whose output is routed to the corresponding SIB bit and GCI upstream C/I octet SI2 bit. If the counter decrements to 0, this latch is cleared and the output bit is set to 0. In other cases, the latch, the SIB status and the SI2 bit in GCI upstream C/I octet remain in their previous state without being changed. In this way, at least six consecutive GK clocks with the debounce input remaining at the same state to effect an output change.

DUAL TONE AND RING GENERATION

Each channel of IDT821068 has two tone generators, Tone 0 generator and Tone1 generator, which can produce a gain-adjustable dual tone signal and output it on VOUT pin. The dual tone signal can be used for the signal generations such as test, DTMF, dial tone, busy tone, congestion tone and Caller-ID Alerting Tone etc.

The Tone0 generator and Tone1 generator of each channel can be enabled or disabled independently by setting the T0E and T1E bits in Local Command 6. The frequency of the tones generated can be programmed from 1 Hz to 4.095 kHz with 4095 steps. Local Command 5 provides 12 bits for each tone generator to set the frequency.

The gain of the Tone0 and Tone1 signal of each channel is programmed by the TG[5:0] bits in Local Command 6, in the range of -3 dB to -39 dB. The gain of each tone can calculated by the formula below:

$$G = 20 \times \lg (Tg \times 2/256) + 3.14$$

where, Tg is the decimal value of TG[5:0].

The Dual Tone Output Invert bit (TOI) of Global Command 19 can invert the output tone signal. When it is '0', it means no inversion; when it is '1', the output tone signal will be inverted.

Ring signal is a special signal generated by the dual tone generators. When only one tone generator is enabled or both tone generators produce the same tone, and frequency of the tone is set as ring signal required (10 Hz to 100 Hz), the VOUT pin will output the Ring signal.

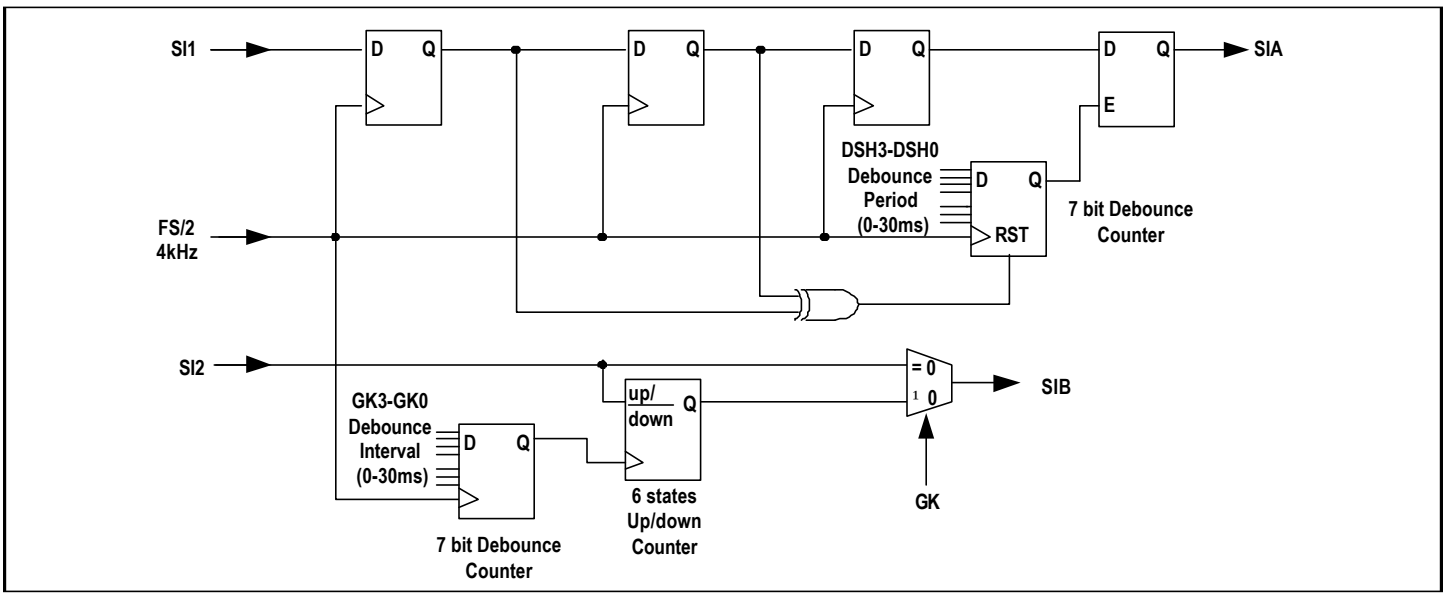


Figure 10. Debounce Filters

FSK SIGNAL GENERATION

The IDT821068 provides a FSK signal generator, which is used to send Caller-ID message. Generally, the procedure of sending Caller-ID FSK signal message is as the following:

Step 1: Start, send Seizure Signal;

Step 2: Send Mark Signal;

Step 3: Send one byte Caller-ID message, then send Flag Signal;

Step 4: If the messages to be sent are finished, stop;
otherwise, return to step 3.

Herein, the Seizure Signal is a string of '01' pairs to inform telephone set that Caller-ID message will come; the Mark Signal is a string of '1', which follows the Seizure Signal to inform telephone set that Caller-ID message is coming; while the Flag Signal is a string of '1' sending between two bytes of Caller-ID message, with this the telephone set can have enough time to processing the received byte.

According to the generic procedure of FSK signal sending, a recommended programming flow chart for IDT821068 FSK generator is shown on the following page.

In order to make it easy for users to understand the flow chart, several notes should be given:

1. The FSK function block will be enabled when FSK On/Off bit (FO) in Global Command 24 is set to 1. After finishing sending the FSK signal, the FO bit should be set to 0 to disable the generation function.

2. The FSK Start bit (FS) in Global Command 24 is used to indicate the start of the FSK signal generation, when FS bit is 0 which means the FSK generator is idle, users can go on with the operation; when FS bit is 1 which means FSK generator is busy, users should wait until it turns to 0 (after the message data in the FSK-RAM having been sent, the FS bit will be cleared to 0 automatically).

3. The length of the Seizure Signal, Mark Signal and Flag Signal are different in different system, for IDT821068, they can be programmed by Global Command 22, 23 and 20 respectively. It should be noted that, the Seizure Length is two times of the value that set in Global Command 22, for example, if the SL[7:0] bits of Global Command 22 is 1(d), it means that the Seizure Length is 2(d).

4. As is described in "Addressing of FSK-RAM", the FSK-RAM consists of 32 words, and each word consists of 16 bits (2 bytes), so it can contain up to 64 bytes of message at one time. If the message data that need to be sent is larger than 64 bytes, then users should write them into the FSK-RAM several times according to the length of the message.

5. The "Data length" is the number of bytes that written in the FSK-RAM and need to be sent out. During the transmission of FSK signal, an internal counter will count the number of data bytes that have been transmitted, once it reaches the Data length, the FSK transmission is completed and the FS bit is set to 0.

6. Because there is only one FSK-RAM shared by eight channels of IDT821068, the FSK signal can only generate on one channel at one time, the channel selection is done by the FCS[2:0] bits of Global Command 24.

7. The FSK signal generated by the IDT821068 follows the BELL 202 and CCITT V.23 specifications. Users can select BT or Bellcore standard by setting the FSK Mode Select bit (FMS) in Global Command 24. The difference between BT and Bellcore is shown in Table 3.

8. The "Mark After Send" bit (MAS) is useful if the total message data is longer than 64 bytes. If the MAS bit is set to 1, then after sending one frame of FSK-RAM message(=< 64 bytes), IDT821068 will keep sending a series of '1' to hold the communication channel for sending next frame of FSK message, and at the same time, users can update the FSK-RAM with new data. This series of '1' will stop by set the MAS bit to 0 or set the FO bit to 0.

9. It should be noted that, when writing/reading message data to/from the FSK-RAM via MPI/GCI interface, the sequence of read/write is MSB first; but the FSK generator will send these signal (message data) out through channel port with LSB first.

Refer to the IDT821068 Application Note for more information.

Table 3 – BT/Bellcore Standard of FSK Signal

Item	BT	Bellcore
Mark(1) frequency	1300 Hz ± 1.5%	1200Hz ± 1.1%
Space (0) frequency	2100 Hz ± 1.1%	2200 Hz ± 1.1%
Transmission rate	1200 baud ± 1%	1200 baud ± 1 %
Word format	1 start bit which is '0', 8 word bits (with least significant bit LSB first), 1 stop bit which is '1'	1 start bit which is '0' 8 word bits (with least significant bit LSB first) 1 stop bit which is '1'

LEVEL METERING

The IDT821068 has a level meter which can be shared by all 8 signal channels. The level meter is designed to emulate the off-chip PCM test equipment so as to facilitate the line-card, subscriber line and user telephone set monitoring. The level meter tests the returned signal and reports the measurement result via MPI/GCI interface. When combined with Tone Generation and Loopback modes, this allows the microprocessor to test channel integrity. CS[2:0] bits in Global Command 19 select the channel, signal on which will be metered.

Level Metering function is enabled by setting LMO bit to 1 in Global Command 19. There is a Level Meter Counter register for this function. It can be accessed by Global Command 18. This register is used to configure the number of time cycles for sampling PCM data (8 kHz sampling rate). The output of Level Metering will be sent to Level Meter Result Low and Level Meter Result High registers (Global Command 16 and 17). The LMRL register contains the lower 7 bits of the output and a data-ready bit (DRLV), while the LMRH register contains the higher 8 bits of the output. An internal accumulator sums the rectified samples until the number configured by Level Meter Counter register is reached. By then, the DRLV bit is set to 1 and accumulation result is latched into the LMRL and LMRH registers simultaneously.

Once the LMRH register is read, the DRLV bit will be reset. The DRLV bit will be set high again by a new data available. The contents in LMRL and LMRH will be overwritten by later metering result if they are not read out yet. In Level Metering result read operation, it is highly recommended to read LMRL first.

L/C bit in Global Command 19 determines the mode of Level Meter operation. When L/C bit is 1, the Level Meter will measure the linear PCM data, and if DRLV bit is 1, the measure result will be

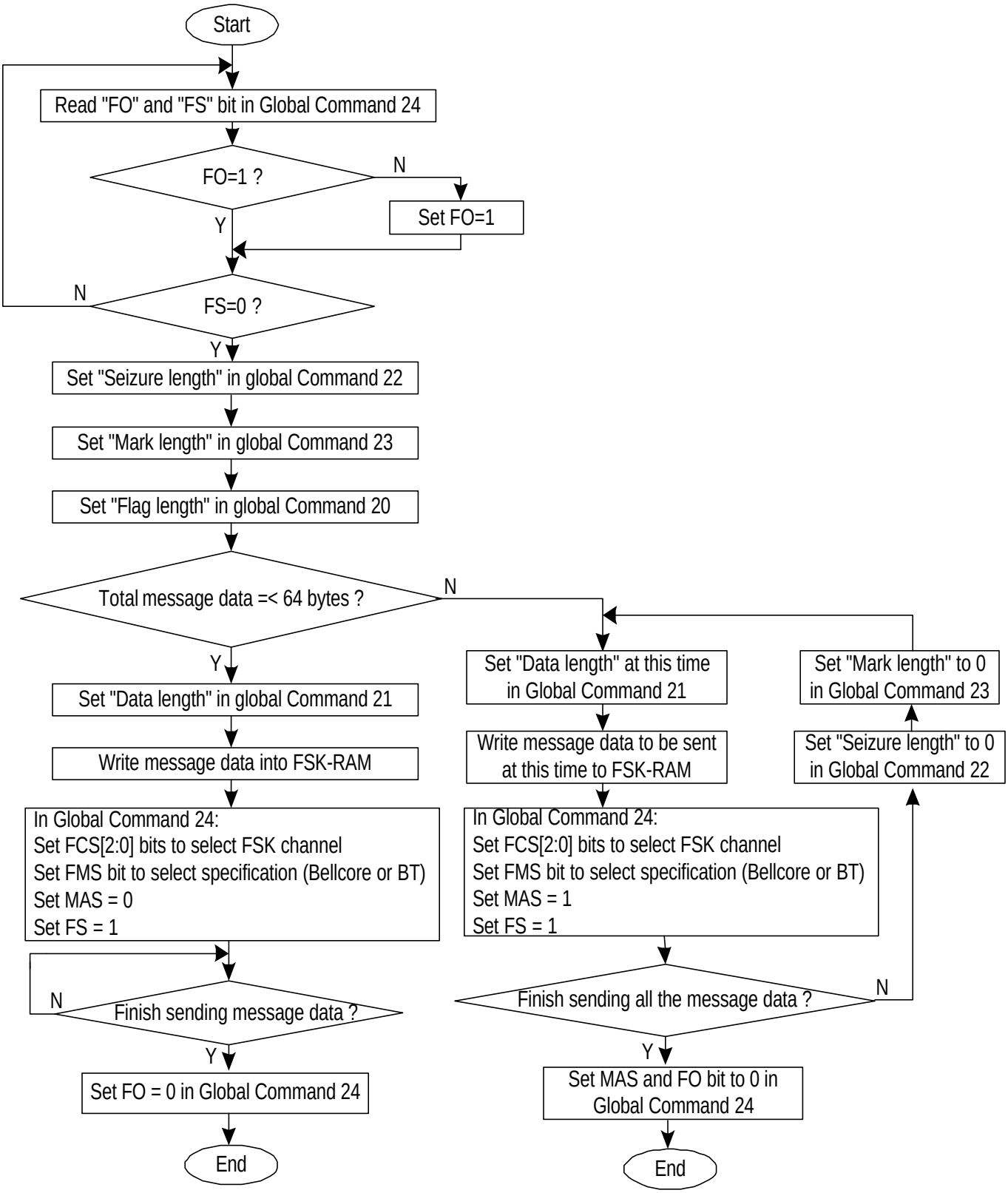


Figure 11. A Recommended Programming Flow Chart for FSK Generator

output to LMRL and LMRH. When L/C bit is 0, compressed PCM will be output transparently to LMRH.

The calculation and method of level metering will be described in Application Note.

TELETAX

The teletax signal is used to sum the telephone fee according to the calling time and tariff. The frequency of teletax signal carrier can be selected as 12 kHz or 16 kHz (± 50 Hz) by Global Command 19, while the amplitude of the teletax signal on specific channel can be programmed by Teletax Gain Setting bits (TGS[7:0]) in Local Command 3. When a '1' appears on Teletax Ramp Start bit (RS) of Local Command 10, the teletax signal will be output from the VOUT pin on the corresponding channel with a 16 ms ± 10% rising time. This teletax signal will last until a '0' on the RS bit for the same channel. It has a falling time of 16 ms ± 10%, as shown in Figure 12.

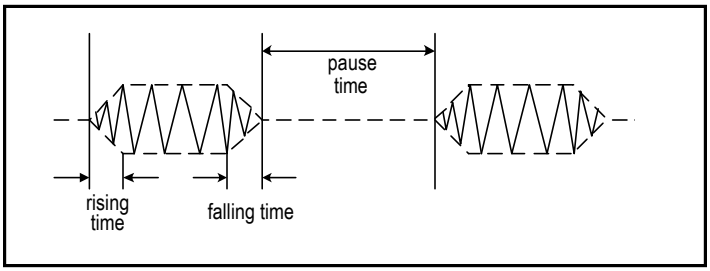


Figure 12. Teletax Signal

CHANNEL POWER DOWN/STANDBY MODE

Each individual channel of IDT821068 can be powered down independently by Local Command 10. When the channel is powered down (enters into standby mode), PCM data transmission and reception, D/A and A/D are disabled. In this way, power consumption of the device can be reduced. When IDT821068 is powered up or reset, all eight channels will be powered down. All circuits that contain programmed information retain their data when powered down. In MPI operation, MPI (Microprocessor Interface) is always active so that new command could be received and executed. In GCI operation, the monitor channel of any time slot is always on so that new command could be accepted at any time.

POWER DOWN PLL/SUSPEND MODE

A suspend mode is offered to the whole chip to save power. In this mode, the PLL block is turned off and DSP operation is disabled. This mode saves much more power consumption than standby mode. In this mode, only Global Command and Local Command can be executed. RAM operation is disabled as internal clock has been turned off. The PLL blocks can be powered down by Global Command 25. Suspend mode can be entered by powering down PLL and all channels.

OPERATING THE IDT821068

PROGRAMMING DESCRIPTION

The IDT821068 can be programmed very flexibly via the serial control interface (MPI mode) or GCI monitor channel (GCI mode). In both MPI mode and GCI mode, the programming is realized by writing commands to registers or RAMs in the chip. In MPI mode, the command data is transmitted/received via CI/CO pin; while in GCI mode, command data is sent/received via DD/DU pin.

BROADCAST MODE FOR MPI PROGRAMMING

A broadcast mode is provided in MPI write-operation (not allowed in a read-operation). Each channel has its own enable bit (CE[0] to CE[7] in Global Register 6) to allow individual channel programming. If more than one Channel Enable bit is high (enable) or if all Channel Enable bits are high, all channels enabled will receive the programming information written; therefore, a Broadcast mode can be implemented by simply enable all the channels in the device to receive the programming information. The Broadcast mode is very useful in initializing IDT821068 such as coefficient setting in a large system.

IDENTIFICATION CODE FOR MPI MODE

In MPI mode, IDT821068 provides an Identification Code to distinguish itself from other device of the system. When being read, IDT821068 outputs an Identification Code of 81H before data bytes, which indicate that the following data is from IDT821068.

PROGRAM START BYTE FOR GCI MODE

The IDT821068 uses the monitor channel for the exchange of status or mode information with high level processors. The messages transmitted in the monitor channel have different data structures. For a complete command operation, the first byte of monitor channel data indicates the address of the device either sending or receiving the data. All monitor channel messages to/from IDT821068 begin with the following Program Start (PS) byte:

Because one monitor channel is shared by two voice data channels to transmit maintenance information, so an $\overline{A}$/B bit is used in the PS byte to identify the two channels. For easy description, we name them as Channel A and Channel B. Herein,

$\overline{A}$/B = 0: means that Channel A is the source (upstream) or destination (downstream) -81H;

$\overline{A}$/B = 1: means that Channel B is the source (upstream) or destination (downstream) -91H.

The Program Start byte is followed by a command (global/local register command or RAM command) byte. For Global Command, the $\overline{A}$/B bit in the PS byte can be ignored. If the command byte specifies a write, then from 1 to 16 additional data bytes may follow (1-4 for registers, 1-16 for RAM). If the command byte specifies a read, additional data bytes may follow. IDT821068 responds to the read command by sending up to 16 data bytes upstream containing the information requested by the upstream controller. Each byte on monitor channel must be transferred at least twice and in two consecutive frames.

IDENTIFICATION COMMAND FOR GCI MODE

In order to distinguish different devices unambiguously by software, a two byte identification command is defined for analog lines GCI devices (8000H):

1	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0

Each device will then respond with its specific identification code. For IDT821068, this two byte identification code is (8082H):

1	0	0	0	0	0	0	0
1	0	0	0	0	0	1	0

COMMAND TYPE AND FORMAT

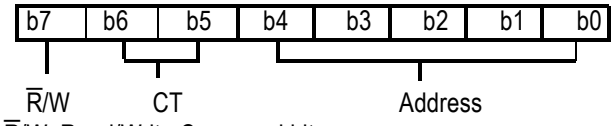
IDT821068 provides three types of register/RAM commands for both MPI and GCI operation, they are:

Local Command, which is used to configure each channel by reading/writing the Local Registers, there are 14 Local Registers per channel available;

Global Command, which is used to configure all 8 channels by reading/writing the Global Registers, there are totally 26 Global Registers shared by the 8 channels;

RAM Command, which is used to read/write the Coe-RAM and FSK-RAM, there are 40 words (divided into 5 blocks) with 14 bits per word Coe-RAM for each channel, and 32 words (divided into 4 blocks) with 16 bits per word FSK-RAM shared by the 8 channels.

The format of the commands is as the following:



$\overline{R}$/W: Read/Write Command bit.
- b7 = 0: Read Command
- b7 = 1: Write Command

CT: Command Type
- b6 b5 = 00: LC - Local Command
- b6 b5 = 01: GC - Global Command
- b6 b5 = 10: Not Allowed
- b6 b5 = 11: RC - RAM Command

Address: Specify which register or which block of RAM will be read or written.

For both Local Command and Global Command, b[4:0] are used to address the Local Registers or Global Registers.

For RAM Command, b4 is used to distinguish the Coe-RAM and the FSK RAM:

b4 = 0: The RAM Command is for Coe-RAM

b4 = 1: The RAM Command is for FSK-RAM

When the RAM Command is for Coe-RAM, b[3:0] are used to address the blocks in the Coe-RAM. When the RAM Command is for FSK-RAM, b3 is always 0' and b[2:0] are used to address the blocks in the FSK-RAM.

ADDRESSING LOCAL REGISTER

In MPI mode, when using Local Command, the Channel Enable Command (Global Command 6) must be used first to specify which channel will be addressed, then the Local Command follows. If Global Command 6 enable more than one channel, then all the channels enabled will be addressed by one Local Command at one time.

In GCI mode, both the location of time slot (determined by S1 and S0 pin) and the b4 bit in Program Start Byte would indicate which channel to be addressed.

The b[4:0] of a Local Command determine which one of the 12 Local Registers will be addressed for the configured channel.

IDT821068 provides a Consecutive Adjacent Addressing for Read/ Write Local Registers. If the address for Local Register is specified in a Local Command, then, according to the value of 'b1b0' of the address, there will be 1 to 4 adjacent local registers will be read/write automatically with the highest order first. For example, if the address of the register specified by the Local Command is end with '11' (b1b0 = '11'), 4 adjacent registers will be Read/Write by this Command. If b1b0 = '10', then 3 adjacent registers will be Read/Write. If b1b0 = '01', then only 2 adjacent registers will be Read/Write. If b1b0 = '00', then only this specified register will be Read/Write. The details of the Consecutive Adjacent Addressing is shown as below:

Table 4 – Consecutive Adjacent Addressing

Address Specified by Local Command	In/Out Data	Registers being $\overline{R}$/W
b4 b3 b2 b1 b0		
X X X 1 1	Byte 1	X X X 11
(b1b0 = 11, 4 bytes DATA)	Byte 2	X X X 10
	Byte 3	X X X 01
	Byte 4	X X X 00
X X X 1 0	Byte 1	X X X 10
(b1b0 = 10, 3 bytes DATA)	Byte 2	X X X 01
	Byte 3	X X X 00
X X X 0 1	Byte 1	X X X 01
(b1b0 = 01, 2 bytes DATA)	Byte 2	X X X 00
X X X 0 0	Byte 1	X X X 00
(b1b0 = 00, 1 byte DATA)		

In MPI mode, when $\overline{CS}$ becomes low, IDT821068 treats the first byte on CI pin as command, and the rest byte(s) as data. To write another command, the $\overline{CS}$ must change from low to high to finish the previous command and then change from high to low to indicate the start of the next command. When a Read/Write operation is completed, $\overline{CS}$ must be pulled to high in 8-bit time.

In MPI mode, the procedure of Consecutive Adjacent Addressing can be stopped by $\overline{CS}$ signal at any time. When $\overline{CS}$ change from low to high, the operation of the current Register and the next adjacent registers will be aborted. But the results of previous operation are still remained.

In GCI mode, the procedure of Consecutive Adjacent Addressing can not be stopped once a command is initiated. For write command, the number of bytes following the command must be the same as the number of registers being written.

ADDRESSING GLOBAL REGISTER

The address of the 26 Global Registers is as the following:

00000 - 11000 (Global Register 1- 25)

11100 (Global Register 26)

It should be noted that the address of Global Register 26 is 11100 and not 11001, because the address space from 11001 to 11011 are reserved.

For the adjacent 25 Global Registers, IDT821068 also provides a Consecutive Adjacent Addressing for Read/Write operation, as it does for Local Registers. In MPI mode, the procedure of Consecutive Adjacent Addressing for Global Register also can be stopped by $\overline{CS}$ signal at any time as it does for Local Registers. But in GCI mode, the procedure can not be stopped once a command is initiated. For the 26th Global Register (address is 11100), once a Read/Write procedure is completed, $\overline{CS}$ must be pulled high. It should be noted that, in GCI mode, the Global Command for all 8 channels can be transferred at any GCI time slot.

ADDRESSING COE-RAM

IDT821068 provides 40 words of Coe-RAM for per channel. They are divided into 5 blocks, each block contains 8 words. The 5 blocks are:

- IMF RAM (Word 0 - Word 7), for Impedance Matching Filter coefficient;
- ECF RAM (Word 8 - Word 15), for Echo Cancellation Filter coefficient;
- GIS RAM (Word 16 - Word 23), for Gain of Impedance Scaling;
- FRX RAM (Word 24 - Word 30) and GTX RAM (Word 31), for coefficient of Frequency Response Correction in Transmit Path and Gain in Transmit Path;
- FRR RAM (Word 32 - Word 38) and GRX RAM (Word 39), for coefficient of Frequency Response Correction in Receive Path and Gain in Receive Path.

Refer to APPENDIX I (Coe-RAM Address Mapping) for the Coe-RAM address.

Each word in the Coe-RAM is 14-bit (b[13:0]) wide. To write a Coe-RAM word, 16 bits (b[15:0]) (or, two 8-bit bytes) are needed to fulfill with MSB first, but the lowest two bits (b[1:0]) will be ignored. When being read, each Coe-RAM word will output 16 bits with MSB first, but the last two bits (b[1:0]) are meaningless.

In MPI mode, when addressing Coe-RAM, Global Command 6 (Channel Enable) must be used first to specify the channel(s), then the Address (b[4:0]) in the followed RAM Command indicates which block of the Coe-RAM for the channel(s) will be addressed.

In GCI mode, both the location of time slot (determined by S1 and S0 pin) and the b4 bit in Program Start Byte would indicate which channel will be addressed.

The address in a Coe-RAM Command locates a block of Coe-RAM. That is, when executing a Coe-RAM Command, then all 8 words in the block will be Read/Write automatically, with the highest order word first.

In MPI mode, when read/write a Coe-RAM block, the procedure of addressing words can be stopped by $\overline{CS}$ signal at any time. When $\overline{CS}$ change from low to high, the operation of the current word and the next adjacent words will be aborted. But for previous operation, the results are still remained.

ADDRESSING FSK-RAM

The FSK-RAM is consisted of 4 blocks, each block has eight 16-bit words. The total 32 words of FSK-RAM are shared by the 8 channels, only one channel can used it at one time.

To write a FSK-RAM word, 16 bits (or, two 8-bit bytes) are needed to fulfill with MSB first. When being read, each FSK-RAM word in FSK-RAM will output 16 bits with MSB first.

Only b[2:0] of a FSK-RAM Command are needed to address the 4 blocks in FSK-RAM, b3 should always be 0, and b4 always be 1 to indicate the address is for FSK-RAM.

The way of addressing FSK-RAM is similar to that of addressing Coe-RAM. When the address of a FSK-RAM block is specified in a FSK-RAM Command, all 8 words in the block will be Read/Write automatically, with the highest order word first.

In MPI mode, when read/write a FSK-RAM block, the procedure of addressing words can be stopped by $\overline{CS}$ signal at any time. When $\overline{CS}$ change from low to high, the operation of the current word and the next adjacent words will be aborted. But this will not change the results of the previous operation.

EXAMPLES OF MPI COMMANDS

Examples of Local Command, Global Command, Coe-RAM Command and FSK-RAM Command are shown in Table 5, 6, 7 and 8 respectively.

Table 5 - Local Command Transmission Sequence in MPI Mode

Data Transmitted On CI Pin	Data Received on CO Pin
Global Command 6 (Channel Program Enable byte) Local Command byte, Write Data byte 1 . . . Data byte m* Global Command 6 (Channel Program Enable byte) Local Command byte, Read	 Identification Code (81H) Data byte 1 . . . Data byte m*

Table 6 - Global Command Transmission Sequence in MPI Mode

Data Transmitted On CI Pin	Data Received on CO Pin
Global Command byte, Write Data byte 1 . . . Data byte m* Global Command byte, Read	 Identification Code (81H) Data byte 1 . . . Data byte m*

Table 7 - Coe-RAM Command Transmission Sequence in MPI Mode

Data Transmitted On CI Pin	Data Received on CO Pin
Global Command 6 (Channel Program Enable byte) Coe-RAM Command byte, Write Data word 1 (Data_H, Data_L**) Data word 2 (Data_H, Data_L) . . . Data word 8 (Data_H, Data_L) Global Command 6 (Channel Program Enable byte) Coe-RAM Command byte, Read	 Identification Code (81H) Data word 1 (Data_H, Data_L **) Data word 2 (Data_H, Data_L) . . . Data word 8 (Data_H, Data_L)

Table 8 - FSK-RAM Command Transmission Sequence in MPI Mode

Data Transmitted On CI Pin	Data Received on CO Pin
FSK-RAM Command byte, Write Data word 1 (Data_H, Data_L**) Data word 2 (Data_H, Data_L) . . . Data word 8 (Data_H, Data_L) FSK-RAM Command byte, Read	 Identification Code (81H) Data word 1 (Data_H, Data_L **) Data word 2 (Data_H, Data_L) . . . Data word 8 (Data_H, Data_L)

EXAMPLES OF GCI COMMANDS

Examples of Local/Global Command and Coe-RAM/FSK-RAM Command are shown in Table 9 and Table 10, respectively.

Table 9 - Local/Global Command Transmission Sequence in GCI Mode

GCI Monitor Channel	
Downstream	Upstream
Program Start byte (81H/91H) Local/Global Command byte, write Data byte 1 . . . Data byte m* Program Start byte (81H/91H) Local/Global Command byte, read	 Program Start byte (81H/91H) Data byte 1 . . . Data byte m*

Table 10 - Coe-RAM/FSK-RAM Command Transmission Sequence in GCI Mode

GCI Monitor Channel	
Downstream	Upstream
Program Start byte (81H/91H) Coe-RAM/FSK-RAM Command byte, write Data word 1 (Data_H , Data_L**) Data word 2 (Data_H , Data_L) . . . Data word 8 (Data_H , Data_L) Program Start byte (81H/91H) Coe-RAM/FSK-RAM Command byte, read	 Program Start byte (81H/91H) Data word 1 (Data_H , Data_L**) Data word 2 (Data_H , Data_L) . . . Data word 8 (Data_H , Data_L)

Notes:

* The number of the data bytes can be 1 to 4 depending on the two bits 'b1b0' of the Local/Global Command.

** When addressing the Coe-RAM, the data word is 14-bit wide, the lowest two bits in Data_L of each word are ignored; When addressing the FSK-RAM, the data word is 16-bit wide.

POWER-ON SEQUENCE

To power on IDT821068, users should follow this sequence:

1. Apply ground first;
2. Apply VCC, finish signal connections and set $\overline{\text{RESET}}$ low, thus the device goes into default state;
3. Set $\overline{\text{RESET}}$ high;
4. Select master clock frequency;
5. Program filter coefficients and other parameters as required.

DEFAULT STATE AFTER RESET

When the IDT821068 is powered on, or reset either by $\overline{\text{RESET}}$ pin or by GCI/MPI Command, the device defaults to the following state:

1. All eight channels are powered down and in standby mode;
2. All loopbacks and cutoff are disabled;
3. DX1/DU pin is selected for all channels to transmit data, DR1/DD pin is selected for all channels to receive data;
4. The master clock frequency is 2.048 MHz;
5. For MPI operation, transmit and receive time slots are set to 0-7 respectively for channel 1-8. The PCM data rate is the same as Bit Clock frequency. Data is transmitted on rising edges and received on falling edges;
   For GCI operation, time slots for transmitting and receiving are determined by TS pin. Data rate is determined by DOUBLE pin. DD, DU clocks data on rising edges of DCL.
6. A-Law is selected;
7. Coefficients of FRX, FRR, GTX and GTR are set to be default values. The analog gains are set to be 0 dB. IMF, GIS and ECF are disabled. HPF is enabled (See Figure 9: Signal Flow of Each Channel);
8. SB1 and SB2 are configured as inputs;
9. SI1 and SI2 are configured as no debounce;
10. All interrupts are disabled, all pending interrupts are cleared;
11. All feature function blocks including FSK, Dual Tone, Teletax, Ring Trip and Level Metering are turned off;
12. CHCLK1 and CHCLK2 are set to be high.

The data stored in RAM will not be changed by any kind of resets. In this way, the RAM data will not be lost unless the device is powered down physically.

COMMANDS LIST

NOTES:

1. $\overline{R}$/W = 0, Read command; $\overline{R}$/W = 1, Write command
2. *"R"* in the command means that bit is reserved for future use, it must be fill in '0' in write operation and be ignored in read operation.
3. The following commands are available for both MPI and GCI mode except for those with special statement.

Global Commands:

1. No Operation (A0H), Write Only

	b7	b6	b5	b4	b3	b2	b1	b0
Command	1	0	1	0	0	0	0	0

When executing this command, a data byte (FFH) must follow to ensure proper operation.

2. Read Version Number (20H), Read Only

	b7	b6	b5	b4	b3	b2	b1	b0
Command	0	0	1	0	0	0	0	0

By executing this read command, users can get the version number of the IDT821068. The default value is 1(d).

3. Software Reset (A2H), Write Only

	b7	b6	b5	b4	b3	b2	b1	b0
Command	1	0	1	0	0	0	1	0

This command resets all Local Registers, but does not reset Global Registers and RAMs. When executing this command, a data byte (FFH) must follow to ensure proper operation.

4. Hardware Reset (A3H), Write Only

	b7	b6	b5	b4	b3	b2	b1	b0
Command	1	0	1	0	0	0	1	1

The action of this command is equivalent to pulling the $\overline{RESET}$ pin low (Refer to Page 22 for information about $\overline{RESET}$ operation). When executing this command, a data byte (FFH) must follow to ensure proper operation.

5. MCLK Select (24H/A4H), Read/Write. (This command is for MPI mode only.)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	0	0	1	0	0
I/O data	*R*	*R*	*R*	*R*	Sel[3]	Sel[2]	Sel[1]	Sel[0]

In MPI mode, this command is used to determine the frequency of Master Clock, which is used by the DSP. There are 9 frequencies can be selected, the default value is 2.048MHz.

Sel [3:0] = 0000: 8.192 MHz
Sel [3:0] = 0001: 4.096 MHz
Sel [3:0] = 0010: 2.048 MHz (default)
Sel [3:0] = 0110: 1.536 MHz
Sel [3:0] = 1110: 1.544 MHz
Sel [3:0] = 0101: 3.072 MHz
Sel [3:0] = 1101: 3.088 MHz
Sel [3:0] = 0100: 6.144 MHz
Sel [3:0] = 1100: 6.176 MHz

(In GCI mode, the frequency of MCLK is the same as that of DCL, which is determined by the CI/DOUBLE pin. Refer to "Pin Description" on Page 4 for further detail.)

6. Channel Program Enable (25H/A5H), Read/Write. (This command is for MPI mode only.)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	0	0	1	0	1
I/O data	CE[7]	CE[6]	CE[5]	CE[4]	CE[3]	CE[2]	CE[1]	CE[0]

Channel Program Enable command is used to specify the channel(s) before Local Commands or a Coe-RAM Commands are executed. This command byte provides one bit per channel to indicate if the channel can receive Local Commands and Coe-RAM Commands.

CE[0] = 0: Disabled, Channel 1 can not receive Local Commands and Coe-RAM Commands (default);
CE[0] = 1: Enabled, Channel 1 can receive Local Commands and Coe-RAM Commands.

CE[1] = 0: Disabled, Channel 2 can not receive Local Commands and Coe-RAM Commands (default);
CE[1] = 1: Enabled, Channel 2 can receive Local Commands and Coe-RAM Commands.
CE[2] = 0: Disabled, Channel 3 can not receive Local Commands and Coe-RAM Commands (default);
CE[2] = 1: Enabled, Channel 3 can receive Local Commands and Coe-RAM Commands.
CE[3] = 0: Disabled, Channel 4 can not receive Local Commands and Coe-RAM Commands (default);
CE[3] = 1: Enabled, Channel 4 can receive Local Commands and Coe-RAM Commands.
CE[4] = 0: Disabled, Channel 5 can not receive Local Commands and Coe-RAM Commands (default);
CE[4] = 1: Enabled, Channel 5 can receive Local Commands and Coe-RAM Commands.
CE[5] = 0: Disabled, Channel 6 can not receive Local Commands and Coe-RAM Commands (default);
CE[5] = 1: Enabled, Channel 6 can receive Local Commands and Coe-RAM Commands.
CE[6] = 0: Disabled, Channel 7 can not receive Local Commands and Coe-RAM Commands (default);
CE[6] = 1: Enabled, Channel 7 can receive Local Commands and Coe-RAM Commands.
CE[7] = 0: Disabled, Channel 8 can not receive Local Commands and Coe-RAM Commands (default);
CE[7] = 1: Enabled, Channel 8 can receive Local Commands and Coe-RAM Commands.

7. PCM Data Offset, PCM Clock Slope, Data Mode Select, and A/m-Law Select (26H/A6H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	1	0	0	1	1	0
I/O data	LS	DMS	CS[2]	CS[1]	CS[0]	DO[2]	DO[1]	DO[0]

PCM Data Offset bits (DO[2:0]) configure the number of clocks that PCM data transmit and receive time slot is offset from the Frame Synchronous Signal (FS). (For MPI mode only)
DO[2:0] = 000: 0 BCLK period (default);
DO[2:0] = 001: 1 BCLK period;
DO[2:0] = 010: 2 BCLK periods;
DO[2:0] = 011: 3 BCLK periods;
DO[2:0] = 100: 4 BCLK periods;
DO[2:0] = 101: 5 BCLK periods;
DO[2:0] = 110: 6 BCLK periods;
DO[2:0] = 111: 7 BCLK periods.
PCM Clock Slope (CS[2:0]) bits select transmit and receive clock edge. (For MPI mode only)
CS[2] = 0: single clock (default);
CS[2] = 1: double clock;
CS[1:0] = 00: IDT821068 transmits data on rising edges of BCLK, and receives data on falling edges of BCLK (default);
CS[1:0] = 01: IDT821068 transmits data on rising edges of BCLK, and receives data on rising edges of BCLK;
CS[1:0] = 10: IDT821068 transmits data on falling edges of BCLK, and receives data on falling edges of BCLK;
CS[1:0] = 11: IDT821068 transmits data on falling edges of BCLK, and receives data on rising edges of BCLK.
Data Mode Select bit (DMS) defines the coding format of the voice data. (For both MPI and GCI mode)
DMS = 0: compressed code (default);
DMS = 1: linear code.
A/μ-law Select bit (LS) selects A-law or μ-law. (For both MPI and GCI mode)
LS = 0: A-law (default);
LS = 1: μ-law.

8. Chopper Clock Select (27H/A7H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	1	0	0	1	1	1
I/O data	*R*	*R*	CHCLK2_ SEL[1]	CHCLK2_ SEL[0]	CHCLK1_ SEL[3]	CHCLK1_ SEL[2]	CHCLK1_ SEL[1]	CHCLK1_ SEL[0]

CHCLK1_SEL bits configure the programmable output pin CHCLK1.
CHCLK1_SEL[3:0] = 0000: CHCLK1 outputs 1 permanently (default);
CHCLK1_SEL[3:0] = 0001: CHCLK1 outputs digital signal at the frequency of 1000/2 Hz;
CHCLK1_SEL[3:0] = 0010: CHCLK1 outputs digital signal at the frequency of 1000/4 Hz;
CHCLK1_SEL[3:0] = 0011: CHCLK1 outputs digital signal at the frequency of 1000/6 Hz;
CHCLK1_SEL[3:0] = 0100: CHCLK1 outputs digital signal at the frequency of 1000/8 Hz;

CHCLK1_SEL[3:0] = 0101: CHCLK1 outputs digital signal at the frequency of 1000/10 Hz;
CHCLK1_SEL[3:0] = 0110: CHCLK1 outputs digital signal at the frequency of 1000/12 Hz;
CHCLK1_SEL[3:0] = 0111: CHCLK1 outputs digital signal at the frequency of 1000/14 Hz;
CHCLK1_SEL[3:0] = 1000: CHCLK1 outputs digital signal at the frequency of 1000/16 Hz;
CHCLK1_SEL[3:0] = 1001: CHCLK1 outputs digital signal at the frequency of 1000/18 Hz;
CHCLK1_SEL[3:0] = 1010: CHCLK1 outputs digital signal at the frequency of 1000/20 Hz;
CHCLK1_SEL[3:0] = 1011: CHCLK1 outputs digital signal at the frequency of 1000/22 Hz;
CHCLK1_SEL[3:0] = 1100: CHCLK1 outputs digital signal at the frequency of 1000/24 Hz;
CHCLK1_SEL[3:0] = 1101: CHCLK1 outputs digital signal at the frequency of 1000/26 Hz;
CHCLK1_SEL[3:0] = 1110: CHCLK1 outputs digital signal at the frequency of 1000/28 Hz;
CHCLK1_SEL[3:0] = 1111: CHCLK1 outputs 0 permanently.

CHCLK2_SEL bits configure the programmable output pin CHCLK2.

CHCLK2_SEL[1:0] = 00: CHCLK2 outputs 1 permanently (default);
CHCLK2_SEL[1:0] = 01: CHCLK2 outputs digital signal at the frequency of 512 kHz;
CHCLK2_SEL[1:0] = 10: CHCLK2 outputs digital signal at the frequency of 256 kHz;
CHCLK2_SEL[1:0] = 11: CHCLK2 outputs digital signal at the frequency of 16.384 MHz.

9. SLIC Debounced Input SI1 (28H), Read Only

	b7	b6	b5	b4	b3	b2	b1	b0
Command	0	0	1	0	1	0	0	0
I/O data	SIA[7]	SIA[6]	SIA[5]	SIA[4]	SIA[3]	SIA[2]	SIA[1]	SIA[0]

SIA is the debounced version of SI1, see Figure 10 (Debounce filters) on Page 15. The SIA bits SIA[7:0] contain SLIC status which SLIC interface pin SI1 receives.

SIA[0]: debounced data of SI1 on Channel 1 (default value is 0);
SIA[1]: debounced data of SI1 on Channel 2 (default value is 0);
SIA[2]: debounced data of SI1 on Channel 3 (default value is 0);
SIA[3]: debounced data of SI1 on Channel 4 (default value is 0);
SIA[4]: debounced data of SI1 on Channel 5 (default value is 0);
SIA[5]: debounced data of SI1 on Channel 6 (default value is 0);
SIA[6]: debounced data of SI1 on Channel 7 (default value is 0);
SIA[7]: debounced data of SI1 on Channel 8 (default value is 0).

10. SLIC Debounced Input SI2 (29H), Read Only

	b7	b6	b5	b4	b3	b2	b1	b0
Command	0	0	1	0	1	0	0	1
I/O data	SIB[7]	SIB[6]	SIB[5]	SIB[4]	SIB[3]	SIB[2]	SIB[1]	SIB[0]

SIB is the debounced version of SI2, see Figure 10 (Debounce filters) on Page 15. The SIB bits SIB[7:0] contain SLIC ground key status which SLIC interface pin SI2 receives.

SIB[0]: debounced data of SI2 on Channel 1 (default value is 0);
SIB[1]: debounced data of SI2 on Channel 2 (default value is 0);
SIB[2]: debounced data of SI2 on Channel 3 (default value is 0);
SIB[3]: debounced data of SI2 on Channel 4 (default value is 0);
SIB[4]: debounced data of SI2 on Channel 5 (default value is 0);
SIB[5]: debounced data of SI2 on Channel 6 (default value is 0);
SIB[6]: debounced data of SI2 on Channel 7 (default value is 0);
SIB[7]: debounced data of SI2 on Channel 8 (default value is 0).

11. SLIC Real-time SB1 Data (2AH/AAH), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	0	1	0	1	0
I/O data	SB1[7]	SB1[6]	SB1[5]	SB1[4]	SB1[3]	SB1[2]	SB1[1]	SB1[0]

SB1 bits contain the information of SLIC bidirectional pin SB1.

SB1[0]: SB1 data on Channel 1 (default value is 0);
SB1[1]: SB1 data on Channel 2 (default value is 0);

SB1[2]: SB1 data on Channel 3 (default value is 0);
SB1[3]: SB1 data on Channel 4 (default value is 0);
SB1[4]: SB1 data on Channel 5 (default value is 0);
SB1[5]: SB1 data on Channel 6 (default value is 0);
SB1[6]: SB1 data on Channel 7 (default value is 0);
SB1[7]: SB1 data on Channel 8 (default value is 0).

12. SLIC Real-time SB2 Data (2BH/ABH), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	1	0	1	0	1	1
I/O data	SB2[7]	SB2[6]	SB2[5]	SB2[4]	SB2[3]	SB2[2]	SB2[1]	SB2[0]

SB2 bits contain the information of SLIC bidirectional pin SB2.
SB2[0]: SB2 data on Channel 1 (default value is 0);
SB2[1]: SB2 data on Channel 2 (default value is 0);
SB2[2]: SB2 data on Channel 3 (default value is 0);
SB2[3]: SB2 data on Channel 4 (default value is 0);
SB2[4]: SB2 data on Channel 5 (default value is 0);
SB2[5]: SB2 data on Channel 6 (default value is 0);
SB2[6]: SB2 data on Channel 7 (default value is 0);
SB2[7]: SB2 data on Channel 8 (default value is 0).

13. SB1 Direction (2CH/ACH), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	1	0	1	1	0	0
I/O data	SB1C[7]	SB1C[6]	SB1C[5]	SB1C[4]	SB1C[3]	SB1C[2]	SB1C[1]	SB1C[0]

SLIC SB1 Direction bits (SB1C[7:0]) configure the directions of SLIC interface pin SB1.
SB1C[0] = 0: SB1 pin on Channel 1 is configured as input (default);
SB1C[0] = 1: SB1 pin on Channel 1 is configured as output;
SB1C[1] = 0: SB1 pin on Channel 2 is configured as input (default);
SB1C[1] = 1: SB1 pin on Channel 2 is configured as output;
SB1C[2] = 0: SB1 pin on Channel 3 is configured as input (default);
SB1C[2] = 1: SB1 pin on Channel 3 is configured as output;
SB1C[3] = 0: SB1 pin on Channel 4 is configured as input (default);
SB1C[3] = 1: SB1 pin on Channel 4 is configured as output;
SB1C[4] = 0: SB1 pin on Channel 5 is configured as input (default);
SB1C[4] = 1: SB1 pin on Channel 5 is configured as output;
SB1C[5] = 0: SB1 pin on Channel 6 is configured as input (default);
SB1C[5] = 1: SB1 pin on Channel 6 is configured as output;
SB1C[6] = 0: SB1 pin on Channel 7 is configured as input (default);
SB1C[6] = 1: SB1 pin on Channel 7 is configured as output;
SB1C[7] = 0: SB1 pin on Channel 8 is configured as input (default);
SB1C[7] = 1: SB1 pin on Channel 8 is configured as output.

14. SB2 Direction (2DH/ADH), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	1	0	1	1	0	1
I/O data	SB2C[7]	SB2C[6]	SB2C[5]	SB2C[4]	SB2C[3]	SB2C[2]	SB2C[1]	SB2C[0]

SLIC SB2 Direction bits (SB2C[7:0]) configure the direction of SLIC interface pin SB2.
SB2C[0] = 0: SB2 pin on Channel 1 is configured as input (default);
SB2C[0] = 1: SB2 pin on Channel 1 is configured as output;
SB2C[1] = 0: SB2 pin on Channel 2 is configured as input (default);
SB2C[1] = 1: SB2 pin on Channel 2 is configured as output;
SB2C[2] = 0: SB2 pin on Channel 3 is configured as input (default);
SB2C[2] = 1: SB2 pin on Channel 3 is configured as output;

SB2C[3] = 0: SB2 pin on Channel 4 is configured as input (default);
SB2C[3] = 1: SB2 pin on Channel 4 is configured as output;
SB2C[4] = 0: SB2 pin on Channel 5 is configured as input (default);
SB2C[4] = 1: SB2 pin on Channel 5 is configured as output;
SB2C[5] = 0: SB2 pin on Channel 6 is configured as input (default);
SB2C[5] = 1: SB2 pin on Channel 6 is configured as output;
SB2C[6] = 0: SB2 pin on Channel 7 is configured as input (default);
SB2C[6] = 1: SB2 pin on Channel 7 is configured as output;
SB2C[7] = 0: SB2 pin on Channel 8 is configured as input (default);
SB2C[7] = 1: SB2 pin on Channel 8 is configured as output;

15. SLIC Ring Trip Setting (2EH/AEH), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	1	0	1	1	1	0
I/O data	OPI	R	IPI	IS	RTE	OS[2]	OS[1]	OS[0]

Output Selection bits OS[2:0] determine which output pin will be selected as the ring control signal source.
OS = 000 - 010: not defined;
OS = 011: SB1 is selected (when it is configured as an output);
OS = 100: SB2 is selected (when it is configured as an output);
OS = 101: SO1 is selected;
OS = 110: SO2 is selected;
OS = 111: SO3 is selected.
Ring Trip Enable bit RTE enables or disables the ring trip function block:
RTE = 0: the ring trip function block is disabled (default);
RTE = 1: the ring trip function block is enabled.
Input Selection bit IS determines which input will be selected as the off-hook indication signal source.
IS = 0: SI1 is selected (default); IS = 1: SI2 is selected.
Input Polarity Indicator bit IPI indicates the valid polarity of input.
IPI = 0: active low (default); IPI = 1: active high.
Output Polarity Indicator bit OPI indicates the valid polarity of output.
OPI = 0: the selected output pin changes from high to low to activate the ring (default);
OPI = 1: the selected output pin changes from low to hight to activate the ring.

16. Level Meter Result Low Register (30H), Read Only

	b7	b6	b5	b4	b3	b2	b1	b0
Command	0	0	1	1	0	0	0	0
I/O data	LMRL[7]	LMRL[6]	LMRL[5]	LMRL[4]	LMRL[3]	LMRL[2]	LMRL[1]	DRLV

This register contains the lower 8 bits of Level Meter output with the default value of '0000-0000', LVLL[0] is the active high data_ready bit. To read the level meter result, users should read the low register which contains LVLL[7:0] data first, then read the high register which contains LVLH[7:0] data. Once the high register is read, the LVLL[0] bit is cleared immediately.

17. Level Meter Result High Register (31H), Read Only

	b7	b6	b5	b4	b3	b2	b1	b0
Command	0	0	1	1	0	0	0	1
I/O data	LMRH[7]	LMRH[6]	LMRH[5]	LMRH[4]	LMRH[3]	LMRH[2]	LMRH[1]	LMRH[0]

This register contains the higher 8 bits of Level Metering output with the default value of 0(d).

18. Level Meter Counter (32H/B2H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	1	1	0	0	1	0
I/O data	CN[7]	CN[6]	CN[5]	CN[4]	CN[3]	CN[2]	CN[1]	CN[0]

Level Meter Counter register is used to configure the number of time cycles for sampling PCM data.
CN = 0 (d): the linear or compressed PCM data is output to LMRH and LMRL directly (default);
CN = N: PCM data is sampled for N * 125 μs (N from 1 to 255).

19. Level Meter Channel Select, Level Meter Mode Select, Level Meter On/off, Teletax Pulse Frequency and Dual Tone Output Invert (33H/B3H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	1	0	0	1	1
I/O data	R	TOI	TF	LMO	L/C	CS[2]	CS[1]	CS[0]

Level Meter Channel Select bits (CS[2:0]) select the channel, data on which will be level metered.

CS = 000: Channel 1 is selected (default);
CS = 001: Channel 2 is selected;
CS = 010: Channel 3 is selected;
CS = 011: Channel 4 is selected;
CS = 100: Channel 5 is selected;
CS = 101: Channel 6 is selected;
CS = 110: Channel 7 is selected;
CS = 111: Channel 8 is selected.

Level Meter Mode Select bit (L/C) determines the mode of level meter operation.

L/C = 0: Message mode is selected. Compressed PCM will be output to LMRH transparently (default);
L/C = 1: Meter mode is selected. Linear PCM data will be metered and output to LMRH and LMRL, when data_ready bit in LMRL register is '1'.

Level Meter On/off bit (LMO) enables the level meter.

LMO = 0: Level meter is disabled (default);
LMO = 1: Level meter is enabled.

Teletax Pulse Frequency bit (TF) selects the frequency of teletax pulse.

TF = 0: Teletax pulse frequency is 16 kHz (default);
TF = 1: Teletax pulse frequency is 12 kHz.

Dual Tone Output Invert bit (TOI) determines whether output tone signal will be inverted or not.

TOI = 0: no inversion (default);
TOI = 1: output signal is inverted.

20. FSK Flag Length (34H/B4H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	1	0	1	0	0
I/O data	FL[7]	FL[6]	FL[5]	FL[4]	FL[3]	FL[2]	FL[1]	FL[0]

Flag Length bits (FL[7:0]) determine the number of flag bits '1' which will be transmitted between the transmission of message bytes. The value is valid from 0 to 255(d). The default value is 0(d). If 0(d) is selected, no flag signal will be sent.

21. FSK Data Length (35H/B5H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	1	0	0	0	1
I/O data	WL[7]	WL[6]	WL[5]	WL[4]	WL[3]	WL[2]	WL[1]	WL[0]

Data Length bits (WL[7:0]) determine the number of all the data bytes which will be transmitted except flag. The value is valid from 0 to 64(d). Any value larger than 64(d) will be taken as 64(d) by the CPU.

The default value of this register is 0(d). When 0(d) is selected, none of the word data will be sent out. When Mark After Send (MAS bit in Global Command 24) is set to '1', the mark signal will be sent; while Mark After Send is set to '0', the transmission of mark signal will be terminated.

22. FSK Seizure Length (36H/B6H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	1	0	1	1	0
I/O data	SL[7]	SL[6]	SL[5]	SL[4]	SL[3]	SL[2]	SL[1]	SL[0]

Seizure Length bits (SL[7:0]) determine the number of '01' pairs which represent seizure phase (Seizure Length is two times of the value in SL[7:0], which is valid from 0 to 255(d), corresponding to Seizure Length 0 to 510). The default value is 0(d). When 0(d) is selected, no seizure signal will be sent.

23. FSK Mark Length (37H/B7H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	1	0	1	1	1
I/O data	ML[7]	ML[6]	ML[5]	ML[4]	ML[3]	ML[2]	ML[1]	ML[0]

Mark Length bits (ML[7:0]) determine the number of mark bits '1' which will be transmitted in initial flag phase. The value is valid from 0 to 255(d), the default value is 0(d). When 0(d) is selected, no mark signal will be sent.

24. FSK Start, Mark After Send, FSK Mode Select, FSK Channel Select and FSK On/Off (38H/B8H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	1	1	0	0	0
I/O data	FO	FCS[2]	FCS[1]	FCS[0]	R	FMS	MAS	FS

FSK Start bit (FS) should be set to '1' when users are going to send out FSK data. It will be cleared TO the default value '0' at the end of word data. When Seizure Length, Mark Length together with Data Length bits are all set to 0(d), the FSK Start bit will be reset to '0' immediately after it is set to '1'.

Mark After Send bit (MAS) determine the FSK block operation after the word data has been sent.

MAS = 0: The output will be muted after sending out word data (default);

MAS = 1: After sending out one frame of message data (=< 64 bytes), IDT821068 keeps sending a series of '1' until the MAS bit is set to 0 and the FS bit is set to 1.

FSK Mode Select bit (FMS) determines which specification the IDT821068 follows:

FMS = 0: Bellcore specification is selected (default);

FMS = 1: BT specification is selected.

FSK Channel Select bits (FCS[2:0]) selects the channel on which FSK operation will be implemented.

FCS[2:0] = 000: Channel 1 is selected (default);
FCS[2:0] = 001: Channel 2 is selected;
FCS[2:0] = 010: Channel 3 is selected;
FCS[2:0] = 011: Channel 4 is selected;
FCS[2:0] = 100: Channel 5 is selected;
FCS[2:0] = 101: Channel 6 is selected;
FCS[2:0] = 110: Channel 7 is selected;
FCS[2:0] = 111: Channel 8 is selected.

FSK On/Off (FO) enables or disables the whole FSK function block.

FO = 0: FSK is disabled (default);

FO = 1: FSK is enabled.

25. Loop Control and PLL Power Down (3CH/BCH), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	1	1	1	0	0
I/O data	R	PLLPD	R	LP[4]	LP[3]	LP[2]	LP[1]	LP[0]

Loop Control bits (LP[4:0]) determine the loopback status. Refer to Figure 9 for detail information.

LP[0] = 0: Analog Loopback via PCM Highway is disabled (default);
LP[0] = 1: Analog Loopback via PCM Highway is enabled;
LP[1] = 0: Digital Loopback via PCM Highway is disabled (default);
LP[1] = 1: Digital Loopback via PCM Highway is enabled;
LP[2] = 0: Digital Loopback via 8 kHz Interface is disabled (default);
LP[2] = 1: Digital Loopback via 8 kHz Interface is enabled;
LP[3] = 0: Analog Loopback via 8 kHz Interface is disabled (default);
LP[3] = 1: Analog Loopback via 8 kHz Interface is enabled;
LP[4] = 0: Digital Loopback via Analog Interface is disabled (default);
LP[4] = 1: Digital Loopback via Analog Interface is enabled.

PLL Power Down Bit (PLLPD) controls the status of Phase Lock Loop.

PLLPD = 0: the device is in normal operation (default);

PLLPD = 1: Phase Lock Loop is powered down. The device works in Power-Saving mode. All clocks stop running.

Local Commands:

1. Coefficient Select (00H/80H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	0	0	0	0	0	0
I/O data	CS[7]	CS[6]	CS[5]	CS[4]	CS[3]	CS[2]	CS[1]	CS[0]

Coefficient Select bits (CS[7:0]) are used to control digital filters and function blocks on corresponding channel such as Impedance Matching Filter, Echo Cancellation Filter, High-Pass Filter, Gain for Impedance Scaling, Gain in Transmit/Receive Path and Frequency Response Correction in Transmit/Receive Path. See Figure 9 for detail. It should be noted that Impedance Matching Filter and Gain for Impedance Scaling are working together to adjust impedance. That is to say, CS[0] and CS[2] should be set to the same value to ensure the correct operation.

CS[0] = 0: Impedance Matching Filter is disabled (default);
CS[0] = 1: Impedance Matching Filter coefficient is set by IMF RAM;
CS[1] = 0: Echo Cancellation Filter is disabled (default);
CS[1] = 1: Echo Cancellation Filter coefficient is set by ECF RAM;
CS[2] = 0: Gain for Impedance Scaling is disabled (default);
CS[2] = 1: Gain for Impedance Scaling coefficient is set by GIS RAM;
CS[3] = 0: High-Pass Filter is bypassed/disabled;
CS[3] = 1: High-Pass Filter is enabled (default);
CS[4] = 0: Frequency Response Correction in Transmit Path is bypassed (default);
CS[4] = 1: Frequency Response Correction in Transmit Path coefficient is set by FRX RAM;
CS[5] = 0: Gain in Transmit Path is 0 dB (default);
CS[5] = 1: Gain in Transmit Path coefficient is set by GTX RAM;
CS[6] = 0: Frequency Response Correction in Receive Path is bypassed (default);
CS[6] = 1: Frequency Response Correction in Receive Path coefficient is set by FRR RAM;
CS[7] = 0: Gain in Receive Path is 0 dB (default);
CS[7] = 1: Gain in Receive Path coefficient is set by GRX RAM.

The mapping method of RAM can be found in Coefficient Memory Address Mapping (Page 42).

2. Loop Status Control, PCM Receive Path Cutoff and SLIC Input Interrupt Enable (01H/81H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	0	0	0	0	0	1
I/O data	IE[3]	IE[2]	IE[1]	IE[0]	PCF	LPC[2]	LPC[1]	LPC[0]

Loop Status Control Bits (LPC[2:0]) determine the loopback status on corresponding channel.

LPC[0] = 0: Digital Loopback via Onebit is disabled on the corresponding channel (default);
LPC[0] = 1: Digital loopback via Onebit is enabled on the corresponding channel;
LPC[1] = 0: Analog Loopback via Onebit is disabled on the corresponding channel (default);
LPC[1] = 1: Analog Loopback via Onebit is enabled on the corresponding channel;
LPC[2] = 0: Digital Loopback via Time slots is disabled on the corresponding channel (default);
LPC[2] = 1: Digital Loopback via Time slots is enabled on the corresponding channel. In this loopback mode, the digital data received from DR will be switched by the time slot setting, and then will be transmitted out from DX pin.

PCM Receive Path Cutoff bit (PCF) is used to cut off the PCM receive path, see Figure 9.

PCF = 0: PCM Receive Path in normal operation;
PCF = 1: PCM Receive Path is cut off.

SLIC Input Interrupt Enable bits (IE[3:0]) enable or disable the interrupt signal on each channel.

IE[0] = 0: Interrupt disable. Interrupt signal on SB2 (when it is selected as an input) will be ignored (default);
IE[0] = 1: Interrupt enable. Interrupt signal on SB2 (when it is selected as an input) will be recognized;
IE[1] = 0: Interrupt disable. Interrupt signal on SB1 (when it is selected as an input) will be ignored (default);
IE[1] = 1: Interrupt enable. Interrupt signal on SB1 (when it is selected as an input) will be recognized;
IE[2] = 0: Interrupt disable. Interrupt signal on SI2 will be ignored (default);
IE[2] = 1: Interrupt enable. Interrupt signal on SI2 will be recognized;
IE[3] = 0: Interrupt disable. Interrupt signal on SI1 will be ignored (default);
IE[3] = 1: Interrupt enable. Interrupt signal on SI1 will be recognized;

3. Teletax Gain Setting (02H/82H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	0	0	0	0	1	0
I/O data	TGS[7]	TGS[6]	TGS[5]	TGS[4]	TGS[3]	TGS[2]	TGS[1]	TGS[0]

Teletax Gain Setting bits (TGS[7:0]) are used to set the gain of teletax on corresponding channel. The default value is '00H' which means the gain is 0, 'FFH' represents the gain of 1. There are totally 255 steps between gain 0 and 1 corresponding to the value of the command I/O data.

4. DSH Debounce and GK Debounce (03H/83H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	0	0	0	0	1	1
I/O data	GK[3]	GK[2]	GK[1]	GK[0]	DSH[3]	DSH[2]	DSH[1]	DSH[0]

DSH Debounce bits (DSH[3:0]) set the debounce time of SI1 input from SLIC on corresponding channel.

DSH [3:0] = 0000: 0 ms (default);
DSH [3:0] = 0001: 2 ms;
DSH [3:0] = 0010: 4 ms;
DSH [3:0] = 0011: 6 ms;
DSH [3:0] = 0100: 8 ms;
DSH [3:0] = 0101: 10 ms;
DSH [3:0] = 0110: 12 ms;
DSH [3:0] = 0111: 14 ms;
DSH [3:0] = 1000: 16 ms;
DSH [3:0] = 1001: 18 ms;
DSH [3:0] = 1010: 20 ms;
DSH [3:0] = 1011: 22 ms;
DSH [3:0] = 1100: 24 ms;
DSH [3:0] = 1101: 26 ms;
DSH [3:0] = 1110: 28 ms;
DSH [3:0] = 1111: 30 ms.

GK Debounce bits (GK[3:0]) set the debounce interval of SI2 input from SLIC on corresponding channel.

GK [3:0] = 0000: 0 ms (default);
GK [3:0] = 0001: 2 ms;
GK [3:0] = 0010: 4 ms;
GK [3:0] = 0011: 6 ms;
GK [3:0] = 0100: 8 ms;
GK [3:0] = 0101: 10 ms;
GK [3:0] = 0110: 12 ms;
GK [3:0] = 0111: 14 ms;
GK [3:0] = 1000: 16 ms;
GK [3:0] = 1001: 18 ms;
GK [3:0] = 1010: 20 ms;
GK [3:0] = 1011: 22 ms;
GK [3:0] = 1100: 24 ms;
GK [3:0] = 1101: 26 ms;
GK [3:0]= 1110: 28 ms;
GK [3:0] = 1111: 30 ms.

5. Dual Tone Frequency Setting (04H, 05H, 06H/84H, 85H, 86H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	0	0	0	1	0	0
I/O data	T0[7]	T0[6]	T0[5]	T0[4]	T0[3]	T0[2]	T0[1]	T0[0]

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	0	0	0	1	0	1
I/O data	T1[3]	T1[2]	T1[1]	T1[0]	T0[11]	T0[10]	T0[9]	T0 [8]

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	0	0	0	1	1	0
I/O data	T1[11]	T1[10]	T1[9]	T1[8]	T1[7]	T1[6]	T1[5]	T1[4]

The decimal value of Dual Tone Frequency Setting bits (T0[11:0]) is the frequency of Tone0 on corresponding channel. The decimal value of T1[11:0] bits is the Tone1 frequency on corresponding channel.

6. Tone Enable and Tone Gain (07H/87H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	0	0	0	1	1	1
I/O data	T1E	T0E	TG[5]	TG[4]	TG[3]	TG[2]	TG[1]	TG[0]

Tone Gain bits (TG[5:0]) are used to determine the gain of dual tone signal on corresponding channel.

$G = 20 \times \lg(Tg \times 2/256) + 3.14$

where: G is the desired tone gain, and Tg is the decimal value of TG[5:0].

Tone 1 Enable and Tone 0 Enable bits T1E and T0E are used to activate tone 1 or tone 0 on corresponding channels.

T1E = 0: Tone1 is disabled at the peak value in phase 90 degree (default);

T1E = 1: Tone1 is enabled at zero-crossing;

T0E = 0: Tone0 is disabled at the peak value in phase 90 degree (default);

T0E = 1: Tone0 is enabled at zero-crossing.

7. Transmit Time slot and Transmit Highway Selection (08H/88H), Read/Write (For MPI mode only)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	0	0	1	0	0	0
I/O data	THS	TT[6]	TT[5]	TT[4]	TT[3]	TT[2]	TT[1]	TT[0]

Transmit Time slot bits (TT[6:0]) determine which time slot will be used to transmit data for corresponding channel. The valid value is 0d - 127d corresponding to TS0 to TS127. The default value of TT[6:0] is N for Channel N+1 (N = 0 to 7).

Transmit Highway Selection bit (THS) selects the PCM highway on corresponding channel to transmit voice data.

THS = 0: DX1 is selected (default);

THS = 1: DX2 is selected.

8. Receive Time slot and Highway Selection (09H/89H), Read/Write (For MPI mode only)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	0	0	1	0	0	1
I/O data	RHS	RT[6]	RT[5]	RT[4]	RT[3]	RT[2]	RT[1]	RT[0]

Receive Time slot bits RT[6:0] determine which time slot will be used to receive data for corresponding channel. The valid value is 0d - 127d corresponding to TS0 to TS127. The default value of RT[6:0] is N for Channel N+1 (N = 0 to 7).

Receive Highway Selection bit RHS selects the PCM highway on corresponding channel to receive voice data.

RHS = 0: DR1 is selected (default);

RHS = 1: DR2 is selected.

9. Channel I/O Data (0AH/8AH), Read/Write (For MPI mode only)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	0	0	1	0	1	0
I/O data	R	SO3	SO2	SO1	SI1	SI2	SB1	SB2

Channel I/O Data bits contain the information of SLIC I/O pins SI1, SI2, SB1, SB2, SO1, SO2 and SO3 on corresponding channel. Default value is '0d'. It should be noted that both SB1 and SB2 are read only in this command.

10. Teletax Ramp Start, D/A Gain, A/D Gain and Channel Power Down (0CH/8CH), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	0	0	1	1	0	0
I/O data	PD	GAD	GDA	RS	R	R	R	R

Teletax Ramp Start bit (RS) starts or stops the teletax on corresponding channel.
RS = 0: Teletax is stopped (default);
RS = 1: Teletax is started.
D/A Gain bit (GDA) sets the gain of analog D/A for corresponding channel.
GDA = 0: 0 dB (default);
GDA = 1: -6 dB.
A/D Gain bit (GAD) sets the gain of analog A/D for corresponding channel.
GAD = 0: 0 dB (default);
GAD = 1: +6 dB.
Channel Power Down bit (PD) disables or enables the corresponding channel.
PD = 0: the corresponding channel is in normal operation;
PD = 1: the corresponding channel is powered down (default).

11. PCM Data Low Byte (0EH), Read Only (For MPI mode only)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	0	0	0	0	1	1	1	0
I/O data	PCM[7]	PCM[6]	PCM[5]	PCM[4]	PCM[3]	PCM[2]	PCM[1]	PCM[0]

This command is used for MCU to monitor the transmit (A to D) PCM data. For linear Code, the low 8 bits of the PCM data will be output at CO pin, and at the same time, the transmit data will be output to PCM bus without any interference. For compressed code (A/μ-Law), the total 8 bit PCM data will be output at CO pin.

12. PCM Data High Byte (0FH), Read Only (For MPI mode only)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	0	0	0	0	1	1	1	1
I/O data	PCM[15]	PCM[14]	PCM[13]	PCM[12]	PCM[11]	PCM[10]	PCM[9]	PCM[8]

This command is used for MCU to monitor the transmit (A to D) PCM data. For linear Code, the high 8 bits of the PCM data will be output at CO pin, and at the same time, the transmit data will be output to PCM bus without any interference. For compressed code (A/μ-Law), this command is not used.

ABSOLUTE MAXIMUM RATINGS

Rating	Com'l & Ind'l	Unit
Power Supply Voltage	≤ 6.5	V
Voltage on Any Pin with Respect to Ground	-0.5 to 5.5	V
Package Power Dissipation	≤1.5	W
Storage Temperature	-65 to +150	°C

NOTE: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature	-40		+85	°C
Power Supply Voltage	4.75		5.25	V

NOTE: MCLK: 1.536 MHz, 1.544 MHz, 2.048 MHz, 3.072 MHz, 3.088 MHz, 4.096 MHz, 6.144 MHz, 6.176 MHz or 8.192 MHz with tolerance of ± 50 ppm

ELECTRICAL CHARACTERISTICS

Digital Interface

Parameter	Description	Min	Typ	Max	Units	Test Conditions
V_{IL}	Input Low Voltage			0.8	V	All digital inputs
V_{IH}	Input High Voltage	2.0			V	All digital inputs
V_{OL}	Output Low Voltage			0.8	V	DX, I_L = 8 mA All other digital outputs, I_L = 4 mA.
V_{OH}	Output High Voltage	VDD - 0.6			V	DX, I_L = -8 mA All other digital outputs, I_L = -4 mA.
I_I	Input Current	-10		10	µA	All digital inputs, GND<VIN<VDD
I_{OZ}	Output Current in High-impedance State	-10		10	µA	DX
C_I	Input Capacitance			5	pF	

Power Dissipation

Parameter	Description	Min	Typ	Max	Units	Test Conditions
I_{DD1}	Operating Current			200	mA	All channels are active.
I_{DD0}	Standby Current			6	mA	All channels and PLL are powered down.

Note: Power measurements are made at MCLK = 4.096 MHz, outputs unloaded

Analog Interface

Parameter	Description	Min	Typ	Max	Units	Test Conditions
V_{OUT1}	Output Voltage, VOUT	2.25	2.4	2.6	V	Alternating ±zero µ-law PCM code applied to DR
V_{OUT2}	Output Voltage Swing, VOUT	3.25			Vp-p	R_L = 300 Ω
R_I	Input Resistance, VIN	40	50	60	kΩ	0.25 V < VIN < 4.75 V
R_O	Output Resistance VOUT			20	Ω	0 dBm0, 1020 Hz PCM code applied to DR.
R_L	Load Resistance, VOUT	300			Ω	External loading
I_I	Input Leakage Current, VIN	-1.0		1.0	µA	0.25 V < VIN < VDD -0.25 V
I_Z	Output Leakage Current, VOUT	-10		10	µA	Power down
C_L	Load Capacitance, VOUT			100	pF	External loading

TRANSMISSION CHARACTERISTICS

0 dBm0 is defined as 0.775 Vrms for A-law and 0.769 Vrms for μ-law, both for 600 Ω load. Unless otherwise noted, the analog input is a 0 dBm0, 1020 Hz sine wave; the input amplifier is set for unity gain. The digital input is a PCM bit stream equivalent to that obtained by passing a 0 dBm0, 1020 Hz sine wave through an ideal encoder. The output level is sin(x)/x-corrected. Typical values are for V_{DD} = 5V and T_A = 25°C.

Absolute Gain

Parameter	Description	Min	Typ	Max	Units	Test Conditions
G_{XA}	Transmit Gain, Absolute					Signal input of 0 dBm0, μ-law or A-law
	0°C to 85°C	-0.25		0.25	dB	
	-40°C	-0.30		0.30	dB	
G_{RA}	Receive Gain, Absolute					Measured relative to 0 dBm0, μ-law or A-law, PCM input of 0 dBm0 1020 Hz, R_L = 10 kΩ
	0°C to 85°C	-0.25		0.25	dB	
	-40°C	-0.30		0.30	dB	

Gain Tracking

Parameter	Description	Min	Typ	Max	Units	Test Conditions
GT_X	Transmit Gain Tracking					Tested by Sinusoidal Method, μ-law/A-law
	+3 dBm0 to –37 dBm0 (exclude –37 dBm0)	-0.25		0.25	dB	
	-37 dBm0 to -50 dBm0 (exclude –50 dBm0)	-0.50		0.50	dB	
	-50 dBm0 to -55 dBm0	-1.40		1.40	dB	
GT_R	Receive Gain Tracking					Tested by Sinusoidal Method, μ-law/A-law
	+3 dBm0 to - 40 dBm0 (exclude –40 dBm0)	-0.10		0.10	dB	
	-40 dBm0 to -50 dBm0 (exclude –50 dBm0)	-0.25		0.50	dB	
	-50 dBm0 to -55 dBm0	-0.50		0.50	dB	

Frequency Response

Parameter	Description	Min	Typ	Max	Units	Test Conditions
G_{XR}	Transmit Gain, Relative to G_{XA}					High-pass filter is enabled.
	f = 50 Hz			-30	dB	
	f = 60 Hz			-30	dB	
	f = 300 Hz	-0.10		0.20	dB	
	f = 300 Hz to 3000 Hz (exclude 3000 Hz)	-0.15		0.15	dB	
	f = 3000 Hz to 3400 Hz	-0.60		0.15	dB	
	f = 3600 Hz			-0.10	dB	
	f ≥ 4600 Hz			-35	dB	
G_{RR}	Receive Gain, Relative to G_{RA}					
	f < 300 Hz			0	dB	
	f = 300 Hz to 3000 Hz (exclude 3000 Hz)	-0.15		0.15	dB	
	f = 3000 Hz to 3400 Hz	-0.60		0.15	dB	
	f = 3600 Hz			-0.20	dB	
	f ≥ 4600 Hz			-35	dB	

Group Delay

Parameter	Description	Min	Typ	Max	Units	Test Conditions
D_{XR}	Transmit Delay, Relative to 1800 Hz					
	f = 500 Hz – 600 Hz			280	μs	
	f = 600 Hz –1000 Hz			150	μs	
	f = 1000 Hz – 2600 Hz			80	μs	
	f = 2600 Hz – 2800 Hz			280	μs	
D_{RR}	Receive Delay, Relative to 1800 Hz					
	f = 500 Hz – 600 Hz			50	μs	
	f = 600 Hz –1000 Hz			80	μs	
	f = 1000 Hz – 2600 Hz			120	μs	
	f = 2600 Hz – 2800 Hz			150	μs	

Distortion

Parameter	Description	Min	Typ	Max	Units	Test Conditions
STDX	Transmit Signal to Total Distortion Ratio A-law : Input level = 0 dBm0 Input level = -30 dBm0 Input level = -40 dBm0 Input level = -45 dBm0 μ-law : Input level = 0 dBm0 Input level = -30 dBm0 Input level = -40 dBm0 Input level = -45 dBm0	 36 36 30 24 36 36 31 27			 dB dB dB dB dB dB dB dB	ITU-T O.132 Sine Wave Method,Psophometric Weighted for A-law, C Message Weighted for μ-law.
STDR	Receive Signal to Total Distortion Ratio A-law : Input level = 0 dBm0 Input level = -30 dBm0 Input level = -40 dBm0 Input level = -45 dBm0 μ-law : Input level = 0 dBm0 Input level = -30 dBm0 Input level = -40 dBm0 Input level = -45 dBm0	 36 36 30 24 36 36 31 27			 dB dB dB dB dB dB dB dB	ITU-T O.132 Sine Wave Method,Psophometric Weighted for A-law;Sine Wave Method,C Message Weighted for μ-law;
SFDX	Single Frequency Distortion, Transmit			-42	dBm0	200 Hz - 3400 Hz, 0 dBm0 input, output any other single frequency ≤ 3400 Hz
SFDR	Single Frequency Distortion, Receive			-42	dBm0	200 Hz - 3400 Hz, 0 dBm0 input, output any other single frequency ≤ 3400 Hz
IMD	Intermodulation Distortion			-42	dBm0	Transmit or receive,two frequencies in the range (300 Hz– 3400 Hz) at –6 dBm0

Noise

Parameter	Description	Min	Typ	Max	Units	Test Conditions
NXC	Transmit Noise, C Message Weighted for μ-law			18	dBrnC0	
NXP	Transmit Noise, Psophometric Weighted for A-law			-68	dBm0p	
NRC	Receive Noise, C Message Weighted for μ-law			12	dBrnC0	
NRP	Receive Noise, Psophometric Weighted for A-law			-78	dBm0p	
NRS	Noise, Single Frequency f = 0 kHz – 100 kHz			-53	dBm0	VIN = 0 Vrms, tested at VOUT
PSRX	Power Supply Rejection Transmit f = 300 Hz – 3.4 kHz f = 3.4 kHz – 20 kHz	 40 25			 dB dB	VDD = 5.0 VDC + 100 mVrms
PSRR	Power Supply Rejection Receive f = 300 Hz – 3.4 kHz f = 3.4 kHz – 20 kHz	 40 25			 dB dB	PCM code is positive one LSB, VDD = 5.0 VDC + 100 mVrms
SOS	Spurious Out-of-Band Signals at VOUT Relative to Input PCM code applied: 4600 Hz – 20 kHz 20 kHz – 50 kHz			 -40 -30	 dB dB	0 dBm0, 300 Hz – 3400 Hz input

Interchannel Crosstalk

Parameter	Description	Min	Typ	Max	Units	Test Conditions
XTX-R	Transmit to Receive Crosstalk		-85	-78	dB	300 Hz – 3400 Hz, 0 dBm0 signal into VIN of interfering channel. Idle PCM code into channel under test.
XTR-X	Receive to Transmit Crosstalk		-85	-80	dB	300 Hz – 3400 Hz, 0 dBm0 PCM code into interfering channel. VIN = 0 Vrms for channel under test.
XTX-X	Transmit to Transmit Crosstalk		-85	-78	dB	300 Hz – 3400 Hz, 0 dBm0 signal into VIN of interfering channel. VIN = 0 Vrms for channel under test.
XTR-R	Receive to Receive Crosstalk		-85	-80	dB	300 Hz – 3400 Hz, 0 dBm0 PCM code into interfering channel. Idle PCM code into channel under test.

Note: Crosstalk into the transmit channels (VIN) can be significantly affected by parasitic capacitive coupling from VOUT outputs. PCB layouts should be arranged to minimize these parasitics.

Intrachannel Crosstalk

Parameter	Description	Min	Typ	Max	Units	Test Conditions
XT_{X-R}	Transmit to Receive Crosstalk		-80	-70	dB	300 Hz – 3400 Hz, 0 dBm0 signal into VIN. Idle PCM code into DR.
XT_{R-X}	Receive to Transmit Crosstalk		-80	-70	dB	300 Hz – 3400 Hz, 0 dBm0 PCM code into DR. VIN = 0 Vrms.

Note: Crosstalk into the transmit channels (VIN) can be significantly affected by parasitic capacitive coupling VOUT outputs. PCB layouts should be arranged to minimize these parasitics.

TIMING CHARACTERISTICS

Reset and Clock

Parameter	Description	Min	Typ	Max	Units	Test Conditions
t0	Reset pulse width	50			µs	
t1	CCLK period	122		100k	ns	
t2	CCLK pulse width	48			ns	
t3	CCLK Rise and Fall Time			25	ns	
t4	BCLK period	122			ns	
t5	BCLK pulse width	48			ns	
t6	BCLK Rise and Fall time			15	ns	
t7	MCLK pulse width	48			ns	
t8	MCLK Rise and Fall time			15	ns	
t9	DCL period F = 2.048 kHz F = 4.096 kHz		488 244		ns	
t10	DCL Rise and Fall Time			60	ns	
t11	DCL pulse width	90			ns	

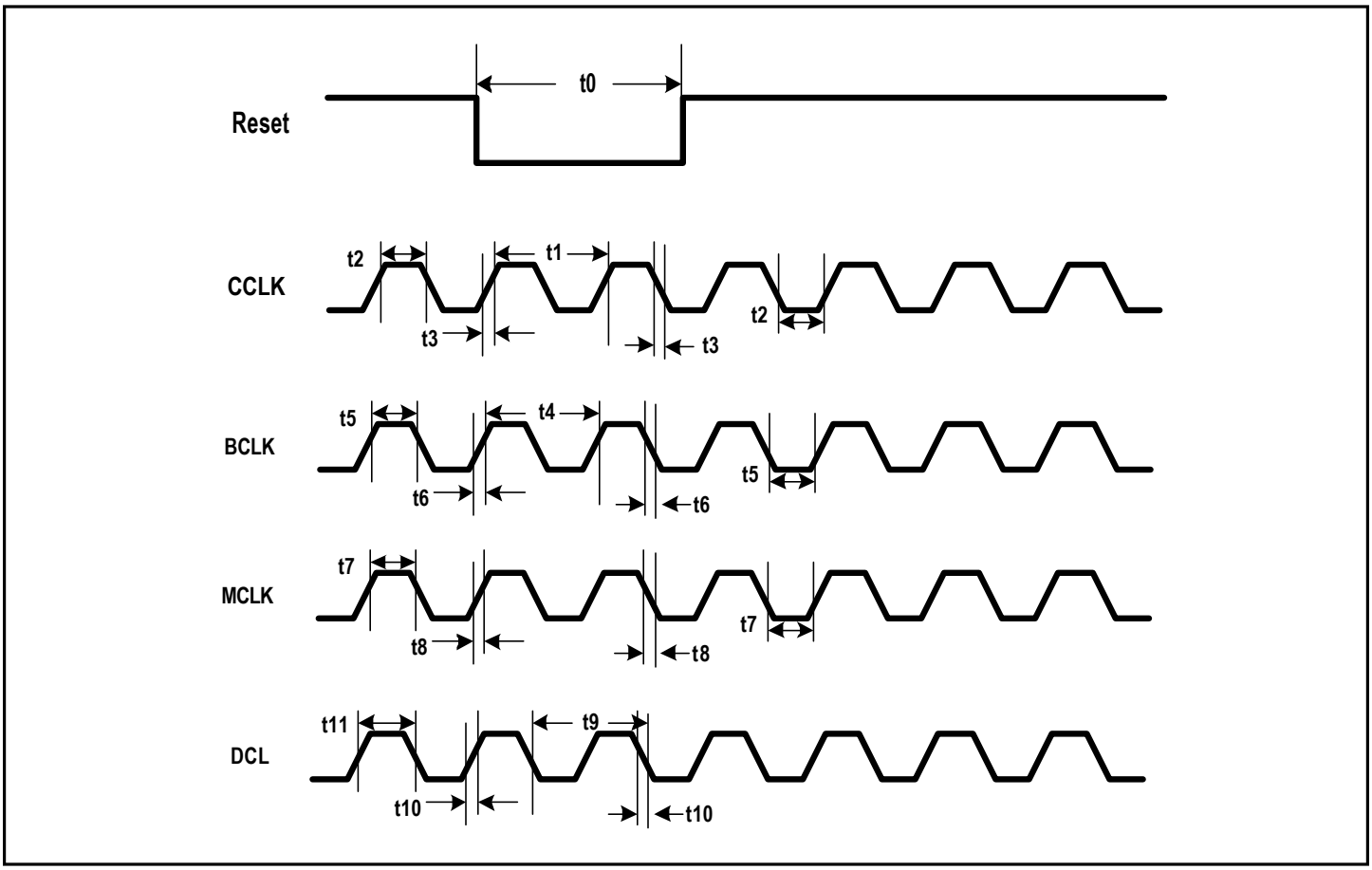


Figure 13. Reset and Clock Timing

Microprocessor Interface

Parameter	Description	Min	Typ	Max	Units	Test Conditions
t12	$\overline{CS}$ setup time	15			ns	
t13	$\overline{CS}$ pulse width		8n*t1 (n>=2)		ns	
t14	$\overline{CS}$ off time	250			ns	
t15	Input data setup time	30			ns	
t16	Input data hold time	30			ns	
t17	SLIC output latch valid			1000	ns	
t21	Output data turn on delay			50	ns	
t22	Output data hold time	0			ns	
t23	Output data turn off delay			50	ns	
t24	Output data valid	0		50	ns	

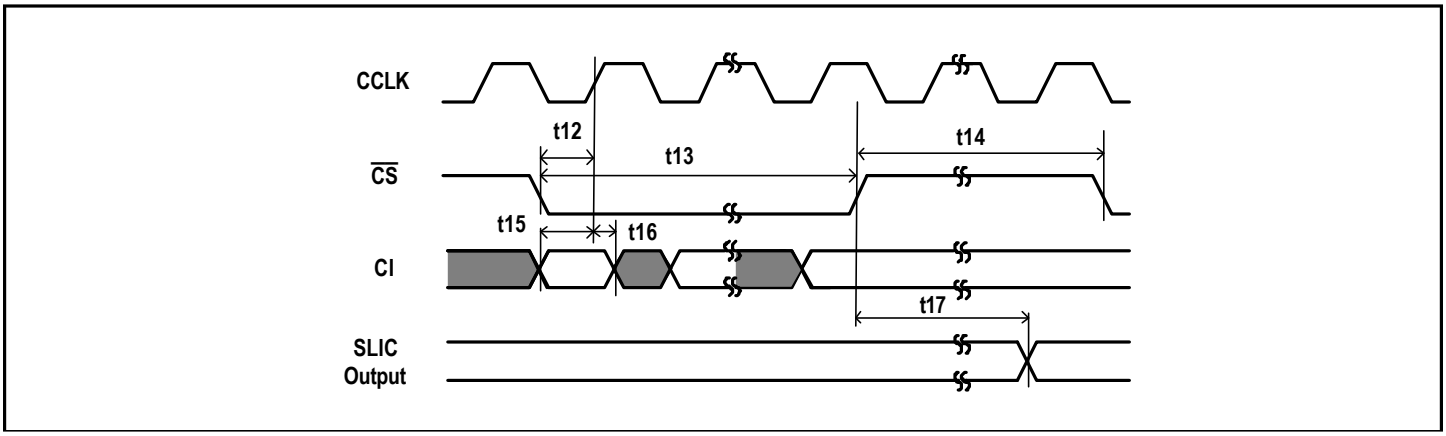


Figure 14. MPI Input Timing

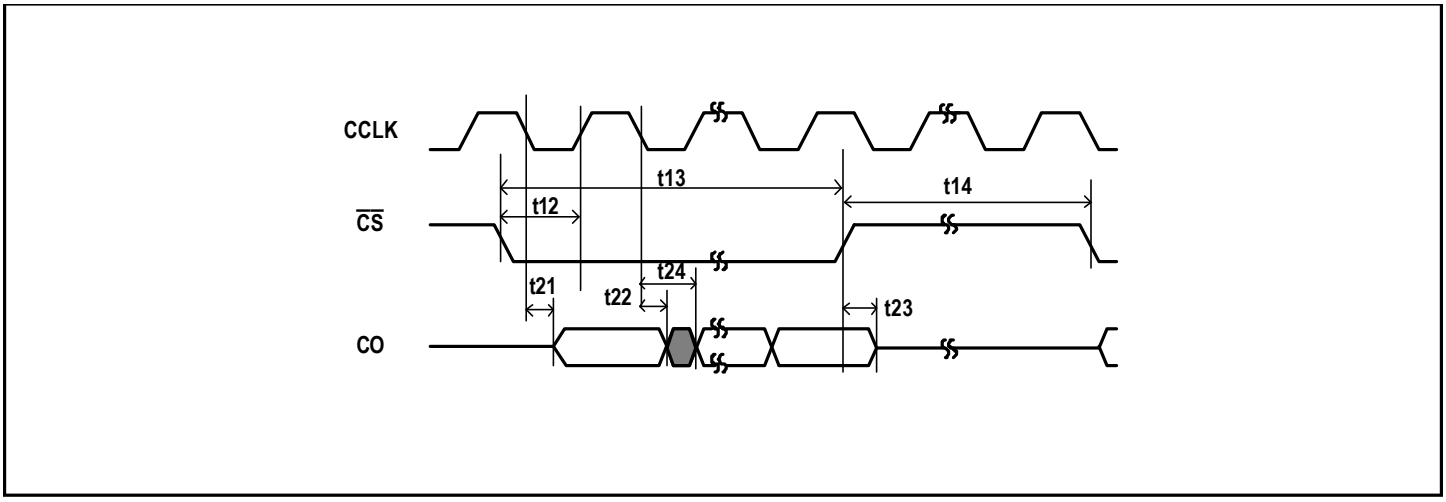


Figure 15. MPI Output Timing

PCM Interface

Parameter	Description	Min	Typ	Max	Units	Test Conditions
t51	Data enable delay time	5		70	ns	
t52	Data delay time from BCLK	5		70	ns	
t53	Data float delay time	5		70	ns	
t54	Frame sync setup time	25		t4 - 50	ns	
t55	Frame sync hold time	50			ns	
t56	$\overline{TSX}$ enable delay time	5		80	ns	
t57	$\overline{TSX}$ disable delay time	5		80	ns	
t61	Receive data setup time	25			ns	
t62	Receive data hold time	5			ns	

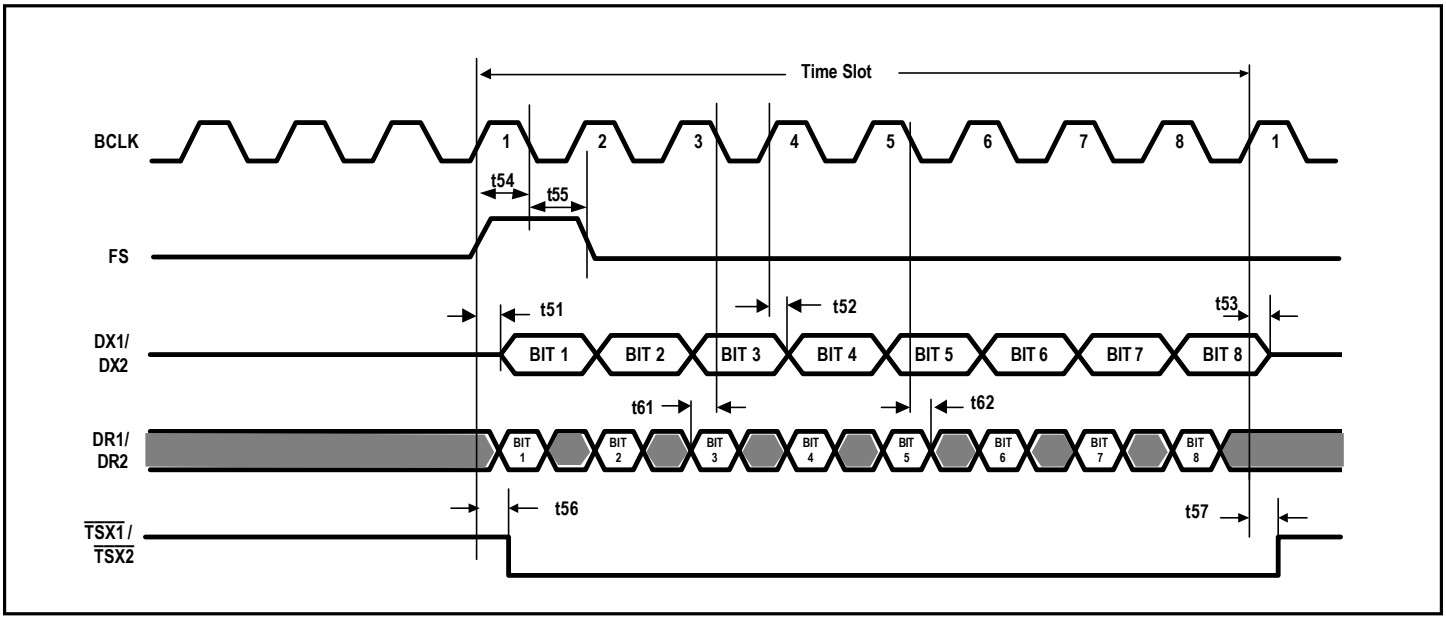


Figure 16. Transmit and Receive Timing *

Note*: These timing diagram only apply to the situation when data clock in on falling edges and clock out on rising edges.

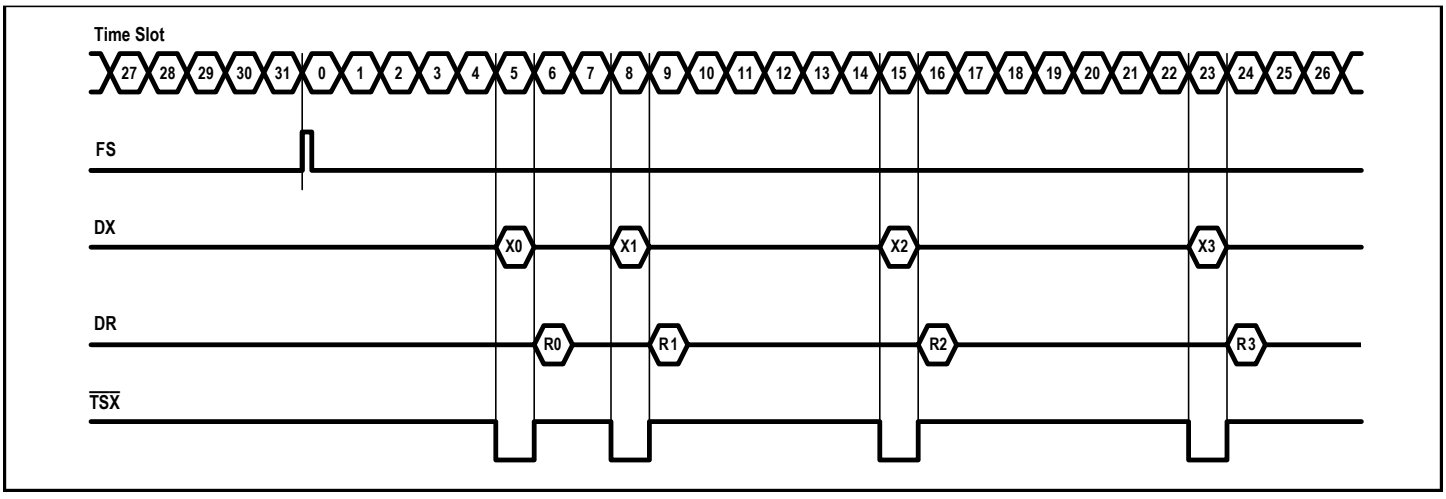


Figure 17. Typical Frame Sync Timing (2 MHz Operation)

GCI Interface

Parameter	Description	Min	Typ	Max	Units	Test Conditions
t71	FSC rise and fall time			60	ns	
t72	FSC setup time	70		t9 - 50	ns	
t73	FSC hold time	50			ns	
t74	FSC high pulse width	130			ns	
t75	DU data delay time			100	ns	
t77	DD data setup time	110			ns	
t78	DD data hold time	50			ns	

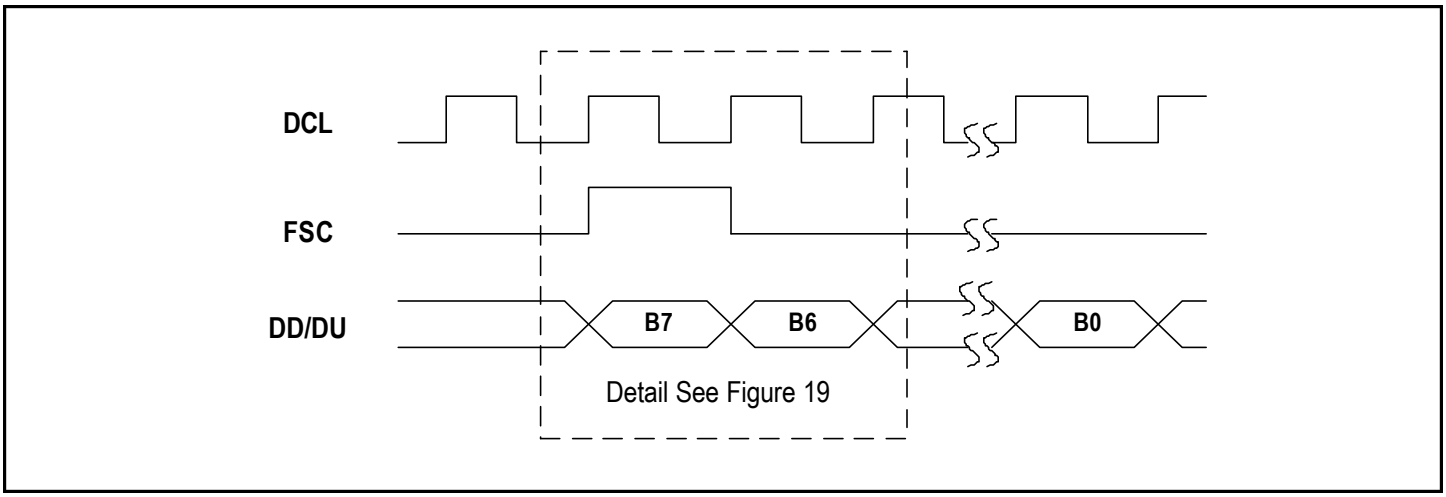
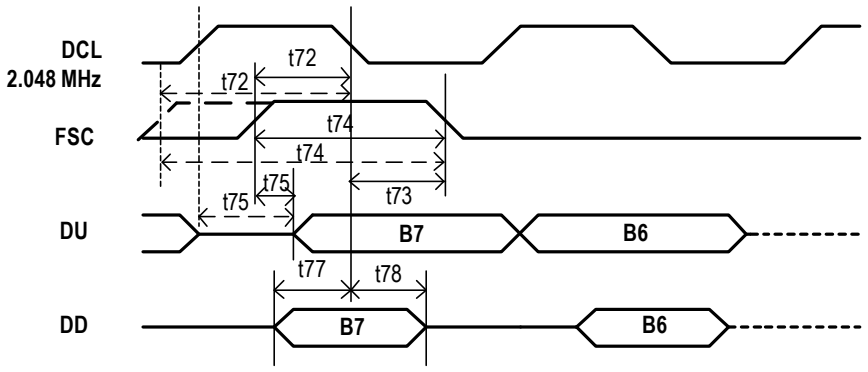
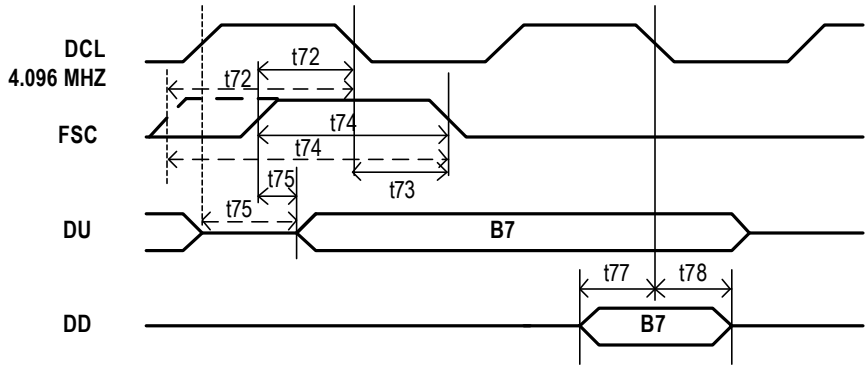


Figure 18. GCI Interface Timing



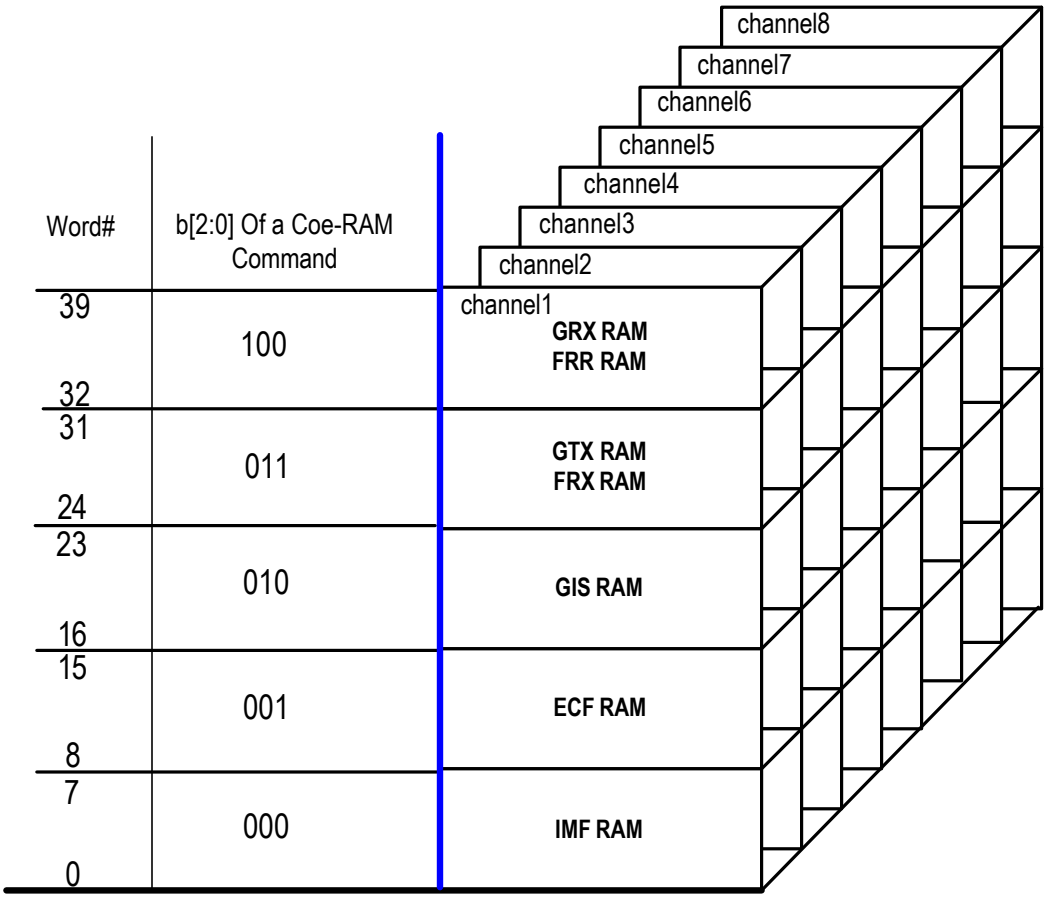
DCL Operation at 2.048 MHz



DCL Operation at 4.096 MHz

Figure 19. Transmit and Receive Timing for GCI Interface (Detail Timing for Figure 18)

APPENDIX I: IDT821068 Coe-RAM Address Mapping



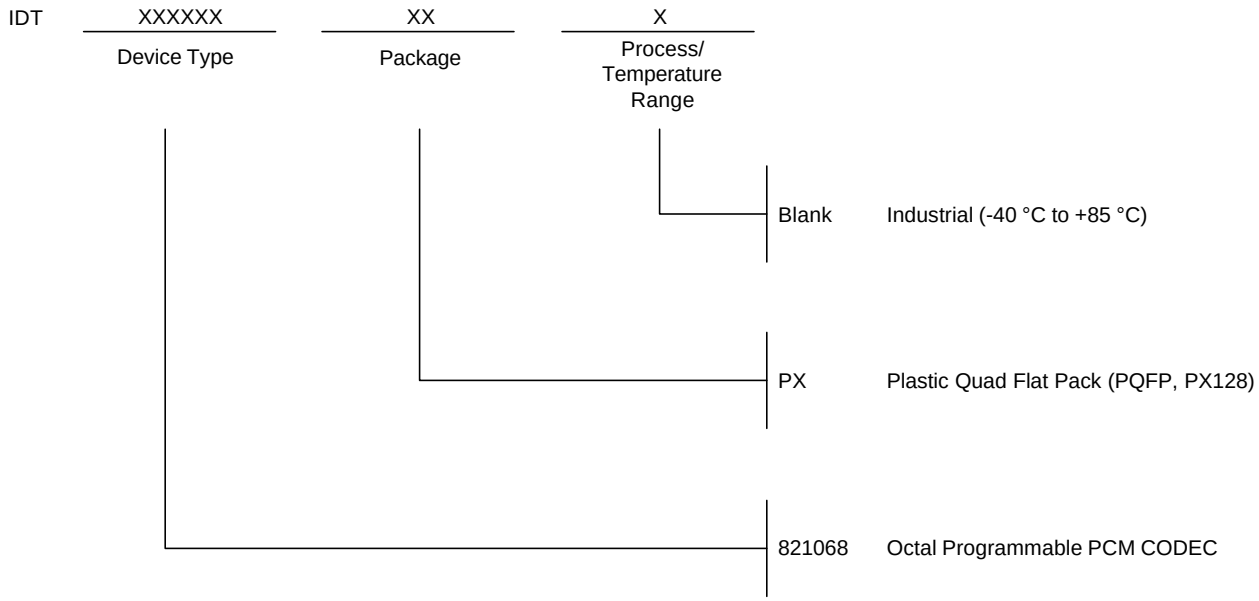
Generally, 6 bits of address are needed to locate each word of the 40 Coe-RAM words. The 40 words of Coe-RAM are divided into 5 blocks with 8 words per block in IDT821068, so only 3 bits of address are needed to locate each of the block. When the address of a Coe-RAM block (b[2:0]) is specified in a Coe-RAM Command, all 8 words of this block will be addressed automatically, with the highest order word first (IDT821068 will count down from '111' to '000' so that it accesses the 8 words successively). Refer to “Addressing the Coe-RAM” on Page 20 for more information.

The address assignment for the 40 words Coe-RAM is shown in the following table. The number in the “Address” column is the actual hexadecimal address of the Coe-RAM word, as the IDT821068 handles the lower 3 bits automatically, only the higher 3 bits (in bold style) are needed for a Coe-RAM Command. It should be noted that, when addressing the GRX RAM, the FRR RAM will be addressed at the same time.

Table 11 - Coe-RAM Address Allocation

Word #	Address	Function
39	**100**,111	GRX RAM
38	**100**,110	FRR RAM
37	**100**,101	
36	**100**,100	
35	**100**,011	
34	**100**,010	
33	**100**,001	
32	**100**,000	
31	**011**,111	GTX RAM
30	**011**,110	FRX RAM
29	**011**,101	
28	**011**,100	
27	**011**,011	
26	**011**,010	
25	**011**,001	
24	**011**,000	
23	**010**,111	GIS RAM
22	**010**,110	
21	**010**,101	
20	**010**,100	
19	**010**,011	
18	**010**,010	
17	**010**,001	
16	**010**,000	
15	**001**,111	ECF RAM
14	**001**,110	
13	**001**,101	
12	**001**,100	
11	**001**,011	
10	**001**,010	
9	**001**,001	
8	**001**,000	
7	**000**,111	IMF RAM
6	**000**,110	
5	**000**,101	
4	**000**,100	
3	**000**,011	
2	**000**,010	
1	**000**,001	
0	**000**,000	

ORDERING INFORMATION



Data Sheet Document History

01/31/2002	pgs. 1, 2, 5, 12, 15, 33
02/19/2002	pg. 35
01/10/2003	pg. 44
12/08/2003	pgs. 28, 29, 32, 35, 38

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