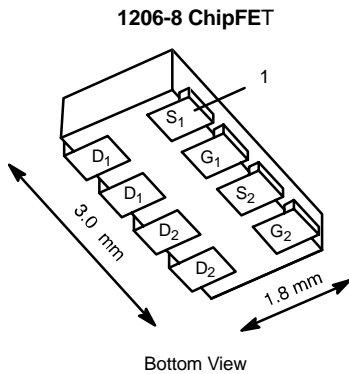


Complementary 30-V (D-S) MOSFET

PRODUCT SUMMARY			
	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
N-Channel	30	0.085 @ $V_{GS} = 10$ V	± 3.9
		0.143 @ $V_{GS} = 4.5$ V	± 3.0
P-Channel	-30	0.165 @ $V_{GS} = -10$ V	± 2.8
		0.290 @ $V_{GS} = -4.5$ V	± 2.1

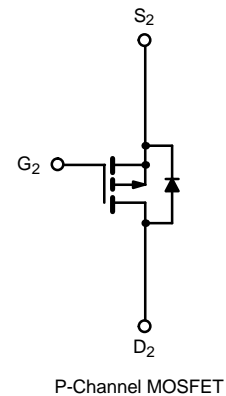
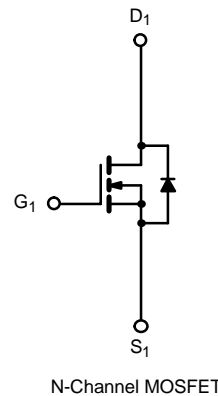
TrenchFET[®]
Power MOSFETs



Marking Code

EA	XX
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 Lot Traceability and Date Code
 Part # Code



Ordering Information: Si5504DC-T1

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	N-Channel		P-Channel		Unit
		5 secs	Steady State	5 secs	Steady State	
Drain-Source Voltage	V_{DS}	30		-30		V
Gate-Source Voltage	V_{GS}	± 20				
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	$T_A = 25^\circ\text{C}$	± 3.9	± 2.9	± 2.8	± 2.1	A
	$T_A = 85^\circ\text{C}$	± 2.8	± 2.1	± 2.0	± 1.5	
Pulsed Drain Current	I_{DM}	± 10				
Continuous Source Current (Diode Conduction) ^a	I_S	1.8	0.9	-1.8	-0.9	
Maximum Power Dissipation ^a	$T_A = 25^\circ\text{C}$	2.1	1.1	2.1	1.1	W
	$T_A = 85^\circ\text{C}$	1.1	0.6	1.1	0.6	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150				$^\circ\text{C}$
Soldering Recommendations (Peak Temperature) ^{b, c}		260				

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	$t \leq 5$ sec	R_{thJA}	50	60	$^\circ\text{C/W}$
	Steady State		90	110	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	30	40	

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- See Reliability Manual for profile. The ChipFET/PowerPAK is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)							
Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Static							
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	1.0			V
		V _{DS} = V _{GS} , I _D = -250 μA	P-Ch	-1.0			
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V	N-Ch			±100	nA
			P-Ch			±100	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 24 V, V _{GS} = 0 V	N-Ch			1	μA
		V _{DS} = -24 V, V _{GS} = 0 V	P-Ch			-1	
		V _{DS} = 24 V, V _{GS} = 0 V, T _J = 85 °C	N-Ch			5	
		V _{DS} = -24 V, V _{GS} = 0 V, T _J = 85 °C	P-Ch			-5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	N-Ch	10			A
		V _{DS} ≤ -5 V, V _{GS} = -10 V	P-Ch	-10			
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 2.9 A	N-Ch		0.072	0.085	Ω
		V _{GS} = -10 V, I _D = -2.1 A	P-Ch		0.137	0.165	
		V _{GS} = 4.5 V, I _D = 2.2 A	N-Ch		0.120	0.143	
		V _{GS} = -4.5 V, I _D = -1.6 A	P-Ch		0.240	0.290	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 2.9 A	N-Ch		6		S
		V _{DS} = -15 V, I _D = -2.1 A	P-Ch		3		
Diode Forward Voltage ^a	V _{SD}	I _S = 0.9 A, V _{GS} = 0 V	N-Ch		0.8	1.2	V
		I _S = -0.9 A, V _{GS} = 0 V	P-Ch		-0.8	-1.2	
Dynamic^b							
Total Gate Charge	Q _g	N-Channel V _{DS} = 15 V, V _{GS} = 10 V, I _D = 2.9 A P-Channel V _{DS} = -15 V, V _{GS} = -10 V, I _D = -2.1 A	N-Ch		5	7.5	nC
			P-Ch		5.5	6.6	
Gate-Source Charge	Q _{gs}		N-Ch		0.8		
			P-Ch		1.2		
Gate-Drain Charge	Q _{gd}		N-Ch		1.0		
			P-Ch		0.9		
Turn-On Delay Time	t _{d(on)}	N-Channel V _{DD} = 15 V, R _L = 15 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _G = 6 Ω P-Channel V _{DD} = -15 V, R _L = 15 Ω I _D ≅ -1 A, V _{GEN} = -10 V, R _G = 6 Ω	N-Ch		7	11	ns
			P-Ch		8	12	
Rise Time	t _r		N-Ch		12	18	
			P-Ch		11	18	
Turn-Off Delay Time	t _{d(off)}		N-Ch		12	18	
			P-Ch		14	21	
Fall Time	t _f		N-Ch		7	11	
			P-Ch		8	12	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 0.9 A, di/dt = 100 A/μs	N-Ch		40	80	
		I _F = -0.9 A, di/dt = 100 A/μs	P-Ch		40	80	

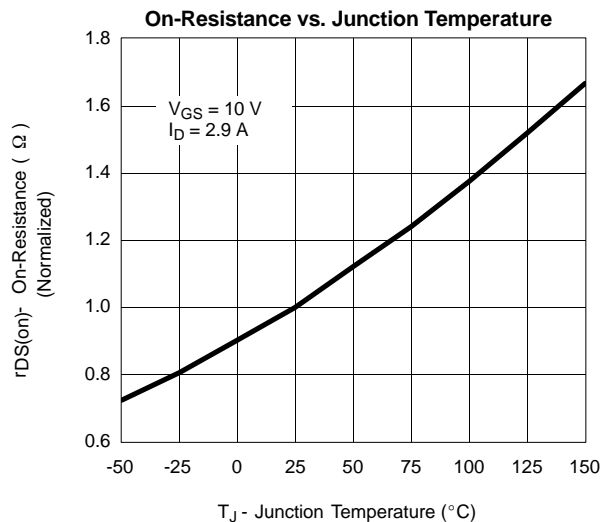
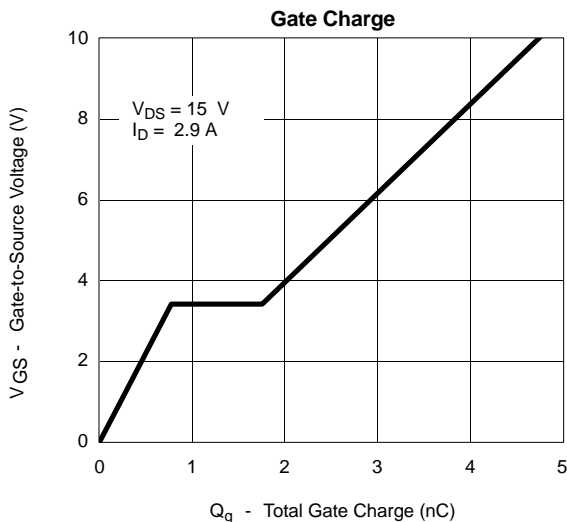
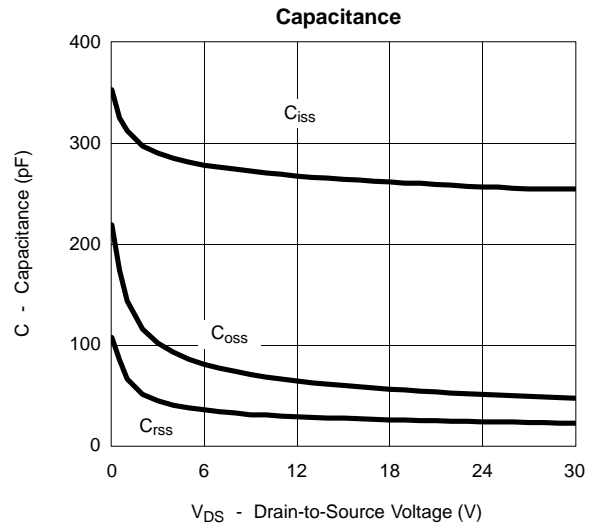
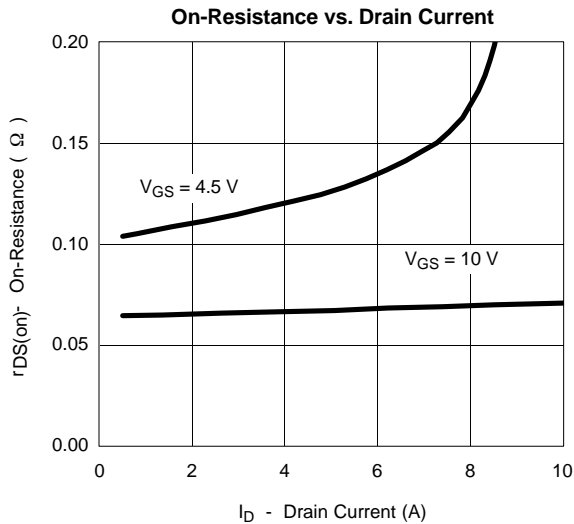
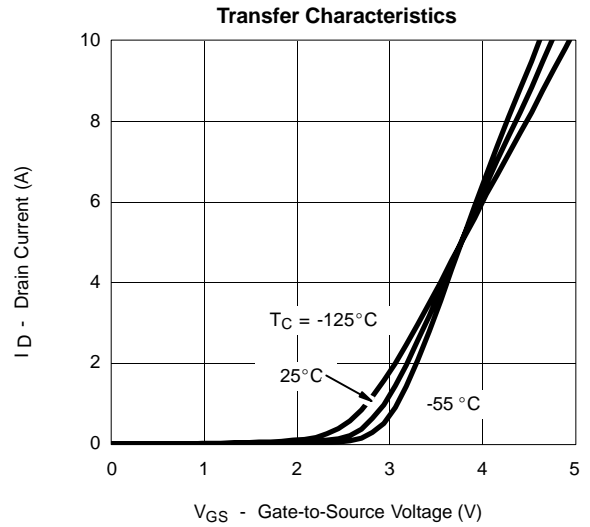
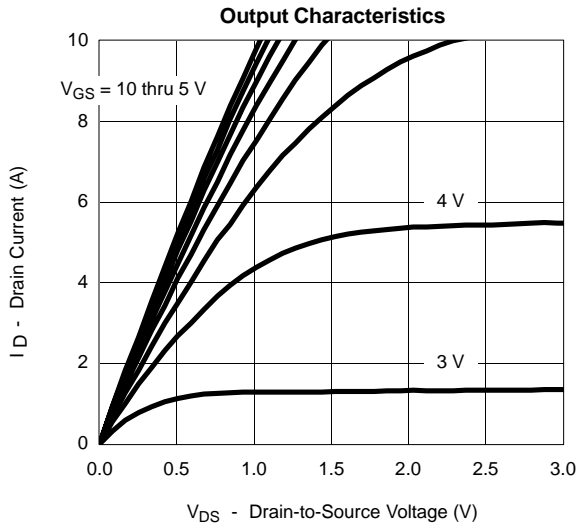
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%,
b. Guaranteed by design, not subject to production testing.

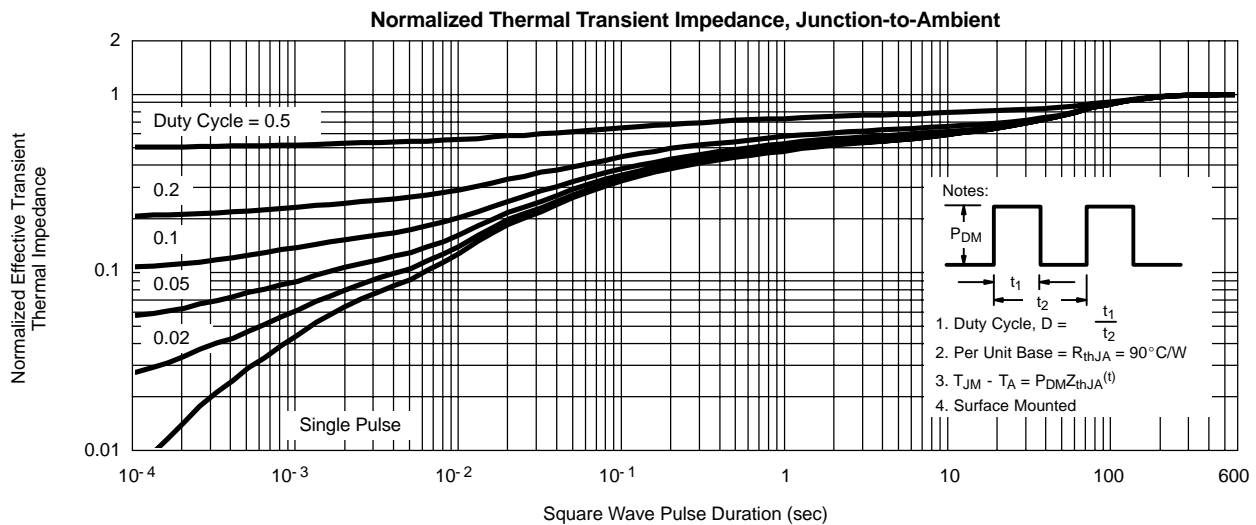
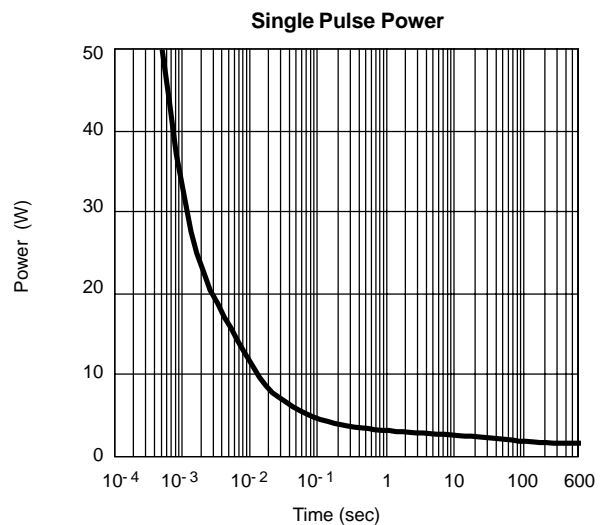
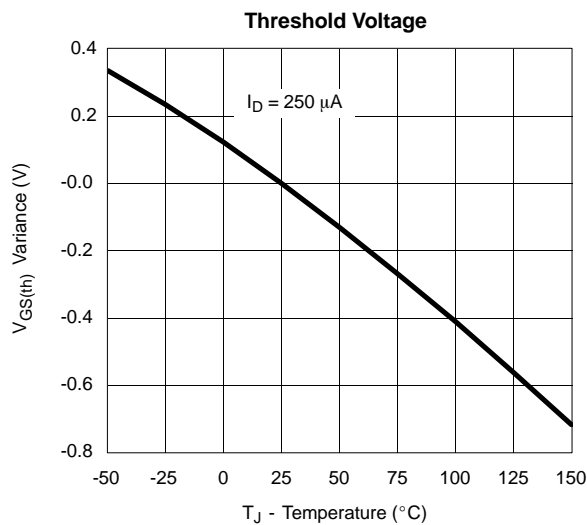
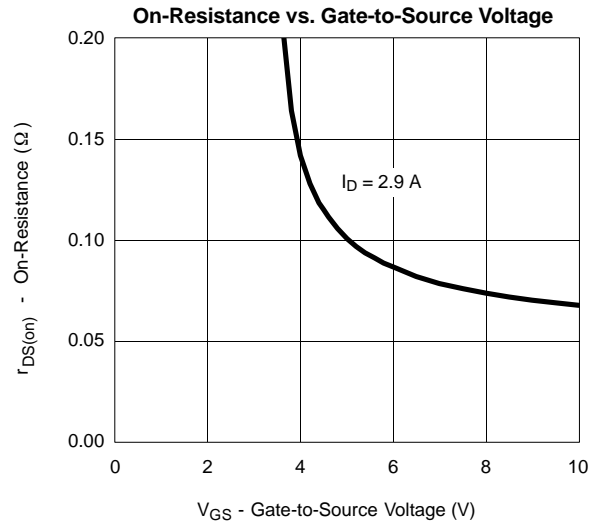
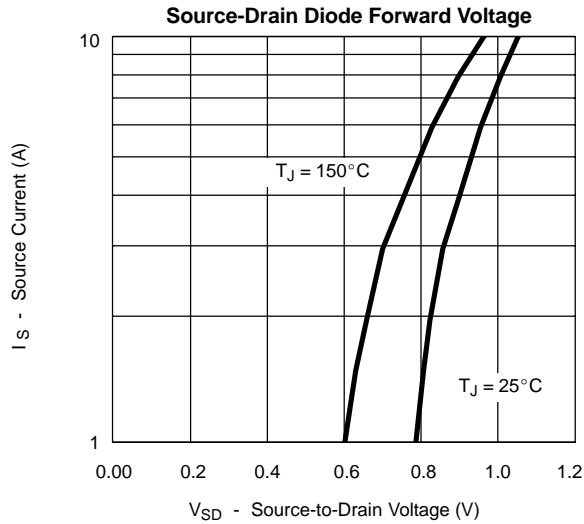


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

N-CHANNEL



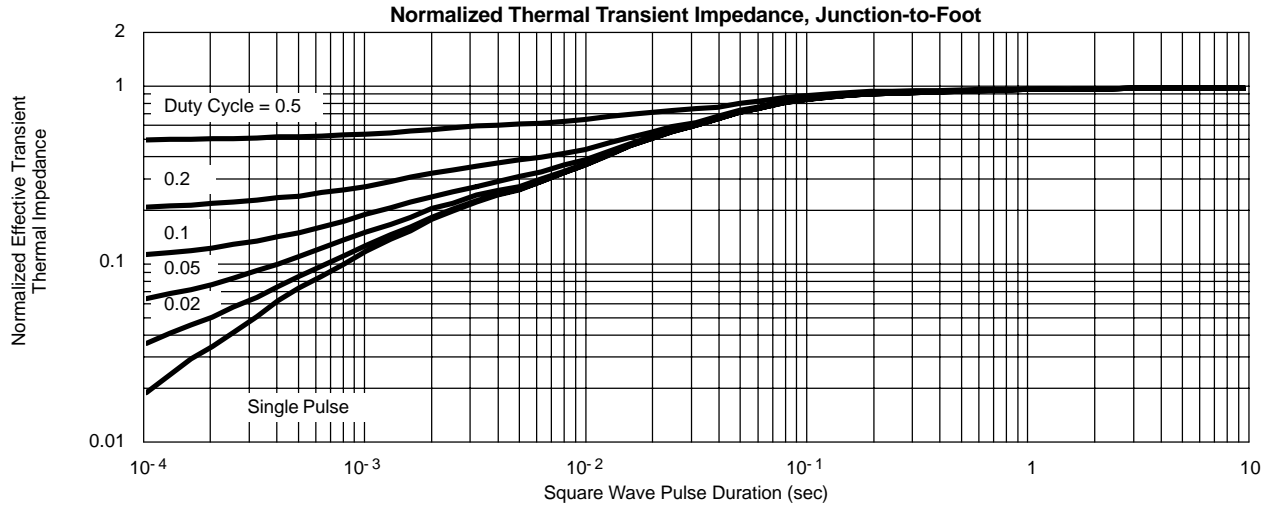
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED) N-CHANNEL





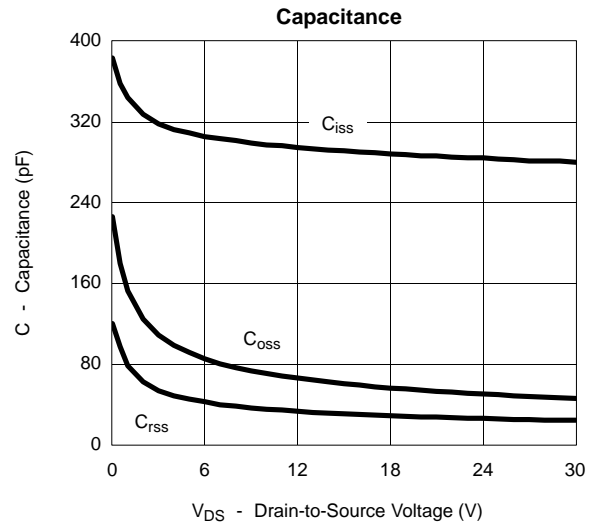
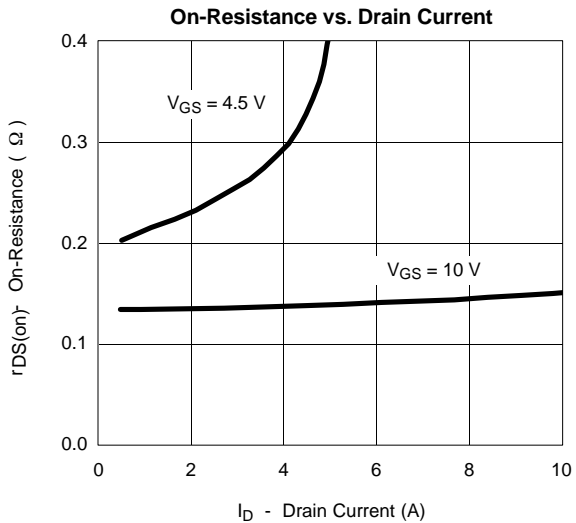
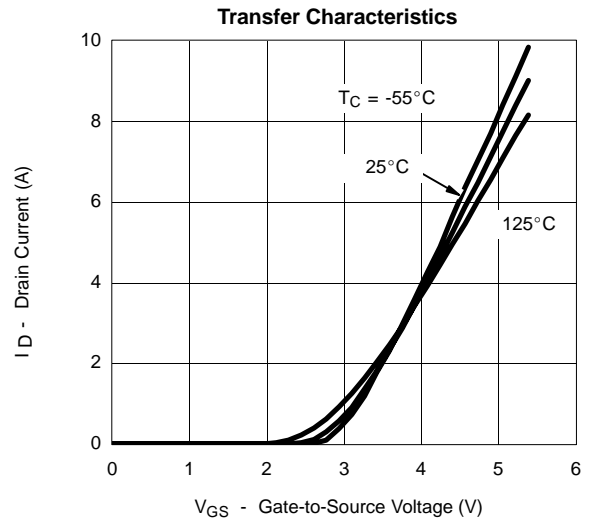
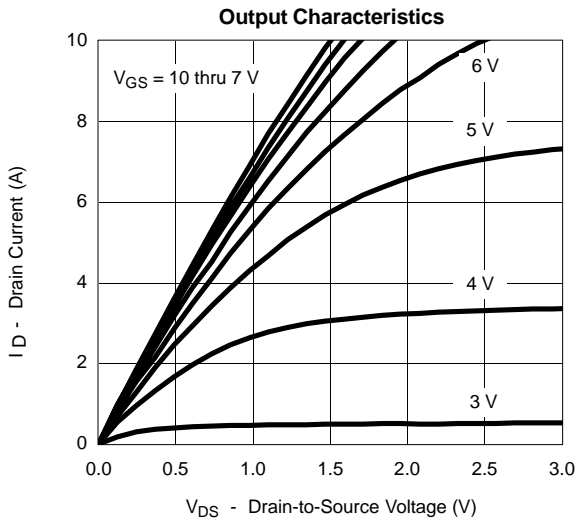
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

N-CHANNEL

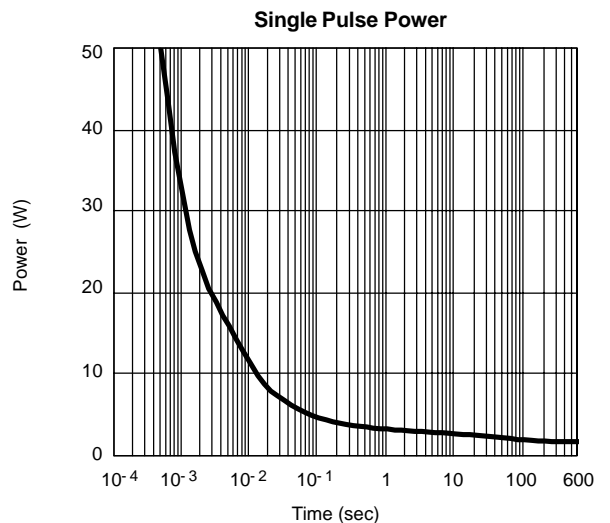
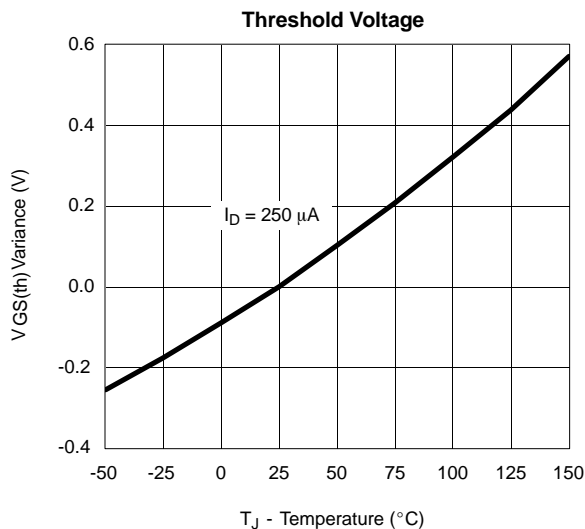
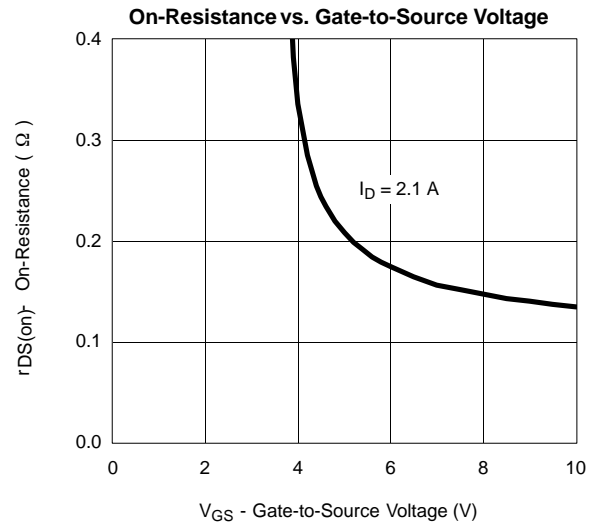
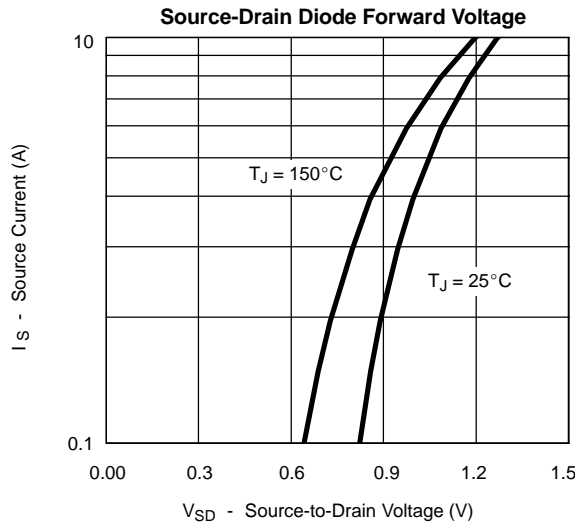
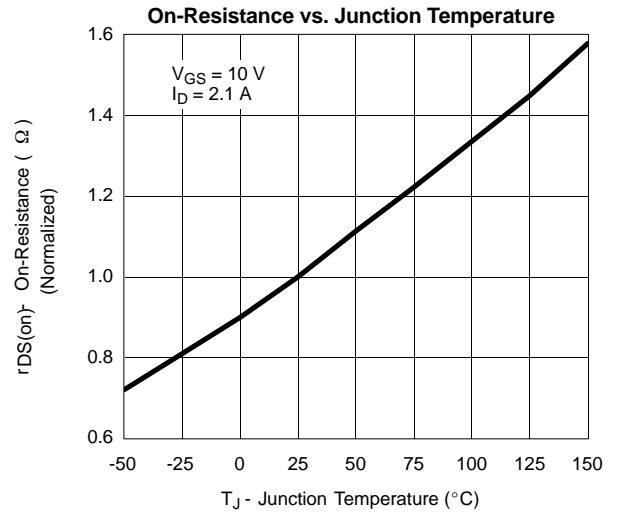
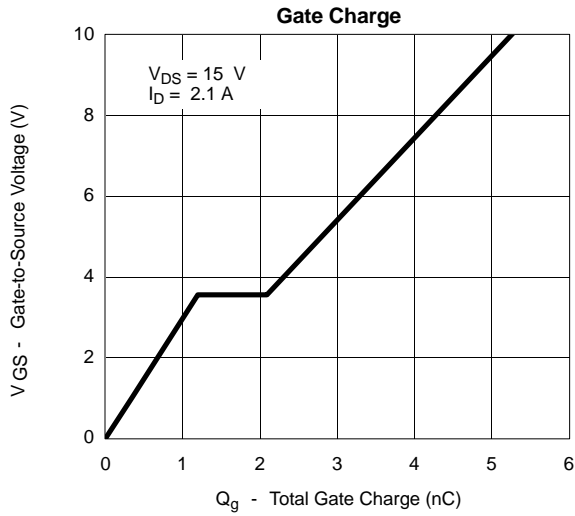


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

P-CHANNEL



TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED) P-CHANNEL





TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) P-CHANNEL

