# M37705M2AXXXSP
# M37705S1ASP

## SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

M37705M2-XXXSP and M37705S1SP
are respectively unified into
M37705M2AXXXSP and M37705S1ASP

## DESCRIPTION

The M37705M2AXXXSP and M37705S1ASP are single-chip microcomputers designed with high-performance CMOS silicon gate technology. These are housed in a 64-pin shrink plastic molded DIP. These single-chip microcomputers have a large 16M bytes address space, three instruction queue buffers, and two data buffers for high-speed instruction execution. The CPU is a 16-bit parallel processor that can also be switched to perform 8-bit parallel processing. These microcomputers are suitable for office, business and industrial equipment controller that require high-speed processing of large data.

Also, the incorporated motor control circuit makes these microcomputers suitable for control of equipment that requires motor control.

The differences between M37705M2AXXXSP and M37705S1 ASP are the ROM size as shown below. Therefore, the following descriptions will be for the M37705M2AXXXFP unless otherwise noted.

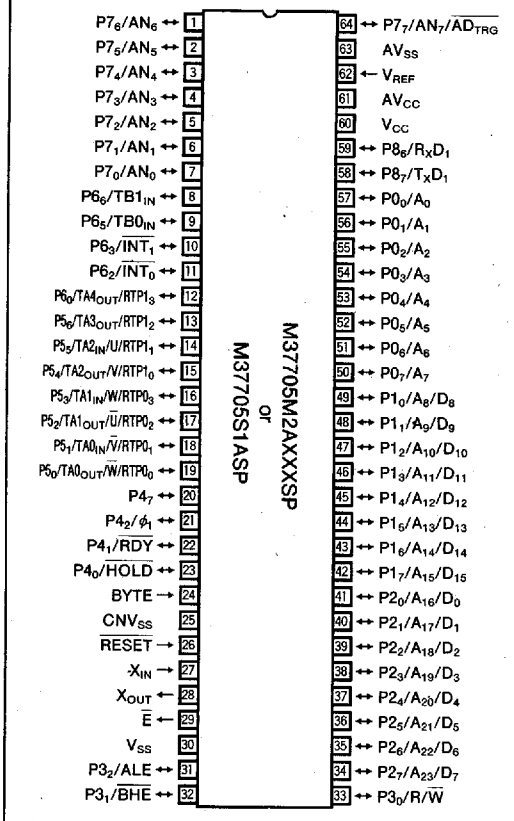
| Type name | ROM size | External clock input frequency |
|---|---|---|
| M37705M2AXXXSP | 16K bytes | 16MHz |
| M37705S1ASP | External | 16MHz |

The M37705M2AXXXSP cuts down the pins of M37704M2A XXXFP. Refer to the BASIC FUNCTION BLOCKS for the functional differences.

## DISTINCTIVE FEATURES

- Number of basic instructions ..... 103
- Memory size ROM ..... 16K bytes
  RAM ..... 512 bytes
- Instruction execution time
  The fastest instruction at 16 MHz frequency ..... 250ns
- Single power supply ..... 5V±10%
- Low power dissipation (at 16 MHz frequency) ..... 60mW (Typ.)
- Interrupts ..... 16 types 7 levels
- Multiple function 16-bit timer ..... 5+3
  (Three-phase motor drive waveform or pulse motor drive waveform can be output.)
- UART ..... 1
- 8-bit A-D converter ..... 8-channel inputs
- 12-bit watchdog timer
- Programmable input/output
  (ports P0, P1, P2, P3, P4, P5, P6, P7, P8) ..... 53

## PIN CONFIGURATION (TOP VIEW)




Outline 64P4B

## APPLICATION

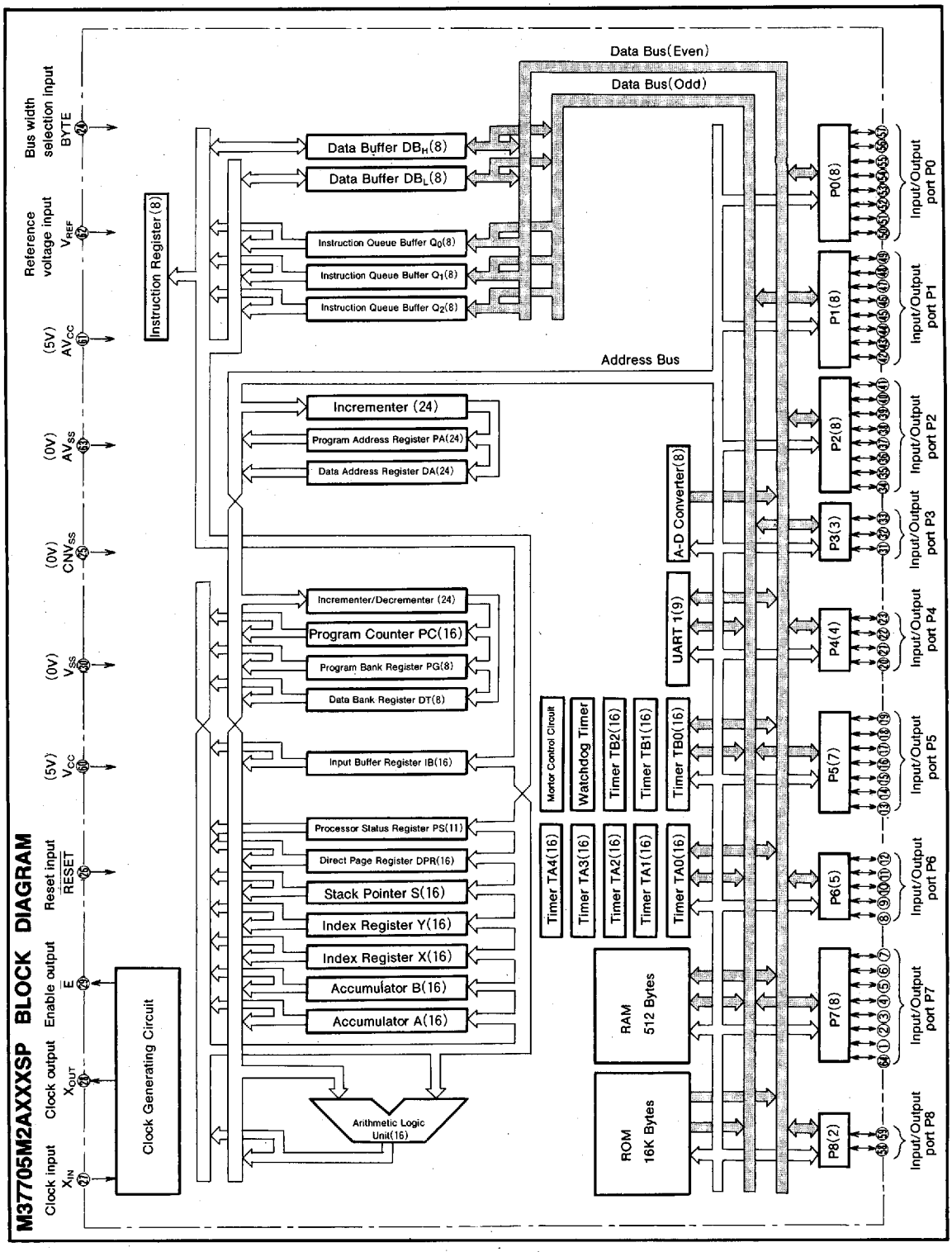
Motor control devices such as inverter type air conditioners and general purpose inverters

Control devices for office equipment such as copiers, printers, typewriters, facsimiles, word processors, and personal computers

## NOTE

Refer to "Chapter 5 PRECAUTIONS" when using this microcomputer.

The M37705M2AXXXSP and M37705S1ASP satisfy the timing requirements and the switching characteristics of the former M37705M2-XXXSP and M37705S1SP


M37705M2AXXSP BLOCK DIAGRAM
Clock input
Clock output
Enable output
Reset input
Bus width selection input
Reference voltage input
(5V)
(0V)
Data Bus(Even)
Data Bus(Odd)
Address Bus
Data Buffer DBH(8)
Data Buffer DBL(8)
Instruction Register(8)
Instruction Queue Buffer Q0(8)
Instruction Queue Buffer Q1(8)
Instruction Queue Buffer Q2(8)
Incrementer (24)
Program Address Register PA(24)
Data Address Register DA(24)
Incrementer/Decrementer (24)
Program Counter PC(16)
Program Bank Register PG(8)
Data Bank Register DT(8)
Input Buffer Register IB(16)
Processor Status Register PS(11)
Direct Page Register DPR(16)
Stack Pointer S(16)
Index Register Y(16)
Index Register X(16)
Accumulator B(16)
Accumulator A(16)
Arithmetic Logic Unit(16)
Clock Generating Circuit
RAM 512 Bytes
ROM 16K Bytes
A-D Converter(8)
UART 1(9)
Motor Control Circuit
Watchdog Timer
Timer TB2(16)
Timer TB1(16)
Timer TB0(16)
Timer TA4(16)
Timer TA3(16)
Timer TA2(16)
Timer TA1(16)
Timer TA0(16)
P0(8)
P1(8)
P2(8)
P3(3)
P4(4)
P5(7)
P6(5)
P7(8)
P8(2)
Input/Output port P0
Input/Output port P1
Input/Output port P2
Input/Output port P3
Input/Output port P4
Input/Output port P5
Input/Output port P6
Input/Output port P7
Input/Output port P8

## FUNCTIONS OF M37705M2AXXXSP

| Parameter | | Functions |
|---|---|---|
| Number of basic instructions | | 103 |
| Instruction execution time | M37705M2AXXXSP, M37705S1ASP | 250ns (the fastest instruction at external clock 16MHz frequency) |
| Memory size | ROM | 16K bytes |
| | RAM | 512 bytes |
| Input/Output ports | P0, P1, P2, P7 | 8-bit× 4 |
| | P5 | 7-bit× 1 |
| | P6 | 5-bit× 1 |
| | P4 | 4-bit× 1 |
| | P3 | 3-bit× 1 |
| | P8 | 2-bit× 1 |
| Multi-function timers | TA0, TA1, TA2, TA3, TA4 | 16-bit× 5 (3 input/output and 2 output functions) |
| | TB0, TB1, TB2 | 16-bit× 3 (2 input functions) |
| Serial I/O | | UART ×1 |
| A-D converter | | 8-bit× 1 ( 8 channels) |
| Watchdog timer | | 12-bit× 1 |
| Dead-time timer | | 8-bit× 3 |
| Interrupts | | 2 external types, 14 internal types<br>(Each interrupt can be set the priority levels to 0 ~ 7.) |
| Clock generating circuit | | Built-in(externally connected to a ceramic resonator or quartz crystal resonator) |
| Supply voltage | | 5 V±10% |
| Power dissipation | | 60mW(at external clock 16MHz frequency) |
| Input/Output characteristic | Input/Output voltage | 5 V |
| | Output current | 5 mA |
| Memory expansion | | Maximum 16M bytes |
| Operating temperature range | | −20~85℃ |
| Device structure | | CMOS high-performance silicon gate process |
| Package | | 64-pin shrink plastic molded DIP |

## PIN DESCRIPTION

| Pin | Name | Input/Output | Functions |
|---|---|---|---|
| $V_{CC}$, $V_{SS}$ | Power supply | | Supply 5 V±10% to $V_{CC}$ and 0 V to $V_{SS}$. |
| $CNV_{SS}$ | $CNV_{SS}$ input | Input | This pin controls the processor mode. Connect to $V_{SS}$ for single-chip mode, and to $V_{CC}$ for external ROM types. |
| $\overline{RESET}$ | Reset input | Input | To enter the reset state, this pin must be kept at a "L" condition which should be maintained for the required time. |
| $X_{IN}$ | Clock input | Input | These are I/O pins of internal clock generating circuit. Connect a ceramic or quartz crystal resonator between $X_{IN}$ and $X_{OUT}$. When an external clock is used, the clock source should be connected to the $X_{IN}$ pin and the $X_{OUT}$ pin should be left open. |
| $X_{OUT}$ | Clock output | Output | |
| $\overline{E}$ | Enable output | Output | Data or instruction read and data write are performed when output from this pin is "L". |
| BYTE | Bus width selection input | Input | In memory expansion mode or microprocessor mode, this pin determines whether the external data bus is 8-bit width or 16-bit width. The width is 16 bits when "L" signal inputs and 8 bits when "H" signal inputs. |
| $AV_{CC}$, $AV_{SS}$ | Analog supply input | | Power supply for the A-D converter. Connect $AV_{CC}$ to $V_{CC}$ and $AV_{SS}$ to $V_{SS}$ externally. |
| $V_{REF}$ | Reference voltage input | Input | This is reference voltage input pin for the A-D converter. |
| $P0_0$~$P0_7$ | I/O port P0 | I/O | In single-chip mode, port P0 becomes an 8-bit I/O port. An I/O directional register is available so that each pin can be programmed for input or output. These ports are in input mode when reset . Address($A_7$~$A_0$)is output in memory expansion mode or microprocessor mode. |
| $P1_0$~$P1_7$ | I/O port P1 | I/O | In single-chip mode, these pins have the same functions as port P0. When the BYTE pin is set to "L" in memory expansion mode or microprocessor mode and external data bus is 16-bit width, high-order data ($D_{15}$~$D_8$)is input or output when $\overline{E}$ output is "L" and an address ($A_{15}$~$A_8$) is output when $\overline{E}$ output is "H". If the BYTE pin is "H" that is an external data bus is 8-bit width, only address($A_{15}$~$A_8$)is output. |
| $P2_0$~$P2_7$ | I/O port P2 | I/O | In single-chip mode, these pins have the same functions as port P0. In memory expansion mode or microprocessor mode low-order data($D_7$~$D_0$) is input or output when $\overline{E}$ output is "L" and an address($A_{23}$~$A_{16}$)is output when $\overline{E}$ output is "H". |
| $P3_0$~$P3_2$ | I/O port P3 | I/O | In single-chip mode , these pins have the same functions as port P0. In memory expansion mode or microprocessor mode, R/$\overline{W}$, $\overline{BHE}$, and ALE signals are output. |
| $P4_0$~$P4_2$, $P4_7$ | I/O port P4 | I/O | In single-chip mode, these pins have the same functions as port P0. In memory expansion mode or microprocessor mode, $P4_0$ and $P4_1$ become $\overline{HOLD}$ and $\overline{RDY}$ input pin respectively. Functions of other pins are the same as in single-chip mode. In single-chip mode or memory expansion mode, port $P4_2$ can be programmed for $\phi_1$ output pin divided the clock to $X_{IN}$ pin by 2. In microprocessor mode, $P4_2$ always has the function as $\phi_1$ output pin. |
| $P5_0$~$P5_6$ | I/O port P5 | I/O | In addition to having the same functions as port P0 in single-chip mode, these pins also function as I/O pins for timer A0, timer A1, timer A2 and output pin for timer A3. These pins also have the function as motor control output pin. |
| $P6_0$, $P6_2$, $P6_3$, $P6_5$, $P6_6$ | I/O port P6 | I/O | In addition to having the same functions as port P0 in single-chip mode, these pins also function as output pins for timer A4, and input pins for external interrupt input $\overline{INT_0}$ and $\overline{INT_1}$ pins, and for timer B0 and timer B1. $P6_0$ also has the function as motor control output pin and $P6_2$ has the function as motor control pin. |
| $P7_0$~$P7_7$ | I/O port P7 | I/O | In addition to having the same functions as port P0 in single-chip mode, these pins also function as analog input $AN_0$~$AN_7$ input pins. $P7_7$ also has an A-D conversion trigger input function. |
| $P8_6$, $P8_7$ | I/O port P8 | I/O | In addition to having the same functions as port P0 in single-chip mode, these pins also function as $R_XD$ and $T_XD$ pins for UART 1. |

# M37705M2AXXXSP
# M37705S1ASP

## SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

## BASIC FUNCTION BLOCKS

The functional differences between the M37705M2AXXXSP and M37704M2AXXXFP are described below. The M37705M2AXXXSP has the same functions as the M37704M2AXXXFP, except these points. Refer to the section on the M37704M2AXXXFP.

## TIMER

Since timers A3 and A4 have no input pin, timers A3 and A4 operate only in the modes except for event counter mode and select only no input function by timer A3 and timer A4 mode register.

Since timer B2 has no input pin, timer B2 operates only in timer mode. Therefore, only clock source can be selected by the bits 7 and 6 of timer B2 mode register. The bits of timer mode register must be "0" except for the clock source selection bits. Other timers A0, A1, A2, B0 and B1 have the same functions as the M37704M2AXXXFP.

## SERIAL I/O

Serial I/O is only UART1. UART1 has only the asynchronous serial communication function and no clock synchronous serial communication function. Therefore, do not select the clock synchronous serial communication function ("001") by the serial communication method selection bits (bits 2, 1 and 0) of UART1 transmit/receive mode register. Since UART1 does not have the functions of $\overline{CTS}$ and $\overline{RTS}$, the $\overline{CTS}$, $\overline{RTS}$ selection bit (bit 2) of UART1 transmit/receive control register must always be "1".

Since UART0 has no function as serial I/O, set all the serial communication method selection bits (bits 2, 1 and 0) of UART0 transmit/receive mode register to "0".

## INPUT/OUTPUT PINS

Though the port registers and directional registers for ports P4, P5, P6 and P8 have eight bits, the directional register bits having no pins must always be set to the output mode. Since port $P3_3$ is not available as a pin although it has port register and directional register, port $P3_3$ must be set to the output mode.

## ADDRESSING MODES

The M37705M2AXXXSP has 28 powerful addressing modes. Refer to the 7700 Family addressing mode description for the details of each addressing mode.

## MACHINE INSTRUCTION LIST

The M37705M2AXXXSP has 103 machine instructions. Refer to the 7700 Family machine instruction list for details.

## DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

(1) M37705M2AXXXSP mask ROM order confirmation form
(2) 64P4B mark specification form
(3) ROM data (EPROM 3 sets)

**The functional differences between the M37705M2AXXXSP and M37704M2AXXXFP**

| Parameter | M37705M2AXXXSP | M37704M2AXXXFP |
|---|---|---|
| I/O port | P0, P1, P2, P7 ····· 8-bit× 4<br>P5 ····· 7-bit× 1<br>P6 ····· 5-bit× 1<br>P4 ····· 4-bit× 1<br>P3 ····· 3-bit× 1<br>P8 ····· 2-bit× 1<br>(without $\overline{HLDA}$ pin) | P0~P2, P4~P8 ····· 8-bit× 8<br>P3 ····· 4-bit× 1<br>(with $\overline{HLDA}$ pin) |
| Timer | Timer A ····· with I/O pins 16-bit× 3<br>with output pins 16-bit× 2<br>Timer B ····· with input pins 16-bit× 2<br>only timer mode 16-bit× 1 | Timer A ····· with I/O pins 16-bit× 5<br>Timer B ····· with input pins 16-bit× 3 |
| Serial I/O | UART (no clock synchronous serial I/O)× 1 | (UART or clock synchronous serial I/O)× 2 |
| Package | 64-pin shrink plastic molded DIP | 80-pin plastic molded QFP |

## M37705M2AXXXSP

## ELECTRICAL CHARACTERISTICS ($V_{CC}$=5V, $V_{SS}$=0V, $T_a$=25℃, f($X_{IN}$)=16MHz, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits Min. | Limits Typ. | Limits Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$, $P3_1$, $P4_0$~$P4_2$, $P4_7$, $P5_0$~$P5_6$, $P6_0$, $P6_2$, $P6_3$, $P6_5$, $P6_6$, $P7_0$~$P7_7$, $P8_6$, $P8_7$ | $I_{OH}$=−10mA | 3 | | | V |
| $V_{OH}$ | High-level output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$, $P3_1$ | $I_{OH}$=−400μA | 4.7 | | | V |
| $V_{OH}$ | High-level output voltage $P3_2$ | $I_{OH}$=−10mA | 3.1 | | | V |
| | | $I_{OH}$=−400μA | 4.8 | | | |
| $V_{OH}$ | High-level output voltage $\overline{E}$ | $I_{OH}$=−10mA | 3.4 | | | V |
| | | $I_{OH}$=−400μA | 4.8 | | | |
| $V_{OL}$ | Low-level output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$, $P3_1$, $P4_0$~$P4_2$, $P4_7$, $P5_6$, $P6_0$, $P6_2$, $P6_3$, $P6_5$, $P6_6$, $P7_0$~$P7_7$, $P8_6$, $P8_7$ | $I_{OL}$=10mA | | | 2 | V |
| $V_{OL}$ | Low-level output voltage $P5_0$~$P5_5$ | $I_{OL}$=20mA | | | 2 | V |
| $V_{OL}$ | Low-level output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$, $P3_1$ | $I_{OL}$=2mA | | | 0.45 | V |
| $V_{OL}$ | Low-level output voltage $P3_2$ | $I_{OL}$=10mA | | | 1.9 | V |
| | | $I_{OL}$=2mA | | | 0.43 | |
| $V_{OL}$ | Low-level output voltage $\overline{E}$ | $I_{OL}$=10mA | | | 1.6 | V |
| | | $I_{OL}$=2mA | | | 0.4 | |
| $V_{T+}$−$V_{T-}$ | Hysteresis $\overline{HOLD}$, $\overline{RDY}$, $TA0_{IN}$~$TA2_{IN}$, $TB0_{IN}$, $TB1_{IN}$, $\overline{INT_0}$, $\overline{INT_1}$, $AD_{TRG}$ | | 0.4 | | 1 | V |
| $V_{T+}$−$V_{T-}$ | Hysteresis $\overline{RESET}$ | | 0.2 | | 0.5 | V |
| $V_{T+}$−$V_{T-}$ | Hysteresis $X_{IN}$ | | 0.1 | | 0.3 | V |
| $I_{IH}$ | High-level input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_2$, $P4_0$~$P4_2$, $P4_7$, $P5_0$~$P5_6$, $P6_0$, $P6_2$, $P6_3$, $P6_5$, $P6_6$, $P7_0$~$P7_7$, $P8_6$, $P8_7$, $X_{IN}$, $\overline{RESET}$, $CNV_{SS}$, BYTE | $V_I$=5V | | | 5 | μA |
| $I_{IL}$ | Low-level input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_2$, $P4_0$~$P4_2$, $P4_7$, $P5_0$~$P5_6$, $P6_0$, $P6_2$, $P6_3$, $P6_5$, $P6_6$, $P7_0$~$P7_7$, $P8_6$, $P8_7$, $X_{IN}$, $\overline{RESET}$, $CNV_{SS}$, BYTE | $V_I$=0V | | | −5 | μA |
| $V_{RAM}$ | RAM hold voltage | When clock is stopped. | 2 | | | V |
| $I_{CC}$ | Power supply current | In single-chip mode output only pin is open and other pins are $V_{SS}$ during reset. f($X_{IN}$)=16MHz, square waveform | | 12 | 24 | mA |
| | | $T_a$=25℃ when clock is stopped. | | | 1 | μA |
| | | $T_a$=85℃ when clock is stopped. | | | 20 | |

## A-D CONVERTER CHARACTERISTICS ($V_{CC}$=5V, $V_{SS}$=0V, $T_a$=25℃, f($X_{IN}$)=16MHz, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits Min. | Limits Typ. | Limits Max. | Unit |
|---|---|---|---|---|---|---|
| — | Resolution | $V_{REF}$=$V_{CC}$ | | | 8 | Bits |
| — | Absolute accuracy | $V_{REF}$=$V_{CC}$ | | | ±2 | LSB |
| $R_{LADDER}$ | Ladder resistance | $V_{REF}$=$V_{CC}$ | 2 | | 10 | kΩ |
| $t_{CONV}$ | Conversion time | | 14.25 | | | μs |
| $V_{REF}$ | Reference voltage | | 2 | | $V_{CC}$ | V |
| $V_{IA}$ | Analog input voltage | | 0 | | $V_{REF}$ | V |

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Ratings | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.3∼7 | V |
| $AV_{CC}$ | Analog supply voltage | | −0.3∼7 | V |
| $V_I$ | Input voltage $\overline{RESET}$, $CNV_{SS}$, BYTE | | −0.3∼12 | V |
| $V_I$ | Input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_2$, $P4_0$∼ $P4_2$, $P4_7$, $P5_0$∼$P5_6$, $P6_0$, $P6_2$, $P6_3$, $P6_5$, $P6_6$, $P7_0$∼$P7_7$, $P8_6$, $P8_7$, $V_{REF}$, $X_{IN}$ | | −0.3∼$V_{CC}$+0.3 | V |
| $V_O$ | Output voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_2$, $P4_0$∼ $P4_2$, $P4_7$, $P5_0$∼$P5_6$, $P6_0$, $P6_2$, $P6_3$, $P6_5$, $P6_6$, $P7_0$∼$P7_7$, $P8_6$, $P8_7$, $X_{OUT}$, $\overline{E}$ | | −0.3∼$V_{CC}$+0.3 | V |
| $P_d$ | Power dissipation | $T_a$=25℃ | 1000 | mW |
| Topr | Operating temperature | | −20∼85 | ℃ |
| Tstg | Storage temperature | | −40∼150 | ℃ |

## RECOMMENDED OPERATING CONDITIONS ($V_{CC}$=5V±10%, $T_a$=−10∼70℃, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| $AV_{CC}$ | Analog supply voltage | | $V_{CC}$ | | V |
| $V_{SS}$ | Supply voltage | | 0 | | V |
| $AV_{SS}$ | Analog supply voltage | | 0 | | V |
| $V_{IH}$ | High-level input voltage $P0_0$∼$P0_7$, $P3_0$∼$P3_2$, $P4_0$∼$P4_2$, $P4_7$, $P5_0$∼$P5_6$, $P6_0$, $P6_2$, $P6_3$, $P6_5$, $P6_6$, $P7_0$∼$P7_7$, $P8_6$, $P8_7$, $X_{IN}$, $\overline{RESET}$, $CNV_{SS}$, BYTE | 0.8$V_{CC}$ | | $V_{CC}$ | V |
| $V_{IH}$ | High-level input voltage $P1_0$∼$P1_7$, $P2_0$∼$P2_7$ (in single-chip mode) | 0.8$V_{CC}$ | | $V_{CC}$ | V |
| $V_{IH}$ | High-level input voltage $P1_0$∼$P1_7$, $P2_0$∼$P2_7$ (in memory expansion mode and microprocessor mode) | 0.5$V_{CC}$ | | $V_{CC}$ | V |
| $V_{IL}$ | Low-level input voltage $P0_0$∼$P0_7$, $P3_0$∼$P3_2$, $P4_0$∼$P4_2$, $P4_7$, $P5_0$∼$P5_6$, $P6_0$, $P6_2$, $P6_3$, $P6_5$, $P6_6$, $P7_0$∼$P7_7$, $P8_6$, $P8_7$, $X_{IN}$, $\overline{RESET}$, $CNV_{SS}$, BYTE | 0 | | 0.2$V_{CC}$ | V |
| $V_{IL}$ | Low-level input voltage $P1_0$∼$P1_7$, $P2_0$∼$P2_7$ (in single-chip mode) | 0 | | 0.2$V_{CC}$ | V |
| $V_{IL}$ | Low-level input voltage $P1_0$∼$P1_7$, $P2_0$∼$P2_7$ (in memory expansion mode and microprocessor mode) | 0 | | 0.16$V_{CC}$ | V |
| $I_{OH(peak)}$ | High-level peak output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_2$, $P4_0$∼$P4_2$, $P4_7$, $P5_0$∼$P5_6$, $P6_0$, $P6_2$, $P6_3$, $P6_5$, $P6_6$, $P7_0$∼$P7_7$, $P8_6$, $P8_7$ | | | −10 | mA |
| $I_{OH(avg)}$ | High-level average output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_2$, $P4_0$∼$P4_2$, $P4_7$, $P5_0$∼$P5_6$, $P6_0$, $P6_2$, $P6_3$, $P6_5$, $P6_6$, $P7_0$∼$P7_7$, $P8_6$, $P8_7$ | | | −5 | mA |
| $I_{OL(peak)}$ | Low-level peak output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_2$, $P4_0$∼$P4_2$, $P4_7$, $P5_6$, $P6_0$, $P6_2$, $P6_3$, $P6_5$, $P6_6$, $P7_0$∼$P7_7$, $P8_6$, $P8_7$ | | | 10 | mA |
| $I_{OL(peak)}$ | Low-level peak output current $P5_0$∼$P5_5$ | | | 20 | mA |
| $I_{OL(avg)}$ | Low-level average output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_2$, $P4_0$∼$P4_2$, $P4_7$, $P5_6$, $P6_0$, $P6_2$, $P6_3$, $P6_5$, $P6_6$, $P7_0$∼$P7_7$, $P8_6$, $P8_7$ | | | 5 | mA |
| $I_{OL(avg)}$ | Low-level average output current $P5_0$∼$P5_5$ | | | 15 | mA |
| $f(X_{IN})$ | External clock frequency input | | | 16 | MHz |

Note 1. Average output current is the average value of a 100ms interval.
2. The sum of $I_{OL(peak)}$ for ports P0, P1, P2, P3, and P8 must be 80mA or less, the sum of $I_{OH(peak)}$ for ports P0, P1, P2, P3, and P8 must be 80mA or less, the sum of $I_{OL(peak)}$ for ports P4, P5, P6, and P7 must be 110mA or less, and the sum of $I_{OH(peak)}$ for ports P4, P5, P6, and P7 must be 80mA or less.

## TIMING REQUIREMENTS ($V_{CC}$=5V±10%, $V_{SS}$=0V, $T_a$=25°C, f($X_{IN}$)=16MHz, unless otherwise noted)

### External clock input

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_C$ | External clock input cycle time | | 62 | | | ns |
| $t_{W(H)}$ | External clock input high-level pulse width | | 25 | | | ns |
| $t_{W(L)}$ | External clock input low-level pulse width | | 25 | | | ns |
| $t_r$ | External clock rise time | | | | 10 | ns |
| $t_f$ | External clock fall time | | | | 10 | ns |

### Single-chip mode

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{SU(P0D-E)}$ | Port P0 input setup time | | 100 | | | ns |
| $t_{SU(P1D-E)}$ | Port P1 input setup time | | 100 | | | ns |
| $t_{SU(P2D-E)}$ | Port P2 input setup time | | 100 | | | ns |
| $t_{SU(P3D-E)}$ | Port P3 input setup time | | 100 | | | ns |
| $t_{SU(P4D-E)}$ | Port P4 input setup time | | 100 | | | ns |
| $t_{SU(P5D-E)}$ | Port P5 input setup time | | 100 | | | ns |
| $t_{SU(P6D-E)}$ | Port P6 input setup time | | 100 | | | ns |
| $t_{SU(P7D-E)}$ | Port P7 input setup time | | 100 | | | ns |
| $t_{SU(P8D-E)}$ | Port P8 input setup time | | 100 | | | ns |
| $t_{h(E-P0D)}$ | Port P0 input hold time | | 0 | | | ns |
| $t_{h(E-P1D)}$ | Port P1 input hold time | | 0 | | | ns |
| $t_{h(E-P2D)}$ | Port P2 input hold time | | 0 | | | ns |
| $t_{h(E-P3D)}$ | Port P3 input hold time | | 0 | | | ns |
| $t_{h(E-P4D)}$ | Port P4 input hold time | | 0 | | | ns |
| $t_{h(E-P5D)}$ | Port P5 input hold time | | 0 | | | ns |
| $t_{h(E-P6D)}$ | Port P6 input hold time | | 0 | | | ns |
| $t_{h(E-P7D)}$ | Port P7 input hold time | | 0 | | | ns |
| $t_{h(E-P8D)}$ | Port P8 input hold time | | 0 | | | ns |

### Memory expansion mode and microprocessor mode

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{SU(P1D-E)}$ | Port P1 input setup time | | 45 | | | ns |
| $t_{SU(P2D-E)}$ | Port P2 input setup time | | 45 | | | ns |
| $t_{SU(RDY-\phi_1)}$ | $\overline{RDY}$ input setup time | | 60 | | | ns |
| $t_{h(E-P1D)}$ | Port P1 input hold time | | 0 | | | ns |
| $t_{h(E-P2D)}$ | Port P2 input hold time | | 0 | | | ns |
| $t_{h(\phi_1-RDY)}$ | $\overline{RDY}$ input hold time | | 0 | | | ns |

## Timer A input (Count input in event counter mode)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{C(TA)}$ | $TAi_{IN}$ input cycle time | | 125 | | | ns |
| $t_{W(TAH)}$ | $TAi_{IN}$ input high-level pulse width | | 62 | | | ns |
| $t_{W(TAL)}$ | $TAi_{IN}$ input low-level pulse width | | 62 | | | ns |

## Timer A input (Gating input in timer mode)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{C(TA)}$ | $TAi_{IN}$ input cycle time | | 500 | | | ns |
| $t_{W(TAH)}$ | $TAi_{IN}$ input high-level pulse width | | 250 | | | ns |
| $t_{W(TAL)}$ | $TAi_{IN}$ input low-level pulse width | | 250 | | | ns |

## Timer A input (External trigger input in one-shot pulse mode)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{C(TA)}$ | $TAi_{IN}$ input cycle time | | 250 | | | ns |
| $t_{W(TAH)}$ | $TAi_{IN}$ input high-level pulse width | | 125 | | | ns |
| $t_{W(TAL)}$ | $TAi_{IN}$ input low-level pulse width | | 125 | | | ns |

## Timer A input (External trigger input in pulse width modulation mode)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{W(TAH)}$ | $TAi_{IN}$ input high-level pulse width | | 125 | | | ns |
| $t_{W(TAL)}$ | $TAi_{IN}$ input low-level pulse width | | 125 | | | ns |

## Timer A input (Up-down input in event counter mode)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{C(UP)}$ | $TAi_{OUT}$ input cycle time | | 2500 | | | ns |
| $t_{W(UPH)}$ | $TAi_{OUT}$ input high-level pulse width | | 1250 | | | ns |
| $t_{W(UPL)}$ | $TAi_{OUT}$ input low-level pulse width | | 1250 | | | ns |
| $t_{SU(UP-T_{IN})}$ | $TAi_{OUT}$ input setup time | | 500 | | | ns |
| $t_{h(T_{IN}-UP)}$ | $TAi_{OUT}$ input hold time | | 500 | | | ns |

## Timer B input (Count input in event counter mode)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{C(TB)}$ | $TBi_{IN}$ input cycle time (one edge count) | | 125 | | | ns |
| $t_{W(TBH)}$ | $TBi_{IN}$ input high-level pulse width (one edge count) | | 62 | | | ns |
| $t_{W(TBL)}$ | $TBi_{IN}$ input low-level pulse width (one edge count) | | 62 | | | ns |
| $t_{C(TB)}$ | $TBi_{IN}$ input cycle time (both edges count) | | 250 | | | ns |
| $t_{W(TBH)}$ | $TBi_{IN}$ input high-level pulse width (both edges count) | | 125 | | | ns |
| $t_{W(TBL)}$ | $TBi_{IN}$ input low-level pulse width (both edges count) | | 125 | | | ns |

## Timer B input (Pulse period measurement mode)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{C(TB)}$ | $TBi_{IN}$ input cycle time | | 500 | | | ns |
| $t_{W(TBH)}$ | $TBi_{IN}$ input high-level pulse width | | 250 | | | ns |
| $t_{W(TBL)}$ | $TBi_{IN}$ input low-level pulse width | | 250 | | | ns |

## Timer B input (Pulse width measurement mode)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{C(TB)}$ | $TBi_{IN}$ input cycle time | | 500 | | | ns |
| $t_{W(TBH)}$ | $TBi_{IN}$ input high-level pulse width | | 250 | | | ns |
| $t_{W(TBL)}$ | $TBi_{IN}$ input low-level pulse width | | 250 | | | ns |

## A-D trigger input

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{C(AD)}$ | $\overline{AD_{TRG}}$ input cycle time (minimum allowable trigger) | | 1000 | | | ns |
| $t_{W(ADL)}$ | $\overline{AD_{TRG}}$ input low-level pulse width | | 125 | | | ns |

## Serial I/O

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{C(CK)}$ | CLKi input cycle time | | 250 | | | ns |
| $t_{W(CKH)}$ | CLKi input high-level pulse width | | 125 | | | ns |
| $t_{W(CKL)}$ | CLKi input low-level pulse width | | 125 | | | ns |
| $t_{d(C-Q)}$ | TxDi output delay time | | | | 90 | ns |
| $t_{h(C-Q)}$ | TxDi hold time | | 0 | | | ns |
| $t_{su(D-C)}$ | RxDi input setup time | | 30 | | | ns |
| $t_{h(C-D)}$ | RxDi input hold time | | 90 | | | ns |

## External interrupt $\overline{INTi}$ input

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{W(INH)}$ | $\overline{INTi}$ input high-level pulse width | | 250 | | | ns |
| $t_{W(INL)}$ | $\overline{INTi}$ input low-level pulse width | | 250 | | | ns |

## SWITCHING CHARACTERISTICS ($V_{CC}$=5V±10%, $V_{SS}$=0V, $T_a$=25℃, f($X_{IN}$)=16MHz, unless otherwise noted)

### Single-chip mode

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{d(E-P0Q)}$ | Port P0 data output delay time | Fig. 1 | | | 100 | ns |
| $t_{d(E-P1Q)}$ | Port P1 data output delay time | | | | 100 | ns |
| $t_{d(E-P2Q)}$ | Port P2 data output delay time | | | | 100 | ns |
| $t_{d(E-P3Q)}$ | Port P3 data output delay time | | | | 100 | ns |
| $t_{d(E-P4Q)}$ | Port P4 data output delay time | | | | 100 | ns |
| $t_{d(E-P5Q)}$ | Port P5 data output delay time | | | | 100 | ns |
| $t_{d(E-P6Q)}$ | Port P6 data output delay time | | | | 100 | ns |
| $t_{d(E-P7Q)}$ | Port P7 data output delay time | | | | 100 | ns |
| $t_{d(E-P8Q)}$ | Port P8 data output delay time | | | | 100 | ns |

### Memory expansion mode and microprocessor mode (when wait bit = "1")

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{d(P0A-E)}$ | Port P0 address output delay time | Fig. 1 | 30 | | | ns |
| $t_{d(E-P1Q)}$ | Port P1 data output delay time (BYTE="L") | | | | 80 | ns |
| $t_{PXZ(E-P1Z)}$ | Port P1 floating start delay time (BYTE="L") | | | | 5 | ns |
| $t_{d(P1A-E)}$ | Port P1 address output delay time | | 30 | | | ns |
| $t_{d(E-P2Q)}$ | Port P2 data output delay time | | | | 80 | ns |
| $t_{PXZ(E-P2Z)}$ | Port P2 floating start delay time | | | | 5 | ns |
| $t_{d(P2A-E)}$ | Port P2 address output delay time | | 30 | | | ns |
| $t_{d(ALE-E)}$ | ALE output delay time | | 4 | | | ns |
| $t_{W(ALE)}$ | ALE pulse width | | 40 | | | ns |
| $t_{d(BHE-E)}$ | $\overline{BHE}$ output delay time | | 30 | | | ns |
| $t_{d(R/W-E)}$ | R/$\overline{W}$ output delay time | | 30 | | | ns |
| $t_{d(E-\phi_1)}$ | $\phi_1$ output delay time | | 0 | | 20 | ns |
| $t_{h(E-P0A)}$ | Port P0 address hold time | | 25 | | | ns |
| $t_{h(ALE-P1A)}$ | Port P1 address hold time (BYTE="L") | | 9 | | | ns |
| $t_{h(E-P1Q)}$ | Port P1 data hold time (BYTE="L") | | 25 | | | ns |
| $t_{PZX(E-P1Z)}$ | Port P1 floating release delay time (BYTE="L") | | 25 | | | ns |
| $t_{h(E-P1A)}$ | Port P1 address hold time (BYTE="H") | | 25 | | | ns |
| $t_{h(ALE-P2A)}$ | Port P2 address hold time | | 9 | | | ns |
| $t_{h(E-P2Q)}$ | Port P2 data hold time | | 25 | | | ns |
| $t_{PZX(E-P2Z)}$ | Port P2 floating release delay time | | 25 | | | ns |
| $t_{h(E-BHE)}$ | $\overline{BHE}$ hold time | | 20 | | | ns |
| $t_{h(E-R/W)}$ | R/$\overline{W}$ hold time | | 20 | | | ns |
| $t_{W(EL)}$ | $\overline{E}$ pulse width | | 95 | | | ns |

## Memory expansion mode and microprocessor mode (when wait bit = "0", and external memory area is accessed)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{d(P0A-E)}$ | Port P0 address output delay time | Fig. 1 | 155 | | | ns |
| $t_{d(E-P1Q)}$ | Port P1 data output delay time (BYTE="L") | | | | 80 | ns |
| $t_{PXZ(E-P1Z)}$ | Port P1 floating start delay time (BYTE="L") | | | | 5 | ns |
| $t_{d(P1A-E)}$ | Port P1 address output delay time | | 155 | | | ns |
| $t_{d(E-P2Q)}$ | Port P2 data output delay time | | | | 80 | ns |
| $t_{PXZ(E-P2Z)}$ | Port P2 floating start delay time | | | | 5 | ns |
| $t_{d(P2A-E)}$ | Port P2 address output delay time | | 155 | | | ns |
| $t_{d(ALE-E)}$ | ALE output delay time | | 4 | | | ns |
| $t_{W(ALE)}$ | ALE pulse width | | 165 | | | ns |
| $t_{d(\overline{BHE}-E)}$ | $\overline{BHE}$ output delay time | | 155 | | | ns |
| $t_{d(R/\overline{W}-E)}$ | R/$\overline{W}$ output delay time | | 155 | | | ns |
| $t_{d(E-\phi_1)}$ | $\phi_1$ output delay time | | 0 | | 20 | ns |
| $t_{h(E-P0A)}$ | Port P0 address hold time | | 25 | | | ns |
| $t_{h(ALE-P1A)}$ | Port P1 address hold time (BYTE="L") | | 9 | | | ns |
| $t_{h(E-P1Q)}$ | Port P1 data hold time (BYTE="L") | | 25 | | | ns |
| $t_{PZX(E-P1Z)}$ | Port P1 floating release delay time (BYTE="L") | | 25 | | | ns |
| $t_{h(E-P1A)}$ | Port P1 address hold time (BYTE="H") | | 25 | | | ns |
| $t_{h(ALE-P2A)}$ | Port P2 address hold time | | 9 | | | ns |
| $t_{h(E-P2Q)}$ | Port P2 data hold time | | 25 | | | ns |
| $t_{PZX(E-P2Z)}$ | Port P2 floating release delay time | | 25 | | | ns |
| $t_{h(E-\overline{BHE})}$ | $\overline{BHE}$ hold time | | 20 | | | ns |
| $t_{h(E-R/W)}$ | R/$\overline{W}$ hold time | | 20 | | | ns |
| $t_{W(\overline{EL})}$ | $\overline{E}$ pulse width | | 220 | | | ns |

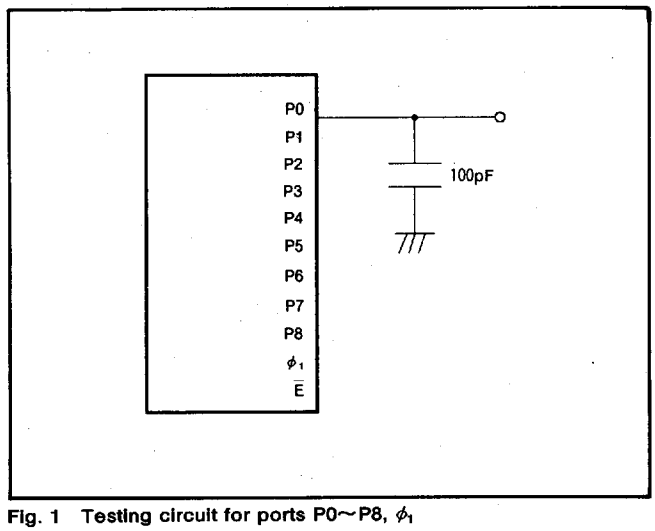
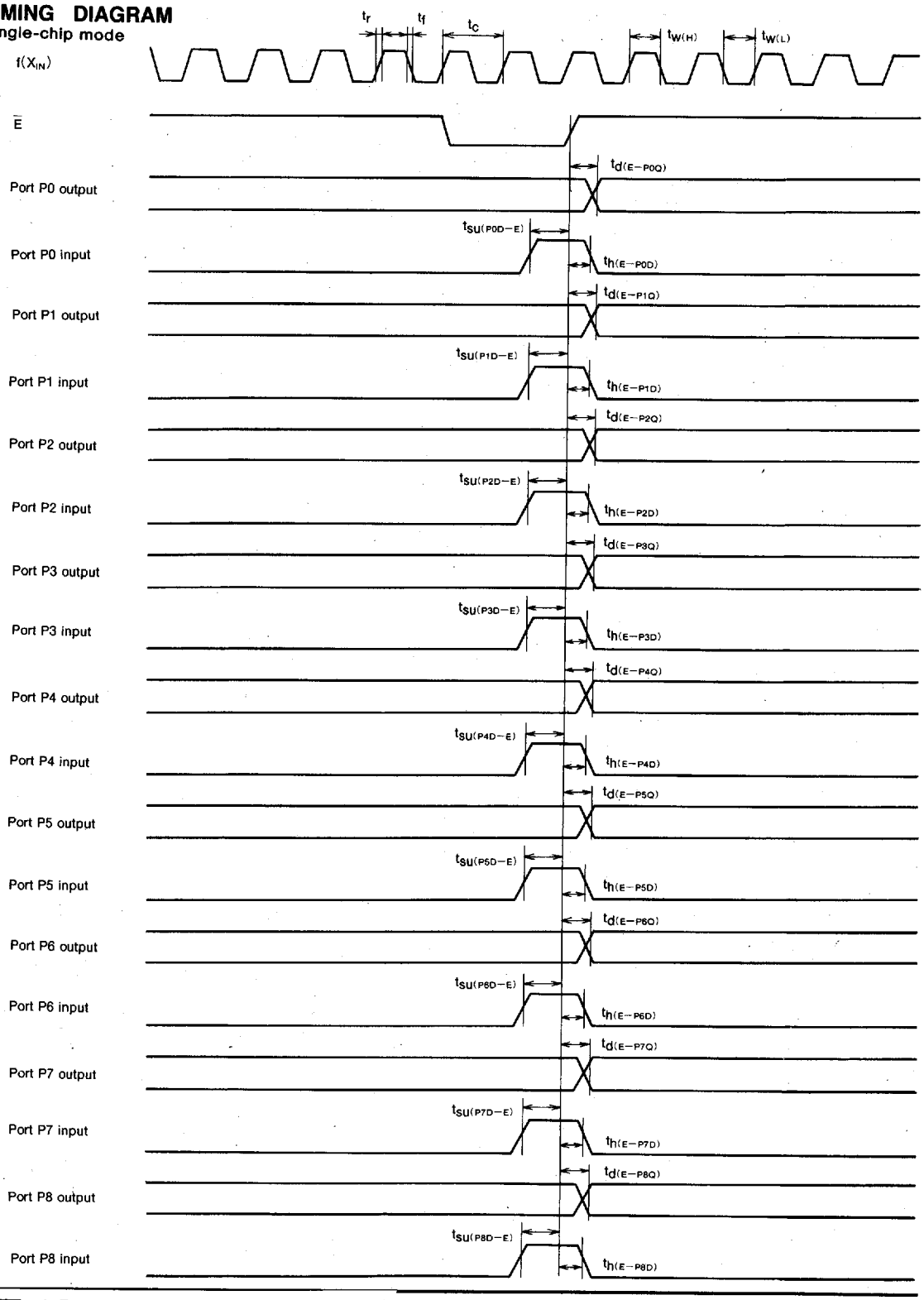
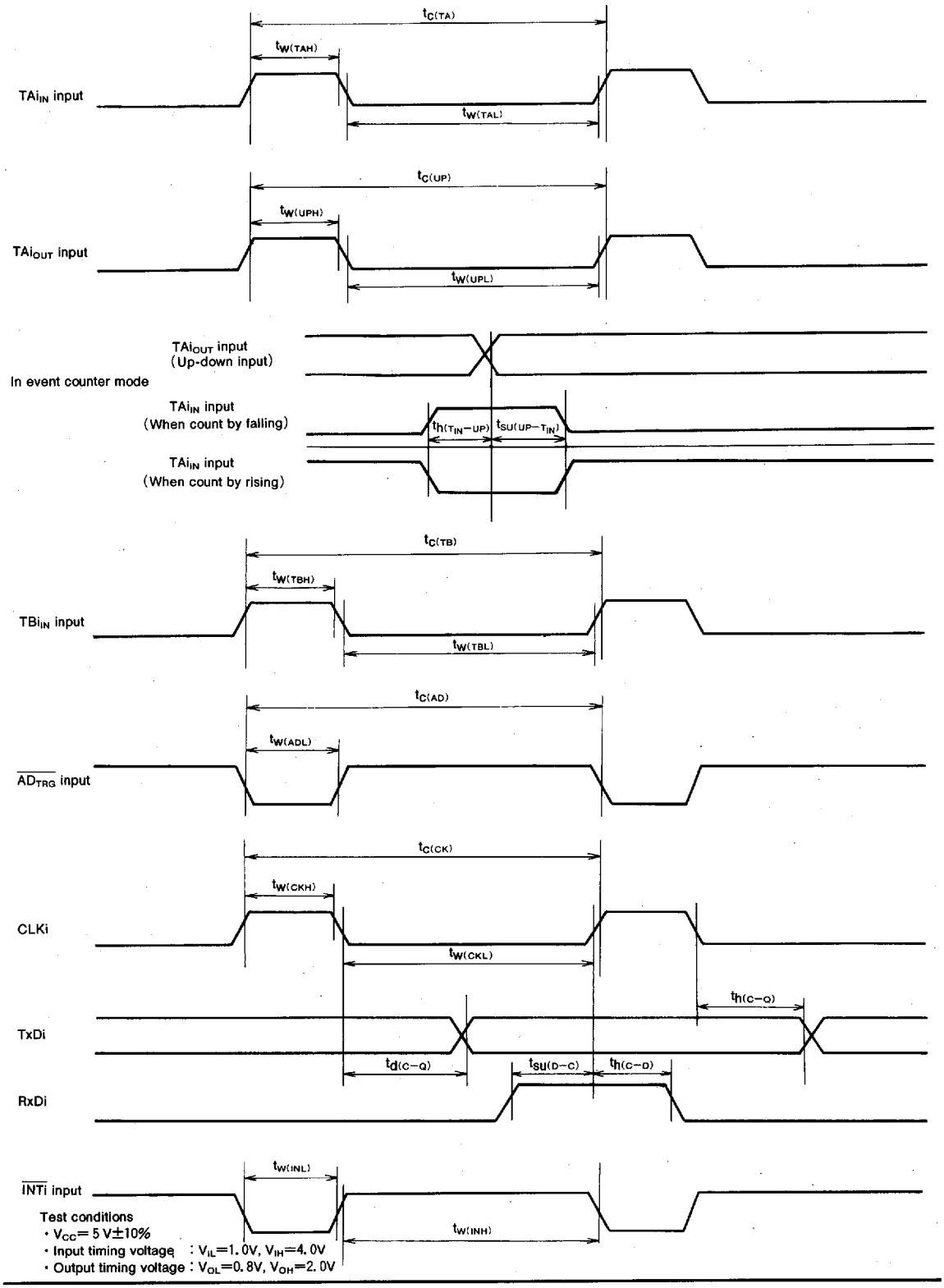



Fig. 1 Testing circuit for ports P0~P8, $\phi_1$

## TIMING DIAGRAM

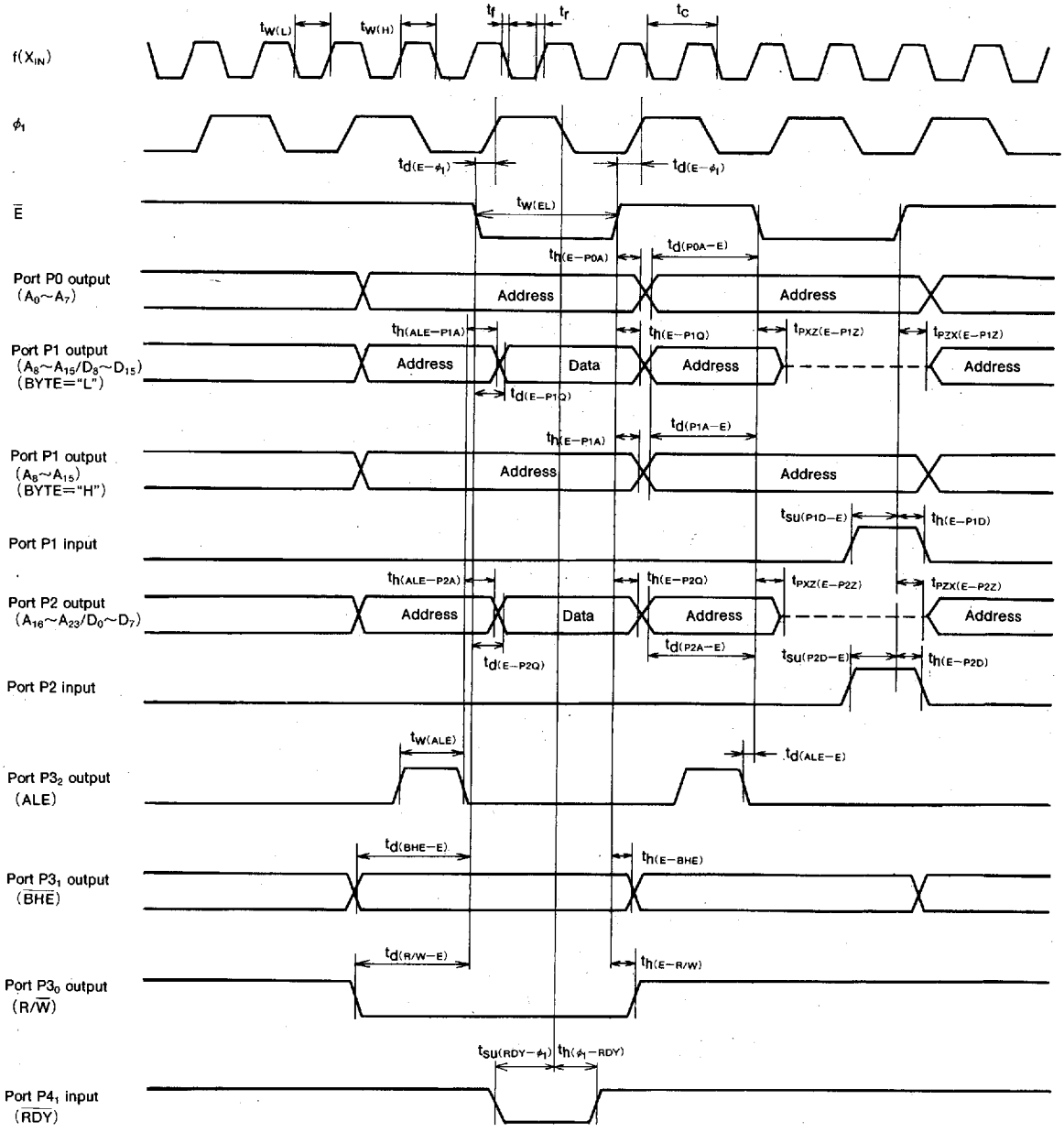
Single-chip mode






Test conditions
- $V_{CC}$= 5 V±10%
- Input timing voltage : $V_{IL}$=1.0V, $V_{IH}$=4.0V
- Output timing voltage : $V_{OL}$=0.8V, $V_{OH}$=2.0V

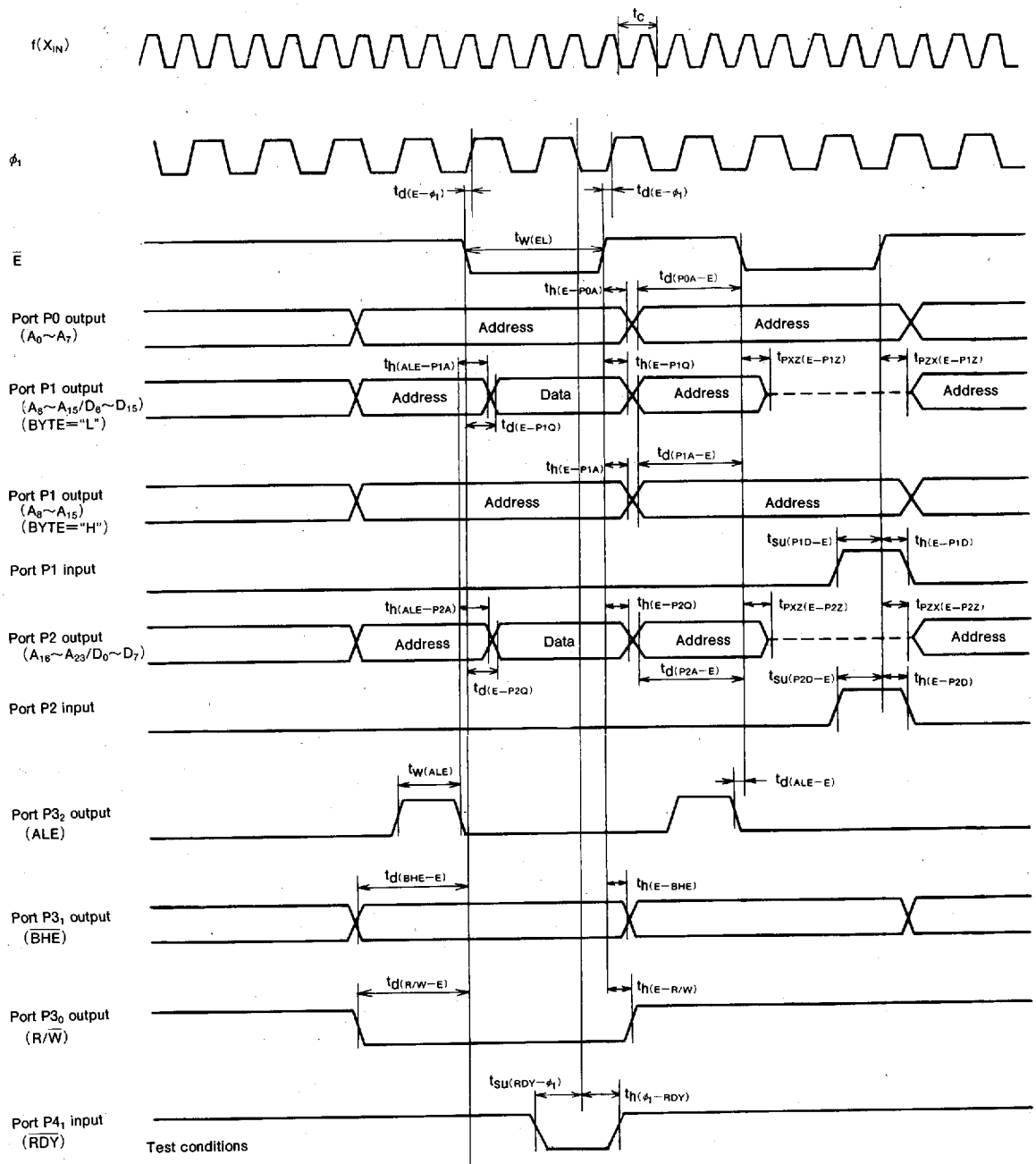
Memory expansion mode and microprocessor mode(When wait bit = "1")




Test conditions

- $V_{CC}$= 5 V±10%
- Output timing voltage : $V_{OL}$=0.8V, $V_{OH}$=2.0V
- Port P1, P2 input : $V_{IL}$=0.8V, $V_{IH}$=2.5V
- Port $P4_1$ input : $V_{IL}$=1.0V, $V_{IH}$=4.0V

Memory expansion mode and microprocessor mode(When wait bit = "0", and external memory area is accessed)

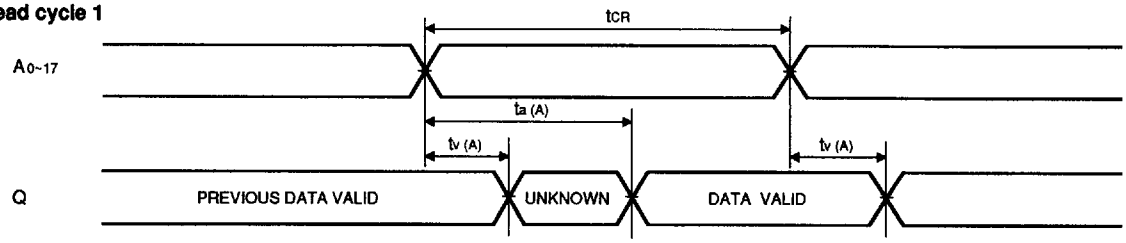



Test conditions

- $V_{CC}$= 5 V±10%
- Output timing voltage : $V_{OL}$=0.8V, $V_{OH}$=2.0V
- Port P1, P2 input : $V_{IL}$=0.8V, $V_{IH}$=2.5V
- Port P4₁ input : $V_{IL}$=1.0V, $V_{IH}$=4.0V

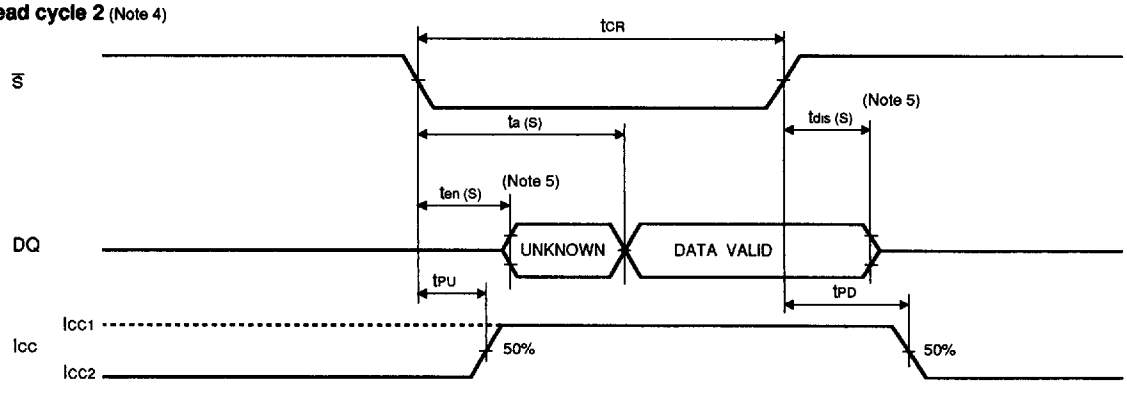
## (4) TIMING DIAGRAMS

### Read cycle 1




$\overline{W}$ = H
$\overline{S}$ = L
$\overline{OE}$ = L

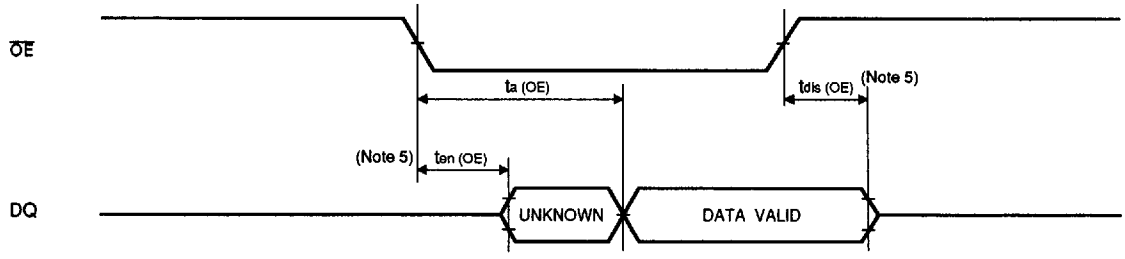
### Read cycle 2 (Note 4)




$\overline{W}$ = H
$\overline{OE}$ = L

Note 4 : Addresses valid prior to or coincident with $\overline{S}$ transition low.
5 : Transition is measured ±500mV from steady state voltage with specified loading in Figure 2.

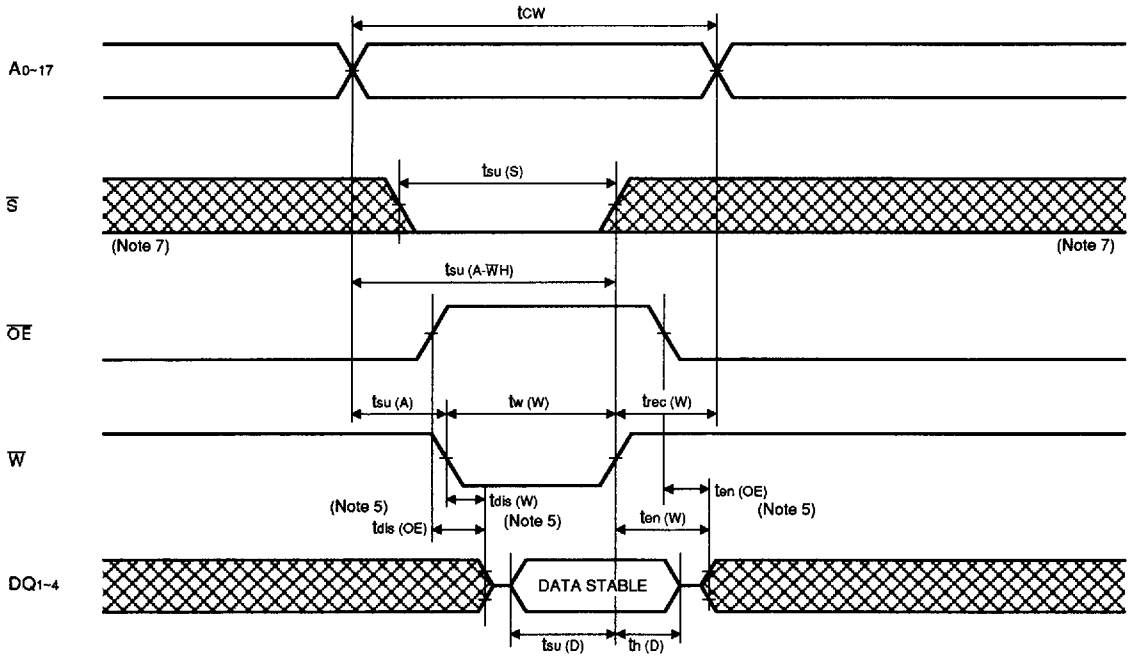
### Read cycle 3 (Note 6)



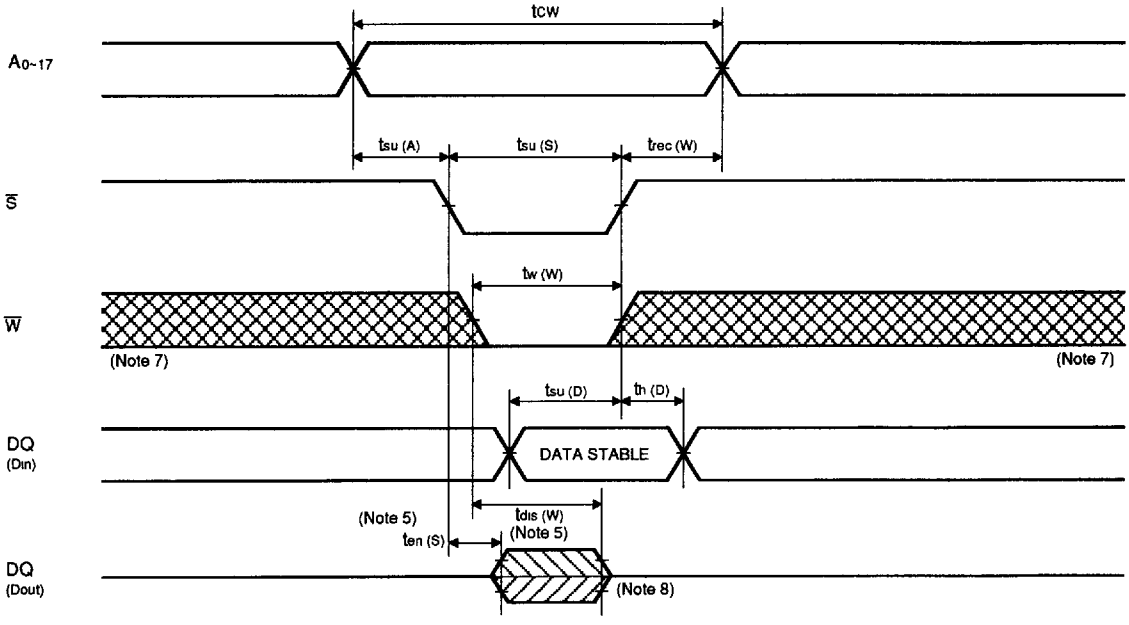

$\overline{W}$ = H
$\overline{S}$ = L

Note 6: Addresses and $\overline{S}$ valid prior to $\overline{OE}$ transition low by (ta (A)-ta (OE)), (ta (S)-ta (OE))

**Write cycle ($\overline{W}$ control mode)**




**Write cycle ($\overline{S}$ control mode)**




Note 7 : Hatching indicates the state is don't care.

8 : When the falling edge of $\overline{W}$ is simultaneous or prior to the falling edge of $\overline{S}$, the output is maintained in the high impedance.

9 : ten, tdis are periodically sampled and are not 100% tested.

PRELIMINARY

Notice: This is not a final specification
Some parameters are subject to change

# M5M5V1001CP,J-15,-20,-25

## 1048576-BIT (1048576-WORD BY 1-BIT) CMOS STATIC RAM

### DESCRIPTION

The M5M5V1001CP,J are a family of 1048576-word by 1-bit static RAMs, fabricated with the high performance CMOS silicon gate process and designed for high-speed application.

The M5M5V1001CP,J are offered in a 28-pin plastic dual-in-line package (DIP), 28-pin plastic small outline J-lead package (SOJ).

These devices operate on a single 3.3V supply, and are directly TTL compatible. They include power down feature as well.

### FEATURES

| Type name | Access time (max) | Power supply current | |
|---|---|---|---|
| | | Active (max) | Stand-by (max) |
| M5M5V1001CP,J - 15 | 15ns | 120mA | 1mA |
| M5M5V1001CP,J - 20 | 20ns | 100mA | |
| M5M5V1001CP,J - 25 | 25ns | 90mA | |

- Single +3.3V power supply
- Fully staric operation : No clocks, No refresh
- Power down by $\overline{S}$
- Easy memory expansion by $\overline{S}$
- Three-state outputs : OR-tie capability
- Directly TTL compatible : All inputs and outputs
- TEST MODE is avaiable

### PACKAGE

M5M5V1001CP ..... 28pin 400mil DIP
M5M5V1001CJ ..... 28pin 400mil SOJ

### APPLICATION

High speed memory units

### FUNCTION

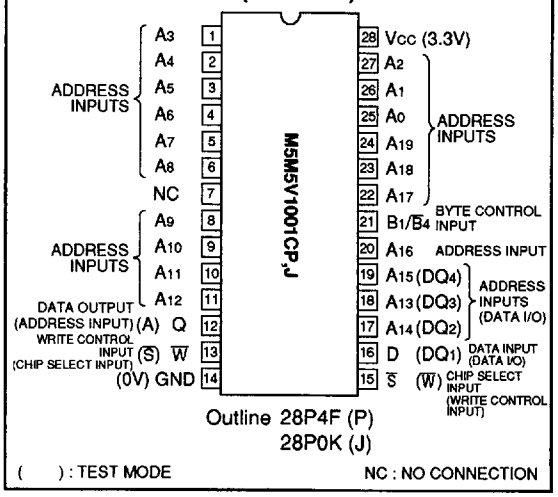
The operation mode of the M5M5V1001C series is determined by a combination of the device control inputs $\overline{S}$ and $\overline{W}$. Each mode is summarized in the function table shown in next page.

The RAM works with an organization of 1048576-word by 1-bit, when $B_1/\overline{B}_4$ is high of floating. And an organization of 262144-word by 4-bit is also obtained for reducing the test time, when $B_1/\overline{B}_4$ is low.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}$. The address must be set-up before the write cycle and must be stable during the entire cycle.

The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S}$ whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. When $\overline{S}$ is high, the chip is non-selectable state, disabling both reading and writing. In the

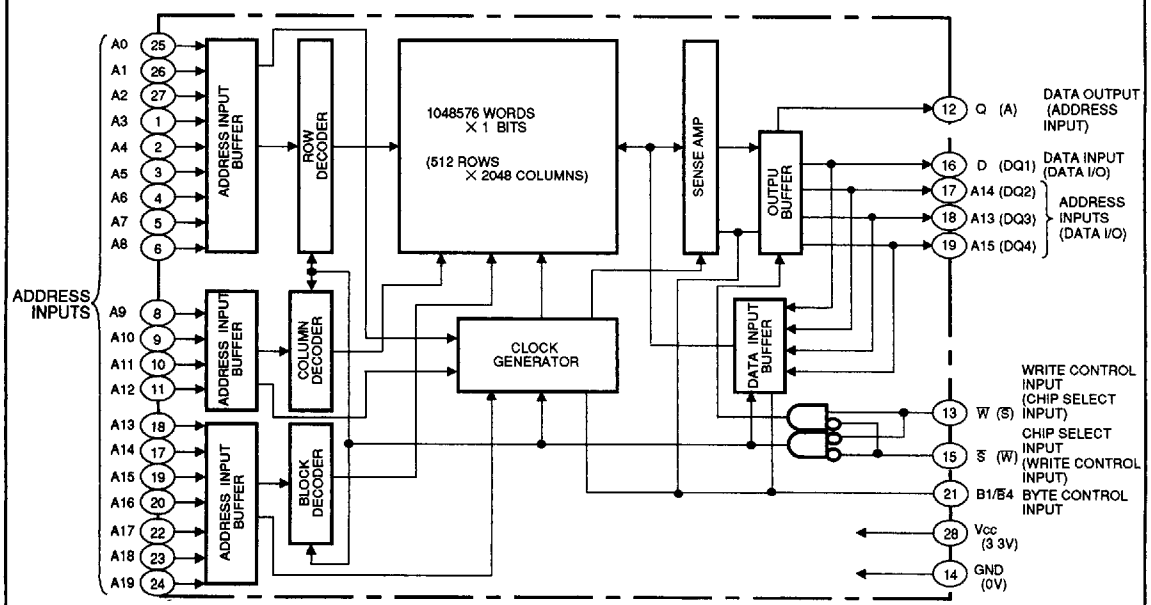
### PIN CONFIGURATION (TOP VIEW)




Outline 28P4F (P)
28P0K (J)

( ) : TEST MODE NC : NO CONNECTION

### BLOCK DIAGRAM




( ) shows TSET MODE PIN CONFIGURATION (×4)

case, the output stage is in a high-impedance state.

A read cycle is executed by setting $\overline{W}$ at a high level while $\overline{S}$ are in an active state ($\overline{S}$ = L)

When setting $\overline{S}$ at a high level, the chip is in a non-selectable mode in which both reading and write are disabled.

In this mode, the output stage is in a high-impedance state, allowing OR -tie with other chips and memory expansion by $\overline{S}$.

Signal-$\overline{S}$ controls the power-down feature. When $\overline{S}$ goes high, power dissipation is reduced extremely. The access time from $\overline{S}$ is equivalent to the address access time.

## FUNCTION TABLE

| $\overline{S}$ | $\overline{W}$ | Mode | Q | D | Icc |
|---|---|---|---|---|---|
| H | X | Non selection | High-impedance | High-impedance | Stand-by |
| L | L | Write | Din | High-impedance | Active |
| L | H | Read | High-impedance | Dout | Active |

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Ratings | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to GND | −2.0*~4.6 | V |
| $V_I$ | Input voltage | With respect to GND | −2.0*~Vcc + 0.5 | V |
| $V_O$ | Output voltage | With respect to GND | −2.0*~Vcc | V |
| $P_d$ | Power dissipation | Ta = 25℃ | 1000 | mW |
| $T_{opr}$ | Operating temperature | | 0~70 | ℃ |
| $T_{stg\ (bias)}$ | Storage temperature (bias) | | −10~85 | ℃ |
| $T_{stg}$ | Storage temperature | | −65~150 | ℃ |

*− 0.5V in case of DC (Pulse width≦20ns)

## DC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, Vcc = 3.3V±10%, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits Min | Limits Typ | Limits Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | | 2.2 | | Vcc+0.3V | V |
| $V_{IL}$ | Low-level input voltage | | | −0.3* | | 0.8 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = −4mA | | 2.4 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 8mA | | | | 0.4 | V |
| $I_I$ | Input current | $V_I$ = 0~Vcc | | | | 2 | μA |
| $I_{OZ}$ | Output current in off-state | $V_{I(\overline{S})}$ = $V_{IH}$<br>$V_{I/O}$ = 0~Vcc | | | | 10 | μA |
| $I_{CC1}$ | Active supply current (TTL level) | $V_{I(\overline{S})}$ = $V_{IL}$<br>other inputs = $V_{IH}$ or $V_{IL}$<br>Output-open (duty 100%) | AC (15ns cycle) | | | 120 | mA |
| | | | AC (20ns cycle) | | | 100 | |
| | | | AC (25ns cycle) | | | 90 | |
| | | | DC | | 45 | 55 | |
| $I_{CC2}$ | Stand-by supply current (TTL level) | $V_{I(\overline{S})}$ = $V_{IH}$ | AC (15ns cycle) | | | 45 | mA |
| | | | AC (20/25ns cycle) | | | 35 | |
| | | | DC | | | 20 | |
| $I_{CC3}$ | Stand-by current (MOS level) | $V_{I(\overline{S})}$≧Vcc − 0.2V<br>other inputs $V_I$≦0.2V or $V_I$≧Vcc − 0.2V | | | 0.1 | 1 | mA |

*− 3.0V in case of AC(Pulse width≦20ns)

## CAPACITANCE (Ta = 0~70℃, Vcc = 3.3V±10%, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits Min | Limits Typ | Limits Max | Unit |
|---|---|---|---|---|---|---|
| $C_I$ | Input capacitance | $V_I$ = GND, $V_I$ = 25mVrms, f = 1MHz | | | 6 | pF |
| $C_O$ | Output capacitance | $V_O$ = GND, $V_O$ = 25mVrms, f = 1MHz | | | 6 | pF |

Note 1 : Direction for current flowing into an IC is positive (no mark).
2 : Typical value is Vcc = 3.3V, Ta = 25℃.
3 : $C_I$, $C_O$ are periodically sampled and are not 100% tested.