ELPIDA

DATA SHEET

512MB Unbuffered SDRAM S.O.DIMM

HB52RF649DC-B (64M words × 72 bits, 2 bank)
HB52RD649DC-B (64M words × 72 bits, 2 bank)

Description

The HB52RF649DC, HB52RD649DC are a 64M × 72 × 2 banks Synchronous Dynamic RAM Small Outline Dual In-line Memory Module (S.O.DIMM), mounted 18 pieces of 256M bits SDRAM sealed in TCP package and 1 piece of serial EEPROM (2k bits) for Presence Detect (PD). An outline of the products is 144-pin Zig Zag Dual tabs socket type compact and thin package. Therefore, they make high density mounting possible without surface mount technology. They provide common data inputs and outputs. Decoupling capacitors are mounted beside TCP on the module board.

Note: Do not push the cover or drop the modules in order to protect from mechanical defects, which would be electrical defects.

Features

- Fully compatible with: JEDEC standard outline 8 bytes S.O.DIMM
- 144-pin Zig Zag Dual tabs socket type (dual lead out)
  - PCB height: 33.02mm (1.30inch)
  - Lead pitch: 0.80mm
- 3.3V power supply
- Clock frequency: 133MHz/100MHz (max.)
- LVTTL interface
- Data bus width: × 72 ECC
- Single pulsed /RAS
- 4 Banks can operates simultaneously and independently
- Burst read/write operation and burst read/single write operation capability
- Programmable burst length (BL): 1, 2, 4, 8
- 2 variations of burst sequence
  - Sequential
  - Interleave
- Programmable /CE latency (CL): 2, 3
- Byte control by DQMB
- Refresh cycles: 8192 refresh cycles/64ms
- 2 variations of refresh
  - Auto refresh
  - Self refresh
- Low self refresh current
  : HB52RF649DC-xxBL (L-version)
  : HB52RD649DC-xxBL (L-version)

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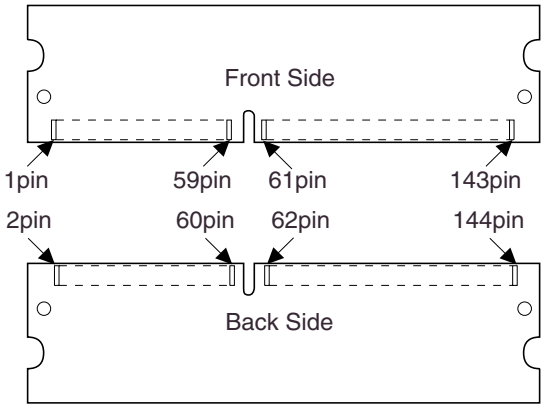
Ordering Information

Part number	Clock frequency MHz (max.)	/CE latency	Package	Contact pad	Mounted devices
HB52RF649DC-75B*1	133 MHz	3	144-pin S.O.DIMM	Gold	256M bits SDRAM TCP*2
HB52RF649DC-75BL*1	133 MHz	3			
HB52RD649DC-A6B*1	100 MHz	2, 3			
HB52RD649DC-A6BL*1	100 MHz	2, 3			

Notes: 1. 100MHz operation at /CE latency = 2.

2. Please refer to the TSOP products HM5225XX5B datasheet (E0082H) for detail information.

Pin Configurations



Front side				Back side			
Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	VSS	73	NC	2	VSS	74	CK1
3	DQ0	75	VSS	4	DQ32	76	VSS
5	DQ1	77	CB2	6	DQ33	78	CB6
7	DQ2	79	CB3	8	DQ34	80	CB7
9	DQ3	81	VCC	10	DQ35	82	VCC
11	VCC	83	DQ16	12	VCC	84	DQ48
13	DQ4	85	DQ17	14	DQ36	86	DQ49
15	DQ5	87	DQ18	16	DQ37	88	DQ50
17	DQ6	89	DQ19	18	DQ38	90	DQ51
19	DQ7	91	VSS	20	DQ39	92	VSS
21	VSS	93	DQ20	22	VSS	94	DQ52
23	DQMB0	95	DQ21	24	DQMB4	96	DQ53
25	DQMB1	97	DQ22	26	DQMB5	98	DQ54
27	VCC	99	DQ23	28	VCC	100	DQ55
29	A0	101	VCC	30	A3	102	VCC
31	A1	103	A6	32	A4	104	A7
33	A2	105	A8	34	A5	106	BA0
35	VSS	107	VSS	36	VSS	108	VSS

Front side				Back side			
Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
37	DQ8	109	A9	38	DQ40	110	BA1
39	DQ9	111	A10 (AP)	40	DQ41	112	A11
41	DQ10	113	VCC	42	DQ42	114	VCC
43	DQ11	115	DQMB2	44	DQ43	116	DQMB6
45	VCC	117	DQMB3	46	VCC	118	DQMB7
47	DQ12	119	VSS	48	DQ44	120	VSS
49	DQ13	121	DQ24	50	DQ45	122	DQ56
51	DQ14	123	DQ25	52	DQ46	124	DQ57
53	DQ15	125	DQ26	54	DQ47	126	DQ58
55	VSS	127	DQ27	56	VSS	128	DQ59
57	CB0	129	VCC	58	CB4	130	VCC
59	CB1	131	DQ28	60	CB5	132	DQ60
61	CK0	133	DQ29	62	CKE0	134	DQ61
63	VCC	135	DQ30	64	VCC	136	DQ62
65	/RE	137	DQ31	66	/CE	138	DQ63
67	/W	139	VSS	68	CKE1	140	VSS
69	/S0	141	SDA	70	A12	142	SCL
71	/S1	143	VCC	72	NC	144	VCC

Pin Description

Pin name	Function
A0 to A12	Address input Row address A0 to A12 Column address A0 to A9
BA0, BA1	Bank select address
DQ0 to DQ63	Data-input/output
CB0 to CB7	Check bit (Data-input/output)
/S0, /S1	Chip select
/RE	Row address asserted bank enable
/CE	Column address asserted
/W	Write enable
DQMB0 to DQMB7	Byte input/output mask
CK0, CK1	Clock input
CKE0, CKE1	Clock enable
SDA	Data-input/output for serial PD
SCL	Clock input for serial PD
VCC	Power supply
VSS	Ground
NC	No connection

Serial PD Matrix*[1]

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
0	Number of bytes used by module manufacturer	1	0	0	0	0	0	0	0	80	128
1	Total SPD memory size	0	0	0	0	1	0	0	0	08	256byte
2	Memory type	0	0	0	0	0	1	0	0	04	SDRAM
3	Number of row addresses bits	0	0	0	0	1	1	0	1	0D	13
4	Number of column addresses bits	0	0	0	0	1	0	1	0	0A	10
5	Number of banks	0	0	0	0	0	0	1	0	02	2
6	Module data width	0	1	0	0	1	0	0	0	48	72
7	Module data width (continued)	0	0	0	0	0	0	0	0	00	0 (+)
8	Module interface signal levels	0	0	0	0	0	0	0	1	01	LVTTL
9	SDRAM cycle time (highest /CE latency) (-75) 7.5ns	0	1	1	1	0	1	0	1	75	CL = 3
	(-A6) 10ns	1	0	1	0	0	0	0	0	A0	
10	SDRAM access from Clock (highest /CE latency) (-75) 5.4ns	0	1	0	1	0	1	0	0	54	
	(-A6) 6ns	0	1	1	0	0	0	0	0	60	
11	Module configuration type	0	0	0	0	0	0	1	0	02	ECC
12	Refresh rate/type	1	0	0	0	0	0	1	0	82	Normal (7.8125µs) Self refresh
13	SDRAM width	0	0	0	0	1	0	0	0	08	× 8
14	Error checking SDRAM width	0	0	0	0	1	0	0	0	08	× 8
15	SDRAM device attributes: minimum clock delay for back-to-back random column addresses	0	0	0	0	0	0	0	1	01	1 CLK
16	SDRAM device attributes: Burst lengths supported	0	0	0	0	1	1	1	1	0F	1, 2, 4, 8
17	SDRAM device attributes: number of banks on SDRAM device	0	0	0	0	0	1	0	0	04	4
18	SDRAM device attributes: /CE latency	0	0	0	0	0	1	1	0	06	2, 3
19	SDRAM device attributes: /S latency	0	0	0	0	0	0	0	1	01	0
20	SDRAM device attributes: /W latency	0	0	0	0	0	0	0	1	01	0
21	SDRAM module attributes	0	0	0	0	0	0	0	0	00	Unbuffer
22	SDRAM device attributes: General	0	0	0	0	1	1	1	0	0E	VCC ± 10%
23	SDRAM cycle time (2nd highest /CE latency) 10ns	1	0	1	0	0	0	0	0	A0	CL = 2
24	SDRAM access from Clock (2nd highest /CE latency) 6ns	0	1	1	0	0	0	0	0	60	
25	SDRAM cycle time (3rd highest /CE latency) Undefined	0	0	0	0	0	0	0	0	00	

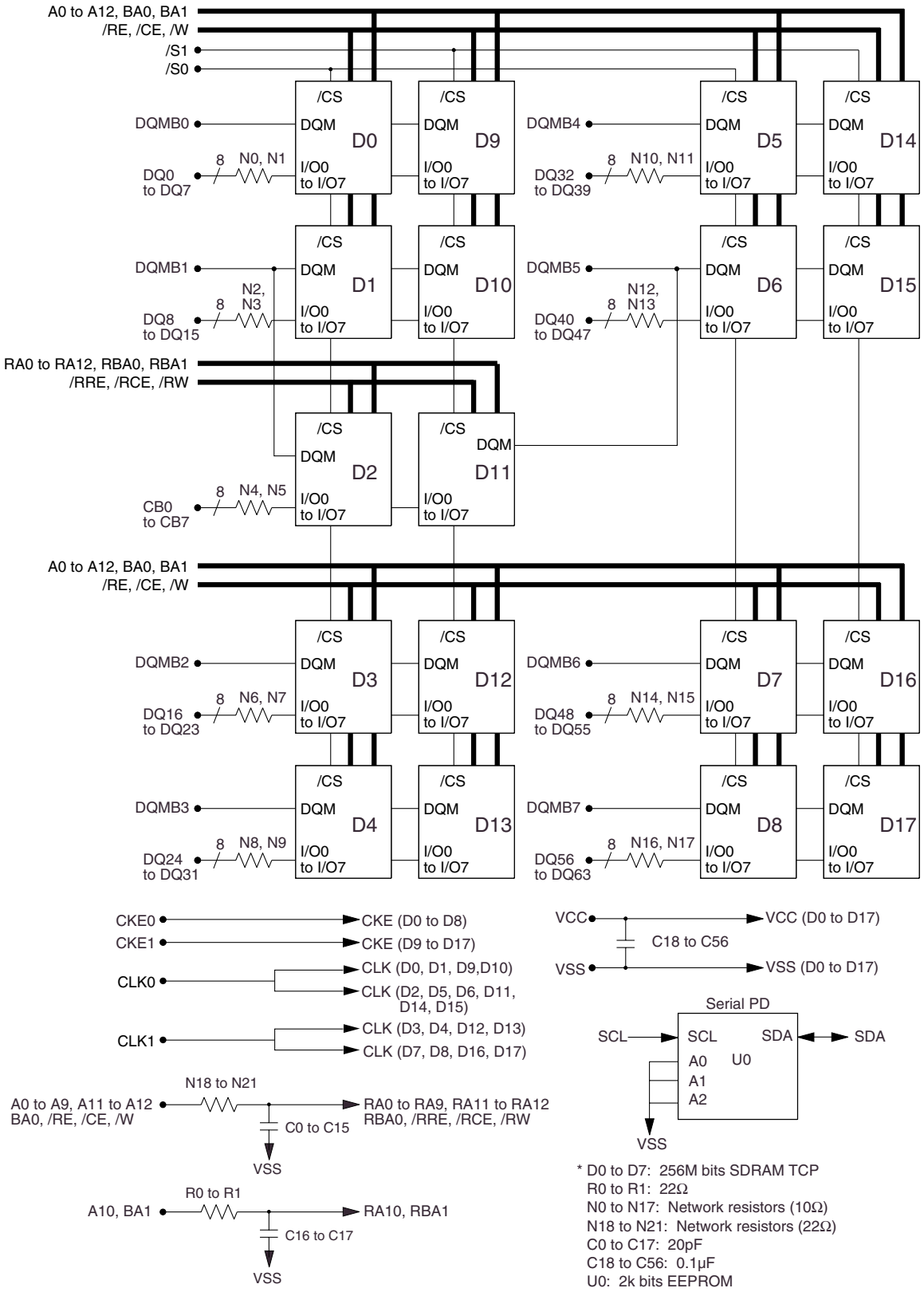
Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
26	SDRAM access from Clock (3rd highest /CE latency) Undefined	0	0	0	0	0	0	0	0	00	
27	Minimum row precharge time	0	0	0	1	0	1	0	0	14	20ns
28	Row active to row active min (-75)	0	0	0	0	1	1	1	1	0F	15ns
	(-A6)	0	0	0	1	0	1	0	0	14	20ns
29	/RE to /CE delay min	0	0	0	1	0	1	0	0	14	20ns
30	Minimum /RE pulse width (-75)	0	0	1	0	1	1	0	1	2D	45ns
	(-A6)	0	0	1	1	0	0	1	0	32	50ns
31	Density of each bank on module	0	1	0	0	0	0	0	0	40	256M byte
32	Address and command signal input setup time (-75)	0	0	0	1	0	1	0	1	15	1.5ns
	(-A6)	0	0	1	0	0	0	0	0	20	2.0ns
33	Address and command signal input hold time (-75)	0	0	0	0	1	0	0	0	08	0.8ns
	(-A6)	0	0	0	1	0	0	0	0	10	1.0ns
34	Data signal input setup time (-75)	0	0	0	1	0	1	0	1	15	1.5ns
	(-A6)	0	0	1	0	0	0	0	0	20	2.0ns
35	Data signal input hold time (-75)	0	0	0	0	1	0	0	0	08	0.8ns
	(-A6)	0	0	0	1	0	0	0	0	10	1.0ns
36 to 61	Superset information	0	0	0	0	0	0	0	0	00	Future use
62	SPD data revision code	0	0	0	1	0	0	1	0	12	Rev. 1.2B
63	Checksum for bytes 0 to 62 (-75)	0	1	0	1	1	1	0	1	5D	93
	(-A6)	1	1	0	0	0	1	0	0	C4	196
64	Manufacturer's JEDEC ID code	0	0	0	0	0	1	1	1	07	HITACHI
65 to 71	Manufacturer's JEDEC ID code	0	0	0	0	0	0	0	0	00	
72	Manufacturing location	×	×	×	×	×	×	×	×	××	*2 (ASCII-8bit code)
73	Manufacturer's part number	0	1	0	0	1	0	0	0	48	H
74	Manufacturer's part number	0	1	0	0	0	0	1	0	42	B
75	Manufacturer's part number	0	0	1	1	0	1	0	1	35	5
76	Manufacturer's part number	0	0	1	1	0	0	1	0	32	2
77	Manufacturer's part number	0	1	0	1	0	0	1	0	52	R
78	Manufacturer's part number (-75)	0	1	0	0	0	1	1	0	46	F
	(-A6)	0	1	0	0	0	1	0	0	44	D
79	Manufacturer's part number	0	0	1	1	0	1	1	0	36	6
80	Manufacturer's part number	0	0	1	1	0	1	0	0	34	4
81	Manufacturer's part number	0	0	1	1	1	0	0	1	39	9
82	Manufacturer's part number	0	1	0	0	0	1	0	0	44	D
83	Manufacturer's part number	0	1	0	0	0	0	1	1	43	C
84	Manufacturer's part number	0	0	1	0	1	1	0	1	2D	—

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
85	Manufacturer's part number (-75)	0	0	1	1	0	1	1	1	37	7
	(-A6)	0	1	0	0	0	0	0	1	41	A
86	Manufacturer's part number (-75)	0	0	1	1	0	1	0	1	35	5
	(-A6)	0	0	1	1	0	1	1	0	36	6
87	Manufacturer's part number	0	1	0	0	0	0	1	0	42	B
88	Manufacturer's part number (-xxB)	0	0	1	0	0	0	0	0	20	(Space)
	(-xxBL)	0	1	0	0	1	1	0	0	4C	L
89	Manufacturer's part number	0	0	1	0	0	0	0	0	20	(Space)
90	Manufacturer's part number	0	0	1	0	0	0	0	0	20	(Space)
91	Revision code	0	0	1	1	0	0	0	0	30	Initial
92	Revision code	0	0	1	0	0	0	0	0	20	(Space)
93	Manufacturing date	×	×	×	×	×	×	×	×	××	Year code (BCD)
94	Manufacturing date	×	×	×	×	×	×	×	×	××	Week code (BCD)
95 to 98	Assembly serial number	*3									
99 to 125	Manufacturer specific data	—	—	—	—	—	—	—	—	—	*4
126	Intel specification frequency	0	1	1	0	0	1	0	0	64	100MHz
127	Intel specification /CE# latency support	1	1	0	0	1	1	1	1	CF	CL = 2, 3

Notes: 1. All serial PD data are not protected. 0: Serial data, "driven Low", 1: Serial data, "driven High". These SPD are based on Rev.1.2B specification.

2. Byte72 is manufacturing location code. (ex: In case of Japan, byte72 is 4AH. 4AH shows "J" on ASCII code.)
3. Bytes 95 through 98 are assembly serial number.
4. All bits of 99 through 125 are not defined ("1" or "0").

Block Diagram



* D0 to D7: 256M bits SDRAM TCP
R0 to R1: 22Ω
N0 to N17: Network resistors (10Ω)
N18 to N21: Network resistors (22Ω)
C0 to C17: 20pF
C18 to C56: 0.1µF
U0: 2k bits EEPROM

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to VSS	VT	–0.5 to VCC + 0.5 (≤ 4.6 (max.))	V	1
Supply voltage relative to VSS	VCC	–0.5 to +4.6	V	1
Short circuit output current	IOUT	50	mA	
Power dissipation	PT	9.0	W	
Operating temperature	Topr	0 to +65	°C	
Storage temperature	Tstg	–55 to +125	°C	

Note: 1. Respect to VSS.

DC Operating Conditions (TA = 0 to +65°C)

Parameter	Symbol	min.	max.	Unit	Note
Supply voltage	VCC	3.0	3.6	V	1, 2
	VSS	0	0	V	3
Input high voltage	VIH	2.0	VCC + 0.3	V	1, 4
Input low voltage	VIL	–0.3	0.8	V	1, 5
Ambient illuminance	—	—	100	lx	

Notes: 1. All voltage referred to VSS.
2. The supply voltage with all VCC pins must be on the same level.
3. The supply voltage with all VSS pins must be on the same level.
4. VIH (max.) = VCC + 2.0V for pulse width ≤ 3ns at VCC.
5. VIL (min.) = VSS – 2.0V for pulse width ≤ 3ns at VSS.

DC Characteristics 1 (TA = 0 to 65°C, VCC = 3.3V ± 0.3V, VSS = 0V)

Parameter	Symbol	Grade	Max.	Unit	Test conditions	Notes
Operating current (CL = 2)	ICC1	-75 -A6	1260 1125	mA	Burst length = 1 tRC = min.	1, 2, 3
(CL = 3)	ICC1	-75 -A6	1260 1125	mA		
Standby current in power down	ICC2P		54	mA	CKE0 = VIL, tCK = 12ns	6
Standby current in power down (input signal stable)	ICC2PS		36	mA	CKE0 = VIL, tCK = ∞	7
Standby current in non power down	ICC2N		360	mA	CKE0, /S = VIH, tCK = 12ns	4
Active standby current in power down	ICC3P		72	mA	CKE0, /S = VIH, tCK = 12ns	1, 2, 6
Active standby current in non power down	ICC3N		540	mA	CKE0, /S = VIH, tCK = 12ns	1, 2, 4
Burst operating current (CL = 2)	ICC4	-75 -A6	1170 1170	mA	tCK = min., BL = 4	1, 2, 5
(CL = 3)	ICC4	-75 -A6	1485 1170	mA		
Refresh current	ICC5		2250	mA	tRC = min.	3
Self refresh current	ICC6		54	mA	VIH ≥ VCC – 0.2V VIL ≤ 0.2V	8
Self refresh current (L-version)	ICC6		36	mA		

Notes: 1. ICC depends on output load condition when the device is selected. ICC (max.) is specified at the output open condition.
2. One bank operation.
3. Input signals are changed once per one clock.
4. Input signals are changed once per two clocks.
5. Input signals are changed once per four clocks.
6. After power down mode, CK0/CK1 operating current.
7. After power down mode, no CK0/CK1 operating current.
8. After self refresh mode set, self refresh current.

DC Characteristics 2 (TA = 0 to 65°C, VCC = 3.3V ± 0.3V, VSS = 0V)

Parameter	Symbol	Grade	min.	Max.	Unit	Test conditions	Notes
Input leakage current	ILI		–10	10	µA	0 ≤ Vin ≤ VCC	
Output leakage current	ILO		–10	10	µA	0 ≤ Vout ≤ VCC DQ = disable	
Output high voltage	VOH		2.4	—	V	IOH = –4 mA	
Output low voltage	VOL		—	0.4	V	IOL = 4 mA	

Pin Capacitance (TA = 25°C, VCC = 3.3V ± 0.3V)

Parameter	Symbol	Pins	max.	Unit	Notes
Input capacitance	CIN	Address	110	pF	1, 2, 4
Input capacitance	CIN	/RE, /CE, /W,	110	pF	1, 2, 4
Input capacitance	CIN	/S0, /S1, CK0, CK1, CKE0, CKE1	65	pF	1, 2, 4
Input capacitance	CIN	DQMB	30	pF	1, 2, 4
Input/Output capacitance	CI/O	DQ, CB	27	pF	1, 2, 3, 4

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. Measurement condition: f = 1MHz, 1.4V bias, 200mV swing.
3. DQMB = VIH to disable Data-out.
4. This parameter is sampled and not 100% tested.

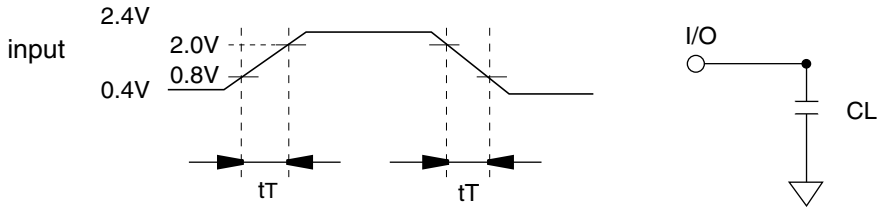
AC Characteristics (TA = 0 to 65°C, VCC = 3.3V ± 0.3V, VSS = 0V)

			-75		-A6			
Parameter	Symbol	PC100 Symbol	min.	max.	min.	max.	Unit	Notes
System clock cycle time (CL = 2)	tCK	Tclk	10	—	10	—	ns	1
(CL = 3)	tCK	Tclk	7.5	—	10	—	ns	
CK high pulse width	tCKH	Tch	2.5	—	3	—	ns	1
CK low pulse width	tCKL	Tcl	2.5	—	3	—	ns	1
Access time from CK (CL = 2)	tAC	Tac	—	6	—	6	ns	1, 2
(CL = 3)	tAC	Tac	—	5.4	—	6	ns	
Data-out hold time	tOH	Toh	2.7	—	3	—	ns	1, 2
CK to Data-out low impedance	tLZ		2	—	2	—	ns	1, 2, 3
CK to Data-out high impedance	tHZ		—	5.4	—	6	ns	1, 4
Input setup time	tAS, tCS, tDS, tCES	Tsi	1.5	—	2	—	ns	1, 5
CKE setup time for power down exit	tCESP	Tpde	1.5	—	2	—	ns	1
Input hold time	tAH, tCH, tDH, tCEH	Thi	0.8	—	1	—	ns	1
Ref/Active to Ref/Active command period	tRC	Trc	67.5	—	70	—	ns	1
Active to Precharge command period	tRAS	Tras	45	120000	50	120000	ns	1
Active command to column command (same bank)	tRCD	Trcd	20	—	20	—	ns	1
Precharge to active command period	tRP	Trp	20	—	20	—	ns	1
Write recovery or data-in to precharge lead time	tDPL	Tdpl	15	—	20	—	ns	1
Active (a) to Active (b) command period	tRRD	Trrd	15	—	20	—	ns	1
Transition time (rise and fall)	tT		1	5	1	5	ns	
Refresh period	tREF		—	64	—	64	ms	

Notes: 1. AC measurement assumes tT = 1ns. Reference level for timing of input signals is 1.5V.
2. Access time is measured at 1.5V. Load condition is CL = 50pF.
3. tLZ (min.) defines the time at which the outputs achieves the low impedance state.
4. tHZ (max.) defines the time at which the outputs achieves the high impedance state.
5. tCES defines CKE setup time to CK rising edge except power down exit command.

Test Conditions

- Input and output timing reference levels: 1.5V
- Input waveform and output load: See following figures



Input waveform and output load

Relationship Between Frequency and Minimum Latency

Parameter			-75	-A6	
Frequency (MHz)			133	100	
t_{CK} (ns)	Symbol	PC100 Symbol	7.5	10	Notes
Active command to column command (same bank)	IRCD		3	2	1
Active command to active command (same bank)	IRC		9	7	= [IRAS+ IRP] 1
Active command to precharge command (same bank)	IRAS		6	5	1
Precharge command to active command (same bank)	IRP		3	2	1
Write recovery or data-in to precharge command (same bank)	IDPL	Tdpl	2	2	1
Active command to active command (different bank)	IRRD		2	2	1
Self refresh exit time	ISREX	Tsrx	1	1	2
Last data in to active command (Auto precharge, same bank)	IAPW	Tdal	5	4	= [IDPL + IRP]
Self refresh exit to command input	ISEC		9	7	= [IRC] 3
Precharge command to high impedance (CL = 2)	IHZP	Troh	2	2	
(CL = 3)	IHZP	Troh	3	3	
Last data out to active command (Auto precharge, same bank)	IAPR		1	1	
Last data out to precharge (early precharge) (CL = 2)	IEP		–1	–1	
(CL = 3)	IEP		–2	–2	
Column command to column command	ICCD	Tccd	1	1	
Write command to data in latency	IWCD	Tdwd	0	0	
DQMB to data in	IDID	Tdqm	0	0	
DQMB to data out	IDOD	Tdqz	2	2	
CKE to CK disable	ICLE	Tcke	1	1	
Register set to active command	IRSA	Tmrd	1	1	
/S to command disable	ICDD		0	0	
Power down exit to command input	IPEC		1	1	

Notes: 1. IRCD to IRRD are recommended value.
2. Be valid [DESL] or [NOP] at next command of self refresh exit.
3. Except [DESL] and [NOP]

Pin Functions

CK0, CK1 (input pin): CK is the master clock input to this pin. The other input signals are referred at CK rising edge.

/S0, /S1 (input pin): When /S is Low, the command input cycle becomes valid. When /S is High, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.

/RE, /CE and /W (input pins): Although these pin names are the same as those of conventional DRAM modules, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.

A0 to A12 (input pins): Row address (AX0 to AX12) is determined by A0 to A12 level at the bank active command cycle CK rising edge. Column address (AY0 to AY9) is determined by A0 to A9 level at the read or write command cycle CK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, both banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by BA0, BA1(BA) is precharged.

BA0, BA1 (input pin): BA0, BA1 is a bank select signal (BA). The memory array is divided into bank0, bank1, bank2 and bank3. If BA0 is Low and BA1 is Low, bank0 is selected. If BA0 is Low and BA1 is High, bank1 is selected. If BA0 is High and BA1 is Low, bank2 is selected. If BA0 is High and BA1 is High, bank3 is selected.

CKE0, CKE1 (input pin): This pin determines whether or not the next CK is valid. If CKE is High, the next CK rising edge is valid. If CKE is Low, the next CK rising edge is invalid. This pin is used for power-down mode, clock suspend mode and self refresh mode.

DQMB0 to DQMB7 (input pins): Read operation: If DQMB is High, the output buffer becomes High-Z. If the DQMB is Low, the output buffer becomes Low-Z (The latency of DQMB during reading is 2 clocks).

Write operation: If DQMB is High, the previous data is held (the new data is not written). If DQMB is Low, the data is written (The latency of DQMB during writing is 0 clock).

DQ0 to DQ63 (DQ pins): Data is input to and output from these pins.

CB0 to CB7 (DQ pins): Data is input to and output from these pins.

VCC (power supply pins): 3.3V is applied.

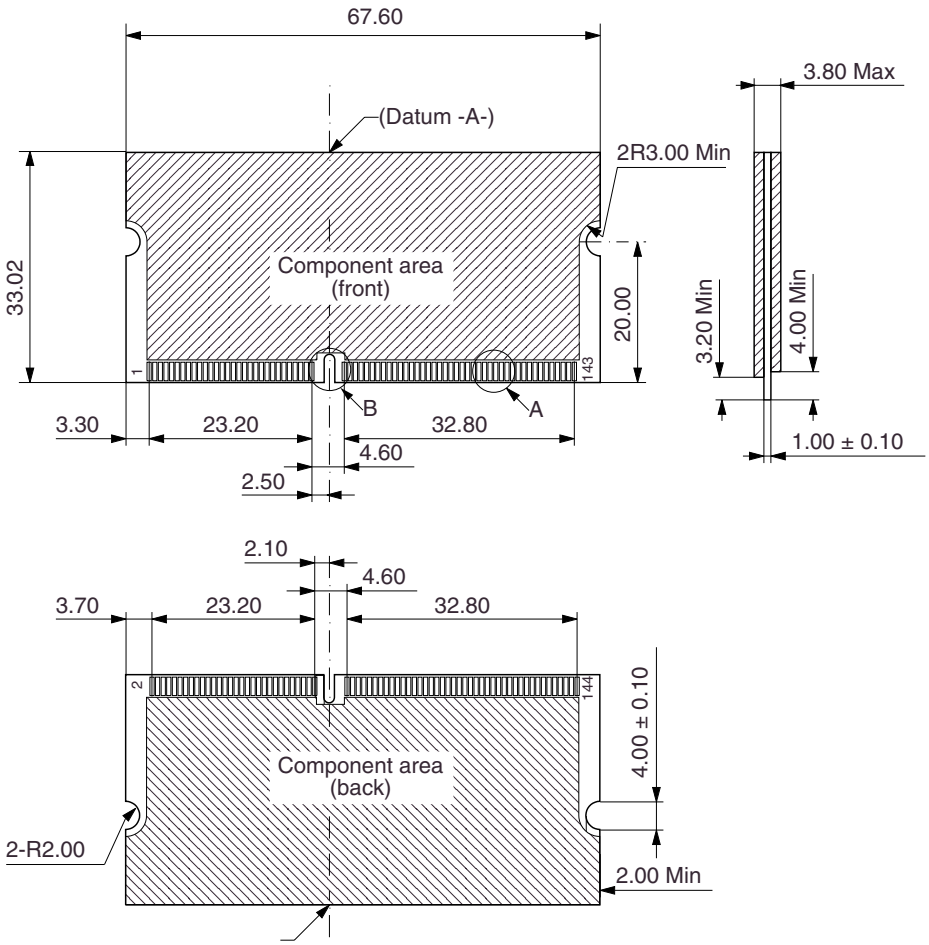
VSS (power supply pins): Ground is connected.

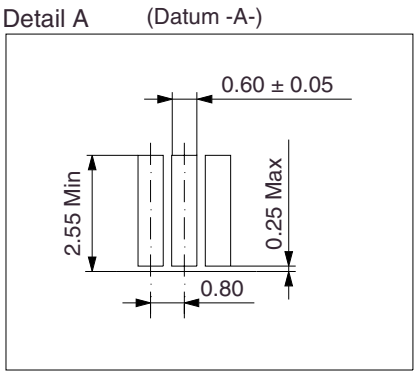
Detailed Operation Part

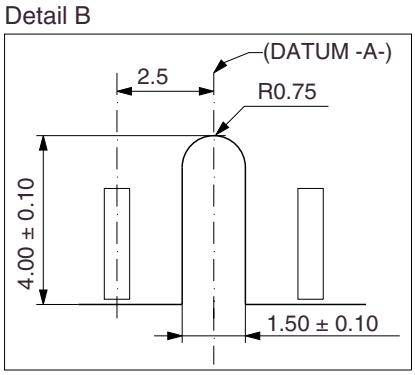
Refer to the HM5225165B/HM5225805B/HM5225405B-75/A6/B6 datasheet.(E0082H)

Physical Outline

Unit: mm







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CAUTION FOR HANDLING MEMORY MODULES

When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory ICs, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stress on these components to prevent damaging them.
In particular, do not push module cover or drop the modules in order to protect from mechanical defects, which would be electrical defects.

When re-packing memory modules, be sure the modules are not touching each other.
Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.

MDE0202

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

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