LAN AND WAN TIMING CONSIDERATIONS FOR PMC-SIERRA ATM PHY DEVICES

APPLICATION NOTE

PRELIMINARY

ISSUE 2

PUBLIC REVISION HISTORY

Issue No.	Issue Date	Details of Change
2		Updated document into new marketing template. Updated requirement references in Section 4 to match the newest revisions of GR-253-CORE. Updated Table 3 to include new SSMs: TNC and ST3E. Updated Section 4.3.2 – Wander Transfer to reflect changes in the GR-253-CORE specification in regards to tolerance for meeting requirements. Added Sections 4.4, and 4.5, to indicate new requirements in the GR-253 regarding SONET NE clock holdover and phase transients. Added OC-48 information to various tables. Updated Section 4.7 History of Requirements to indicate major changes in the GR-253-CORE documentation since the creation of this application note. Updated Section 6.1.5 to reflect changes in standards that now require loop timed equipment to be capable of entering holdover. Updated Table 14. PMC-Sierra Device Jitter and Wander Compliance to include devices developed since 1996. Updated Section 7 A Circuit to Meet WAN Requirements to reflect changes in the PLL implementation.
1	Sep 1996	Document created.

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1 REFERENCES

[1] Bellcore GR-253-CORE –Jan/99, “Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria”

[2] Bellcore GR-436-CORE -June/96, “Digital Network Synchronization Plan”

[3] Bellcore GR-1244-CORE -June/95, “Clock for the Synchronized Network: Common Generic Criteria”

[4] ITU-T G.783, “Characteristic of Synchronous Digital Hierarchy (SDH) Equipment Functional Blocks"

[5] ITU-T G.811-1988, “Timing Requirements at the Outputs of Primary Reference Clocks Suitable for Plesiochronous Operation of International Digital Links”

[6] ITU-T G.812-1988, “Timing Requirements at the Outputs of Slave Clocks Suitable for Plesiochronous Operation of International Digital Links”

[7] ITU-T G.813-1996, “Timing Characteristics of SDH Equipment Slave Clocks”

[8] ITU-T G.821-1988, “Error Performance of an International Digital Connection Forming Part of an Integrated Services Digital Network”

[9] ITU-T G.822-1988, “Controlled Slip Rate Objectives on an International Digital Connection”

[10] ITU-T G.823-1988, “The Control of Jitter and Wander Within Digital Networks Which are Based on the 2048 kbit/s Hierarchy”

[11] ITU-T G.824-1988, “The Control of Jitter and Wander Within Digital Networks Which are Based on the 1544 kbit/s Hierarchy”

[12] ITU-T G.825-1993, “The Control of Jitter and Wander within Digital Networks Which are Based on the Synchronous Digital Hierarchy (SDH)”

[13] ITU-T G.826-1993, “Error Performance Parameters and Objectives for International, Constant Bit Rate Digital Paths at or above the Primary Rate”

[14] ITU-T G.957-1993, “Optical Interfaces for Equipments and Systems relating to the Synchronous Digital Hierarchy”

[15] ITU-T G.958-1994, “Digital Line Systems Based on the Synchronous Digital Hierarchy”

[16] ITU-T I.356-1993, “B-ISDN ATM Layer Cell Transfer Performance”

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[18] ANSI T1.101-1994, “Synchronization Interface Standard”

[19] ANSI T1.105.03-1994, “Synchronous Optical Network (SONET): Jitter at Network Interfaces”

[20] ANSI T1.105.03-1994, “Synchronous Optical Network (SONET): Jitter at Network Interfaces DS1 Supplement”

[21] ANSI T1.105.03a-1995, “Synchronous Optical Network (SONET): Jitter at Network Interfaces DS1 Supplement”

[22] ANSI T1.105.09-1995, “Timing and Synchronization”

[23] ANSI T1.646-1995, “Physical Layer Specification for User-Network Interfaces Including DS1/ATM”

[24] The ATM Forum Technical Committee, af-phy-0046.000, January 1996, “622.08 Mbps Physical Layer Specification”

[25] The ATM Forum Technical Committee, af-saa-0032.000, September 1995, “Circuit Emulation Service Interoperability Specification”

[26] The ATM Forum Technical Committee, af-saa-0049.000, January 1996, “Audiovisual Multimedia Services: Video on Demand Specification 1.0”

2 OVERVIEW

PMC-Sierra's ATM Physical Layer products comply to the North American Synchronous Optical Network (SONET) and the European Synchronous Digital Hierarchy (SDH) framing formats. Local Area Network (LAN) systems designed with these devices can easily be interfaced to SONET/SDH-based Wide Area Network (WAN) equipment without the need for data format conversion; more traditional LAN technologies, such as Ethernet, require some form of format conversion or encapsulation in order to be carried over the WAN. However, even with compatible data formats, the LAN equipment at this interface needs to satisfy certain WAN timing requirements. LAN equipment may be connected to the WAN via a "gateway" or by making the LAN network elements part of the WAN. In either case, the gateway or the LAN element is now part of the WAN, and this Network Element (NE) now has to deal with specific WAN timing issues such as jitter accumulation and wander (low frequency jitter).

Timing requirements for the LAN are usually not an issue. Local area networks connect points physically close together, typically less than 100 meters to no more than 1-2 km. Because of their proximity, these connections are usually implemented with few or no repeaters. There is typically one source of timing that is used to time all nodes, and as a result, jitter accumulation and timing issues due to wander do not exist.

Metropolitan Area Networks (MAN) typically cover larger distances, up to 100 km. These networks can have a large number of repeaters, so jitter accumulation can pose a problem. In this case, WAN jitter-related specifications for NE should be observed. The distances covered are not large enough to cause significant wander-related problems.

Wide Area Networks cover even larger distances and consist of large numbers of NE and repeaters. Jitter accumulation in these networks is significant and the NE should satisfy jitter-related requirements for the particular type of WAN. Synchronous WAN (i.e., SONET based) will also experience problems related to wander, therefore, the NE should satisfy the wander-related requirements for SONET NE. To meet the wander specification, the transmit clock synthesis must utilize a narrow Phase Locked Loop (PLL) bandwidth.

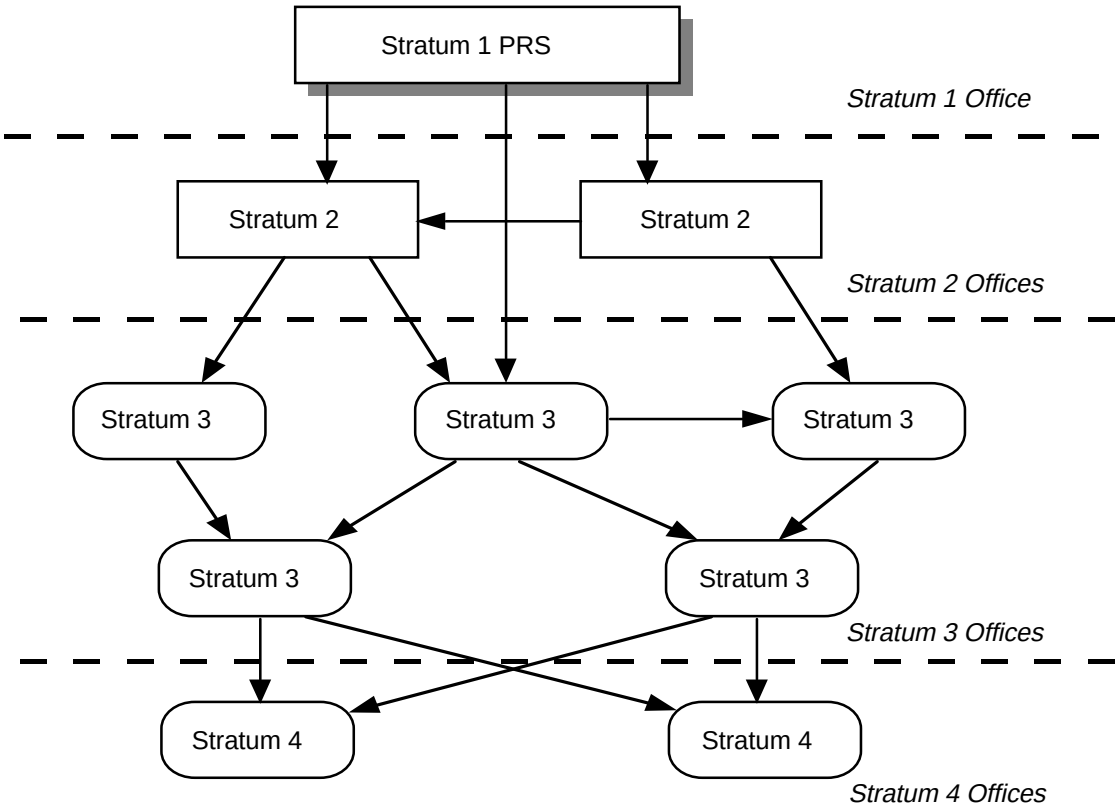
Most of this application note deals with addressing the North American SONET timing requirements. The European SDH requirements are somewhat different due to SDH not using the traditional North American hierarchical timing distribution scheme.

3 BACKGROUND AND DEFINITIONS

3.1 Network Synchronization

In the past, a method of synchronizing the North American digital network was specified to handle the timing requirements of digital communications. These requirements were defined in Bellcore GR-436-CORE Digital Network Synchronization Plan. This plan defined a hierarchical network based on stratified clocks. At the top of the network hierarchy there are the Stratum 1, or Primary Reference Source (PRS), clocks that are used to reference Stratum 2 clocks. These Stratum 2 clocks, in turn, reference Stratum 3 clocks. This is illustrated in Figure 1.

Figure 1. Timing Hierarchy



The quality of these clocks is shown in Table 1 and Table 2. The hierarchy dictates that equipment be timed by either a higher layer stratum clock (lower stratum number) or a peer layer clock that itself is timed to a higher stratum layer. A new stratum clock is being defined; the SONET Minimum Clock (SMC).

Table 1. Stratum Timing

Stratum Level	Free-Run Accuracy (ppm)	Holdover Stability (ppm)	Pull-in/ Hold-in (min ppm) [1]	Typical Clock Source
1	$\pm 10^{-5}$	N/A	N/A	Cesium beam atomic clock
2	$\pm 1.6 \infty 10^{-2}$	$\pm 1 \infty 10^{-4}$ per day	capable of sync'ing to clock with accuracy of $\pm 1.6 \infty 10^{-2}$	Double Oven VCXO or Rubidium atomic oscillators, digital long time constants
3E	± 4.6	$\pm 1 \infty 10^{-2}$	capable of sync'ing to clock with accuracy of ±4.6	Ovenized or TC VCXO with better stability in holdover than stratum 3
3	± 4.6	<255 slips during first day of holdover	capable of sync'ing to clock accuracy of ±4.6	Ovenized or TC VCXO
SMC	± 20	Under Study. See Section 4.4 for details.	capable of sync'ing to clock accuracy of ±20	VCXO
4E	± 32	no holdover	capable of sync'ing to clock accuracy of ±32	VCXO
4	± 32	no holdover	capable of sync'ing to clock accuracy of ±32	VCXO

Table 2. Stratum Timing cont'd

Stratum Level	Filtering of Clock	Transient Response
1	N/A	N/A
2	Yes (f_c= 0.01Hz)	MTIE ≤ 150ns (see Figure 15)
3E	Yes (f_c= 0.01Hz)	MTIE ≤ 150ns (see Figure 15)
3	No (f_c= 3Hz)	MTIE ≤ 150ns and Phase Change slope ≤81ns in any 1.326ms interval
SMC	MTIE, TDEV per GR-253 (f_c= 0.1Hz)	MTIE ≤ 1µs (see Figure 15)
4E	No	MTIE ≤ 1µs and Phase Change slope ≤81ns in any 1.326ms interval
4	No	No requirement

[1] The clock requires 2x the min ppm pull-in range in order to achieve lock since it may be running at one end of its accuracy range and the reference it is locking to is running at the other end of its range.

3.2 Timing Distribution

Digital network synchronization in North America is based on the Building Integrated Timing Supply (BITS) clock. The BITS unit clock is the master timing supply for an entire building. It is the most accurate and stable clock in the building (i.e. the lowest stratum number clock in the building). The stratified clock in the BITS unit is locked to an "upstream" timing reference such as a PRS, or one of a number of recovered clocks from the incoming digital services. The BITS unit outputs a number of DS-1 framed all-ones signals that are distributed through the building to various equipment. The timing is independent of type of service provided by the equipment. For redundancy, usually two BITS clocks are delivered to time the equipment in the unlikely event that there is a connection failure within the building.

The GR-436-CORE specification requires that the facility data link in the Extended Super Frame (ESF) format be used to carry a *Synchronization Message*, identifying the source of the timing used by the equipment. Equipment that uses a BITS clock as its timing reference is defined to be *externally timed*.

3.3 Evolution of the Network Synchronization Plan

SONET provides a high quality, low bit error rate network. Transport overhead bytes allow Bit Interleaved Parity (BIP) errors and Far End Block Errors[1] (FEBE) to be monitored to check the integrity and quality of the transmission. In addition, the deployment of SONET created the need for new nodes, many of which did not have access to BITS clocks. As a result, the SONET optical signal (OC-N) began being used to carry timing synchronization.

This prompted a need to merge the classic digital network synchronization with the new SONET-based one. In the future, the digital network synchronization will likely be entirely SONET-based, but at present it is a hybrid between the two concepts. It is recommended that, when available, the OC-N signal be used to generate a DS-1 framed all-ones signal as a reference for the BITS unit to, in turn, derive an output DS-1 framed all-ones signal timing source. In addition, a few "rules" are defined for the NE to ensure the compatibility of network synchronization using BITS clocks and SONET-based synchronization:

1) Where BITS timing is available, SONET NE (Network Elements) clocks are *externally* timed to the BITS clock;

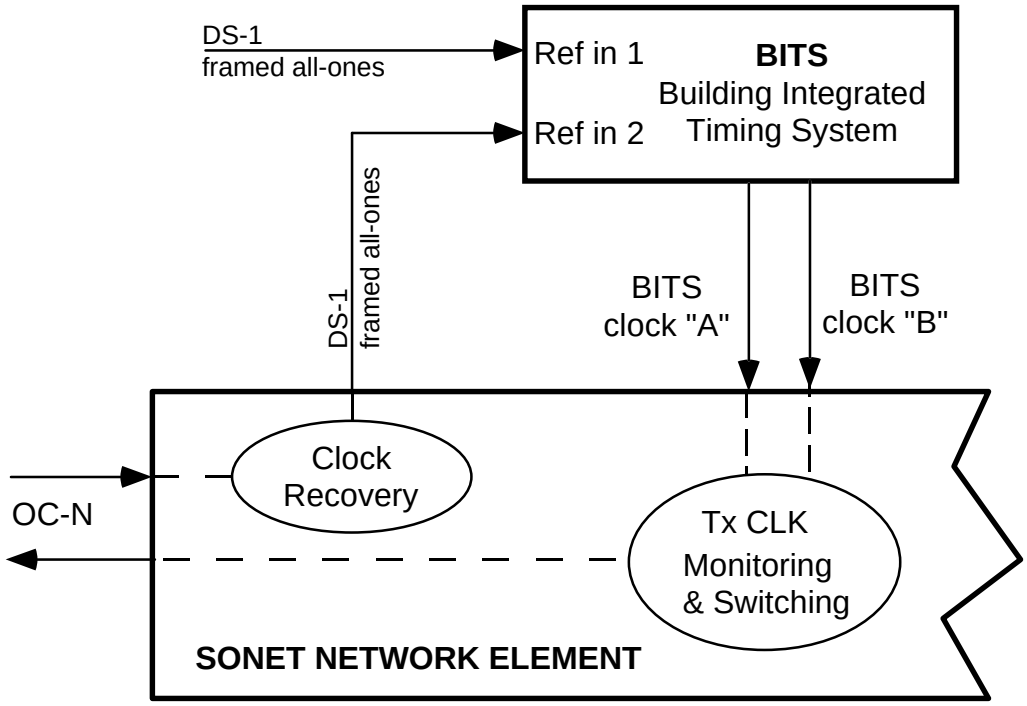
2) External-timing references to a SONET NE are from a BITS clock of stratum 3 or better quality.

[1] An indication of BIP errors occurring at the remote receiver.

3) Where no BITS timing is available, SONET NE clocks are timed from a received OC-N signal;

4) Timing signals delivered to the synchronization network from a SONET NE are derived directly from a terminating OC-N, not a VT1.5 mapped signal.

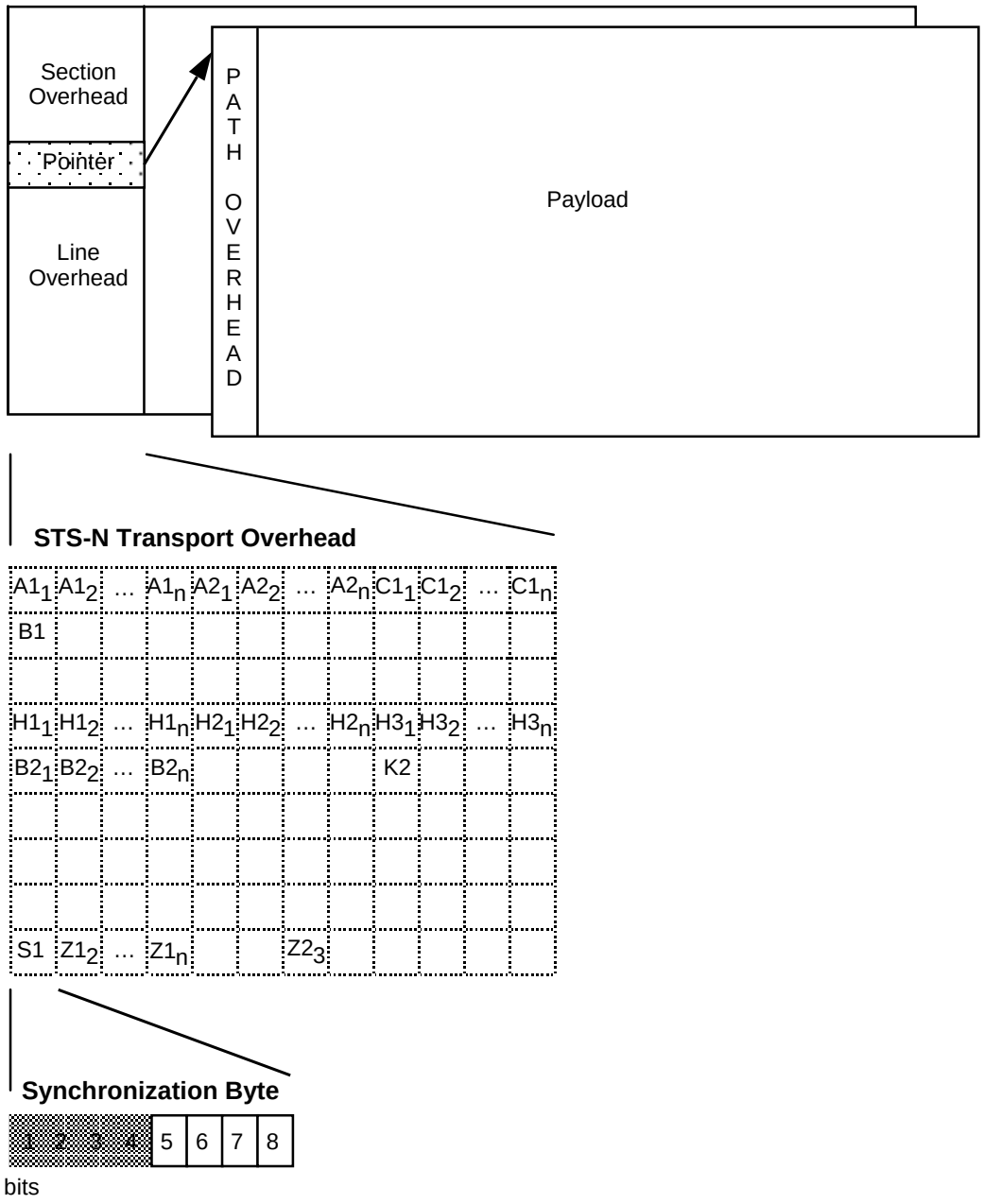
Figure 2. BITS Timing Reference Derived From Incoming OC-N



3.4 Synchronization Messaging

As mentioned previously, the GR-436-CORE specification requires that a *Synchronization Message*, identifying the source of the timing used by the equipment be carried in the ESF facility datalink. SONET has a similar way to carry the synchronization status message, using the lower order nibble (bits 5-8) of the S1 (Z1) byte in the line overhead.

Figure 3. Synchronization Status Byte Location



Synchronization status messages convey clock quality information that allows the SONET network element to select the most suitable synchronization reference from the set of available references. Unlike plesiochronous digital networks that relied on the defined timing hierarchy topology, SONET topology allows for rings which can result in the creation of timing loops.

Figure 4. Generation of Timing Loops In SONET Rings

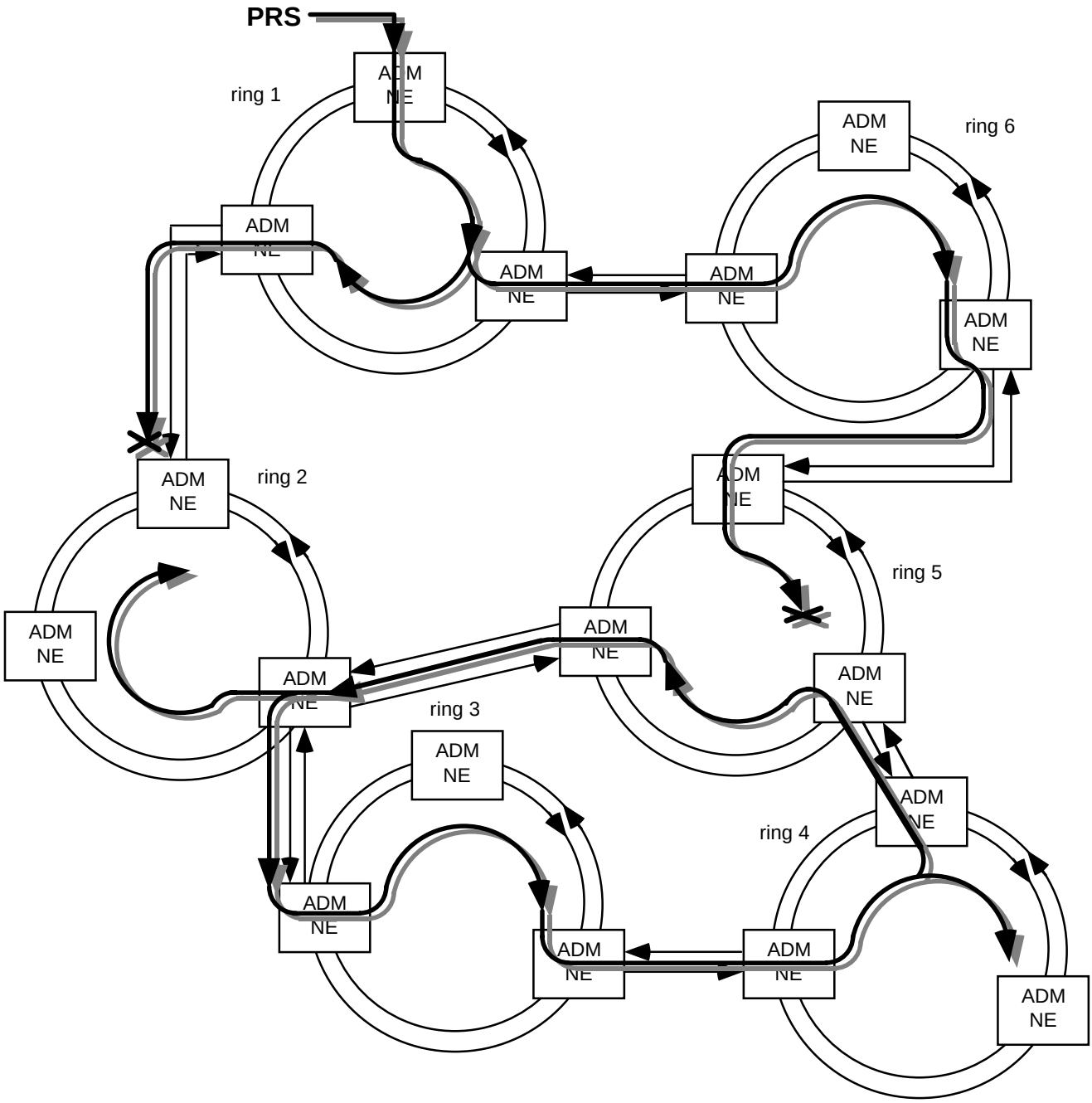


Figure 4 illustrates a potential occurrence of a timing loop. In this example, the head-end (top node, ring 1) is externally timed with a PRS and all other nodes are line timed. Ideally, the nodes interconnecting adjacent rings should all derive their timing from a line such that every node in every ring is ultimately timed back to the

PRS (i.e., the bottom-right node of ring 5 derives its timing from the top node of ring 5, and the timing path from ring 4 to ring 5 does not exist). A possibility exists, through mis-configuration or through an automatic switch of reference timing to an alternate source in the event of signal degradation, that a timing loop is created. Here, a timing loop arises when the bottom-right node of ring 5 changes the source of its derived timing from the active "inner fiber ring" to the line from the top-node of ring 4. The clock frequency in this loop will very slowly change depending on the stability of the oscillators in the node and any perturbations introduced in the loop.

The Synchronization Status Messages (shown in Table 3) were defined to help avoid creating this timing loop by "tagging" each line with an indication of the quality of its timing source. The intent is that each NE choose the better quality level clock to time itself to. However, in a ring topology, the potential to create a loop still exists even with these status messages. Again, using Figure 4 as an example, each node will see each incoming line tagged with the "PRS" status message, indicating that the timing traces back to an externally applied Stratum 1 source. Therefore, any node can decide to reference itself to any number of potential timing sources, including ones that would result in the creation of a loop. To assist in minimizing timing loops GR-253 states that a "SONET NE may be required to be able to be provisioned by the user to ignore the incoming S1 byte at its provisioned reference and/or derived DS1 source." Note that this specification is not a requirement, and careful synchronization planning is still necessary to avoid timing loops.

Table 3. Synchronization Status Messages

Description	Acronym	Quality level	DS-1 FDL Code Word	S1 (bits 5-8)
Stratum 1 Traceable	PRS	1	0000010011111111	0001
Synchronized-Traceability Unknown	STU	2	0000100011111111	0000
Stratum 2 Traceable	ST2	3	0000110011111111	0111
Transit Node Clock Traceable	TNC	4	0111100011111111	0100
Stratum 3E Traceable	ST3E	5	0111110011111111	1101
Stratum 3 Traceable	ST3	6	0001000011111111	1010
SONET Minimum Clock Traceable	SMC	7	0010001011111111	1100
Stratum 4 Traceable	ST4	8	0010100011111111	N/A
Don't Use for Synchronization	DUS	9	0011000011111111	1111
Reserved for Network Synchronization Use	RES	—	0100000011111111	1110

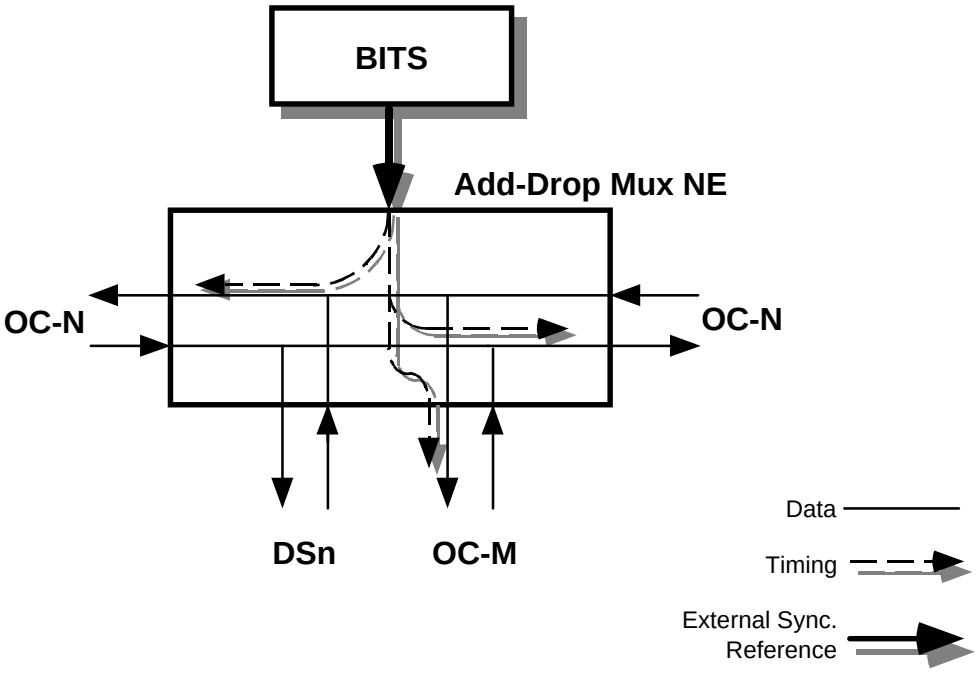
An additional problem with timing can arise due to the use of status messages. Older NE that do not support the Synchronization Status Message in the S1 byte will transmit the default all-zeros SONET overhead byte in the S1 position, resulting in an all-zero status nibble corresponding to the “Synchronized-Traceability Unknown” code. This status message indicates that the timing for this OC-N is synchronized and has a very good quality clock (low Quality Level number), second only to the PRS. A NE receiving this OC-N and this status message would conclude that this timing should be used. However, the older NE originating this “false” message may not be synchronized to any reference and could be free-running with a ± 20 ppm oscillator. Careful synchronization planning is required to avoid this pitfall.

3.5 SONET Timing Modes

SONET offers four timing modes: external, line, loop and through mode.

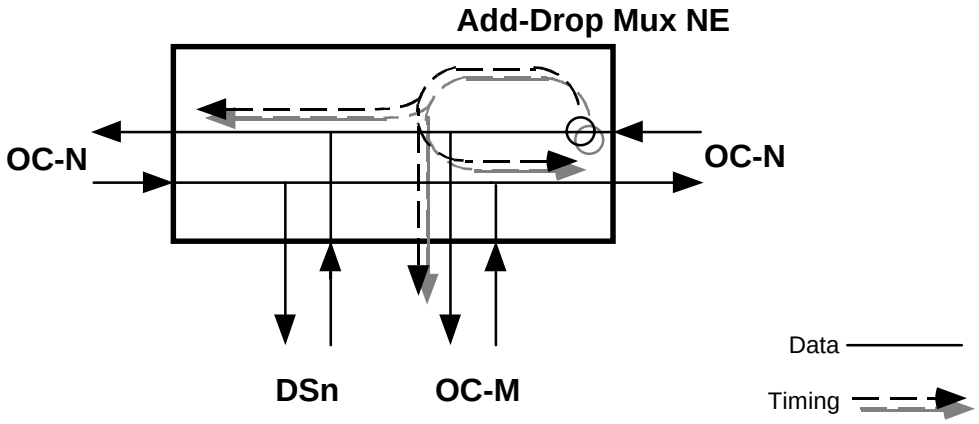
In *external-timing* mode, the BITS clock provides the timing to the NE. The BITS unit can itself be referenced to an OC-N signal or some other timing source.

Figure 5. External Timing Mode



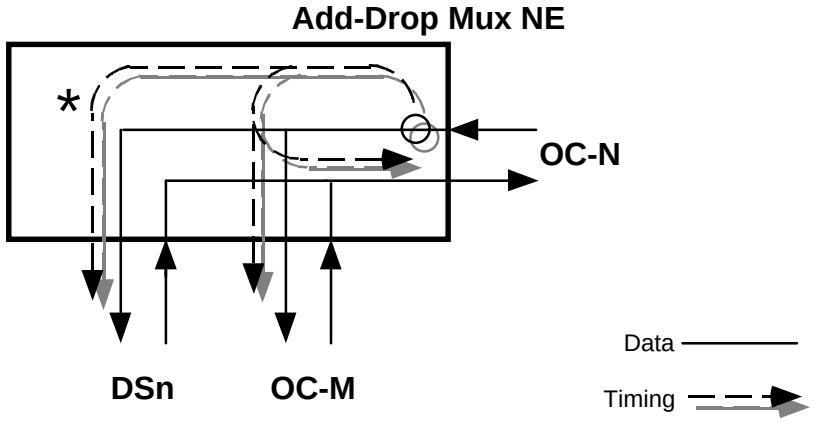
In *line-timing* mode, one of the received OC-N signals is used to derive timing for the entire NE.

Figure 6. Line Timing Mode



The *loop-timing* mode is a special case of the line timing mode. It applies to NE that have only one OC-N interface.

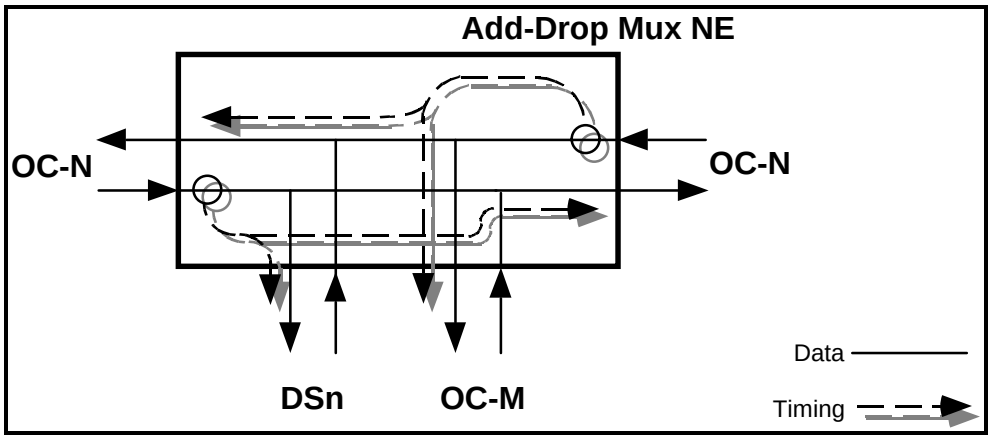
Figure 7. Loop Timing Mode



***** timing used in synchronous mapped;
not used in async mapped.

The *through-timing* mode is the standard timing mode for regenerators. It is not recommended as a timing mode for NE because it creates two timing sources in a network that is supposed to be synchronous.

Figure 8. Through Timing Mode



3.6 WANDER in WAN Timing

3.6.1 Sources of Wander

Digital clocks exhibit pulse position modulation, that is, a deviation of the edges from the ideal clock edge positions . Pulse position modulation frequencies above 10 Hz are defined as jitter, while modulation frequencies below 10 Hz are defined as wander. Jitter is typically attributable to additive Gaussian noise, whereas wander is typically attributable to slowly varying environmental conditions.

The sources of low frequency modulation resulting in wander can be varied; these include changes in operating temperature and $\frac{1}{f}$ (or "flicker"[1]) noise . An oscillator locked to wander-free reference clock in a narrow bandwidth phase lock loop will exhibit wander above the frequencies where the open loop gain is below 0 dB. In digital network synchronization, a very narrow PLL (below 0.1 Hz) is used in order to filter accumulated wander from the PRS to the generated timing reference. These clocks have to satisfy short term stability requirements and limit the amount of wander they produce. In Bellcore and ANSI, the clocks are stratified according to their long term stability and limits are set for short term stability.

Changes in operating temperature cause wander due to the resulting variations in the light propagation properties of the fiber. A light pulse propagates through a long fiber cable with a given velocity. When the index of refraction is changed due

[1] Flicker noise is found in all active devices and in some passive devices. The origins of flicker noise are varied, but its characteristic is a1/f spectrum. This noise is always associated with flow of direct current.

to a temperature variation, the propagation velocity through fiber cable is also changed. Effectively, it looks like the length of the fiber cable is changing and the transmitter is moving away or toward the receiver. This is similar to a Doppler effect; at one end, the transmitted data is sent at one frequency and the data is received at other end with a different frequency. Once the temperature variation stops, the index of refraction settles down to a new value and the transmitted and received frequencies once again become the same.

The LASER output frequency also changes with temperature. Similarly, the propagation delay of the light pulses in the fiber differs with the different wavelengths. This results in a similar frequency differential effect as before.

The resultant magnitude of the wander becomes significant as the length of the fiber increases; for example, in an above-ground fiber cable 250 km long carrying an OC-3 signal, a 20 degree temperature change will result in a 26 bit difference between the transmitted and received data! Appendix A shows the derivation of the temperature effects.

3.6.2 Effects of Wander

The synchronous optical network has several advantages to a plesiochronous network: buffer size is minimal because the receive and transmit rate of OC-N signals are the same; and there is a minimal delay for through traffic because the rate of dropped and added traffic is the same. Although all the nodes run synchronously, two NE are not always operating with exactly the same clock due to jitter and wander effects. SONET uses a concept of pointer movements to allow the Synchronous Payload Envelope (SPE) to run synchronously with the transport overhead. The line overhead bytes H1 and H2 contain a pointer value indicating a relative offset position to the start of the SPE. Pointer movements provide the ability to insert or remove an entire byte of the SPE to rate-adapt it to the transmit line rate; they should happen infrequently.

In Add-Drop Multiplex (ADM) NE, the through-traffic SPE bytes are put into a FIFO buffer together with any add-traffic bytes at that node. These bytes are read from the FIFO using the transmit clock and inserted into the outgoing SONET frame. The number of bytes written to the FIFO and the number of bytes read from the FIFO should be the same. If more bytes are written into the FIFO than are read from it, then eventually the FIFO will overflow and data will be lost. Pointer movements are performed to manage this FIFO depth and to keep it from overflowing.

The FIFO size should be small enough to minimize the delay through it but large enough to tolerate input jitter and infrequent pointer movements. The problems associated with wander are two-fold; a pointer movement (equivalent to 8 UI of

instantaneous jitter) coupled with “normal” line jitter can cause the FIFO to overflow, or a large number of pointer movements can cause the FIFO to overflow. Typically, the overflow will happen at some receiving NE downstream after wander and jitter have had a chance to accumulate, hence the need for wander filtering and control of wander generation.

Finally, even a simple difference in average frequency between the transmit and receive data, although small, can result in substantial phase change if it persists for a long time. This will also introduce pointer movements which, depending upon the FIFO fill levels and accumulated jitter of downstream NE, can result in a FIFO overflow. Although the SONET Minimum Clock (SMC) accuracy is ± 20 ppm, GR-253 notes that payload integrity is not guaranteed for frequency offsets larger than ±4.6 ppm. Actually, some Bellcore Client Companies (BCC) may require stratum 3 clocks for SONET NEs used in applications that do not explicitly require stratum 3 clocks (such as ATM). It is advisable to use stratum 3 clocks when interfacing LAN services to the WAN so that the free-running accuracy of the ATM traffic transmit clock will be better than 4.6 ppm and not perturb the pointer positions in downstream NE.

Excessive pointer movements culminate in desynchronizer FIFO errors. For example, corruption of the DS1 streams mapped into VT1.5 tributaries by pointer movements in the desynchronizer will cause downstream network impairments (i.e., loss of frame). In ATM payloads carried over SONET, excessive pointer movement should not present a problem. Nevertheless a SONET network is designed to carry both ATM and VT-mapped payloads; ATM services are burdened with the synchronization requirements for VT structured SPEs.

4 STANDARDS REQUIREMENTS

4.1 What do the Standards bodies want?

For proper operation of the WAN network, NE timing circuits must meet the following:

- satisfy requirements for frequency accuracy, stability, pull-in and hold-in;
- configurable for various timing modes;
- designed for high reliability (i.e., redundancy);
- transition “gracefully” when switching from one timing reference to another;
- provide filtering of wander and jitter;
- high tolerance to incoming wander and jitter; and
- minimize generation of jitter and wander.

4.2 Clock Stratification and Reliability:

As mentioned previously, GR-1244-CORE defines different layers of clocks with various degrees of accuracy and stability. In North America, the master-slave network synchronization approach is used, which defines certain pull-in and hold-in ranges for each stratified clock. These ranges are required to ensure that a certain level clock can lock to a reference clock of the same or better stratum level. There is also a requirement for the stratum clock to reject a reference that is outside the frequency band defined by the pull-in and hold-in range (this frequency band is approximately three times the free-run accuracy range of the clock).

In a WAN NE, a timing failure can result in loss of a large amount of traffic and potential revenue. Therefore, it is important to provide redundancy for NE timing circuitry, usually in the form of two separate synchronization cards. One card acts as a timing master and supplies the clock to all NE interfaces as well as to the slave synchronization card. In the case of a master card failure, the slave card will take over and supply the clock to all interface cards. This is explained fully in section 3.3, Duplication of Equipment of General Functional Requirements, of [3]; and in section 5.4.4.3.1, Clock Hardware, of [1].

Similarly, to avoid loss of traffic, the transition of timing from one reference to another (as in the case of a redundancy switch or simply a change in timing reference) must be graceful, i.e., it should not cause phase transients above an allowed level. In addition, in the event there is no reference to switch to, holdover requirements should be met. Holdover requires that the timing circuitry maintain the last known good frequency for as long as possible once the reference is lost. Holdover frequency stability is defined for a period of 24 hours over a temperature range. This temperature range differs for different types of equipment. For normal central office equipment, ±5 °F variation over a day is considered reasonable. Previous versions of the SONET specifications required a holdover stability of ±4.6 ppm in 24 hours and over ±32 °F; the applicable temperature range depends on the actual operating environment.

4.3 Wander

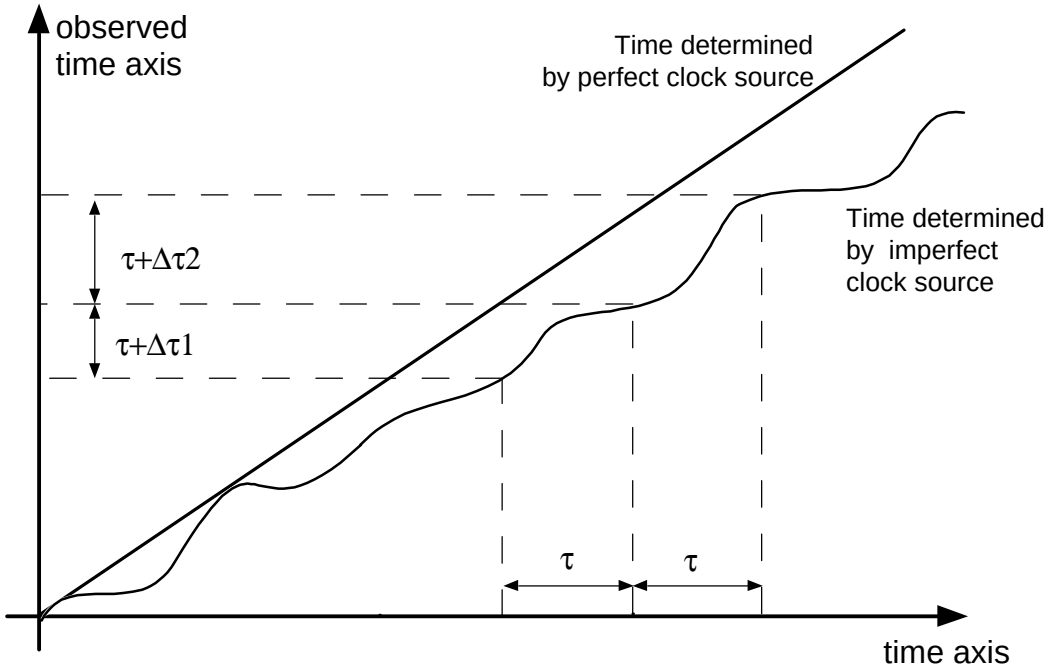
WAN equipment has to satisfy certain requirements regarding wander and jitter. Jitter is a familiar term, used to describe "… the short-term variations of a digital signal's significant instants (e.g., optimum sampling instants) from their ideal positions in time." [3] Wander is defined "… as the long-term variations of the significant instants (e.g., zero level crossings) of a digital signal from their ideal positions in time." [3] The distinction comes down to frequency: jitter is defined at frequencies of 10 Hz and above, while wander is defined at frequencies below 10 Hz . As a result, there is a distinction in the way the limits are specified. Jitter is specified in terms of UI (unit Interval) RMS or Peak-to-Peak, but sometimes it can be specified in units of time (e.g. nanoseconds) or phase (e.g. degrees); wander is specified in terms of Maximum Time Interval Error (MTIE) and Time Deviation (TDEV).

The MTIE is used to describe the frequency offset of a clock from its ideal frequency, and the phase changes of the clock, over an "observation" period. MTIE is in units of nanoseconds of peak-to-peak wander.

The TDEV is used to describe the spectral content of the clock. Its units are RMS nanoseconds of wander.

In order to determine the MTIE and TDEV parameters of a clock, the Time Interval Error (TIE) must be measured. TIE is the time difference between a perfect clock and the observed clock (in Figure 9, below, it is $\Delta\tau 1$, $\Delta\tau 2$, ...).

Figure 9. Definition of Time Interval Error

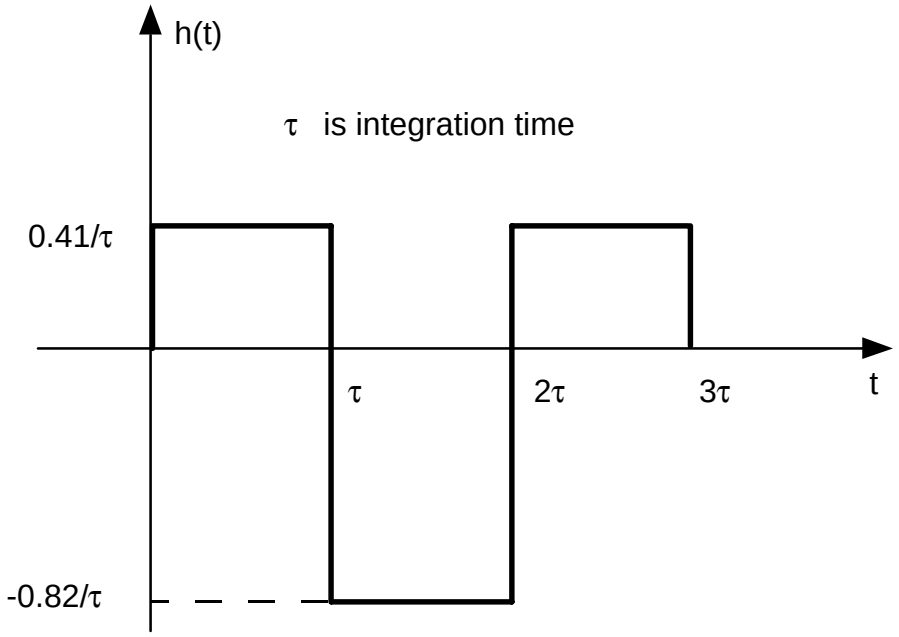


The observation time, τ, can be set to any convenient value (it is independent of clock frequency). At the end of the observation time interval a measure is made of how much the observed imperfect clock has deviated from the perfect clock (the phase difference). Longer observation times should produce larger values of $\Delta\tau$. The MTIE for a certain observation interval is simply the maximum TIE that results from an infinite number of TIE measurements, each performed after a certain observation interval. In practice, only a finite number of measurements can be performed before MTIE is declared. Even so, a measure of MTIE for different observation intervals would require a prohibitively long period of time. Fortunately, MTIE measurements can be performed in a more efficient manner. The maximum wander frequency by definition is 10 Hz so it is possible to completely describe the wander signal up to 10 Hz if the TIE is sampled at twice this rate (the Nyquist rate of 20 Hz – it is probably better to use a higher rate to avoid any aliasing). The TIE can be measured and recorded at 50 ms intervals, then by setting different "sliding windows" equal to different observation intervals, the maximum TIE values can be determined by grouping the measured values into the sliding windows. A constant frequency offset will produce the same MTIE value for a given observation period; MTIE will increase linearly with increasing observation time. MTIE is a good metric of frequency offsets between an observed clock and a perfect clock. It will also show a record of any phase transients (one-shot phase jumps). Increasing observation times will show an increasing MTIE until the

maximum deviation is reached, at which point MTIE will stay at a constant value for larger values of observation time.

MTIE does not reveal how “noisy” the observed clock signal is. The TDEV measurement is used to represent the spectral components of the observed clock. To measure TDEV the same TIE measurements previously collected at 50 ms or faster are used along with digital signal processing filtering to quantify the spectral components. The DSP filter, with impulse response shown below in Figure 10, blocks DC, therefore frequency offsets are not included in this measurement. Any phase transients that may happen do so rarely and any resulting energy from these transients will integrate out over the long integration intervals.

Figure 10. Impulse Response of DSP TDEV Filter



4.3.1 Bellcore GR-253-CORE, January 1999; ANSI T1.101-1994 specifications:

Bellcore and ANSI have specified limits to wander at interfaces to SONET systems. The specifications cover five different areas of wander:

1. Short term stability. This is a measurement of the wander on the outgoing OC-N signal produced by the equipment when the input reference is wander-free.

2. Wander Transfer. This is a measurement of the amount of wander that is transferred from a “wandering” input reference to the outgoing OC-N signal.

The input reference clock wander is modulated to meet a given mask (Figure 11 below).

3. Phase Transient Criteria. When the equipment changes reference, the resulting phase transient will produce wander. No errors should result when switching reference or changing timing modes.

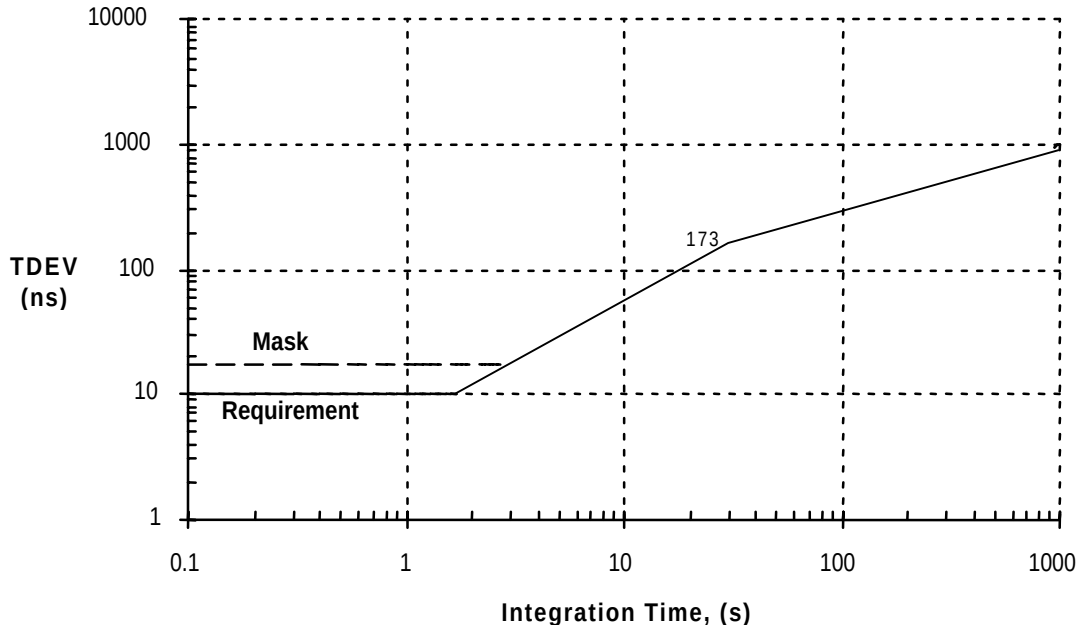
4. Derived DS1 Wander. The OC-N signal can be used to generate DS1 timing (e.g.., for BITS reference), and this process will produce wander even if the OC-N signal is wander-free[1].

5. Interface Wander. ANSI limits the amount of wander on both DS1 and OC-N signals at specific interface points.

4.3.2 Wander Transfer (Bellcore Section 5.4.4.2.4, Req 5-131, 5-132):

OC-N or STS-N electrical outputs referenced to an external timing signal that meets the required TDEV curve, shown below in Figure 11, must be 'less than or equal to' (defined to allow a phase gain of up to 0.2 dB in the pass-band of the clock) the wander TDEV mask, also shown below in Figure 11.

Figure 11. Wander Transfer Requirement



[1] Flicker noise will induce phase fluctuations in a VCXO even with a fixed control voltage.

A SONET NE's output OC-N or STS-N signal must be less than or equal to the mask curve below when referenced to an input OC-N or STS-N signal that meets the required TDEV curve.

4.3.3 Wander Generation (Bellcore Section 5.4.4.3.2, Req 5-134, 5-135):

A SONET NE optical or electrical output must meet the MTIE and TDEV wander curves of Figure 12 and Figure 13. Conformance to this requirement is tested with a wander free external OC-N reference having bandlimited white noise phase modulations (jitter) of 1000 ns p-p. The jitter is bandlimited with 3dB cut-off frequencies at 10 Hz and 150 Hz. This specification tests the short term stability of the clock source. Note that not all VCXO clock sources will be able to meet both wander generation and wander transfer requirements.

Figure 12. MTIE Wander Generation Requirement

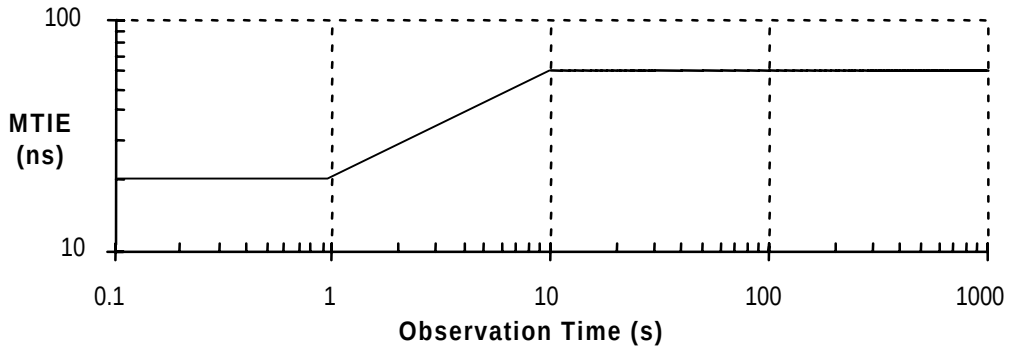
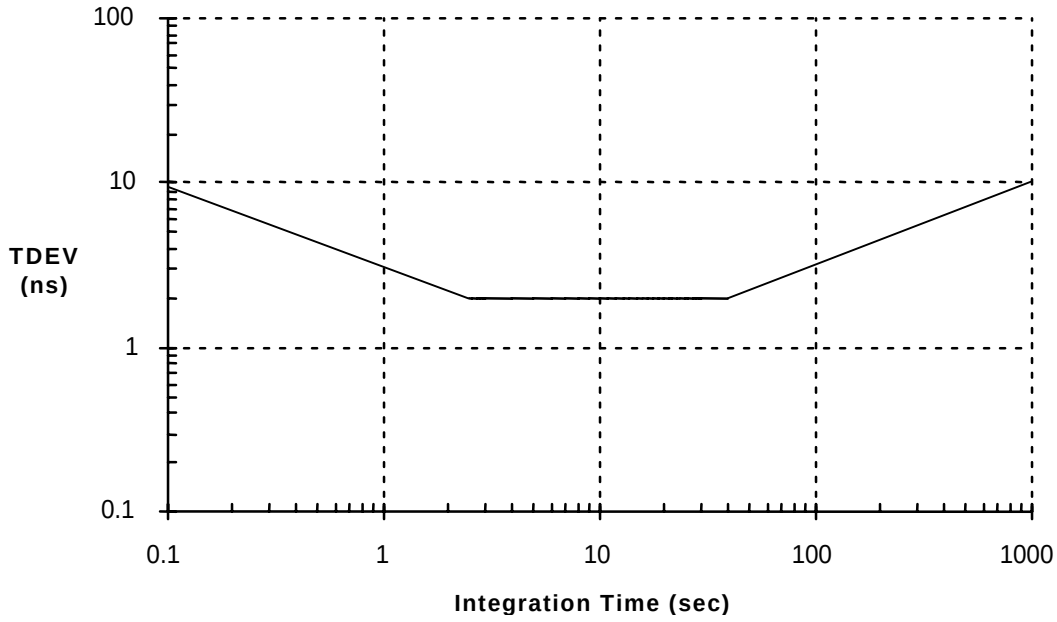


Figure 13. TDEV Wander Generation Requirement



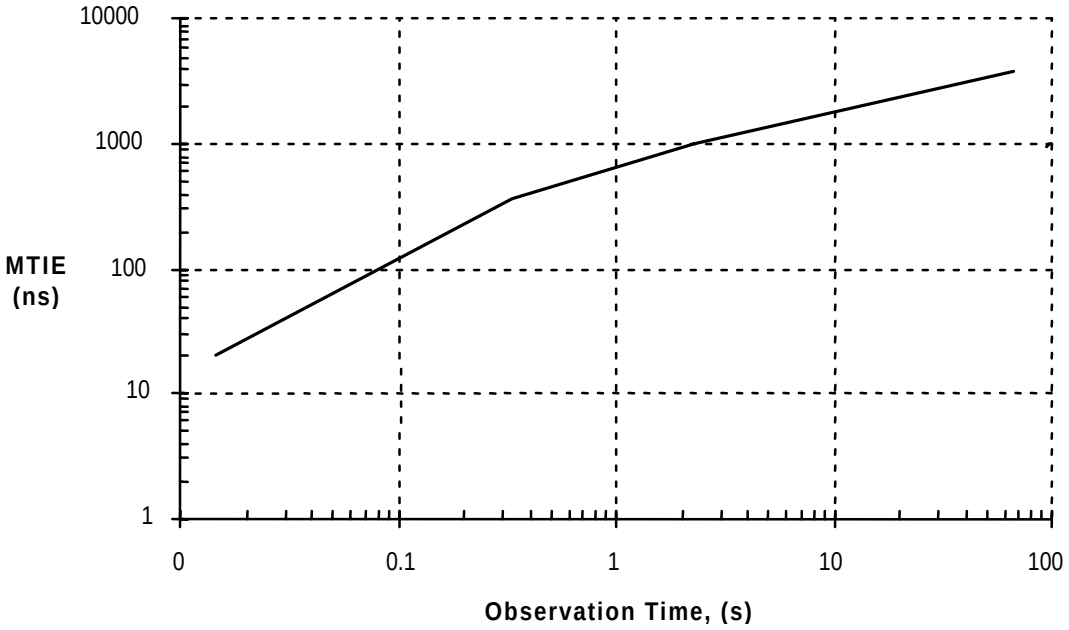
4.4 Clock Holdover GR-253-CORE January 1999 (Section 5.4.4.2.2 Req. 5-122, 5-123)

This section deals with clock holdover specifications for SMCs. Stratum Clocks are specified to meet the criteria outlined in Section 5.4.4.2 of [1]. Note that GR-253 requirements have been revised to require clock holdover compliance in all timing modes. In previous versions loop timed systems were not required to meet clock holdover.

A SONET NE containing an SMC shall be capable of entering holdover when all of its timing references are determined to be failed or contain the “DON’T USE for Synchronization” synchronization status message.

A phase transient may be generated in the first 64 seconds after entry into holdover. Any such transient shall be bounded by the MTIE mask in Figure 14 below. The transient is measured relative to a signal with the frequency of the input reference immediately before the reference loss.

Figure 14. Phase Transient for Entry Into Holdover



Maximum allowable Holdover frequency offsets are shown below in Table 4, and defined in Section 5.2 of [3].

Table 4. Holdover Components for Stratum 3, 3E and SMC.

Component	Stratum 3	Stratum 3E	SMC
Initial Offset	$50x10^{-9}$	$1x10^{-9}$	$50x10^{-9}$
Temperature	$280x10^{-9}$	$10x10^{-9}$	$500x10^{-9}$
Drift	$40x10^{-9}$	$1x10^{-9}$	$4.1x10^{-6}$

Note that the requirements are not as stringent for SMC timed equipment, but all requirements are set to establish a cumulative maximum holdover offset of less than 4.6 ppm for the first 24 hours in the holdover state.

4.5 Phase Transients (GR-253-CORE Section 5.4.4.3.3 Req. 5-136)

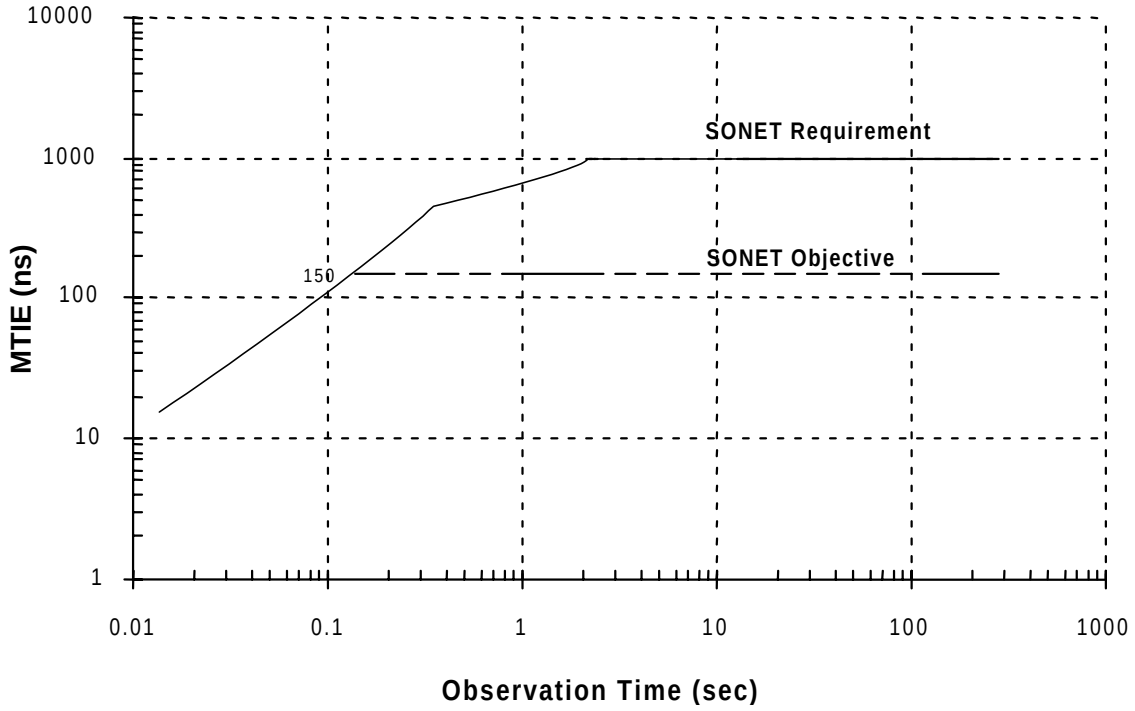
Phase transients are defined in [3] as an unusual sudden change, with respect to the surrounding variations, or step in phase-time of a signal over a period of time. Specifications are in place to minimize the impact of these transients on outgoing signals and on downstream clocks that are timed using these signals. Phase

transients are often associated with rearrangement activity which include the following:

- Manual timing reference switching
- Automatic timing reference switching
- Entry into self-timing operation (free-run or holdover) for the first 2.33 seconds of self-timing.
- Automatic clock diagnostics.
- Clock hardware protection switching.
- Manual or automatic switching between equipment units.
- Phase transients on an external or OC-N synchronization input with the rate of change as specified in ANSI T1.101-1994.

All SONET NE with OC-N/OC-M or STS-N/STS-M electrical outputs shall exhibit an MTIE of no greater than the requirement mask shown below in Figure 15 for OC-N phase transients during synchronization rearrangement operations.

Figure 15. MTIE for Phase Transients from SONET Clocks



4.6 Jitter

Jitter related specifications for SONET/SDH equipment are given in GR-253-CORE, ANSI T1.105, ANSI T1.646 , ITU-T/CCITT G.825, G.958 and G.813. Jitter specifications for ATM equipment are given in the ATM Forum UNI 3.1 specification.

The jitter specifications defined in GR-253-CORE and ITU-T G.825 fall into several categories: interface jitter; jitter generation; jitter tolerance; and jitter transfer.

Interface jitter and jitter generation categories are measured in absolute values of jitter at designated interface points. These are WAN specifications and are required to be met by any equipment used in the WAN. Network planners rely on these values when projecting new routes or changes to existing ones. LAN equipment does not necessarily have to meet these two requirements; however, the ATM Forum UNI specification refers to the GR-253 specifications as a requirement.

Jitter tolerance and jitter transfer categories for WAN equipment are specified based on a hypothetical network model as defined in ITU-T G.801. G.801 specifies a standard digital hypothetical reference connection with a maximum length of 27500 km. These network models are hypothetical entities of defined length and equipment composition for use in studying the effects of digital transmission impairments such as bit errors, jitter and wander, transmission delay, and slips on the overall network performance. These specifications for jitter tolerance and jitter transfer are not absolute and, strictly speaking, are not necessary for equipment to operate correctly. It is a good practice, however, to comply with these specifications so that severe network impairments can be minimized. Again, for LAN applications, the network span is small so jitter tolerance and jitter transfer effects cannot accumulate; there should be no need to meet the WAN specifications for jitter tolerance and jitter transfer. However, the WAN jitter tolerance is useful for determining clock recovery jitter margin in the LAN.

4.6.1 Interface Jitter

4.6.1.1 Bellcore GR-253-CORE Jan 1999 and ANSI T1.105.03-1994: (Bellcore Section 5.6.1, Req 5-226; ANSI Section 5, Table 7)

Timing jitter at the network interface shall not exceed A1 Unit Intervals peak-to-peak (UIpp) when measured over a 60-second interval with a bandpass filter having a high-pass cutoff frequency of B1 and a low-pass cutoff frequency of at least B3; each filter has a roll-off of 20 dB/decade.

Timing jitter at the network interface shall not exceed A2 Unit Intervals peak-to-peak (UIpp) when measured over a 60-second interval with bandpass filter having a high-pass cutoff frequency of B2 and a low-pass cutoff frequency of at least B3; each filter has a roll-off of 20 dB/decade.

Table 5. GR-253 Interface Jitter

OC-N/STS-N level	B1 (Hz)	B2 (kHz)	B3 (MHz)	A1 (UIpp)	A2 (UIpp)
1	100	20	0.4	1.5	0.15
3	500	65	1.3	1.5	0.15
12	1000	250	5	1.5	0.15
48	5000	1000	20	1.5	0.15
48(B)	5000	12	20	1.5	0.15

4.6.1.2 ITU-T /CCITT G.825, March 1993 (Section 3.1, Table 1):

At any SDH network interface, the following jitter specifications must be met:

Timing jitter as measured over a 60-second interval with a bandpass filter with a lower cutoff frequency of f1 and a minimum upper cutoff frequency f4 shall not exceed B1 Unit Intervals (UI) peak-to-peak. Also, timing jitter as measured over a 60-second interval with bandpass filter with a lower cutoff frequency of f3 and a minimum upper cutoff frequency f4 shall not exceed B2 Unit Intervals (UI) peak-to-peak. The roll off at the lower cut-off frequency and upper cut-off frequency shall be 20dB/decade.

Table 6. G.825 Interface Jitter

STM level	f1 (Hz)	f3 (kHz)	f4 (MHz)	B1 (UIpp)	B2 (UIpp)
STM-1	500	65	1.3	1.5	0.15
STM-4	1000	250	5	1.5	0.15
STM-16	5000	Under study	20	1.5	0.15

This is the same specification as in GR-253-CORE.

4.6.1.3 ANSI T1.646 ," Broadband ISDN Physical Layer Specification for User-Network Interfaces, Including DS1/ATM , 1995(Section 7.6 .2..4):

This specification deals with the 155.52 Mbps Physical Layer Interface with LED into Multimode Fiber (MMF) . Here, the interface jitter is specified separately for the transmitter and the receiver in terms of contributions to “eye closure”.

Transmitter Characteristics:

The worst case interface jitter at the transmitter output shall be less than 1.6 ns for systematic jitter and 0.6ns for random jitter.

Rise and fall times of the transmitter should be less than 3.0ns. This specifies one of the bandlimiting factors of the system that influence the receive jitter tolerance. Overshoot is limited to 25 percent.

Receiver Characteristics:

The worst case interface jitter at the receiver input shall be less than 2.0 ns for systematic jitter and 0.6ns for random jitter.

The minimum receiver eye opening shall be 1.23 ns.

4.6.1.4 ATM Forum Technical Committee AF-PHY-0046.000, January 1996 (Section 2):

This specification deals with the 622.08 Mbps Physical Layer.

Single Mode Fiber:

The interface jitter is defined in ANSI T1.646, which points to T1.105.03 which is the same as GR-253-CORE.

Multi-Mode Fiber:

Again, jitter is defined in terms of contributions to eye closure.

Transmitter Characteristic:

The systematic interface jitter at the transmitter output shall be less than 0.40 ns peak-to-peak. (0.249 UI pp).

The random interface jitter at the transmitter output shall be less than 0.15 ns peak-to-peak. (0.093 UI pp).

Receiver Characteristic:

The systematic interface jitter at the receiver input shall be less than 0.50 ns peak-to-peak. (0.311 UI pp).

The random interface jitter at the receiver input shall be less than 0.15 ns peak-to-peak. (0.093 UI pp).

The minimum receiver eye opening at a 10^{-10} BER shall be 0.31ns.

4.6.2 Jitter Generation

A jitter generation criteria exists for both Category I and Category II interfaces. Category I interfaces are defined as asynchronous DSn interfaces to a SONET NE; Category II interfaces are defined as OC-N, STS-N electrical and synchronous DS1 interfaces to a SONET NE (synchronous DS1 interfaces are DS1 interfaces where the incoming DS1 is byte-synchronously mapped into a VT SPE). For Category I interfaces the jitter generation criteria is divided into two areas: mapping jitter generation and pointer adjustment jitter generation. For both Category I and Category II, jitter generation is measured with no jitter or wander applied at the input. Furthermore, a bandpass filter is used to limit the jitter generation measurements. For OC-N and STS-N, the bandpass filter has a 12

kHz highpass cutoff frequency with a roll-off of 20 dB/decade and a lowpass cut-off frequency of at least B3 (from Table 5).

4.6.2.1 Bellcore GR-253-CORE , January 1999 (Section 5.6.2.3.6, Req 5-248):

The jitter generated at Category II interfaces shall be less than 0.01 UI rms, and shall also be less than 0.10 UI pp.

4.6.2.2 ITU-T G.958, November 1994 (Section 9.3.1):

An SDH regenerator shall not generate more than 0.01 UIrms jitter, with no jitter applied at the STM-N input. The measurement bandwidth and technique are under study.

4.6.2.3 ITU-T G.813, August 1996 (Section 7.3):

Jitter generation for optical STM-N output interfaces shall be less than 0.10 UIpp measured with a bandpass filter with characteristics outlined in Table 7 below.

Table 7. G.813 Jitter Generation Requirements

Interface	Measuring filter
STM-1	12kHz to 1.3 MHz
STM-4	12kHz to 5 MHz
STM-16	12kHz to 20MHz

4.6.3 Jitter Tolerance

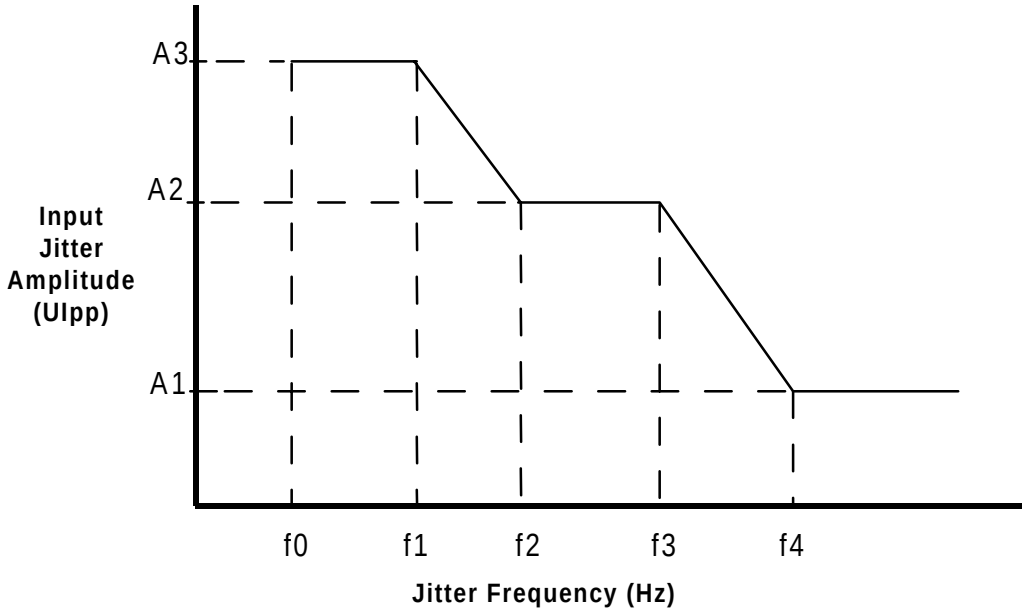
4.6.3.1 Bellcore GR-253-CORE, December 1995 (Section 5.6.2.2.2, Req 5-232, Fig 5-28):

STS-N and OC-N interfaces, with the exception of OC-48 interfaces, shall tolerate, as a minimum, input jitter applied according to the parameters in Table 8 and mask in Figure 16, below.

Table 8. GR-253 Input Jitter Tolerance

OC-N	f0 (Hz)	f1 (Hz)	f2 (Hz)	f3 (Hz)	f4 (Hz)	A1 (UIpp)	A2 (UIpp)	A3 (UIpp)
1	10	30	300	2k	20k	0.15	1.5	15
3	10	30	300	6.5k	65k	0.15	1.5	15
12	10	30	300	25k	250k	0.15	1.5	15
48	10	600	6000	100k	1000k	0.15	1.5	15

Figure 16. Input Jitter Mask



4.6.3.2 ITU-T G.958, November 1994 (Section 9.3.3):

Jitter tolerance in G.958 is defined the same as in GR-253-CORE. The one exception is the 15 UIpp amplitude at low frequency is not required. This specification is valid for ADM and Type A regenerators (i.e., those devices that meet the jitter transfer of Table 12) and is given in Table 9. Type B regenerators (i.e., those devices that meet the jitter transfer of Table 13) have reduced tolerance requirements (Table 10).

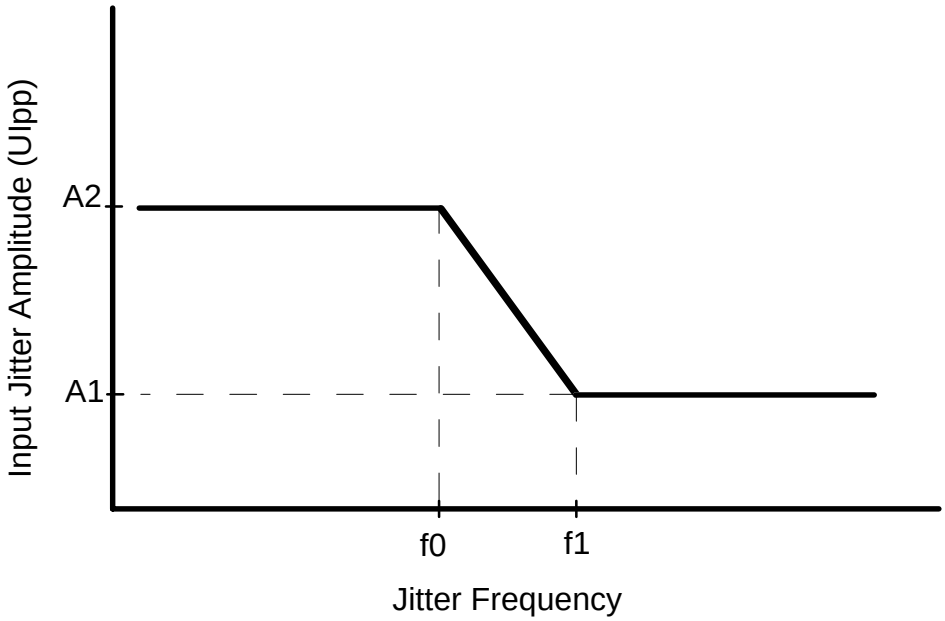
Table 9. G.958 Jitter Tolerance (Type A)

STM-N	f0 (Hz)	f1 (Hz)	A1 (Uipp)	A2 (UIpp)
1	6.5k	65k	0.15	1.5
4	25k	250k	0.15	1.5
16	100k	1M	0.15	1.5

Table 10. G.958 Reduced Jitter Tolerance

STM-N	f0 (Hz)	f1 (Hz)	A1 (Uipp)	A2 (UIpp)
1	1.2k	12k	0.15	1.5
4	1.2k	12k	0.15	1.5
16	1.2k	12M	0.15	1.5

Figure 17. G.958 Input Jitter Tolerance



4.6.4 Jitter Transfer

4.6.4.1 Bellcore GR-253-CORE, January 1999 (Section 5.6.2.1.2, Req 5-230, Fig 5-27):

Jitter transfer parameters shown below in Table 9 for Category II interfaces shall be under the mask in Figure 18:

Figure 18. GR-253 Jitter Transfer Mask.

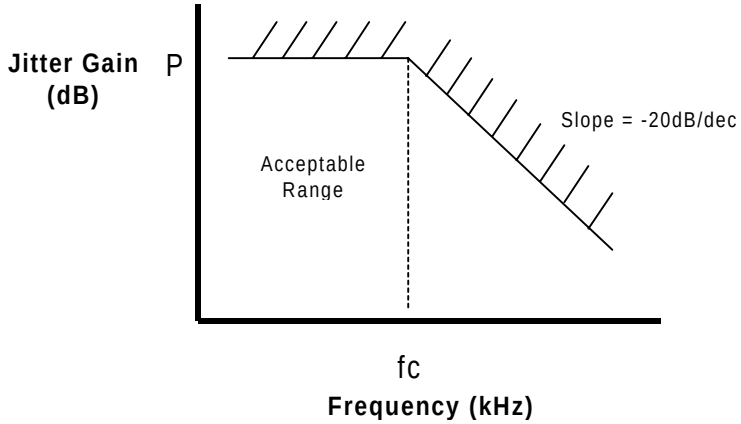


Table 11. GR-253 Jitter Transfer Requirements

OC-N	f0 (kHz)	P (dB)
1	40	0.1
3	130	0.1
12	500	0.1
48	2000	0.1

4.6.4.2 ITU-T G.958, November 1994 (Section 9.3.2):

Jitter transfer requirements for ADM and Type A regenerators (Table 12):

Table 12. G.958 Jitter Transfer (for Type A)

STM-N	f0 (Hz)	P (dB)
1	130k	0.1
4	500k	0.1
16	2000k	0.1

Jitter transfer requirements for type B regenerators (Table 13):

Table 13. G.958 Jitter Transfer (for Type B)

STM-N	f0 (Hz)	P (dB)
1	30k	0.1
4	30k	0.1
16	30k	0.1

4.7 History of Requirements

In North America, the GR-253 specification is constantly evolving. In the past (pre-1994), GR-253 required that all equipment in the WAN meet the specifications for interface jitter, jitter tolerance, intrinsic jitter, and jitter transfer, as well as clocking requirements such as short term stability, interface wander, wander transfer, and holdover. This was a tough specification that required expensive system clocking cards and synchronization.

In December 1994, GR-253 was revised to reduce the timing requirements on equipment that was interfaced to the WAN in *line-timed* mode. In this mode, the transmit timing was derived directly from the received line, so only jitter tolerance, intrinsic jitter and jitter transfer were needed. The requirements for wander and holdover were removed.

Then, in December 1995, GR-253 was again revised, this time to add another requirement for the line-timed mode. In reducing the number of requirements in the Dec. 1994 specification, a problem arose with equipment deriving their timing from the line: in the event the receive line signal is lost, where would the transmit timing come from? Most practical solutions had a back-up timing source, typically an SMC, which would be switched in when the receive signal was lost; however, the SMC and the line timing were not in phase. This caused a *phase transient* to occur in the transmit timing, usually an abrupt phase change which resulted in receiving equipment slipping a bit and going out of frame alignment. This caused network impairment and loss of revenue during the recovery time. Therefore, the Dec 1995 revision added a phase transient requirement dictating that a switch to a back-up transmit clock shall be “hit-less”, i.e., it will not cause a bit error at the receiving equipment.

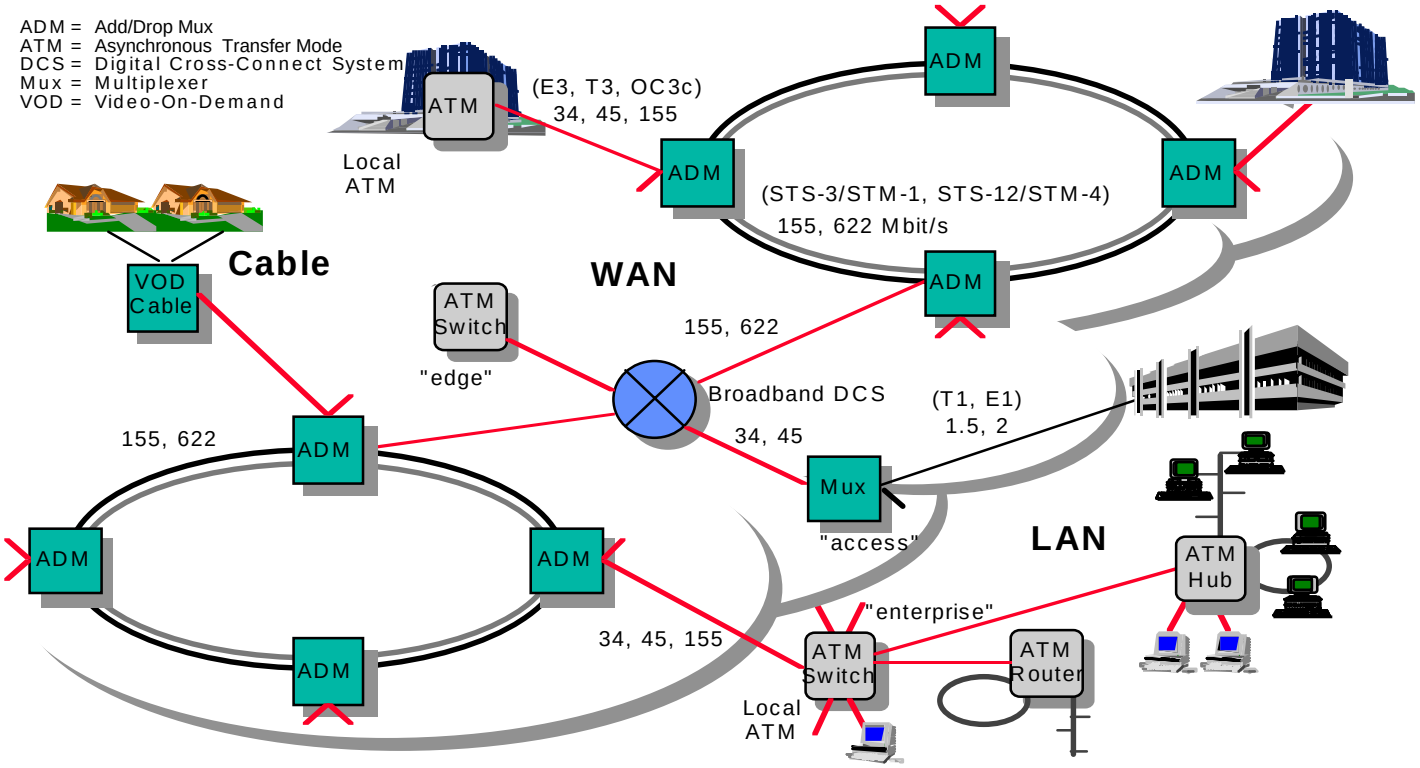
Since the release of the December 1995 Issue 2, GR-253-CORE has undergone two revisions, in January 1997 and January 1999. The revisions applicable to this application note deal mostly with timing requirements: Revision 2 redefines the input signal for testing jitter requirements and changes clock holdover and phase transient requirements to include all SONET NE (including loop timed equipment which was previously exempt). In addition, revisions have been made to allow optional processing of synchronization status messages aiding synchronization planning to avoid timing loops.

5 EQUIPMENT CLASSIFICATIONS

5.1 Location in the Network

The classification of equipment arises from its location in the network. Figure 19 below outlines a common WAN architecture. In the WAN, the traditional telco equipment, such as ADMs and DCS, make up the SONET/SDH ring network. Networking equipment may be connected at the periphery or incorporated into the WAN directly.

Figure 19. Typical WAN Network



5.2 Types of Equipment

5.2.1 Enterprise Switch

An Enterprise Switch is a premise-based system, privately owned and maintained which acts as the gateway interface between the local environment (LAN) and the

public network (WAN). It acts as an aggregation point for WAN access, providing a wide range of both telephony and LAN interface options on the premise side, and providing WAN-compliant telephony interfaces (e.g. T1, T3, SONET) on the network side. Enterprise switches are typically based on ATM technology and have a capacity of 5 GBits or more. They are used to interconnect campus switches, workgroup switches, routers, hubs, as well as integrate various disparate services (video, voice, ethernet, etc.) existing in the enterprise network. Both enterprise and campus switches can carry mission critical traffic. Various levels of hardware protection are an option.

5.2.2 Campus or Backbone Switch

This is a premise-based switch generally used to provide a local backbone for interconnecting various IP or ATM-based LAN equipment such as routers and workgroup switches. The Campus switch resides at the core of the private network. It may provide direct access to the WAN, or may access the WAN via an Enterprise switch.

5.2.3 Workgroup Switch

A Workgroup Switch resides in the LAN and provides desktop level switching services to ethernet client NICS. These switches are typically optimized for low-cost, high-performance workgroup applications, do not provide redundancy and are generally based on IP switching technology.

5.2.4 NIC

A Network Interface Card (NIC) resides within a desktop client computer, is generally based on ethernet technology (e.g. 10 Mbit/s or 100 Mbit/s) and provides client access to the LAN.

5.2.5 Core Switch

A Core Switch is a high capacity WAN switch used by public network service providers to provision their backbone network. Core switches typically provide only OC-3 rate interfaces or higher and have a capacity of 50 GB or more. Core switches generally interface directly only to other switching equipment in the public network such as Edge switches and Access muxes and not to customer equipment. As this class of switch is used in mission-critical public network applications, it will have a high degree of redundancy and fault tolerance.

5.2.6 Edge Switch

An Edge Switch is a high capacity WAN switch used by public network service providers to provision their backbone or access network. Edge switches typically provide only DS-3 rate interfaces or higher and have a capacity of 20 GB or more. Edge switches interface directly to both other switching equipment in the public network such as Core switches and Access muxes and to customer premise equipment such as Enterprise switches. Edge switches provide access services such as Frame Relay and ATM to end customers, provide aggregation of customer traffic and provide high speed trunk interfaces to the public backbone network. As this class of switch is used in mission-critical public network applications, it will have a high degree of redundancy and fault tolerance.

5.2.7 Access MUX

An Access MUX provides traffic aggregation of a number low speed interfaces to a single high speed trunk interface. Access muxes are used in both public and private networks, and are based on either TDM or ATM technology. In a private network, the Access Mux provides a gateway to the WAN (similar to an Enterprise switch), aggregating traffic from a range of local equipment including PBX's, video conference systems, routers, and backbone switches. In a public network, the access mux is used to provide WAN access services to private networks (e.g. T1 Frame Relay or T1 ATM) and aggregating this traffic onto a single higher speed link to an Edge or Core switch. In mission-critical public network applications, Access MUXes will have a high degree of redundancy and fault tolerance.

6 APPLICABLE STANDARDS REQUIREMENTS

6.1 What really needs to be met

The equipment classification reduces to two distinct types: “mission-critical” equipment, and “other” equipment. Mission-critical equipment (Core switches, Edge switches, Access Mux, Enterprise Backbone equipment) cannot tolerate outages due to high throughput or interfaces to public network equipment which cannot tolerate outages. “Other” equipment resides in the LAN or customer premises (Enterprise, Campus, Workgroup, NIC). Here redundancy is rarely provided as outages are more tolerable and typically do not affect a large number of users or revenue generating services.

The requirements on mission-critical equipment can further be classified by the timing mode the equipment is configured for.

6.1.1 External Timing Mode:

Equipment that has an available BITS clock must use external-timing. This equipment has to provide wander filtering to meet the wander requirements, including wander transfer, therefore it will automatically meet the jitter transfer requirement. Jitter generation and jitter tolerance requirements must also be met.

Holdover is also required in external-timing mode. The overall stability during a 24 hour period with temperature changes must be less than ±4.6 ppm (Stratum 3 clock).

Phase transient criteria also has to be met. During synchronization rearrangement the operating MTIE should be no greater than the requirement mask in Figure 15.

6.1.2 Line Timing Mode:

Equipment that does not have an available BITS clock can use line-timing. Equipment in this timing mode must meet wander transfer and wander generation specifications. Since the line timing this equipment is referenced to already meets the wander transfer TDEV specification, this equipment is not required to filter wander. The transmit clock PLL bandwidth can therefore be as wide as the jitter transfer specification will allow. The wander generation specification can still be met with this wide bandwidth.

The specification for phase transients and holdover are same as for externally-timed equipment. These can only be met with a narrow transmit clock PLL

bandwidth, somewhere in the order of 10-20 Hz. This narrow loop bandwidth will automatically meet the jitter transfer requirements. Jitter generation and jitter tolerance requirements will still need to be met.

6.1.3 Loop Timing Mode:

Some equipment may simply be loop-timed. The requirements for loop-timing are not as strict as those for line-timing:

1) Phase transient criteria is looser: it is an objective to meet the Requirement curve of Figure 15. This requires a narrow transmit clock PLL bandwidth, thereby automatically meeting the jitter transfer requirement;

2) Must be capable of entering holdover. See Section 4.4 for details.

3) Clock accuracy has to be ±20 ppm and must meet the SMC requirement for a SONET minimum clock. This implies that the clock be more than just a 20 ppm fixed oscillator;

4) Interface jitter, jitter tolerance, and jitter generation requirements still need to be met.

6.1.4 What does current equipment meet?

Most equipment is located in the LAN or interfaces to the WAN through an ADM or Access Mux. In most cases, this equipment is loop-timed and it is necessary to meet only the interface jitter, jitter tolerance, jitter generation, and jitter transfer requirements. Currently, there is some question as to whether the jitter transfer requirement really needs to met. Jitter transfer is specified to limit the jitter gain in repeaters; and interface equipment is typically connected directly to the WAN without any repeaters. As long as the jitter transfer curve of the equipment is flat (with peaking <0.1dB in the pass band) and eventually rolls-off (at a finite frequency somewhere between 130kHz and 500kHz), jitter gain is not a problem. If the output from the WAN equipment meets the interface jitter requirements, and the input of the WAN equipment meets the jitter tolerance requirements, as long as the loop-timed equipment does not add jitter, the location of the transfer curve corner is irrelevant.

Going forward, the evolving GR-253 standard is placing more emphasis on the phase transient requirement, even for loop-timed equipment. This requirement adds complexity to the timing generation by requiring that the equipment fall back to an SMC in the event that the received timing signal is lost. The fall-back must be such that the transmit signal is not disturbed. The practical benefit of this is that the transmitted data stream is unaffected by the receive stream.

Ultimately, the equipment requirements are subject to final “approval” by the intended recipient of the interface signal. For example, certain public network service providers may either waive specific requirements as unnecessary or may have their own, more stringent set of requirements for accessing their network. Unfortunately, in some cases meeting the WAN standards may be a necessary *but* not sufficient condition for equipment acceptance by the end customer.

6.1.5 What is met by PMC-Sierra Devices:

PMC-Sierra physical layer interface devices deal with most of the jitter requirements directly. The LAN PHY devices have been optimized for jitter tolerance, therefore, they will not meet the jitter transfer requirement with respect to the mask in Figure 18. Their typical transfer characteristic is flat (<0.1dB) up to the cut-off frequency of around 400kHz. As mentioned above, this will not cause any operational issues.

The WAN PHY devices have been optimized for both the jitter tolerance and jitter transfer requirements.

In all cases, these devices do not address the wander requirements; these can only be satisfied with external, narrow bandwidth clock circuits.

Table 14. PMC-Sierra Device Jitter and Wander Compliance

		Jitter			
Device	**Wander**	Tolerance	Generation	Transfer	**SSM**
PM5346 (LITE)	No	Yes	Yes	No	No (defaults S1 to 0000, STU)
PM5347 (PLUS)	No	Yes	Yes	Yes	Yes
PM5348 (DUAL)	No	Yes	Yes	No	Yes
PM5349 (QUAD)	No	Yes	Yes	No	Yes
PM5350(ULTRA)	No	Yes	Yes	No	S1 defaults to 0000.- STU
PM5351(TETRA)	No	Yes	Yes	Yes	Yes
PM5356(MAX)	No	Yes	Yes	No	Yes
PM5357(POS)	No	Yes	Yes	Yes	Yes
PM5342 (SPECTRA)	No	Yes	Yes	Yes	Yes

7 A CIRCUIT TO MEET THE WAN REQUIREMENTS

The following circuit provides a method of meeting the requirements of external-timed equipment using the S/UNI-PLUS[1]. Certain portions may be omitted if the equipment is to operate in line-timed or loop-timed, as the requirements are less onerous. However, even in the case of loop-timed, this circuit will still be necessary to achieve the phase transient requirement and the SMC requirement. If even these two requirements are not necessary, then the S/UNI-PLUS can be used on its own. If the equipment is being designed with devices whose performance has been optimized for jitter tolerance (such as the S/UNI-LITE or S/UNI-DUAL), then this minimum circuit is necessary to meet the jitter transfer requirement (a by-product of the narrow bandwidth PLL used to meet the phase transient requirement).

The timing circuit is a microprocessor-controlled VCXO. The PLL loop filter is implemented digitally within the microprocessor. An added benefit of using the micro is that accurate clock holdover can be achieved, and temperature compensation can be performed in software.

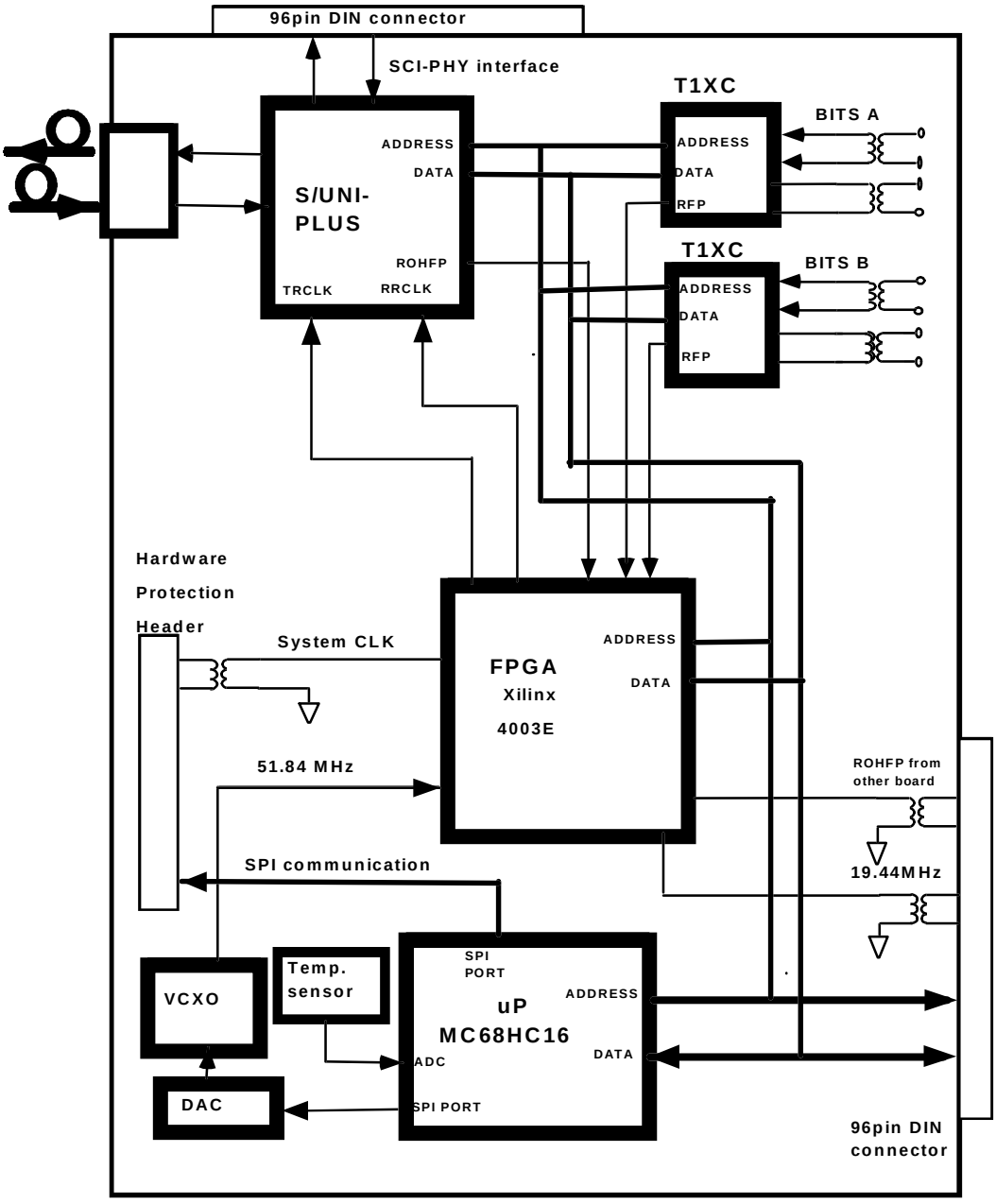
The block diagram (Figure 20) below represents a single timing circuit. If hardware protection (i.e., redundancy) is required, two circuits would be used in a master-slave configuration to provide back-up timing that could be switched in the event of a timing failure.

The main component of the synchronization circuit is the phase locked loop. The PLL consists of a VCXO, a phase detector, digital loop filter (implemented in software in the microprocessor), and some selection circuitry (muxes) for choosing the reference signal and the appropriate comparison signal. In addition to implementing the loop filter, the microprocessor monitors the reference signal (for protection switching) and provides holdover and temperature compensation.

The VCXO has ±20 ppm frequency accuracy and a ±60 ppm frequency adjustment range. This wide adjustment range is necessary to satisfy the requirements for a SMC; the pull-in range for the SMC requires that the VCXO have a minimum frequency adjustment range of ±40 ppm, the ±60 ppm range provides some margin. The choice of VCXO is critical. The TDEV of the VCXO must be measured on its own (outside of the loop) to find its spectral performance. As well, the MTIE for the oscillator when free-running must be less than the 20 ns requirement for observation times below 1 second. These measurements check that the VCXO on its own can meet the wander generation requirements for integration and observation times shorter than 1 second.

[1] This circuit can also be used with the LAN PHY devices.

Figure 20. Microprocessor Controlled PLL



The reference clock for the PLL can be from many different sources, depending on the timing option used and whether redundancy is used. In the case of Line-timing or loop-timing, the PLL reference is the 8 kHz RFP (Receive Frame Pulse) signal from S/UNI-PLUS. In the case of external-timing with an available BITS source, the PLL reference is one of the two 8 kHz RFPO signals from T1XC

devices that can receive the BITS clock. In the case of redundant timing, the PLL reference is the 19.44 MHz clock from the master clock circuit.

The microprocessor monitors the input capture interrupt pin (IC1). This interrupt is scheduled to occur every 125µsec, based on the signal from the FPGA. To generate the 125 µsec interrupt, the FPGA uses either the ROHFP or the GROCLK signals derived from the received line timing. GROCLK is a 19.44 MHz clock synchronous to the recovered clock from the received optical signal. The S/UNI-PLUS recovers the GROCLK clock from the OC-N signal using its CRU (Clock Recovery Unit) module. In the case of an OC-3 signal, this is a 155.52 MHz clock divided by 8 to produce a GROCLK at 19.44 MHz. Furthermore, the GROCLK is divided (in the S/UNI-PLUS) by 2430 to produce an ROHFP at 8KHz. Either of these two outputs can be used by the WAN circuitry. The advantage of using the GROCLK is that it allows a higher comparison frequency than 8KHz, and reduces the aliasing of noise components to frequencies within the loop bandwidth.

Digital signal processing of the phase detector output results in a digital value that can be used to control the VCXO frequency through an external 12-bit DAC. The value is sent to the DAC using the QSPI port of the on board microprocessor. At the beginning of each IC1 interrupt handling routine (125µsec), a new value is latched into the DAC.

If the OC-N signal is lost, the S/UNI-PLUS switches the Clock Recovery Unit (CRU) from the incoming data to the on-board reference signal, RRCLK+/-. ROHFP then has a fixed phase relationship with RRCLK+/-. Similarly, TOHFP will have a fixed phase relationship with TRCLK+/-, which is also the RRCLK+/-. In this situation, the loop will have no gain and the VCXO can slowly wander in frequency because it is referenced to itself. The microprocessor is used, therefore, to monitor the S/UNI-PLUS alarms at all times. When a loss of signal occurs, the microprocessor breaks the PLL and enters a holdover mode. In holdover the microprocessor tries to maintain the last known good frequency for as long as it can in the presence of temperature changes and in the absence of a reference signal.

In order to maintain the last known good frequency with changing temperatures, the microprocessor needs to be able to measure the temperature. It then uses this temperature measurement and an algorithm to compensate for the changes in frequency due to temperature. To determine the compensation factors for such an algorithm, the synchronization unit must go through a learning cycle during factory testing. The unit must be cycled in a temperature chamber while a precise data rate OC-N signal is applied to the S/UNI-PLUS receiver. The microprocessor then records the digital values needed by the DAC to maintain frequency lock over the temperature range.

The microprocessor, in addition to performing the digital filtering, also monitors and generates the Synchronization Status Messages in the S/UNI-PLUS. If external-timing is used, the microprocessor also monitors the SSM from the BITS sources. Furthermore, the microprocessor can monitor the performance of the optical link (LOS, AIS, LOF, BIP-8 from the S/UNI-PLUS) for an indication of the quality of the OC-3 signal being used to line or loop-time to. Finally, if clocking redundancy is used, the microprocessor can monitor the status of the other timing circuit to determine when to switch to back-up.

The program code that runs the microprocessor is held in Flash PROM. In addition, the Flash PROM can be used to store temperature compensation information. There are a number of ways to implement temperature compensation. The simplest way is to store the average values of frequency offsets vs. temperature for the VCXO (this information should be available from the manufacturer); this method should be able to achieve ±4.6 ppm in 24 hours over the given temperature change. The other method is more precise , but it involves recording in Flash the particular frequency offsets from nominal vs. temperature for the particular VCXO during temperature cycling. This method is capable of achieving less than ±1 ppm over a period of months, but it can be more expensive to implement because every timing circuit must be temperature cycled at a decreased rate (less than 1 °F per 2 minutes to avoid recording biased values due to inertia of the thermal process) in order to calibrate the VCXO. An added benefit of this method is that the on-board temperature sensor accuracy and DAC temperature dependency are calibrated as well.

Finally, it should be noted that in the case of external-timing with BITS clocks, the RFPO signal from the T1XC will contain up to 1/8 UIpp of jitter from the recovered PCM clock generated by the clock recovery block. This jitter is produced by the limited resolution of the digital PLL implemented in the receive clock recovery circuit of the T1XC. This jitter is high frequency and will be averaged out within the microprocessor.

APPENDIX A

Derivation of Wander Contribution from Temperature Variations

Length of the fiber in open air: L = 250,000 m

Permittivity of free space: $\varepsilon_0 = 8.854 \bullet 10^{-12} \frac{farad}{m}$

Permeability of free space: $\mu_0 = 4 \bullet \pi \bullet 10^{-7} \frac{henry}{m}$

Velocity of light: $c = \frac{1}{\sqrt{\varepsilon_0 \bullet \mu_0}}$ $c = 2.99796 \bullet 10^{8} \frac{m}{sec}$

Index of refraction of pure silica fiber: n = 1.46

Propagation delay through fiber of length, L: $\tau = \frac{L \bullet n}{c}$ $\tau = 0.0012175$ sec

Temperature change in degrees Kelvin: $\Delta T = 1$ °K

Temperature sensitivity of thermal expansion coefficient of silica: $\Delta L = 5 \bullet 10^{-7} \bullet \Delta T \frac{m}{°K}$

Temperature sensitivity of refractive index: $\Delta n = -10^{-5} \bullet \Delta T \frac{1}{°K}$

Change of propagation delay due to the temperature change:

$$\Delta\tau = \left(\frac{n}{c} \bullet \frac{\Delta L}{\Delta T} + \frac{L}{c} \bullet \frac{\Delta n}{\Delta T} \right) \bullet \Delta T$$

$\frac{L}{c} \bullet \frac{\Delta n}{\Delta T} = -8.339013934 \bullet 10^{-9} \frac{sec}{°K}$ $\frac{n}{c} \bullet \frac{\Delta L}{\Delta T} = 2.434992069 * 10^{-15} \frac{sec}{°K}$

$\frac{\Delta \tau}{\Delta T} = -8.3390115 \bullet 10^{-9} \frac{sec}{°K}$

The fiber expansion term (•L component) is negligible, most of the change in delay comes from the change in the index of refraction. A 250km fiber line in open air gives -8.3ns/°K of delay; for OC-3, this is equivalent to:

$N = \frac{\Delta \tau}{\Delta T} \bullet 155.52 \bullet 10^{-6} \frac{UI}{sec} \Rightarrow N = -1.2969 \frac{UI}{°K} \Rightarrow N \bullet 20°K = -25.94$ UI

With a change of temperature of 1°K, the 250km length of fiber will produce approximately 1.3 bits difference between transmitted and received data rate. If the temperature change is 20 degrees

(possible over a 24 hour period), it will result in approximately 26 bits difference! For fiber in ground, the ΔT is in the order of 2-3°K, which is still 2.6 to 3.9 bits difference.

Change in LASER wavelength due to change in temperature: $\Delta\lambda = 0.1 \bullet 10^{-9} \bullet \Delta T \frac{m}{°K}$

Change in index of refraction as a function of wavelength change:

$\Delta n_{1300} = 3 \bullet 10^5 \bullet \Delta\lambda \frac{1}{m}$ at 1300 nm, there is little change because of negligible chromatic dispersion

$\Delta n_{1500} = 51 \bullet 10^5 \bullet \Delta\lambda \frac{1}{m}$ at 1500 nm, index of refraction changes due to the change of wavelength

LASER temperature change results in wavelength change that results in delay difference:

$$\frac{\Delta\tau}{\Delta T} = \frac{L}{c} \bullet \frac{\Delta n}{\Delta\lambda^{\circ}} \bullet \frac{\Delta\lambda}{\Delta T} \frac{UI}{\sec} \quad \Rightarrow \quad \frac{\Delta\tau}{\Delta T} = 4.2529 \bullet 10^{-7} \frac{\sec}{°K}$$

NOTES

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