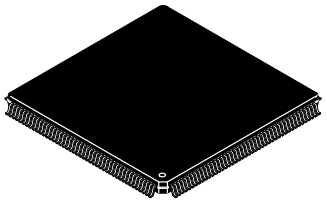
MCM69D536

32K x 36 Bit Synchronous Dual I/O, Dual Address SRAM



TQ PACKAGE
176 LEAD TQFP
CASE 1101–01

The MCM69D536 is a 1M–bit static random access memory, organized as 32K words of 36 bits. It features common data input and data output buffers and incorporates input and output registers on–board with high speed SRAM.

The MCM69D536 allows the user to concurrently perform reads, writes, or pass–through cycles in combination on the two data ports. The two address ports (AX, AY) determine the read or write locations for their respective data ports (DQX, DQY).

The synchronous design allows for precise cycle control with the use of an external single clock (K). All signal pins except output enables ($\overline{GX}$, $\overline{GY}$) are registered on the rising edge of clock (K).

The pass–through feature allows data to be passed from one port to the other, in either direction. The $\overline{PTX}$ input must be asserted to pass data from port X to port Y. The $\overline{PTY}$ will likewise pass data from port Y to port X. A pass–through operation takes precedence over a read operation.

For the case when AX and AY are the same, certain protocols are followed. If both ports are read, the reads occur normally. If one port is written and the other is read, the read from the array will occur before the data is written. If both ports are written, only the data on DQY will be written to the array.

- Single 3.3 V ± 5% Power Supply
- Fast Access Times: 5/6/8 ns Max
- Throughput of 2.98 Gigabits/Second
- Single Clock Operation
- Address, Data Input, $\overline{E1}$, E2, $\overline{PTX}$, $\overline{PTY}$, $\overline{WX}$, $\overline{WY}$, and Data Output Registers On–Chip
- 100 MHz Maximum Clock Frequency
- Self–Timed Write
- Two Bi–Directional Data Buses
- Can be Configured as Separate I/O
- Pass–Through Feature
- Asynchronous Output Enables ($\overline{GX}$, $\overline{GY}$)
- LVTTL Compatible I/O
- Concurrent Reads and Writes
- 176–Pin TQFP Package

Suggested Applications

— ATM — Ethernet Switches — Routers
— Cell/Frame Buffers — SNA Switches — Shared Memory

Product Family Configurations

Part Number	Dual Address	Single Address	Dual I/O	Separate I/O	Configuration	V_{DD}
MCM69D536	✓	Note 1	✓	Note 2	32K x 36	3.3 V
MCM69D618	✓	Note 1	✓	Note 2	64K x 18	3.3 V
MCM67Q709A		✓		✓	128K x 9	5.0 V
MCM67Q909		✓		✓	512K x 9	5.0 V

NOTES:
1. Tie AX and AY address ports together for the part to function as a single address part.
2. Tie $\overline{GX}$ high for DQX to be inputs and tie $\overline{WY}$ high and $\overline{GY}$ low for DQY to be outputs.

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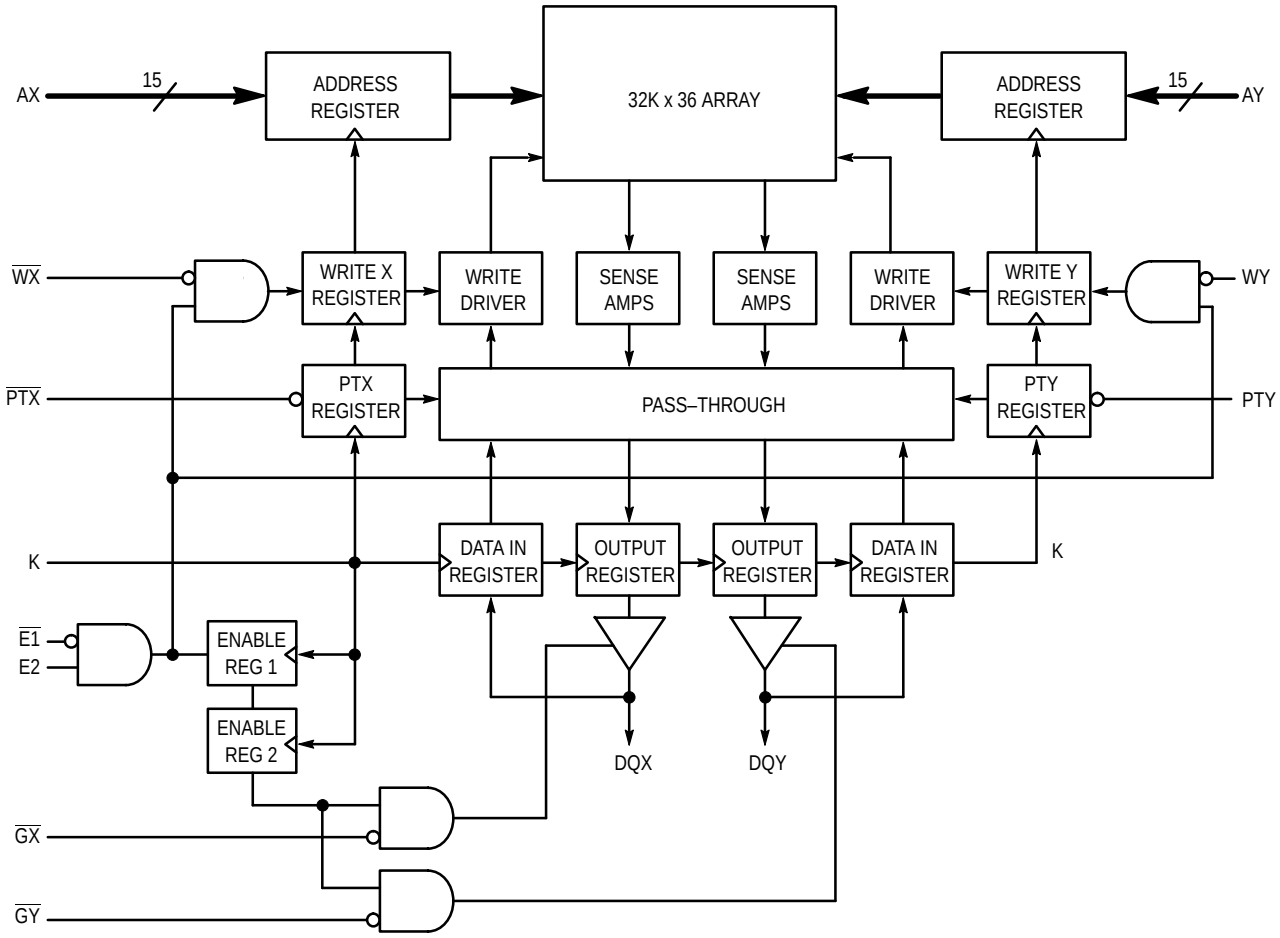
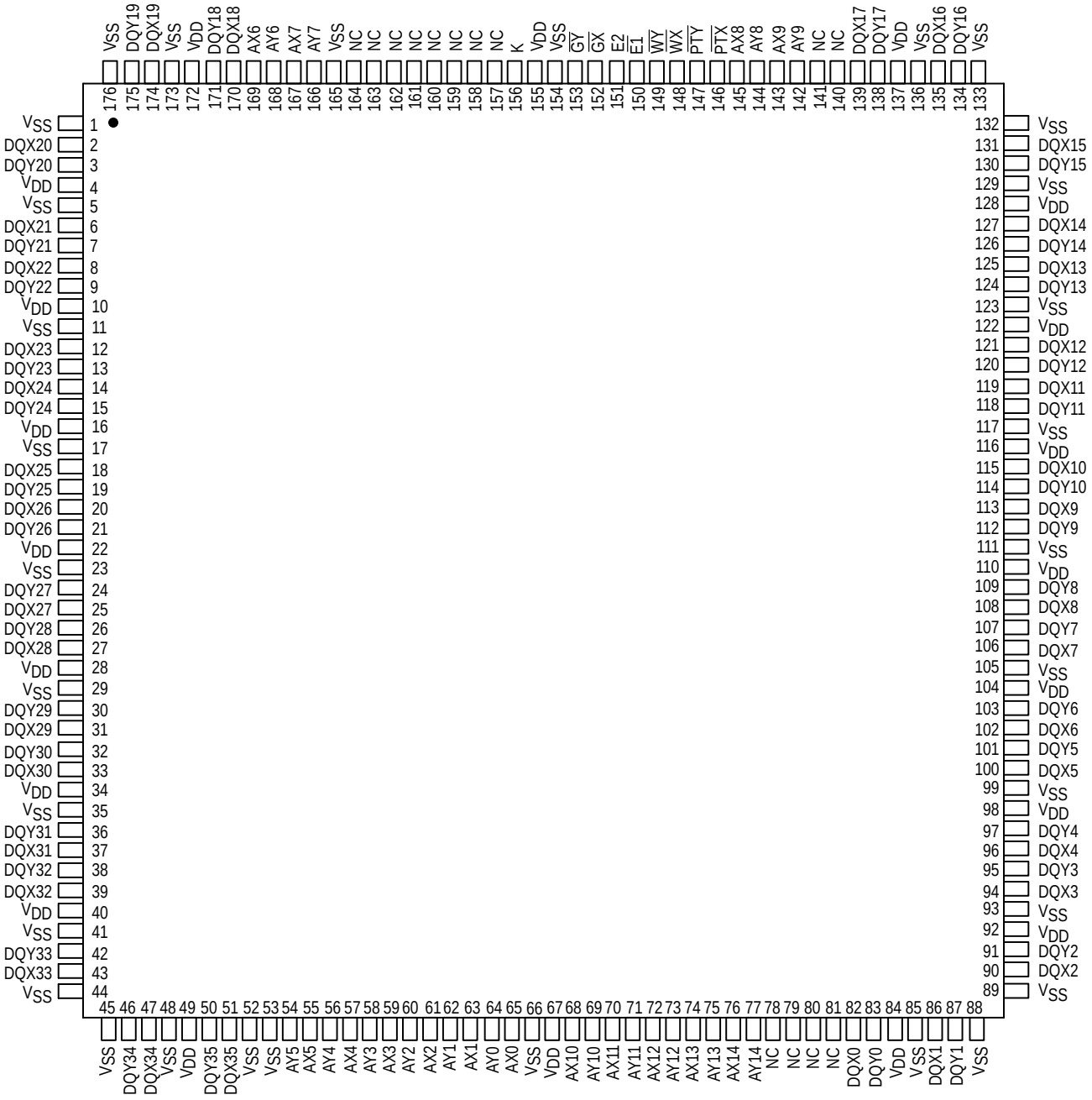
BLOCK DIAGRAM



PIN ASSIGNMENT



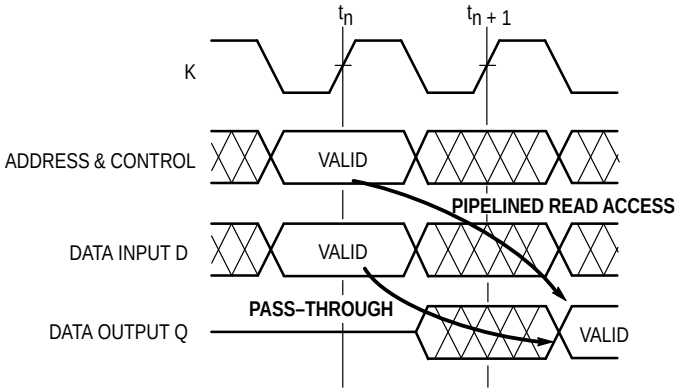
PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
65, 63, 61, 59, 57, 55, 169, 167, 145, 143, 68, 70, 72, 74, 76	AX0 – AX14	Input	Address Port X: Never allow floating addresses for inputs AX0 – AX14. A pullup resistor is needed.
64, 62, 60, 58, 56, 54, 168, 166, 144, 142, 69, 71, 73, 75, 77	AY0 – AY14	Input	Address Port Y: Never allow floating addresses for inputs AY0 – AY14. A pullup resistor is needed.
82, 86, 90, 94, 96, 100, 102, 106, 108, 113. 115, 119, 121, 125, 127, 131, 135, 139, 170, 174, 2, 6, 8, 12, 14, 18, 20, 25, 27, 31, 33, 37, 39, 43, 47, 51	DQX0 – DQX35	I/O	Data Input/Output Port X.
83, 87, 91, 95, 97, 101, 103, 107, 109, 112, 114, 118, 120, 124, 126, 130, 134, 138, 171, 175, 3, 7, 9, 13, 15, 19, 21, 24, 26, 30, 32, 36, 38, 42, 46, 50	DQY0 – DQY35	I/O	Data Input/Output Port Y.
150	$\overline{E1}$	Input	Synchronous Chip Enable: Active low.
151	E2	Input	Synchronous Chip Enable: Active high.
152	$\overline{GX}$	Input	Asynchronous Output Enable Port X Input: Low — enables output buffers (DQXx pins). High — DQXx pins are high impedance.
153	$\overline{GY}$	Input	Asynchronous Output Enable Port Y Input: Low — enables output buffers (DQYx pins). High — DQYx pins are high impedance.
156	K	Input	Clock: This signal registers the address, data in, and all control signals except $\overline{G}$.
146	$\overline{PTX}$	Input	Pass–Through Port X.
147	$\overline{PTY}$	Input	Pass–Through Port Y.
148	$\overline{WX}$	Input	Synchronous Write Enable Port X.
149	$\overline{WY}$	Input	Synchronous Write Enable Port Y.
4, 10, 16, 22, 28, 34, 40, 49, 67, 84, 92, 98, 104, 110, 116, 122, 128, 137, 155, 172	V_{DD}	Supply	+ 3.3 V Power Supply.
5, 11, 17, 23, 29, 35, 41, 48, 66, 85, 93, 99, 105, 111, 117, 123, 129, 136, 154, 173	V_{SS}	Supply	Ground.
1, 44, 45, 52, 53, 88, 89, 132, 133, 165, 176	V_{SS}	Supply	Bonded to die flag. No chip current flows through these pins.
78 – 81, 140, 141, 157 – 164	NC	—	No Connection: There is no connection to the chip.

TRUTH TABLE (See Notes 1 through 5)

Operation Number	Input at t_n Clock						
	$\overline{E1}$	E2	$\overline{WX}$	$\overline{WY}$	$\overline{PTX}$	$\overline{PTY}$	Operation
1	H	X	X	X	X	X	Deselected
2	X	L	X	X	X	X	Deselected
3	L	H	0	X	X	X	Write X Port
4	L	H	X	0	X	X	Write Y Port
5	L	H	X	X	0	X	Pass–Through X to Y
6	L	H	X	X	X	0	Pass–Through Y to X
7	L	H	1	X	1	1	Read X
8	L	H	X	1	1	1	Read Y

NOTES:
1. $\overline{GX}/\overline{GY}$ must be controlled to avoid bus contention issues during write and pass–through cycles.
2. Operation numbers 3 – 6 can be used in any combination.
3. Operation numbers 4 and 7, 3 and 8, 7 and 8 can be combined.
4. Operation number 5 can not be combined with operation number 7 or 8 because pass–through takes precedence over a read operation.
5. Operation number 6 can not be combined with operation number 7 or 8 because pass–through takes precedence over a read operation.



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	– 0.5 to 4.6	V
Voltage Relative to V_{SS} for Any Pin Except V_{DD}	V_{in}, V_{out}	– 0.5 to V_{DD} + 0.5	V
Output Current	I_{out}	± 20	mA
Power Dissipation	P_D	866	mW
Temperature Under Bias	T_{bias}	– 10 to 85	°C
Operating Temperature	T_A	0 to 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This is a synchronous device. All synchronous inputs must meet specified setup and hold times with stable logic levels for ***ALL*** rising edges of clock (K) while the device is selected.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

PACKAGE THERMAL CHARACTERISTICS (See Note 1)

Rating		Symbol	TQFP	Unit	Notes
Junction to Ambient (@ 200 lfm)	Single–Layer Board Four–Layer Board	$R_{\theta JA}$	40 35	°C/W	2
Junction to Board (Bottom)		$R_{\theta JB}$	23	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	9	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V ± 5%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)		V_{DD}	3.135	3.465	V
Input High Voltage		V_{IH}	2.0	V_{DD} + 0.5**	V
Input Low Voltage		V_{IL}	– 0.5*	0.8	V
Input Leakage Current (All Inputs, V_{in} = 0 to V_{DD})		$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{DD})		$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current (Outputs Toggling at CMOS Levels) (V_{DD} = Max, f = f_{max})	MCM69D536–5 ns MCM69D536–6 ns MCM69D536–8 ns	I_{DDA}	— —	250 250 250	mA
CMOS Standby Supply Current (Deselected, Clock (K) Cycle Time ≥ t_{KHKH}, All Inputs Toggling at CMOS Levels V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{DD} – 0.2 V)	MCM69D536–5 ns MCM69D536–6 ns MCM69D536–8 ns	I_{SB1}	— — —	100 100 100	mA
Output Low Voltage (I_{OL} = + 8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)		V_{OH}	2.4	V_{DD}	V

* V_{IL} ≥ – 1.5 V for t ≤ t_{KHKH}/2.
** V_{IH} ≤ V_{DD} + 1.0 V for t ≤ t_{KHKH}/2.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 0 to 70°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address and Data Input Capacitance	C_{in}	6	pF
Control Pin Input Capacitance	C_{in}	6	pF
Output Capacitance	C_{out}	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V ± 5%, T_A = 0 to 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 3 ns

Output Timing Reference Level . . . . . 1.5 V
Output Load . . . . . Figure 1 Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	MCM69D536–5		MCM69D536–6		MCM69D536–8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	10	—	12	—	15	—	ns	1
Clock Access Time	t_{KHQV}	—	5	—	6	—	8	ns	
Clock Low Pulse Width	t_{KLKH}	4	—	4	—	6	—	ns	
Clock High Pulse Width	t_{KHKL}	4	—	4	—	6	—	ns	
Clock High to Data Output Active	t_{KHQX1}	0	—	0	—	0	—	ns	
Clock High to Data Output Invalid	t_{KHQX2}	2	—	2	—	2	—	ns	
Clock High to Data Output High–Z	t_{KHQZ}	—	4	—	5	—	5	ns	2
Output Enable Low to Data Output Valid	t_{GLQV}	—	4	—	6	—	8	ns	
Output Enable Low to Data Output Low–Z	t_{GLQX}	0	—	0	—	0	—	ns	
Output Enable High to Data Output High–Z	t_{GHQZ}	—	4	—	5	—	8	ns	2
Setup Times: AWR0 – AWR14	t_{AVKH}	2	—	2.5	—	3	—	ns	3
ARD0 – ARD14	t_{AVKH}								
$\overline{W}$	t_{WVKH}								
$\overline{PT}$	t_{PTVKH}								
$\overline{E1}$, E2	t_{EVKH}								
D0 – D35	t_{DVKH}								
Hold Times: AWR0 – AWR14	t_{KHAX}	0.5	—	0.5	—	1	—	ns	3
ARD0 – ARD14	t_{KHAX}								3
$\overline{W}$	t_{KHWX}								3
$\overline{PT}$	t_{KHPTX}								3
$\overline{E1}$, E2	t_{KHEX}								3
D0 – D35	t_{KHDX}								3, 4

NOTES:
1. All read and write cycles are referenced from K.
2. This parameter is sampled and not 100% tested.
3. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for ***ALL*** rising edges of clock (K) while the device is selected.
4. t_{KHDX} minimum for Port Y only extends to 4.0 ns only for the special case when the Y– and X–address are identical on the same rising clock edge.

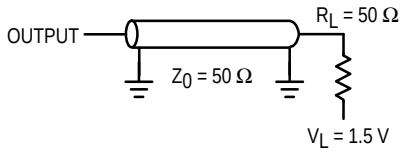
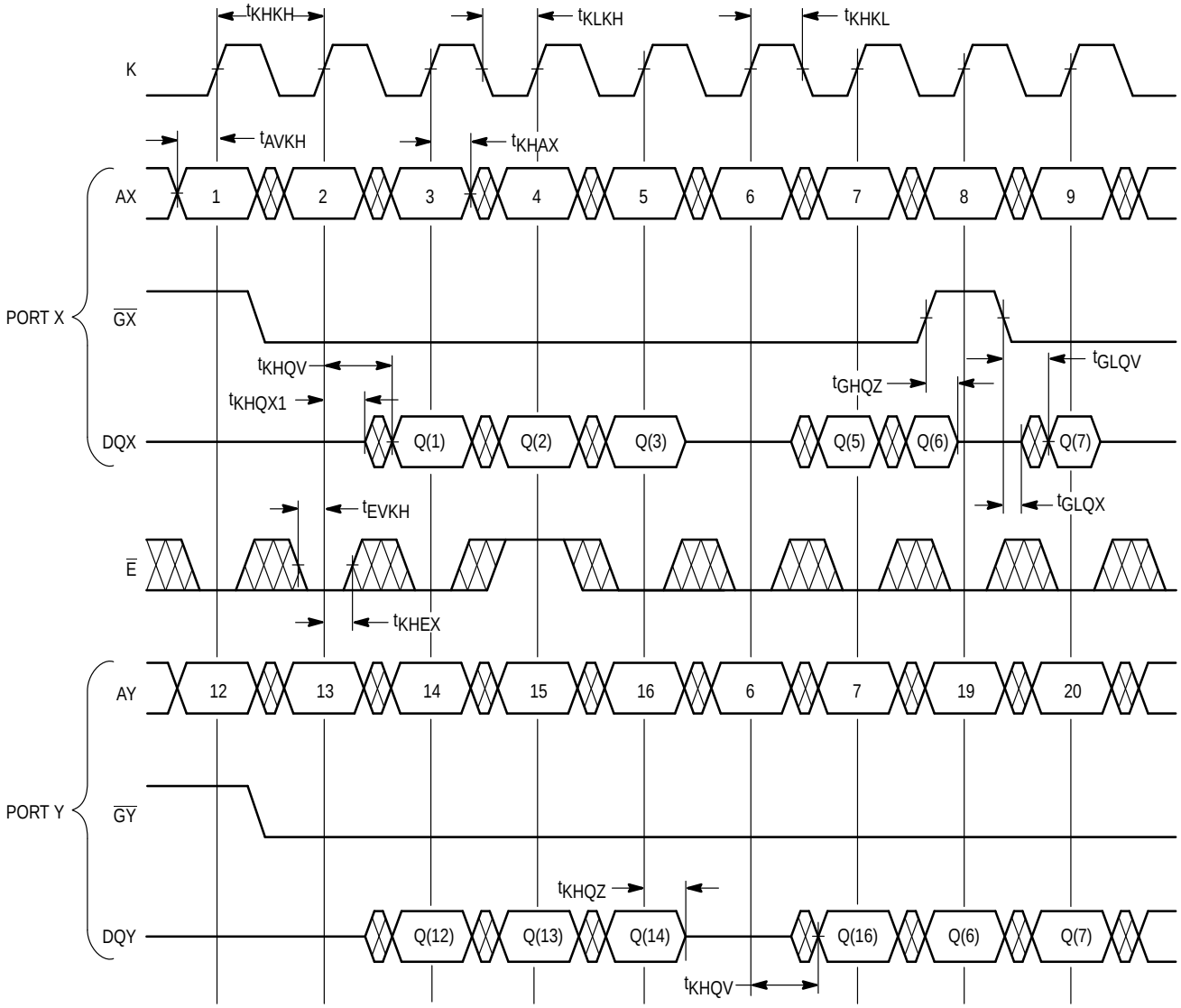


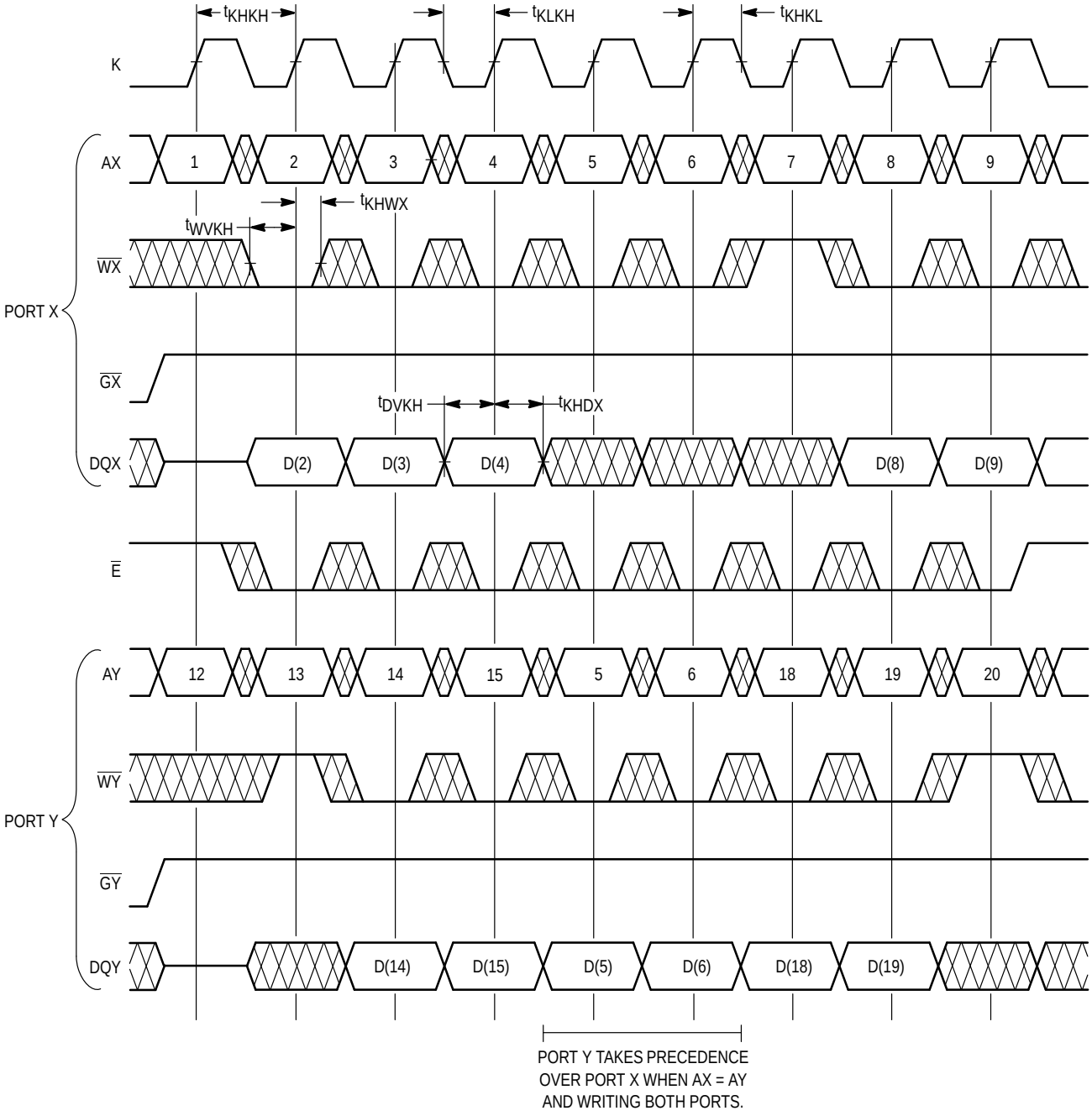
Figure 1. AC Test Load

READ CYCLE TIMING FROM BOTH PORTS ($\overline{WX}$, $\overline{WY}$, $\overline{PTX}$, $\overline{PTY}$ HIGH)



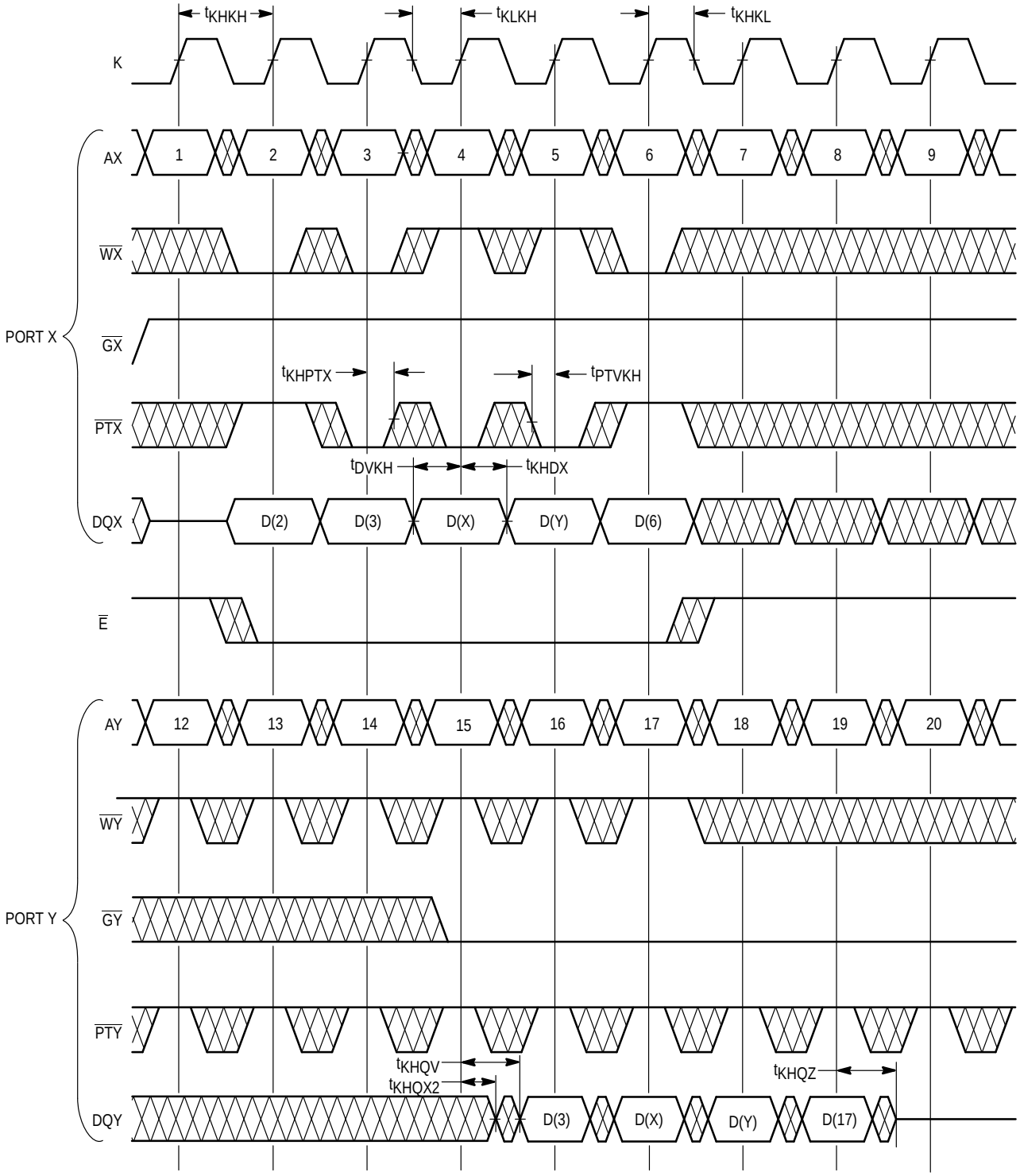
NOTE: $\overline{E}$ Low = $\overline{E1}$ Low and E2 High. $\overline{E}$ High = $\overline{E1}$ High or E2 Low.

WRITE CYCLE TIMING TO BOTH PORTS ($\overline{PTX}$, $\overline{PTY}$ HIGH)



NOTE: $\overline{E}$ Low = $\overline{E1}$ Low and E2 High. $\overline{E}$ High = $\overline{E1}$ High or E2 Low.

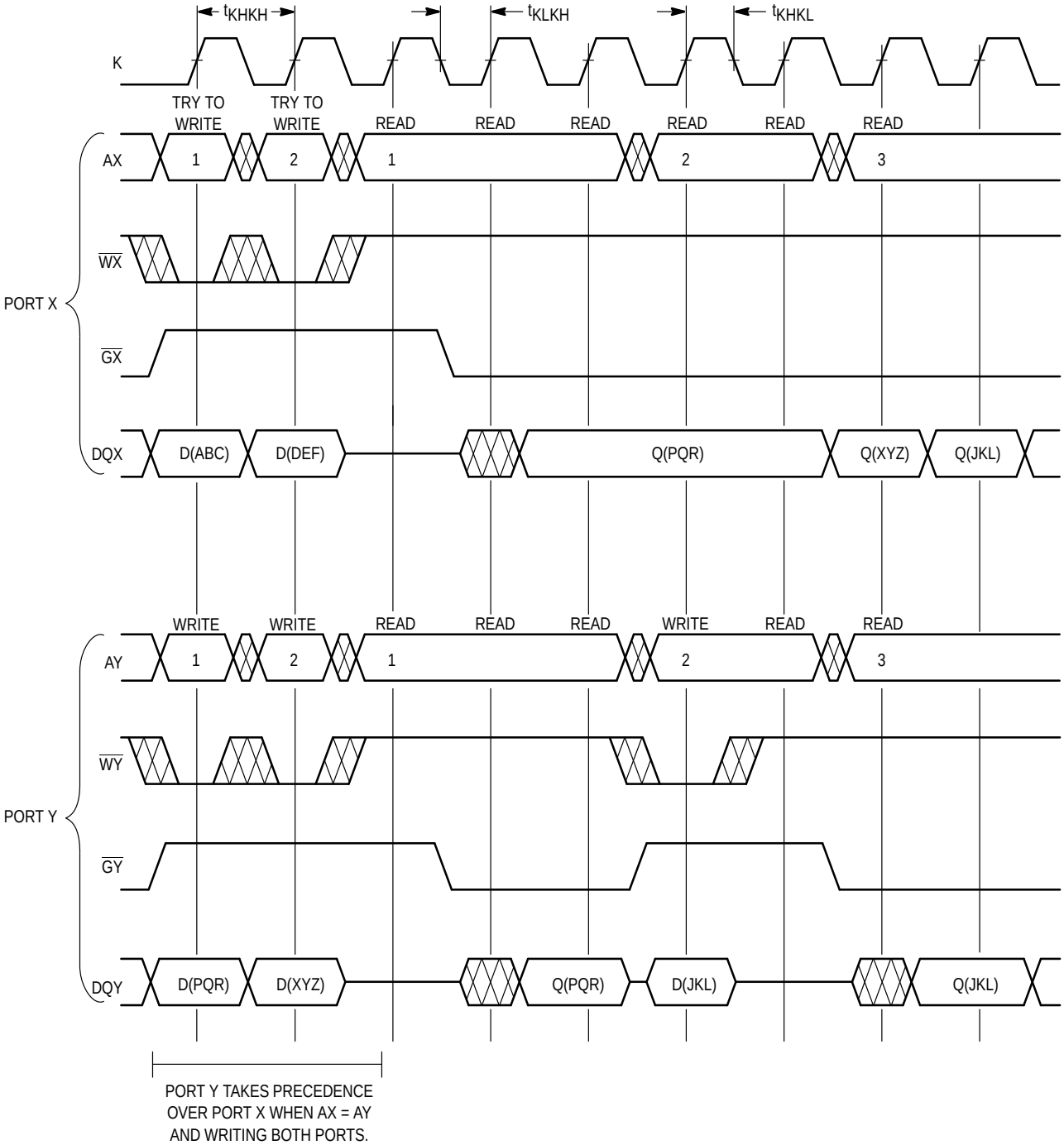
WRITE TO PORT X AND PASS–THROUGH TO PORT Y (SEE NOTE)



$\overline{E}$ Low = $\overline{E1}$ Low and E2 High. $\overline{E}$ High = $\overline{E1}$ High or E2 Low.

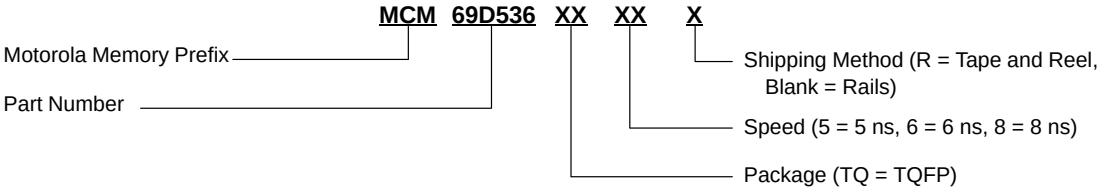
NOTE: The timing diagram is valid for the opposite case as well, i.e., writing to Port Y and passing through to Port X.

COMBINATION READ/WRITE WITH SAME ADDRESS ON EACH PORT



$\overline{PTX}$ = $\overline{PTY}$ = high.
D(Value) = Value is the input to the data port.
Q(Value) = Value is the output from the data port.

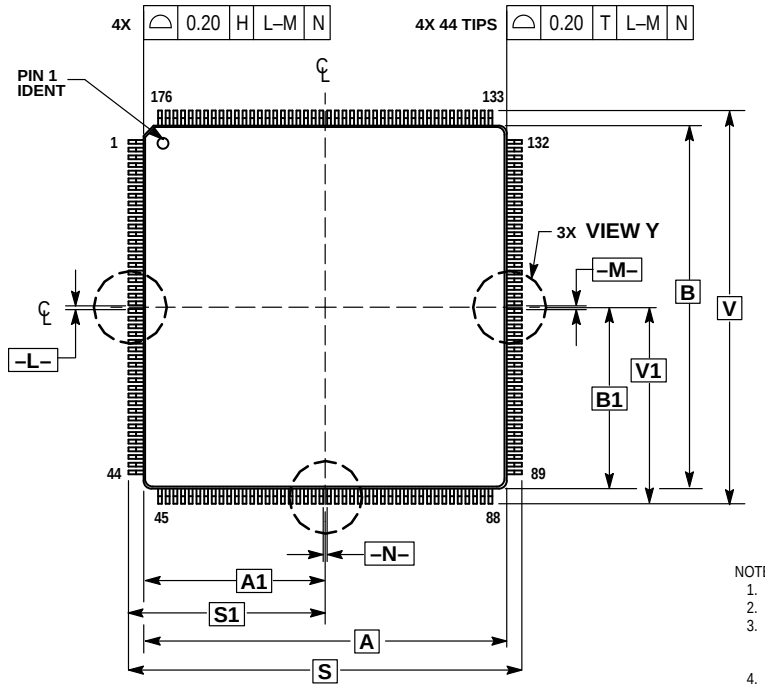
ORDERING INFORMATION
(Order by Full Part Number)

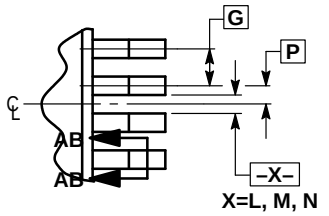


Full Part Numbers — MCM69D536TQ5 MCM69D536TQ6 MCM69D536TQ8
MCM69D536TQ5R MCM69D536TQ6R MCM69D536TQ8R

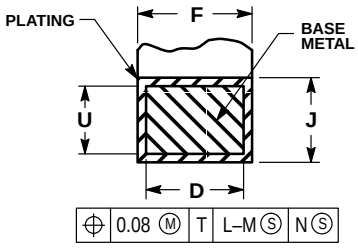
PACKAGE DIMENSIONS

TQFP PACKAGE
176 LEAD
CASE 1101–01

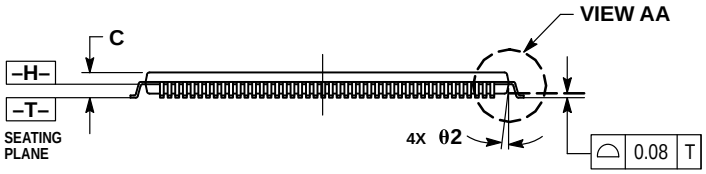


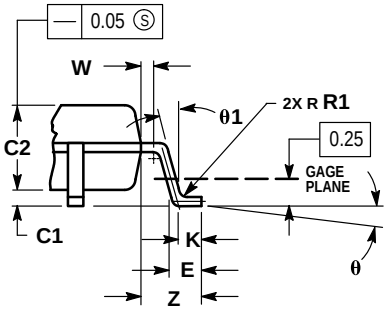


VIEW Y



SECTION AB–AB
ROTATED 90° CLOCKWISE





VIEW AA

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –L–, –M–, AND –N– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –T–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INLCUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35 (0.014) MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD 0.07 (0.003).

	MILLIMETERS	
DIM	MIN	MAX
A	24.00 BSC	
A1	12.00 BSC	
B	24.00 BSC	
B1	12.00 BSC	
C	—	1.60
C1	0.05	—
C2	1.35	1.45
D	0.17	0.23
E	0.45	0.75
F	0.17	0.27
G	0.50 BSC	
J	0.09	0.20
K	0.50 REF	
P	0.25 BSC	
R1	0.10	0.20
S	26.00 BSC	
S1	13.00 BSC	
U	0.09	0.16
V	26.00 BSC	
V1	13.00 BSC	
W	0.20 REF	
Z	1,00 REF	
θ	0°	7°
θ1	0°	—
θ2	12° REF	

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