

DATA SHEET

74ABT16652

16-bit transceiver/register, non-inverting
(3-State)

Product data

Replaces 74ABT16652/74ABTH16652 dated 1998 Feb 27

2002 Apr 03

16-bit transceiver/register, non-inverting (3-State)

74ABT16652

FEATURES

- Independent registers for A and B buses
- Multiple V_{CC} and GND pins minimize switching noise
- Power-up 3-State
- Power-up reset
- Live insertion/extraction permitted
- Multiplexed real-time and stored data
- Output capability: +64 mA/-32 mA
- Latch-up protection exceeds 500 mA per JEDEC Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT16652 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16652 transceiver/register consists of two sets of bus transceiver circuits with 3-State outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes HIGH. Output Enable ($nOEAB$, $nOEBA$) and Select ($nSAB$, $nSBA$) pins are provided for bus management.

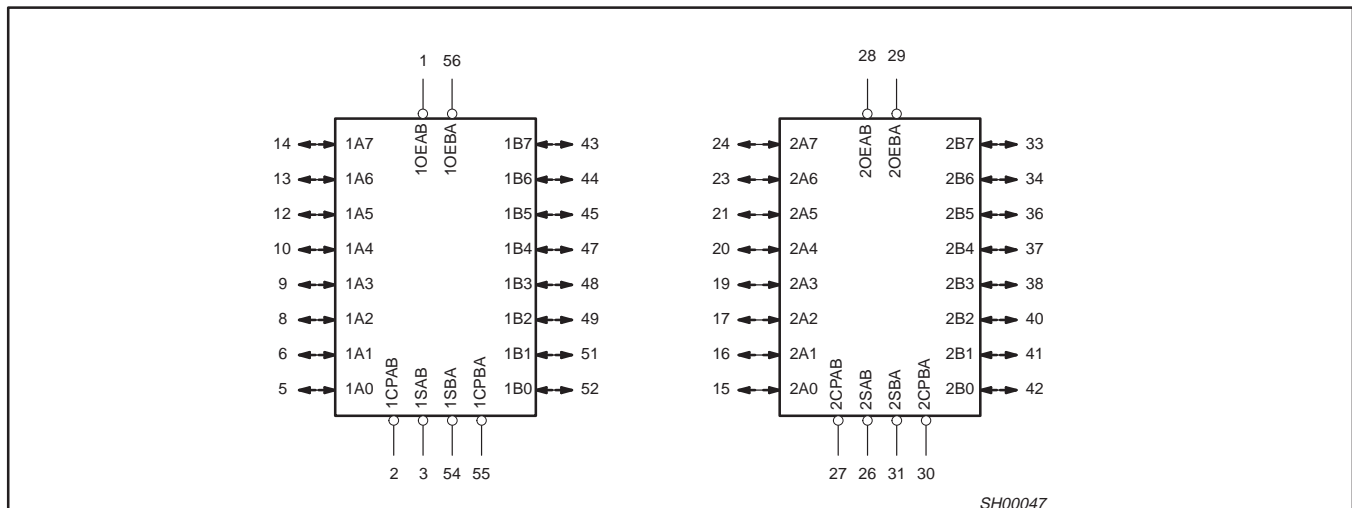
QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS $T_{amb} = 25\text{ }^{\circ}\text{C}; GND = 0\text{ V}$ | TYPICAL | UNIT |
|------------------------|------------------------------|--|------------|---------------|
| t_{PLH} t_{PHL} | Propagation delay nAx to nBx | $C_L = 50\text{ pF}; V_{CC} = 5\text{ V}$ | 2.3 1.8 | ns |
| C_{IN} | Input capacitance | $V_I = 0\text{ V or }V_{CC}$ | 4 | pF |
| $C_{I/O}$ | I/O capacitance | $V_O = 0\text{ V or }V_{CC}; 3\text{-State}$ | 7 | pF |
| I_{CCZ} | Quiescent supply current | Outputs disabled; $V_{CC} = 5.5\text{ V}$ | 500 | μA |
| I_{CCL} | | Outputs low; $V_{CC} = 5.5\text{ V}$ | 8 | mA |

ORDERING INFORMATION

| PACKAGES | TEMPERATURE RANGE | ORDER CODE | DWG NUMBER |
|------------------------------|-------------------|---------------|------------|
| 56-Pin Plastic SSOP Type III | -40 °C to +85 °C | 74ABT16652DL | SOT371-1 |
| 56-Pin Plastic TSSOP Type II | -40 °C to +85 °C | 74ABT16652DGG | SOT364-1 |

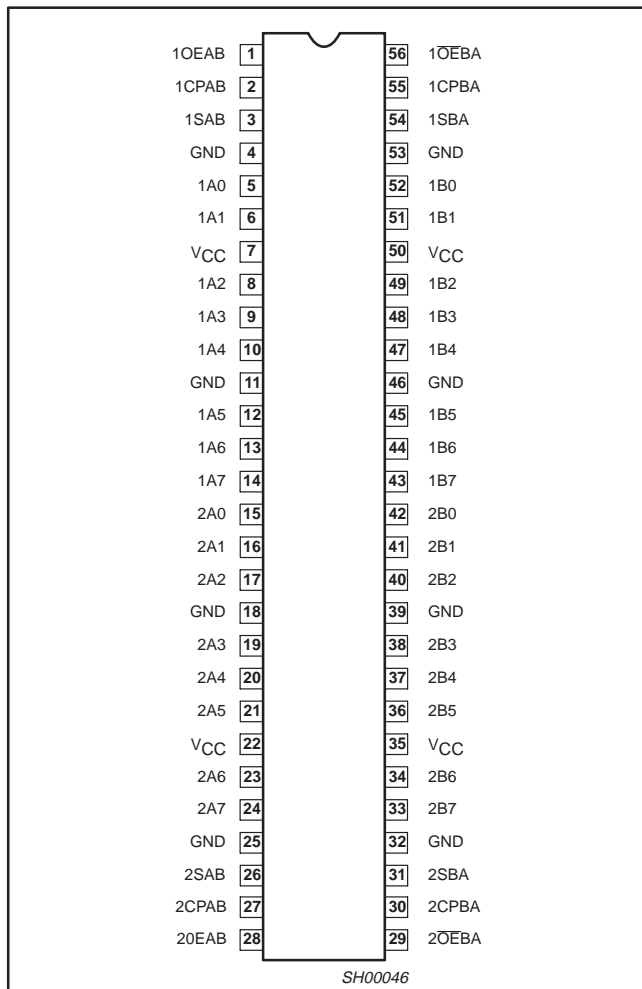
LOGIC SYMBOL



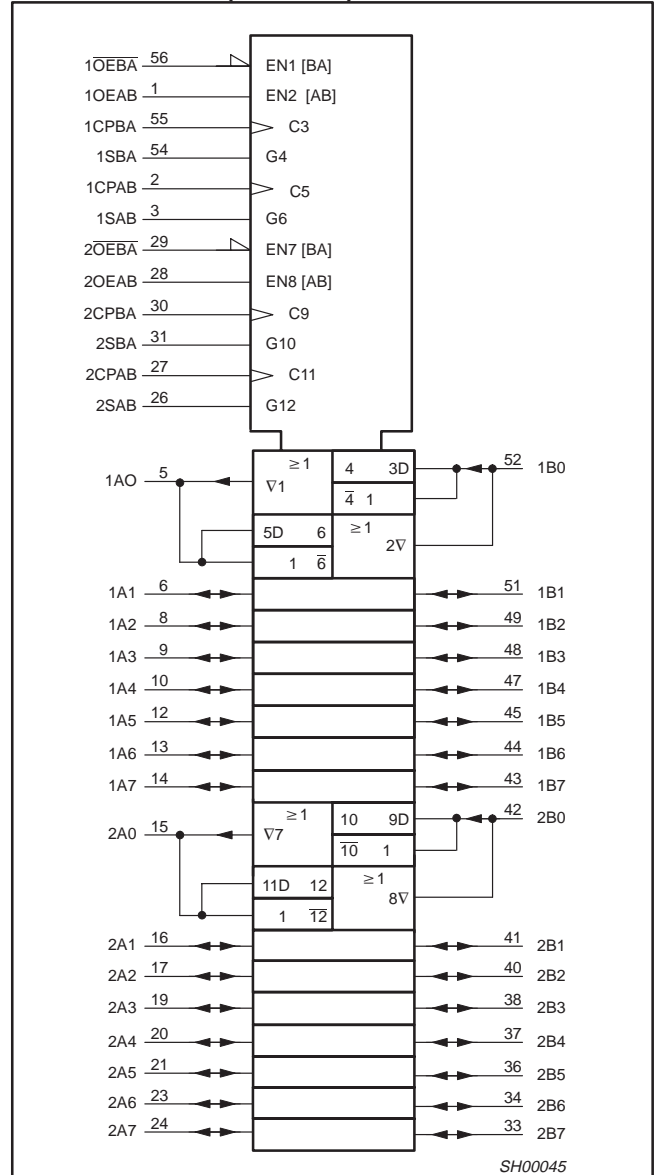
16-bit transceiver/register, non-inverting (3-State)

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PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



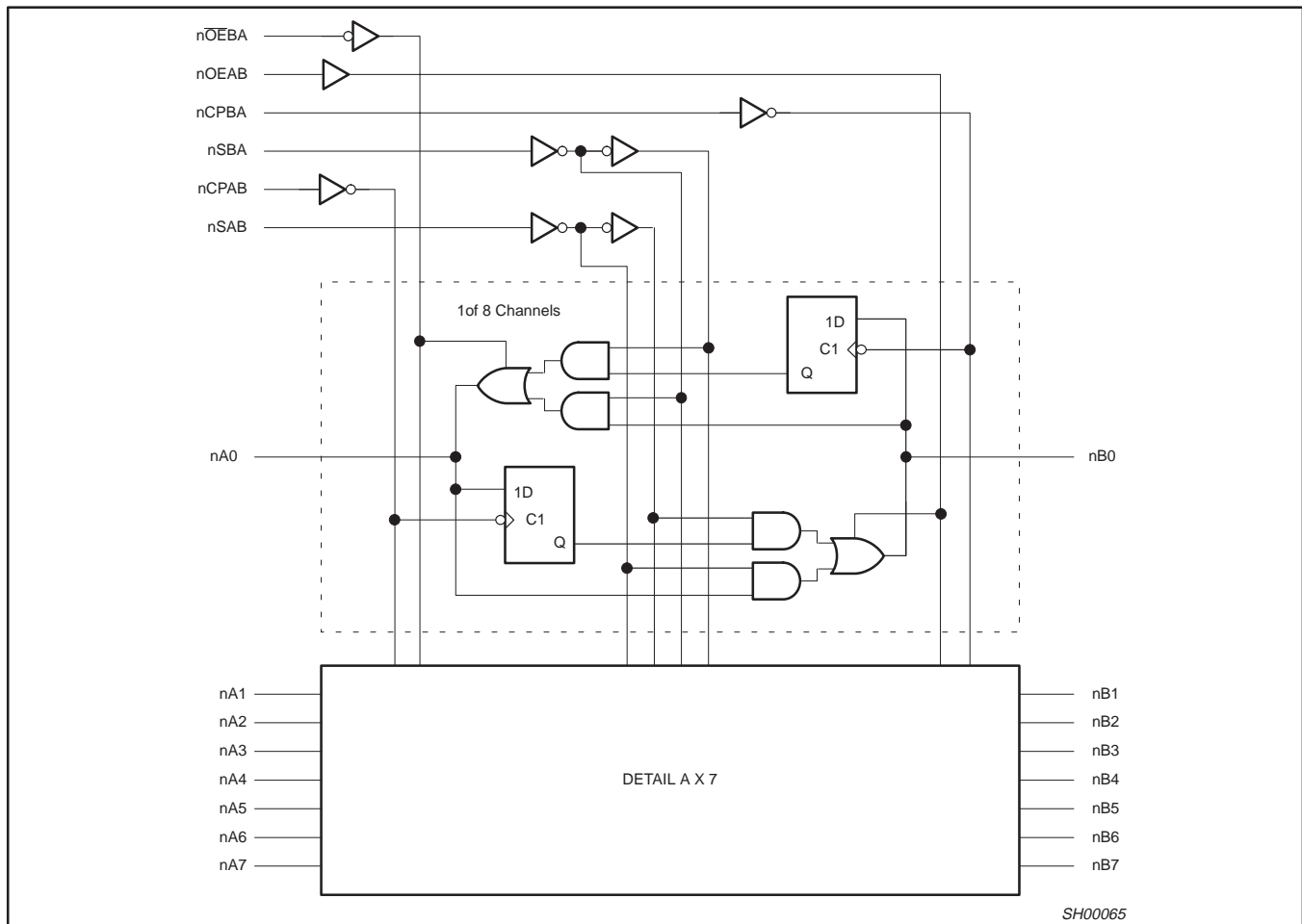
PIN DESCRIPTION

| PIN NUMBER | SYMBOL | NAME AND FUNCTION |
|--|-------------------------------|---|
| 2, 55, 27, 30 | 1CPAB, 1CPBA, 2CPAB, 2CPBA | Clock input A-to-B / Clock input B-to-A |
| 3, 54, 26, 31 | 1SAB, 1SBA, 2SAB, 2SBA | Select input A-to-B / Select input B-to-A |
| 5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24 | 1A0 – 1A7, 2A0 – 2A7 | Data inputs/outputs (A side) |
| 52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33 | 1B0 – 1B7, 2B0 – 2B7 | Data inputs/outputs (B side) |
| 1, 56, 28, 29 | 1OEAB, 1OEBA, 2OEAB, 2OEBA | Output enable inputs |
| 4, 11, 18, 25, 32, 39, 46, 53 | GND | Ground (0 V) |
| 7, 22, 35, 50 | V _{CC} | Positive supply voltage |

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LOGIC DIAGRAM



FUNCTION TABLE

| INPUTS | | | | | | DATA I/O | | OPERATING MODE |
|--------|-------|--------|--------|------|------|---------------------|---------------------|---|
| nOEAB | nOEBA | nCPAB | nCPBA | nSAB | nSBA | nAx | nBx | |
| L | H | H or L | H or L | X | X | Input | Input | Isolation Store A and B data |
| L | H | ↑ | ↑ | X | X | Input | Input | Store A, Hold B Store A in both registers |
| X | H | ↑ | H or L | X | X | Input | Unspecified output* | Store A, Hold B Store A in both registers |
| H | H | ↑ | ↑ | ** | X | Unspecified output* | Input | Hold A, Store B Store B in both registers |
| L | X | H or L | ↑ | X | X | Unspecified output* | Input | Hold A, Store B Store B in both registers |
| L | L | X | X | X | L | Output | Input | Real time B data to A bus Stored B data to A bus |
| L | L | X | H or L | X | H | Output | Input | Real time B data to A bus Stored B data to A bus |
| H | H | X | X | L | X | Input | Output | Real time A data to B bus Store A data to B bus |
| H | H | H or L | X | H | X | Input | Output | Real time A data to B bus Store A data to B bus |
| H | L | H or L | H or L | H | H | Output | Output | Stored A data to B bus Stored B data to A bus |

H = HIGH voltage level

L = LOW voltage level

X = Don't care

↑ = Low-to-High clock transition

* The data output function may be enabled or disabled by various signals at the nOEBA and nOEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the clock.

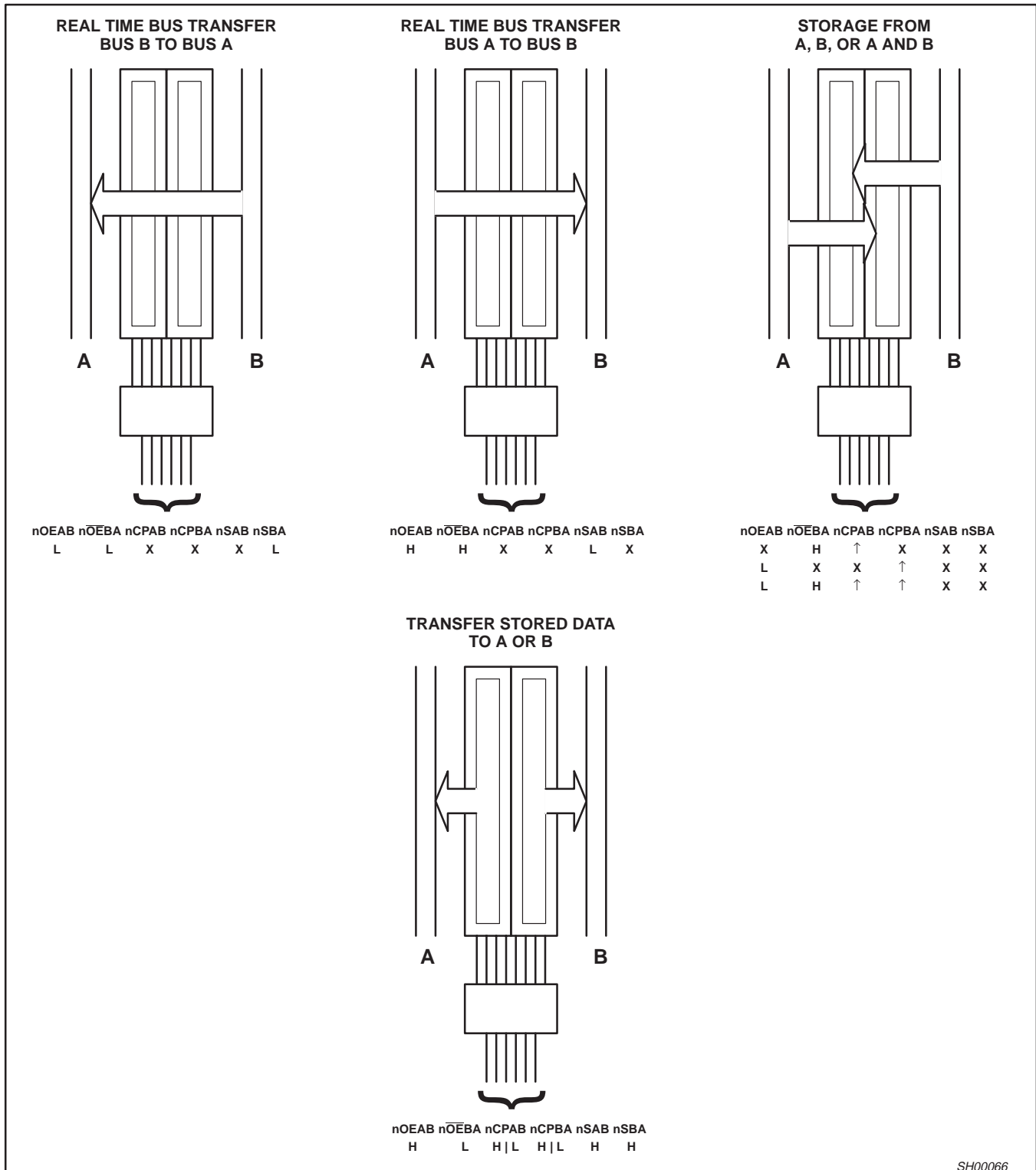
** If both Select controls (nSAB and nSBA) are LOW, then clocks can occur simultaneously. If either Select control is HIGH, the clocks must be staggered in order to load both registers.

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The following examples demonstrate the four fundamental bus-management functions that can be performed with the 74ABT16652. The select pins determine whether data is stored or

transferred through the device in real time. The output enable pins determine the direction of the data flow.



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ABSOLUTE MAXIMUM RATINGS^{1, 2}

| SYMBOL | PARAMETER | CONDITIONS | RATING | UNIT |
|------------------|--------------------------------|-----------------------------|--------------|------|
| V _{CC} | DC supply voltage | | -0.5 to +7.0 | V |
| I _{IK} | DC input diode current | V _I < 0 | -18 | mA |
| V _I | DC input voltage ³ | | -1.2 to +7.0 | V |
| I _{OK} | DC output diode current | V _O < 0 | -50 | mA |
| V _{OUT} | DC output voltage ³ | output in Off or HIGH state | -0.5 to +5.5 | V |
| I _{OUT} | DC output current | output in LOW state | 128 | mA |
| | | output in HIGH state | -64 | |
| T _{stg} | Storage temperature range | | -65 to 150 | °C |

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | UNIT |
|------------------|--------------------------------------|--------|-----------------|------|
| | | MIN | MAX | |
| V _{CC} | DC supply voltage | 4.5 | 5.5 | V |
| V _I | Input voltage | 0 | V _{CC} | V |
| V _{IH} | HIGH-level input voltage | 2.0 | - | V |
| V _{IL} | LOW-level Input voltage | - | 0.8 | V |
| I _{OH} | HIGH-level output current | - | -32 | mA |
| I _{OL} | LOW-level output current | - | 64 | mA |
| Δt/Δv | Input transition rise or fall rate | 0 | 10 | ns/V |
| T _{amb} | Operating free-air temperature range | -40 | +85 | °C |

16-bit transceiver/register, non-inverting (3-State)

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DC ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | | | UNIT |
|------------------------------------|--|--|---------------------------|-------|------|-------------------------------------|------|------|
| | | | T _{amb} = +25 °C | | | T _{amb} = -40 °C to +85 °C | | |
| | | | MIN | TYP | MAX | MIN | MAX | |
| V _{IK} | Input clamp voltage | V _{CC} = 4.5 V; I _{IK} = -18 mA | | -0.9 | -1.2 | | -1.2 | V |
| V _{OH} | HIGH-level output voltage | V _{CC} = 4.5 V; I _{OH} = -3 mA; V _I = V _{IL} or V _{IH} | 2.5 | 2.9 | | 2.5 | | V |
| | | V _{CC} = 5.0 V; I _{OH} = -3 mA; V _I = V _{IL} or V _{IH} | 3.0 | 4.0 | | 3.0 | | V |
| | | V _{CC} = 4.5 V; I _{OH} = -32 mA; V _I = V _{IL} or V _{IH} | 2.0 | 2.4 | | 2.0 | | V |
| V _{OL} | LOW-level output voltage | V _{CC} = 4.5 V; I _{OL} = 64 mA; V _I = V _{IL} or V _{IH} | | 0.35 | 0.55 | | 0.55 | V |
| V _{RST} | Power-up output low voltage ³ | V _{CC} = 5.5 V; I _{OL} = 1 mA; V _I = GND or V _{CC} | | 0.13 | 0.55 | | 0.55 | V |
| I _I | Input leakage current | V _{CC} = 5.5 V; V _I = GND or V _{CC} Control pins | | ±0.01 | ±1.0 | | ±1.0 | µA |
| I _{OFF} | Power-off leakage current | V _{CC} = 0 V; V _O = 4.5 V; V _I = 0 V or 5.5 V | | ±1.0 | ±100 | | ±100 | µA |
| I _{PU/PD} | Power-up/down 3-State output current ⁴ | V _{CC} = 2.1 V; V _O = 0.0 V; V _I = GND or V _{CC} | | ±1.0 | ±50 | | ±50 | µA |
| I _{IH} + I _{OZH} | 3-State output HIGH current | V _{CC} = 5.5 V; V _O = 5.5 V; V _I = V _{IL} or V _{IH} | | 1.0 | 10 | | 10 | µA |
| I _{IL} + I _{OZL} | 3-State output LOW current | V _{CC} = 5.5 V; V _O = 0.0 V; V _I = V _{IL} or V _{IH} | | -1.0 | -10 | | -10 | µA |
| I _{CEX} | Output HIGH leakage current | V _{CC} = 5.5 V; V _O = 5.5 V; V _I = GND or V _{CC} | | 5.0 | 50 | | 50 | µA |
| I _O | Output current ¹ | V _{CC} = 5.5 V; V _O = 2.5 V | -50 | -80 | -180 | -50 | -180 | mA |
| I _{CCH} | Quiescent supply current | V _{CC} = 5.5 V; Outputs HIGH, V _I = GND or V _{CC} | | 0.5 | 2 | | 2 | mA |
| I _{CCL} | | V _{CC} = 5.5 V; Outputs LOW, V _I = GND or V _{CC} | | 8 | 19 | | 19 | mA |
| I _{CCZ} | | V _{CC} = 5.5 V; Outputs 3-State; V _I = GND or V _{CC} | | 0.5 | 2 | | 2 | mA |
| ΔI _{CC} | Additional supply current per input pin ² | V _{CC} = 5.5 V; one input at 3.4 V, other inputs at V _{CC} or GND | | 5.0 | 50 | | 50 | µA |

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4 V.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
- This parameter is valid for any V_{CC} between 0 V and 2.1 V. When the part enables with V_{CC} between 2.1 V and 4.5 V, the outputs will correctly function with respect to all input logic states.

16-bit transceiver/register, non-inverting (3-State)

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AC CHARACTERISTICS

GND = 0 V, $t_R = t_F = 2.5$ ns, $C_L = 50$ pF, $R_L = 500$ Ω

| SYMBOL | PARAMETER | WAVEFORM | LIMITS | | | | | UNIT |
|------------------------|---|----------|---|------------|------------|---|------------|------|
| | | | $T_{amb} = +25$ °C $V_{CC} = +5.0$ V | | | $T_{amb} = -40$ °C to $+85$ °C $V_{CC} = +5.0$ V ± 0.5 V | | |
| | | | MIN | TYP | MAX | MIN | MAX | |
| f_{MAX} | Maximum clock frequency | 1 | 125 | | | 125 | | MHz |
| t_{PLH} t_{PHL} | Propagation delay nCPAB to nBx or nCPBA to nAx | 1 | 1.5 1.5 | 3.3 2.8 | 4.0 4.1 | 1.5 1.5 | 4.9 4.7 | ns |
| t_{PLH} t_{PHL} | Propagation delay nAx to nBx or nBx to nAx | 2 | 1.0 1.0 | 2.3 1.8 | 3.2 4.1 | 1.0 1.0 | 3.9 4.6 | ns |
| t_{PLH} t_{PHL} | Propagation delay nSAB to nBx or nSBA to nAx | 3 | 1.0 1.0 | 3.4 2.6 | 4.3 4.3 | 1.0 1.0 | 5.0 5.0 | ns |
| t_{pZH} t_{pZL} | Output enable time nOEBA to nAx | 5 6 | 1.0 1.5 | 2.5 2.2 | 4.1 4.4 | 1.0 1.5 | 5.0 5.3 | ns |
| t_{pHZ} t_{pLZ} | Output disable time nOEBA to nAx | 5 6 | 1.5 1.5 | 3.6 2.7 | 4.4 3.6 | 1.5 1.5 | 4.9 4.0 | ns |
| t_{pZH} t_{pZL} | Output enable time nOEAB to nBx | 5 6 | 1.0 1.5 | 2.9 3.0 | 3.6 3.9 | 1.0 1.5 | 4.2 4.6 | ns |
| t_{pHZ} t_{pLZ} | Output disable time nOEAB to nBx | 5 6 | 2.0 1.5 | 3.1 2.3 | 5.5 4.5 | 2.0 1.5 | 5.9 5.2 | ns |

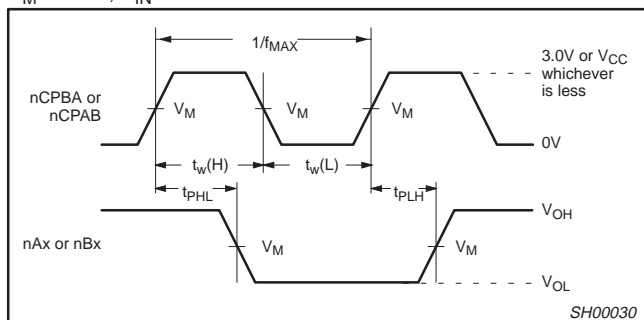
AC SET-UP REQUIREMENTS

GND = 0 V, $t_R = t_F = 2.5$ ns, $C_L = 50$ pF, $R_L = 500$ Ω

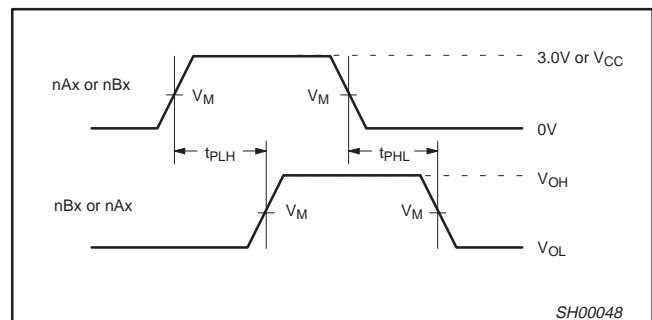
| SYMBOL | PARAMETER | WAVEFORM | LIMITS | | | UNIT |
|----------------------|--|----------|---|--------------|---|------|
| | | | $T_{amb} = +25$ °C $V_{CC} = +5.0$ V | | $T_{amb} = -40$ °C to $+85$ °C $V_{CC} = +5.0$ V ± 0.5 V | |
| | | | MIN | TYP | MIN | |
| $t_s(H)$ $t_s(L)$ | Set-up time nAx to nCPBA, nBx to nCPAB | 4 | 3.0 3.0 | 1.2 0.8 | 3.0 3.0 | ns |
| $t_h(H)$ $t_h(L)$ | Hold time nAx to nCPBA, nBx to nCPAB | 4 | 1.0 1.0 | -0.7 -1.1 | 1.0 1.0 | ns |
| $t_w(H)$ $t_w(L)$ | Pulse width, HIGH or LOW nCPAB or nCPBA | 1 | 4.3 4.3 | 1.0 1.0 | 4.3 4.3 | ns |

AC WAVEFORMS

$V_M = 1.5$ V, $V_{IN} =$ GND to 3.0 V



Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



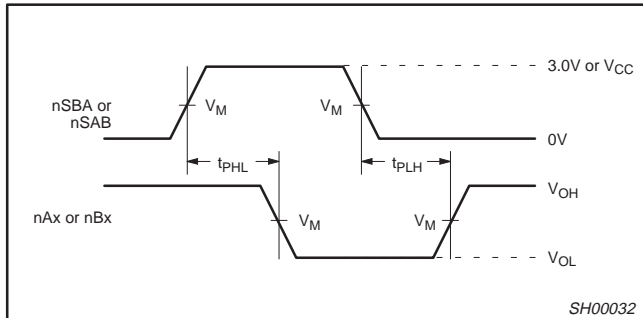
Waveform 2. Propagation Delay, nAx to nBx or nBx to nAx

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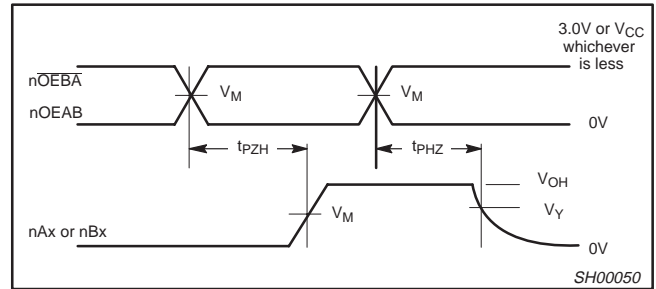
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AC WAVEFORMS (Continued)

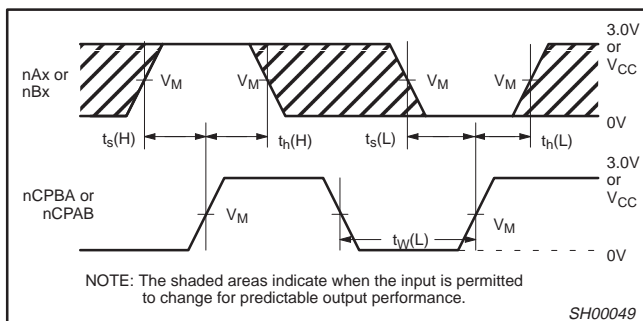
$V_M = 1.5\text{ V}$, $V_{IN} = \text{GND to } 3.0\text{ V}$



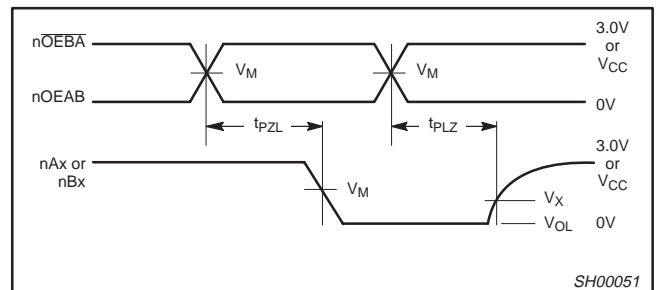
Waveform 3. Propagation Delay, SBA to nAx or SAB to nBx



Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 4. Data Set-up and Hold Times



Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS

Test Circuit for 3-State Outputs

**$V_M = 1.5\text{ V}$
Input Pulse Definition**

SWITCH POSITION

| TEST | SWITCH |
|-----------|--------|
| t_{PLZ} | closed |
| t_{PZL} | closed |
| All other | open |

DEFINITIONS:

R_L = Load resistor; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

| FAMILY | INPUT PULSE REQUIREMENTS | | | | |
|---------|--------------------------|-----------|-------|-------|-------|
| | Amplitude | Rep. Rate | t_w | t_R | t_F |
| 74ABT16 | 3.0V | 1MHz | 500ns | 2.5ns | 2.5ns |

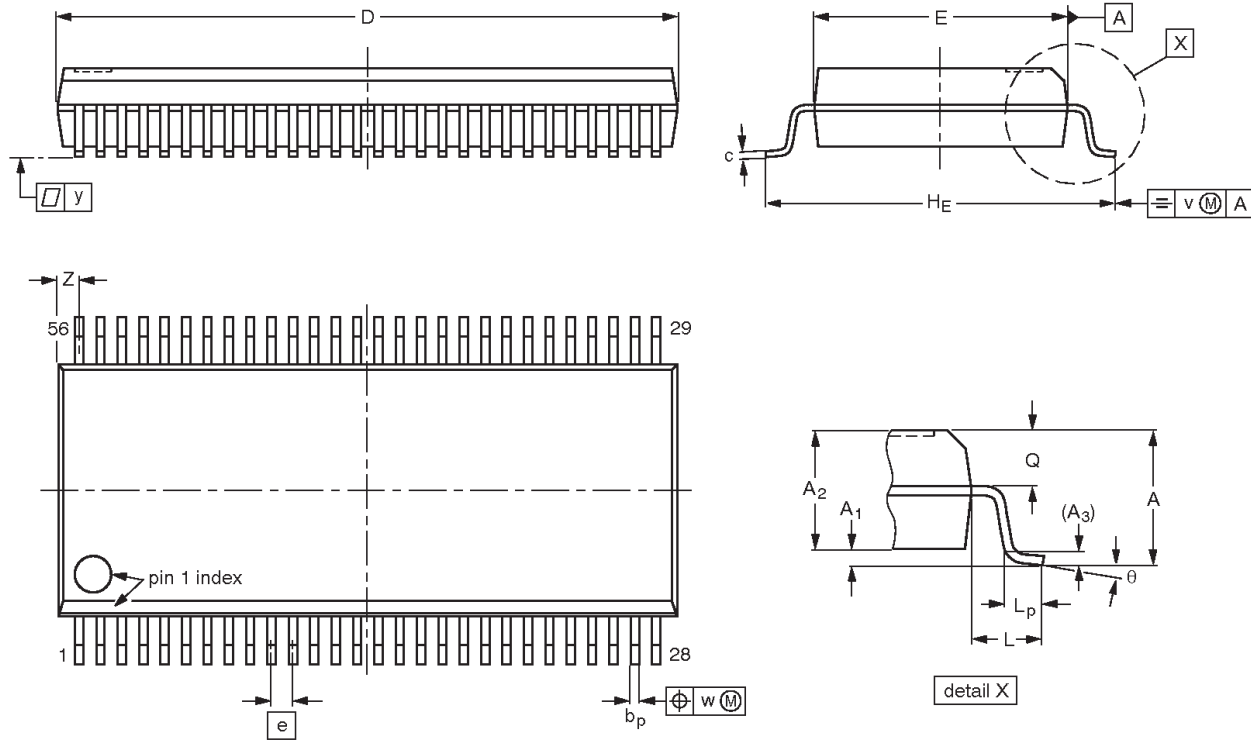
SH00022

16-bit transceiver/register, non-inverting (3-State)

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SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _E | L | L _p | Q | v | w | y | Z ⁽¹⁾ | θ |
|------|--------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|-------|----------------|-----|----------------|------------|------|------|-----|------------------|----------|
| mm | 2.8 | 0.4 0.2 | 2.35 2.20 | 0.25 | 0.3 0.2 | 0.22 0.13 | 18.55 18.30 | 7.6 7.4 | 0.635 | 10.4 10.1 | 1.4 | 1.0 0.6 | 1.2 1.0 | 0.25 | 0.18 | 0.1 | 0.85 0.40 | 8° 0° |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

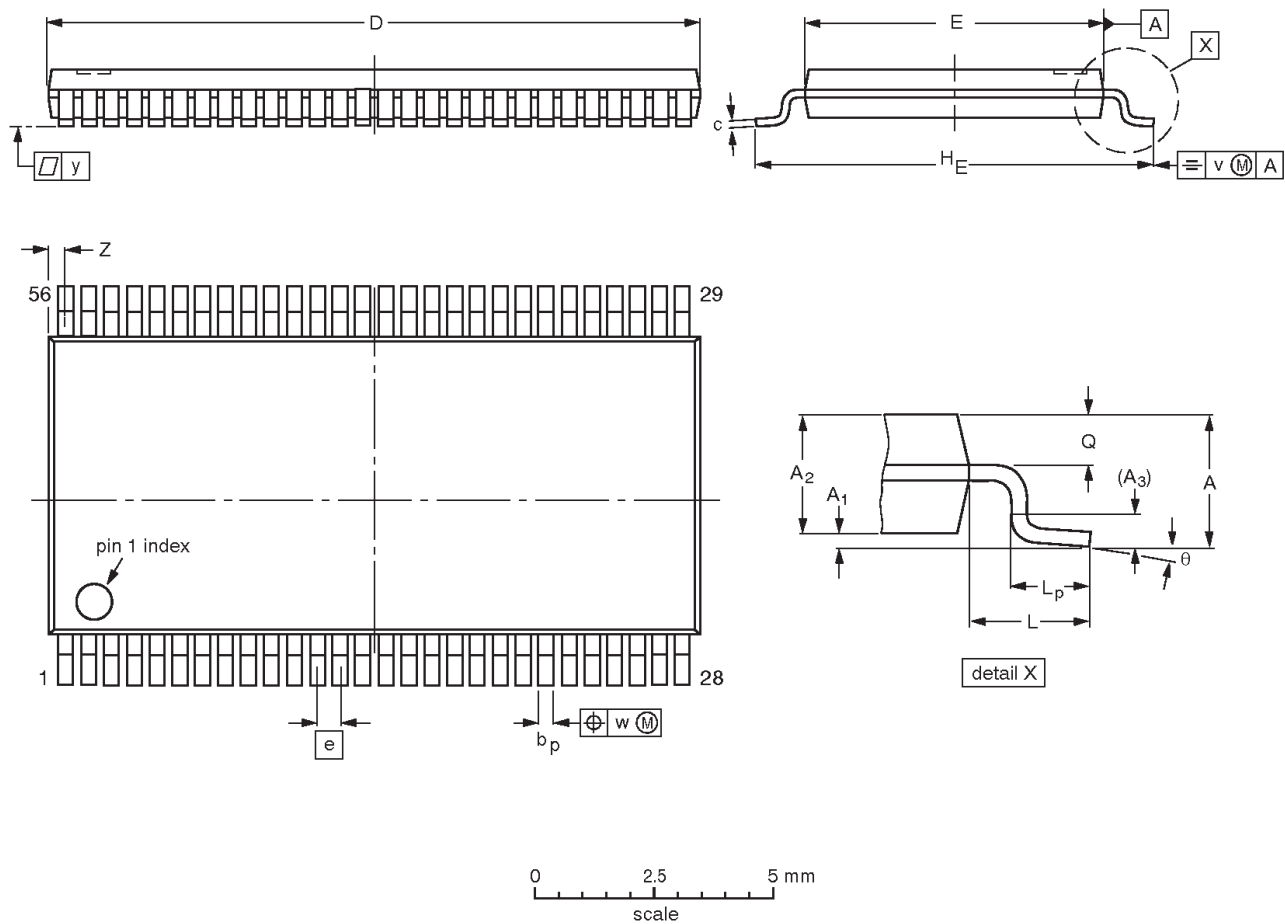
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|--------|------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT371-1 | | MO-118 | | | | 95-02-04 99-12-27 |

16-bit transceiver/register, non-inverting (3-State)

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TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1



DIMENSIONS (mm are the original dimensions).

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽²⁾ | e | H _E | L | L _p | Q | v | w | y | Z | θ |
|------|--------|----------------|----------------|----------------|----------------|------------|------------------|------------------|-----|----------------|-----|----------------|--------------|------|------|-----|------------|----------|
| mm | 1.2 | 0.15 0.05 | 1.05 0.85 | 0.25 | 0.28 0.17 | 0.2 0.1 | 14.1 13.9 | 6.2 6.0 | 0.5 | 8.3 7.9 | 1.0 | 0.8 0.4 | 0.50 0.35 | 0.25 | 0.08 | 0.1 | 0.5 0.1 | 8° 0° |

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|--------|------|--|---------------------|-----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT364-1 | | MO-153 | | | | -95-02-10 99-12-27 |

16-bit transceiver/register, non-inverting (3-State)

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Data sheet status

| Data sheet status ^[1] | Product status ^[2] | Definitions |
|----------------------------------|-------------------------------|--|
| Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
| Preliminary data | Qualification | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product. |
| Product data | Production | This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A. |

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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