

GaAs MMIC Power Amplifier 2 - 6 GHz

MAAM26100-P1

V1.A

Features

- +30 dBm Saturated Output Power
- 18 dB Typical Gain
- 30% Power Added Efficiency
- On-Chip Bias Network
- DC Decoupled RF Input and Output
- High Performance Ceramic Bolt Down Package

Description

M/A-COM's MAAM26100-P1 is a GaAs MMIC two stage high efficiency power amplifier in a high performance bolt down ceramic package. The MAAM26100-P1 is a fully monolithic design for operation in 50-ohm systems, with an on-chip negative bias network which eliminates the need for external bias circuitry.

The MAAM26100-P1 is ideally suited for driver amplifiers and transmitter outputs in Electronic Warfare Jammers, Missile Subsystems and Phased Array Radars.

M/A-COM's MAAM26100-P1 is fabricated using a mature 0.5-micron gate length GaAs process. The process features full passivation for increased performance reliability.

Ordering Information

Part Number	Package		
MAAM26100-P1	Ceramic Bolt Down		

CR-15



Notes: (unless otherwise specified) 1. Dimensions are inches. 2. Tolerance: in .xxx = ±.010

Typical Electrical Specifications, $T_A = +25^{\circ}C$, $V_{DD} = +8 V$, $V_{GG} = -5 V$

Parameter	Test Conditions		Units	Min.	Тур.	Max.
Small Signal Gain	$P_{IN} \le -10 \text{ dBm}$	2 - 6 GHz	dB		18	
Input VSWR	P _{IN} ≤ -10 dBm	2 - 6 GHz			2.0:1	
Output VSWR	P _{IN} ≤-10 dBm	2 - 6 GHz			2.2:1	
Output Power	P _{IN} = +15 dBm	2 - 6 GHz	dBm		+30	
Power Added Efficiency	P _{IN} = +15 dBm	2 - 6 GHz	%		30	
Output IP ₃		2, 5 & 6 GHz	dBm		40	

The Preliminary Specifications Data Sheet Contains Typical Electrical Specifications Which May Change Prior to Final Introduction.

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Absolute Maximum Ratings^{1, 2}

Parameter	Absolute Maximum		
V _{DD}	10 Volts		
V _{GG}	-10 Volts		
Power Dissipation	8.4 W		
RF Input Power	+23 dBm		
Channel Temperature	150°C		
Storage Temperature	-65°C to +150°C		
Thermal Resistance (Channel to Case)	15°C/W		

1. Exceeding these limits may cause permanent damage.

2. Case Temperature (Tc) = $+25^{\circ}C$

Functional Diagram^{3,4}



- Nominal bias is obtained by first connecting -5 volts to pin 6 (VGG),followed by connecting +9 volts to pin 10 (VDD). Note sequence.
- 4. RF ground and thermal interface is the flange (case bottom). Adequate heat sinking is required.











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Typical Performance @+25°C

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