



6-Channel Audio DAC, 24-bit, 192kHz

DESCRIPTION

The CE2746 is a mixed signal CMOS monolithic audio digital to analog converter. It contains six 1-bit sigma delta DAC. The system consists of 128-time interpolation filters, 4th order $\Sigma\Delta$ modulators, switch capacitors and analog reconstruction filters. The one bit $\Sigma\Delta$ converter offers superior differential linearity, with no distortion due to component mis-match. high tolerance to clock jitter.

The CE2746 support data conversion from 32K to 192KHz. The analog section operates at 5 volt while the digital section at 3.3 volt. This dual voltage system reduces not only the power consumption but also the noise caused by the digital circuit switching. The CE2746 is ideal for DVD player, AV receiver and set-top box application.

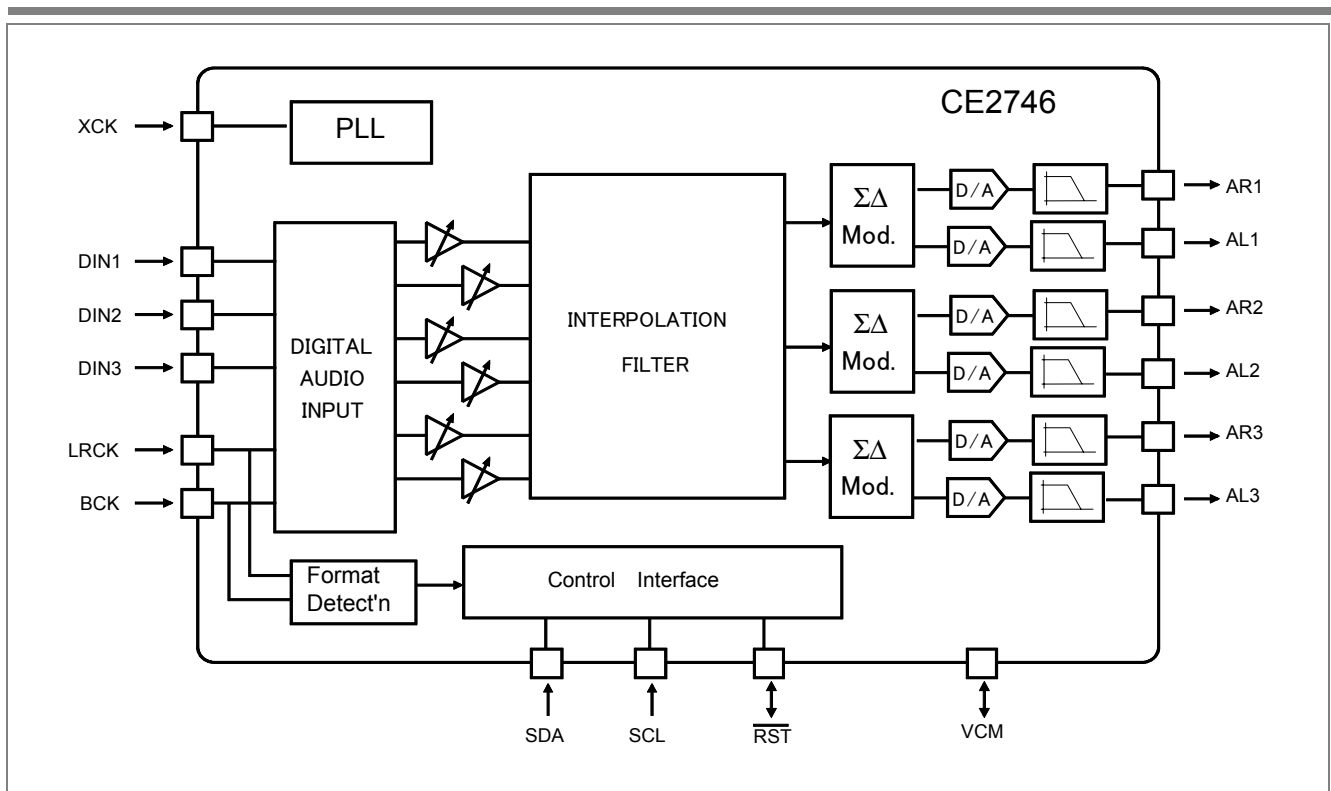
The CE2746 support 24, 20, 18 and 16-bit input data. It also support multiple sampling frequency data. Each DAC has its own individual volume control.

FEATURES

- Six Channel Audio DAC.
 - 104 dB SNR (A Weighted).
 - -94 dB THD + N Ratio (A Weighted).
 - 8K - 192 KHz. Sampling Rates.
 - Independent Digital Volume Control.
 - I²S, Left and Right Justified Digital Input Formats.
 - On -chip Reconstruction Filters.
- 3.3 -volt Digital Interface.
- 2-wire Serial Control Interface.
- 3.3 Volt Digital. 5 Volt Analog Power Supply.

Applications

- Digital Surround Sound For Home Theatre
- DVD
- Car Audio.



DAC Performance

Item	PERFORMANCE SPECIFICATIONS	Spec.
1	Audio Output Level	1 Vrms
2	Audio Bandwidth 20Hz - 20 KHz	+/- 0.1 dB
3	SNR (A-weight)	>104 dB
4	THD + NOISE (A-weight, 0 dB input)	< -88 dB
5	Dynamic Range	98 dB
6	Channel Separation	< -90 dB
7	Nonlinear Distortion	< 0.25 dB
8	Channel Gain Error	< 0.1 dB

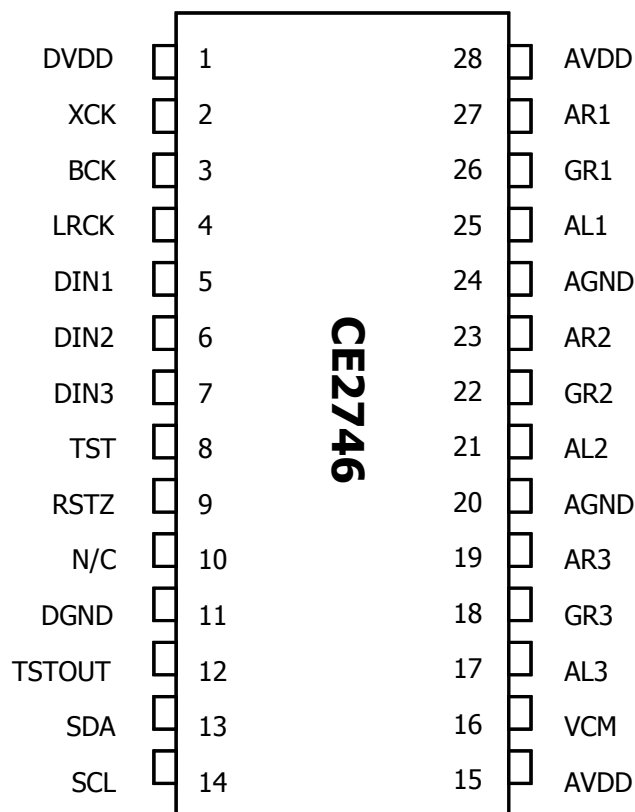
All Measurement were taken with only one channel active.

XCK REQUIREMENT

The CE2746 supports 384 and 256 times sampling clock for 32, 44.1, 48, 96 and 192K audio; 192 or 128 times for the 96 K audio.; and 96 and 64 times for the 192K audio.

XCK Requirement

Sampling Rate	XCK Freq.					
	CREG1[5:4]=[0 0]		CREG1[5:4]=[1 0]		CREG1[5:4]=[0 1]	
	Normal XCK		4 times XCK		2 times XCK	
fs	384*fs	256*fs	4*384*fs	4*256*fs	2*384*fs	2*256*fs
32 K	12.288 MHz	8.192 MHz	49.152 MHz	32.768 MHz	24.576 MHz	16.384 MHz
44.1	16.934 Mhz	11.29 Mhz.	67.738 Mhz	45.158 Mhz.	33.869 Mhz	22.579 Mhz.
48 K	18.432 MHz	12.288 Mhz.	73.728 MHz	49.152 Mhz.	36.864 MHz	24.576 Mhz.
96 K	18.432 MHz	12.288 Mhz.	73.728 MHz	49.152 Mhz.	36.864 MHz	24.576 Mhz.
192 K	18.432 Mhz	12.288 Mhz.	73.728 Mhz	49.152 Mhz.	36.864 Mhz	24.576 Mhz.

PIN ASSIGNMENT
**PIN DESCRIPTION**

Pin Name	Pin #	Type	Description
DIGITAL			
DVDD	1	+3.3V	Digital power supply, 3.3 Volt.
XCK	2	I	External Master Clock Input.
BCK	3	I	Audio Serial Data Clock Input.
LRCK	4	I	Left/Right Channel Clock pin. For Left justified or Right justified mode, a high in SF indicates Left Channel Data, a low in SF indicates Right Channel Data. For I2S mode, a low in SF indicates Left Channel Data, a high in SF indicates Right Channel Data.
DIN1	5	I	Channel 1 Serial Audio Data Input.
DIN2	6	I	Channel 2 Serial Audio Data Input.
DIN3	7	I	Channel 3 Serial Audio Data Input.
TST	8	I	Test pin. This pin should be connected to ground.
RSTZ	9	I/O	Active Low Reset Pin. <i>Open drain output</i> with a 5 Kohms pull-up resistor. Should leave open if not connected to system reset.
N/C	10		Not used. can connected to ground.

PIN DESCRIPTION (Continued)

Pin Name	Pin #	Type	Description
DGND	11	GND	Digital ground
TSTOUT	12	T	Tri-state output pin, This pin can be connected to ground or leave open
SDA	13	I/O	I2C data bus. <i>Open drain output</i> . Externally this pin should tie to a 680 ohm pull up resistor.
SCL	14	I	I2C clock input.

Analog

AVDD	28	+5V	Analog circuits power supply.Should be Connected to a 22 uF capacitor in parallel with a 0.1 uF.
AR1	27	O	Analog right channel 1 output
GR0	26	GND	Analog circuits ground
AL1	25	O	Analog left channel 1 output
AGND	24	GND	Analog circuits ground
AR2	23	O	Analog right channel 2 output
GR1	22	GND	Analog circuits ground
AL2	21	O	Analog left channel 2 output
AGND	20	GND	Analog circuits ground
AR3	19	O	Analog right channel 3 output
GR2	18	GND	Analog circuits ground
AL3	17	O	Analog right channel 3 output
VCM	16	I/O	Common voltage De-coupling Pin Should be Connected to a 22 uF capacitor in parallel with a 0.1 uF.
AVDD	15	+5V	Analog circuits power supply.Should be Connected to a 22 uF capacitor in parallel with a 0.1 uF.

DIGITAL AUDIO SERIAL INTERFACE

The digital serial interface consists of 3 serial input pins, DIN1, DIN2, DIN3, and one serial clock input pin, BCK, and one left/right indicator input pin, LRCK. The data are 2's complement MSB first numbers. The CE2746 supports four resolution, which are selected programming the control register CREG0[5:4] via the I²C serial control port. Table 1 describes these four resolution.

Table (1): Audio Serial Data Input Resolution,

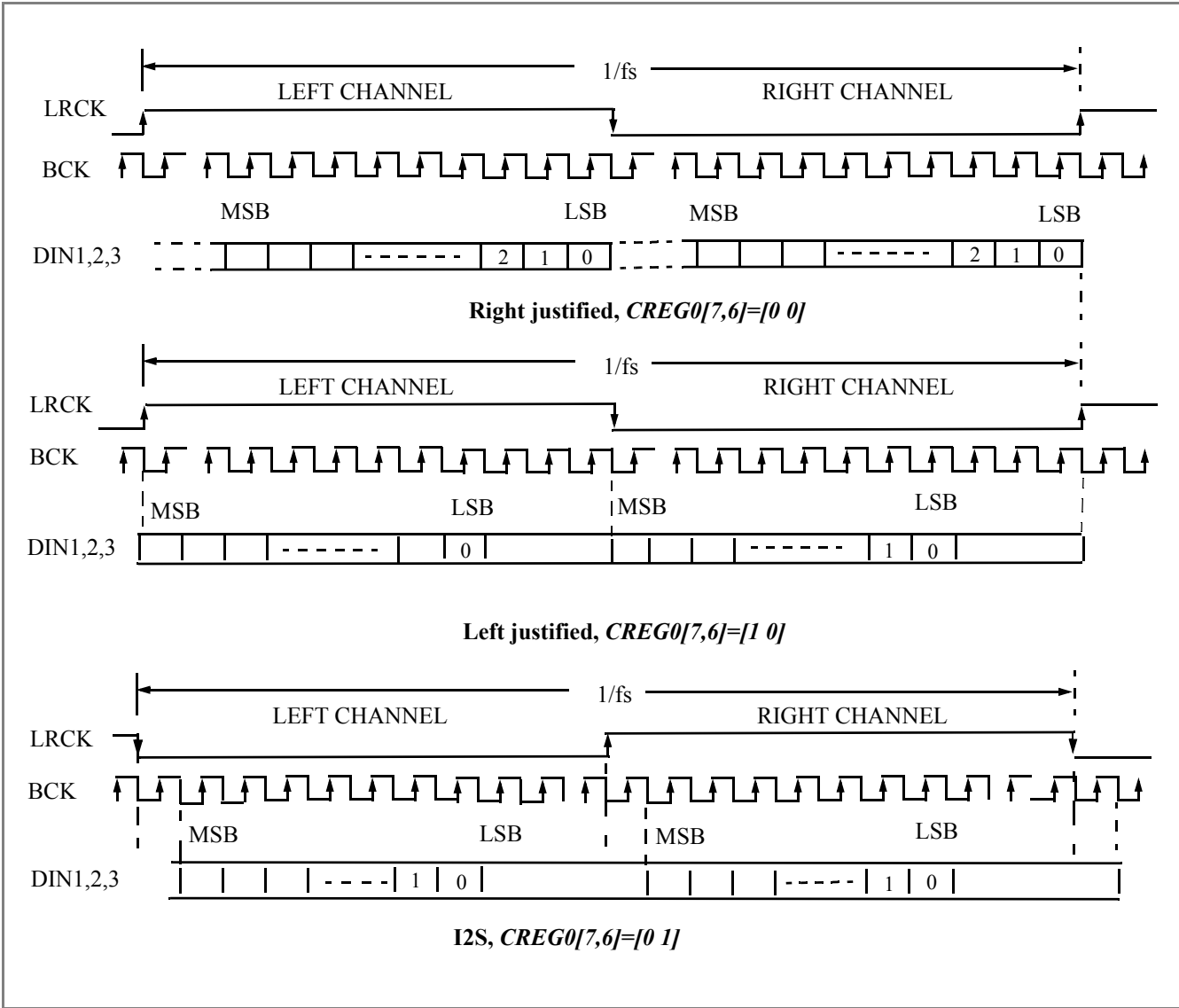
Format	CREG0[5:4]	DIN[3:1]
0	00	24-bit (default)
1	01	20-bit
2	10	18-bit
3	11	16-bit

The DIN3, DIN2 and DIN1 can be either 24-bit or 32-bit per frame as well as left justified, right justified or I2S. The CE2746 counts the number of BCK per frame to determine whether the input is 24 or 32 bits format.

Table (2): Audio Serial Data Input Modes

Mode	CREG0[7:6]	DIN[3:1]
0	00	Right Justified
1	01	I2S
2	10	Left Justified (default)
3	11	Invalid

Figure 1. Audio Serial Input Data Timing Diagram



INFINITE ZERO DETECTION

The CE2746 has an Infinite Zero Detection circuit which detects zero in the Audio Serial Port that lasts for approximately 0.2 sec. By default, the zero detection circuit is on.

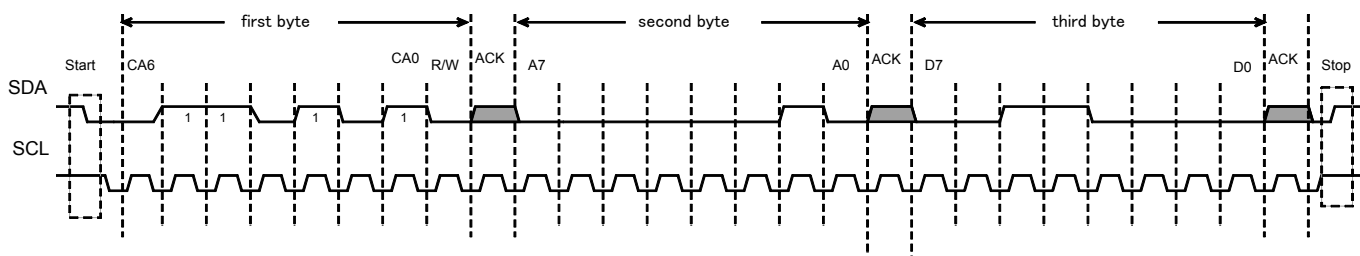
Serial Command Port

The user can select the chip operation mode by programming the internal control registers through serial I²C port. The Chip Address for the CE2746 is 35H. The protocol for write operation consists of sending 3 byte data to CE2746, following each byte is the acknowledges generated by CE2746. The first byte is the 7-bit Chip Address followed by the read/write bit (read is high, write is low). The second byte is the control register address. The third byte is the control register data.

Upon power up, all programmable registers are set to default values. Figure 2 describes the serial command port timing relationship.

Figure 2. Serial Command Port Timing

I²C Bus Control Register Write Example:



Example

Set channel 1L volume to 30H:

first byte: [CA R/W] = 6AH (Note: Chip address: CA<6:0> = 35H, R/W = 0.)

second byte: register address: A<7:0> = 02H

third byte: data D<7:0> = 30H

SERIAL PORT CONTROL REGISTER ASSIGNMENT

There are 8 registers dedicated to the CE2746 for chip functional programming, The register addresses assignments are

Address (decimal)	Register	Default Value	Register Function
0	CREG0[7:0]	81	Data input format, de-emphasis filter selection
1	CREG1[7:0]	80	Input format and PLL output frequency selection
2	VOLREG0[7:0]	80	Volume control for channel 1, left
3	VOLREG1[7:0]	80	Volume control for channel 1, right
4	VOLREG2[7:0]	80	Volume control for channel 2, left
5	VOLREG3[7:0]	80	Volume control for channel 2, right
6	VOLREG4[7:0]	80	Volume control for channel 3, left
7	VOLREG5[7:0]	80	Volume control for channel 3, right

CONTROL REGISTERS DESCRIPTION
Control Register 0(ADRS=hex00, default=hex81)

ADDR[3:0]	CREG0[7:0]							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Hex 00	LF	I2S	FMT[1:0]		AMUTE	DEEMP	FSMPL[1:0]	
Default Value	1	0	0	0	0	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[LF, I2S] Digital Serial Bus Format Select

00: - Normal or Right Justified Format.

01: - I2S Format.

10: - Left Justified Format. (default)

11: - Not allowed.

FMT[1:0]: - These two bits define the serial audio input resolution

00: - 24-bit resolution. (default)

01: - 20-bit resolution.

10: - 18-bit resolution.

11: - 16-bit resolution.

AMUTE: - Auto-mute detection enable.

0: - Auto-mute enabled. (default)

1: - No auto-mute.

DEEMP: - Enable de-emphasis (active only when FSMPL is 2'b00).

0: - Normal. (default)

1: - enable de-emphasis when FSMPL is 0.

FSMPL: - Sampling rate:

00: - 44.1 K sampling.

01: - 48K sampling. (default)

10: - 96K sampling.

11: - 192K sampling.

Control Register 1 (ADRS=hex01, default=hex80)

ADDR[3:0]	CREG1[7:0]							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Hex 01	AUTODET	FS384	CKDIV4	CKDIV2	spare	MUTE56	MUTE34	MUTE12
Default Value	1	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

AUTODET Automatically detects the serial audio input data sampling rate

0: - do not use auto-detect

1: - automatically detects the serial audio input data sampling rate.

FS384: 384 fs or 256 fs control for the PLL clock output

0: the PLL takes the reference clock and multiplies it by 2 to generate a 512 bit clock

1: the PLL takes the reference clock and multiplies it by 4/3 to generate a 512 bit clock

CKDIV4: Clock divider enable control

0: do not enable input clock divided by 4

1: enable input clock divided by 4

CKDIV2: Clock divider enable control

0: do not enable input clock divided by 2

1: enable input clock divided by 2

MUTE56: Mute control for channels 5 and 6

0: do not mute channels 5 and 6

1: simultaneously mute channels 5 and 6

MUTE34: Mute control for channels 3 and 4

0: do not mute channels 3 and 4

1: simultaneously mute channels 3 and 4

MUTE12: Mute control for channels 1 and 2

0: do not mute channels 1 and 2

1: simultaneously mute channels 1 and 2

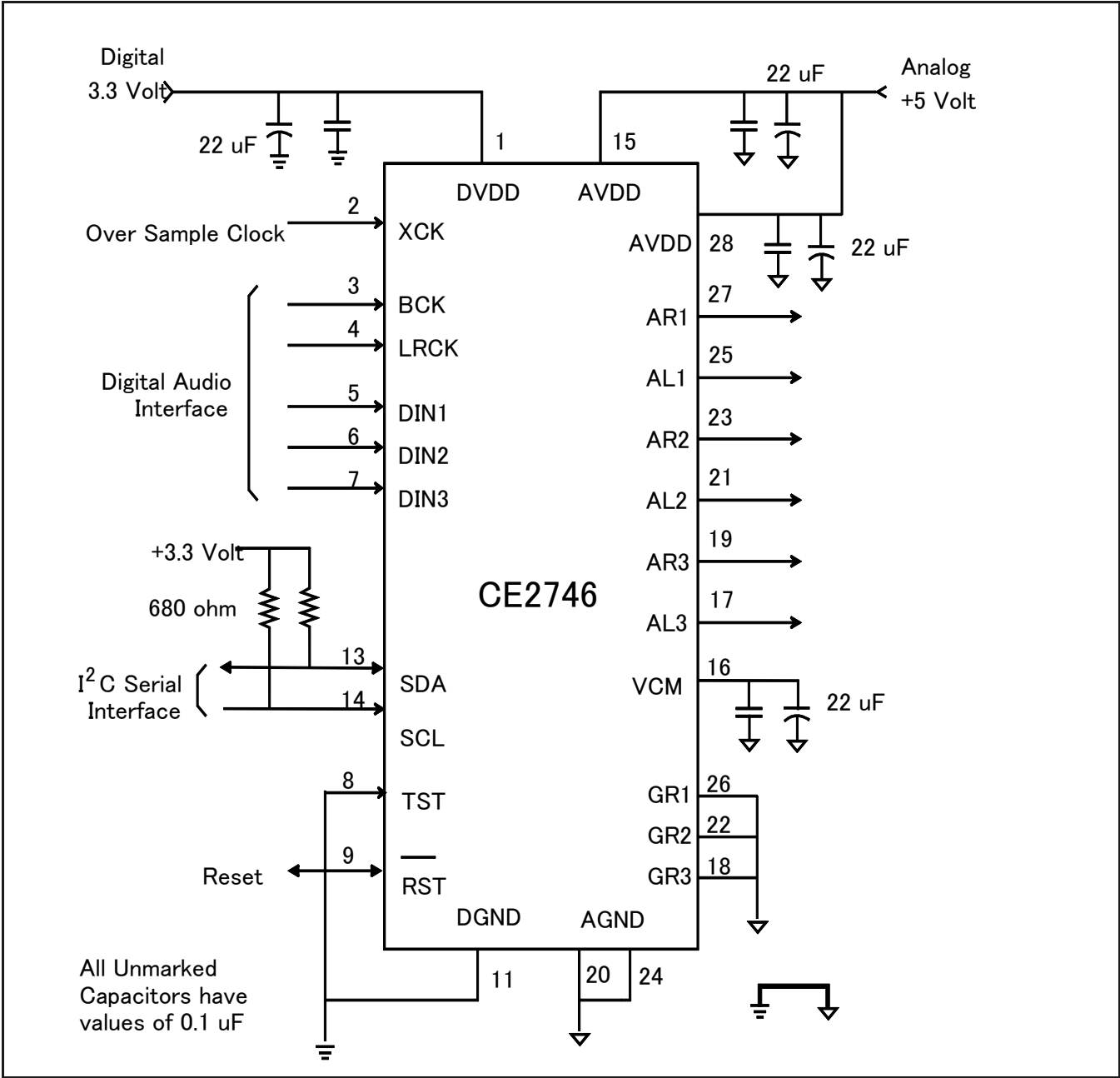
Volume Registers for channel 1 to channel 3, (ADRS=hex02 - hex07, default=hex80)

ADDR[3:0]	Volume Registers							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Hex 02	Channel 1 left volume register, VOLREGL1[7:0]							
Hex 03	Channel 1 right volume register, VOLREGR1[7:0]							
Hex 04	Channel 2 left volume register, VOLREGL2[7:0]							
Hex 05	Channel 2 right volume register, VOLREGR2[7:0]							
Hex 06	Channel 3 left volume register, VOLREGL3[7:0]							
Hex 07	Channel 3 right volume register, VOLREGR3[7:0]							
Default Value	1	0	0	0	0	0	0	0

VOLREG:- Control the volume of the 6 DAC's

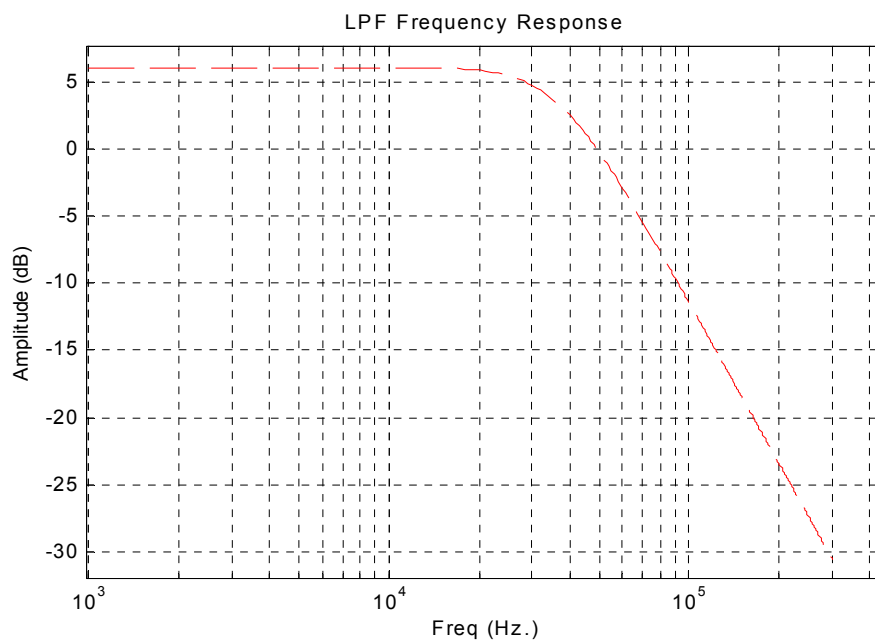
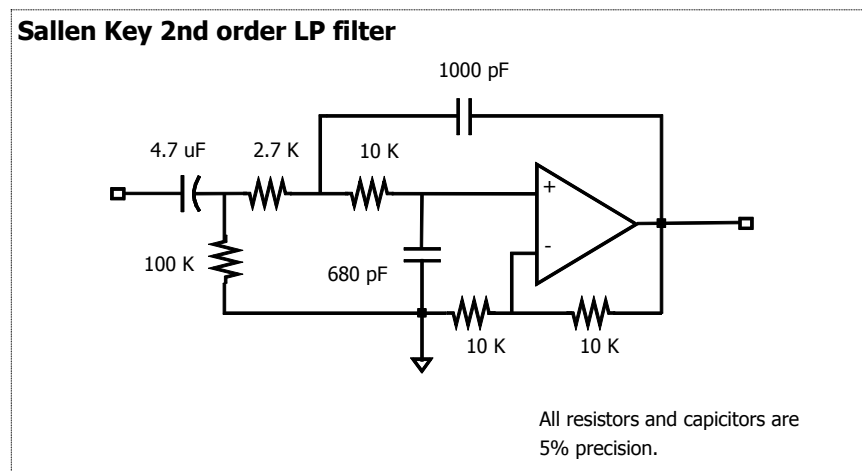
80h- corresponds to 0 dB setting. Value should not be programmed greater than 80h.

APPLICATION CONNECTION EXAMPLE:



SUGGESTED ANALOG RECONSTRUCTION FILTER

A second Sallen Key low pass reconstruction filter is recommended to remove the high frequency sigma delta modulator noise. The filter's component values and characteristic are shown in the following figures.



TIMING DIAGRAM

Figure 3. Audio Serial Interface Timing Requirement

Figure 4. Serial Command Port Write Timing Requirement

ABSOLUTE MAXIMUM RATINGS

Symbol	Characteristics	Min	Max	Units
V _{DD}	Power Supply Voltage (Measured to GND)	-0.5	+7.0	V
V _i	Digital Input Applied Voltage ²	GND-0.5		V
A _i	Digital Input Forced Current ^{3,4}	-100	100	mA
V _o	Digital Output Applied Voltage ²	GND-0.5	V _{DD} +0.5	V
A _o	Digital Output Forced Current ^{3,4}	-100	100	mA
TDsc	Digital Short Circuit Duration (single output high state to Vss)		1	Sec
TA _{SC}	Analog Short Circuit Duration (single output to VSS1)		infinite	Sec
T _a	Ambient Operating Temperature Range	-25	+125	°C
T _j	Junction Temperature (Plastic Package)	-65	+150	°C
Tsol	Lead Soldering Temperature (10 sec., 1/4" from pin)		280	°C
Tvsol	Vapor Phase Soldering (1 minute)		220	°C
Tstor	Storage Temperature	-65	+150	°C

Notes:

1. Absolute maximum ratings are limiting values applied individually, while all other parameters are within specified operating conditions.
2. Applied voltage must be current limited to specified range, and measured with respect to VSS.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current, flowing into the device.

ELECTRICAL CHARACTERISTICS

Parameter	Characteristics	Min	Typ	Max	Units
Power Supply					
AVDD	Analog power supply voltage	4.5	5	5.5	V
DVDD	Digital power supply voltage	3.0	3.3	3.6	V
I _{DA}	Analog Current		60		mA
I _{DD}	Digital Current		20		mA

Audio DAC Characteristics

	Full Scale Output Voltage to a 10K load	.98	1	1.02	V _{rms}
V _{VCM}	Reference voltage		2.25	2.41	V

Digital Characteristics

V _{IH}	Digital Input Voltage, Logic HIGH, TTL Compatible Inputs.	2.0		V _{DD}	V
I _{OZH}	Hi-Z Leakage Current, HIGH, V _{DD} =Max, V _{IN} =3.3 Volt			33	μ A
I _{OZL}	Hi-Z Leakage Current, LOW, V _{DD} =Max, V _{IN} =V _{SS})			-10	μ A
C _I	Digital Input Capacitance (T ^A =25°C, f=1Mhz)			8	pF
C _O	Digital Output Capacitance (T ^A =25°C, f=1Mhz)			10	pF

Audio Serial Interface Timing

tbck	BCK Cycle Time	80			ns
tbck _H	BCK Pulse Width, HIGH	30			ns
tbck _L	BCK Pulse Width, LOW	30			ns
tkd _{su}	Audio Data Setup Time With Respect To Rising Edge of BCK	10			ns
tkd _{hd}	Audio Data Hold Time With Respect to Rising Edge of BCK	15			ns
tkr _{su}	Audio LRCK Setup Time With Respect To Rising Edge of BCK	10			ns

Parameter	Characteristics	Min	Typ	Max	Units
$t_{kr_{hd}}$	Audio LRCK Hold Time With Respect To Rising Edge of BCK	15			ns

Serial Command Port

fSCL	SCL Clock Frequency			100	kHz
$t_{SU,sta}$	Start condition set up time	4.7			us
$t_{HD,sta}$	Start condition hold time	4.0			us
$t_{SU,stp}$	Stop condition set up time	4.0			us
tLOW	SCL Low time	4.7			us
tHIGH	SCL High time	4.0			us
tR	SCL & SDA rise time			1.0	us
tF	SCL & SDA fall time			0.3	us
$t_{SU,DAT}$	Data set-up time	250			ns
$t_{HD,DAT}$	Data hold time	0			ns
tBF	Bus Free time	4.7			us

PACKAGING INFORMATION

Dimensions

	mm.				mm.		
	min	norm	max		min	norm	max
A			2.13	E1	5.0	5.3	5.6
A1	0.05		0.25	E2	7.4	7.8	8.2
b	0.22	0.3	0.38	e		0.65	
C	0.09		0.20	L	0.63	0.9	1.03
D	9.90	10.20	10.50				

28-Pin (SSOP)

