

OMAP5912 Applications Processor

Data Manual



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REVISION HISTORY

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PAGE(S) NO.	ADDITIONS/CHANGES/DELETIONS
132	Updated Table 3–56, L3 OCP Initiator Registers
133	Table 3–57, MPU Interface (MPUI) Registers: <ul style="list-style-type: none"> – updated RESET VALUE column – FFFE:C91C – changed REGISTER NAME and DESCRIPTION – added DSP_MISC_CONFIG (FFFE:C920) – added ENHANCED_CTL (FFFE:C924)
136	Table 3–65, DSP MMU Registers: <ul style="list-style-type: none"> – changed ACCESS WIDTH of all registers from 32 bits to 16 bits
141	Table 3–71, DSP Timer1 Registers: <ul style="list-style-type: none"> – updated DSP WORD ADDRESS column
141	Table 3–72, DSP Timer2 Registers: <ul style="list-style-type: none"> – updated DSP WORD ADDRESS column
142	Table 3–73, DSP Timer3 Registers: <ul style="list-style-type: none"> – updated DSP WORD ADDRESS column
142	Updated Table 3–74, DSP Watchdog Timer Registers
143	Updated Table 3–78, DSP TIPB Bridge Configuration Registers
144	Updated Table 3–81, DSP Clock Mode Registers
145	Updated Table 3–82, DSP TIPB Bus Switch Registers

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1 OMAP5912 Features

- **Low-Power, High-Performance CMOS Technology**
 - 0.13- μm Technology
 - 1.6-V Core Voltage
- **ARM926EJ-S™ (MPU) Core**
 - Support for 32-Bit and 16-Bit (Thumb® Mode) Instruction Sets
 - 16K-Byte Instruction Cache
 - 8K-Byte Data Cache
 - Data and Program Memory Management Unit (MMU)
 - 17-Word Write Buffer
 - Two 64-Entry Translation Look-Aside Buffers (TLBs) for MMUs
- **TMS320C55x™ (C55x™) DSP Core**
 - One/Two Instructions Executed per Cycle
 - Dual Multipliers (Two Multiply-Accumulates per Cycle)
 - Two Arithmetic/Logic Units
 - Five Internal Data/Operand Buses (3 Read Buses and 2 Write Buses)
 - 32K x 16-Bit On-Chip Dual-Access RAM (DARAM) (64K Bytes)
 - 48K x 16-Bit On-Chip Single-Access RAM (SARAM) (96K Bytes)
 - Instruction Cache (24K Bytes)
 - Video Hardware Accelerators for DCT, iDCT, Pixel Interpolation, and Motion Estimation for Video Compression
- **250K Bytes of Shared Internal SRAM**
- **Memory Traffic Controller (TC)**
 - 16-Bit EMIFS to Access up to 256M Bytes of Flash (for Burst, Programmable NOR Flash)
 - 16-Bit EMIFF to Access up to 128M Bytes of SDRAM, Mobile SDRAM, or Mobile DDR
- **DSP Memory Management Unit**
- **Digital Phase-Locked Loop (DPLL) for MPU/DSP/TC Clocking Control**
- **DSP Peripherals**
 - Three 32-Bit Timers and Watchdog Timer
 - Six-Channel DMA Controller
 - Two Multichannel Buffered Serial Ports
 - Two Multichannel Serial Interfaces
- **MPU Peripherals**
 - Three 32-Bit Timers and Watchdog Timer
 - USB 1.1 Host and Client Controllers
 - USB On-the-Go (OTG) Controller
 - 3 USB Ports, One With an Integrated Transceiver
 - Specially Optimized Screen Interface (SoSSI)
 - Compact Camera Port Interface For Parallel CMOS Sensors
 - Real-Time Clock (RTC)
 - Pulse-Width Tone (PWT) Interface
 - Pulse-Width Light (PWL) Interface
 - Keyboard Matrix Interface (6 x 5 or 8 x 8)
 - HDQ/1-Wire® Interface
 - Multimedia Card (MMC) and Secure Digital (SD) Interface
 - CompactFlash™ Controller
 - Up to 16 MPU General-Purpose I/Os
 - Two LED Pulse Generators (LPGs)
 - ETM9™ Trace Module for ARM926EJ-S Debug
 - 16-/18-Bit LCD Controller With Dedicated System DMA Channel
 - 32-kHz Operating System (OS) Timer
- **Shared Peripherals**
 - 8 General-Purpose Timers
 - Serial Port Interface (SPI)
 - VLYNQ™ Interface (WLAN 802.11x)
 - Three Universal Asynchronous Receiver/Transmitters (UARTs) (Two Supporting SIR mode for IrDA)
 - Inter-Integrated Circuit (I²C) Master and Slave Interface
 - Multimedia Card (MMC) and Secure Digital (SD) Interface
 - Multichannel Buffered Serial Port (McBSP)
 - Up to 64 Shared General-Purpose I/Os
 - 32-kHz Synchro Counter
- **Hardware Accelerators for Cryptographic Functions**
 - Random Number Generation
 - DES and 3DES
 - SHA-1 and MD5
- **Individual Power-Saving Modes for MPU/DSP/TC**
- **On-Chip Scan-Based Emulation Logic**
- **IEEE Std 1149.1† (JTAG) Boundary Scan Logic**
- **Two 289-Ball Lead-Free BGA (Ball Grid Array) Packages (ZDY and ZZG)**

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† IEEE Standard 1149.1-1990 Standard Test-Access Port and Boundary Scan Architecture.

2 Introduction

This section describes the main features of the OMAP5912 device, lists the terminal assignments, and describes the function of each terminal. This data manual also provides a detailed description section, electrical specifications, parameter measurement information, and mechanical data about the available packaging.

2.1 Description

OMAP5912 is a highly integrated hardware and software platform, designed to meet the application processing needs of next-generation embedded devices.

The OMAP™ platform enables OEMs and ODMs to quickly bring to market devices featuring rich user interfaces, high processing performance, and long battery life through the maximum flexibility of a fully integrated mixed processor solution.

The dual-core architecture provides benefits of both DSP and reduced instruction set computer (RISC) technologies, incorporating a TMS320C55x DSP core and a high-performance ARM926EJ-S ARM® core.

The OMAP5912 device is designed to run leading open and embedded RISC-based operating systems, as well as the Texas Instruments (TI) DSP/BIOS™ software kernel foundation, and is available in two 289-ball lead-free ball grid array (BGA) packages (ZDY and ZZG).

The OMAP5912 device is targeted at the following applications:

- Applications Processing Devices
- Mobile Communications
 - WAN 802.11X
 - Bluetooth™
 - GSM, GPRS, EDGE
 - CDMA
- Video and Image Processing (MPEG4, JPEG, Windows® Media Video, etc.)
- Advanced Speech Applications (text-to-speech, speech recognition)
- Audio Processing (MPEG-1 Audio Layer3 [MP3], AMR, WMA, AAC, and Other GSM Speech Codecs)
- Graphics and Video Acceleration
- Generalized Web Access
- Data Processing

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ARM926EJ-S and ETM9 are trademarks of ARM Limited in the EU and other countries.

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CompactFlash is a trademark of CompactFlash Association.

Bluetooth is a trademark owned by Bluetooth SIG, Inc.

Windows is a registered trademark of Microsoft Corporation in the United States and/or other countries.

2.1.1 TMS320C55x DSP Core

The DSP core of the OMAP5912 device is based on the TMS320C55x DSP generation CPU processor core. The C55x DSP architecture achieves high performance and low power through increased parallelism and total focus on reduction in power dissipation. The CPU supports an internal bus structure composed of one program bus, three data read buses, two data write buses, and additional buses dedicated to peripheral and DMA activity. These buses provide the ability to perform up to three data reads and two data writes in a single cycle. In parallel, the DMA controller can perform up to two data transfers per cycle independent of the CPU activity. The C55x CPU provides two multiply-accumulate (MAC) units, each capable of 17-bit x 17-bit multiplication in a single cycle. A central 40-bit arithmetic/logic unit (ALU) is supported by an additional 16-bit ALU. Use of the ALUs is under instruction set control, providing the ability to optimize parallel activity and power consumption. These resources are managed in the address unit (AU) and data unit (DU) of the C55x CPU.

The C55x DSPs support a variable byte width instruction set for improved code density. The instruction unit (IU) performs 32-bit program fetches from internal or external memory and queues instructions for the program unit (PU). The program unit decodes the instructions, directs tasks to AU and DU resources, and manages the fully protected pipeline. Predictive branching capability avoids pipeline flushes on execution of conditional instructions. The OMAP5912 DSP core also includes a 24K-byte instruction cache to minimize external memory accesses, improving data throughput and conserving system power.

2.1.1.1 DSP Tools Support

The 55x DSP core is supported by the industry's leading eXpressDSP™ software environment including the Code Composer Studio™ Integrated Development Environment (IDE), DSP/BIOS software kernel foundation, the TMS320™ DSP Algorithm Standard, and the industry's largest third-party network. Code Composer Studio features code generation tools including a C-Compiler, Visual Linker, simulator, Real-Time Data Exchange (RTDX™), XDS510™ emulation device drivers, and Chip Support Libraries (CSL). DSP/BIOS is a scalable real-time software foundation available for no cost to users of Texas Instruments' DSP products, providing a preemptive task scheduler and real-time analysis capabilities with very low memory and megahertz overhead. The TMS320 DSP Algorithm Standard is a specification of coding conventions allowing fast integration of algorithms from different teams, sites, or third parties into the application framework. Texas Instruments' extensive DSP third-party network of over 400 providers brings focused competencies and complete solutions to customers.

2.1.1.2 DSP Software Support

Texas Instruments has also developed foundation software available for the 55x DSP core. The C55x DSP Library (DSPLIB) features over 50 C-callable software routines (FIR/IIR filters, Fast Fourier Transforms (FFTs), and various computational functions). The DSP Image/Video Processing Library (IMGLIB) contains over 20 software routines highly optimized for C55x DSPs and is compiled with the latest revision of the C55x DSP code generation tools. These imaging functions support a wide range of applications that include compression, video processing, machine vision, and medical imaging.

2.1.2 ARM926EJ-S RISC Processor

The MPU core is a ARM926EJ-S reduced instruction set computer (RISC) processor. The ARM926EJ-S is a 32-bit processor core that performs 32-bit or 16-bit instructions and processes 32-bit, 16-bit, or 8-bit data. The core uses pipelining so that all parts of the processor and memory system can operate continuously.

The MPU core incorporates:

- A coprocessor 15 (CP15) and protection module
- Data and program Memory Management Units (MMUs) with table look-aside buffers.
- Separate 16K-byte instruction and 8K-byte data caches. Both are four-way associative with virtual index virtual tag (VIVT).

The OMAP5912 device uses the ARM926EJ-S core in little-endian mode only. To minimize external memory access time, the ARM926EJ-S includes an instruction cache, data cache, and a write buffer. In general, these are transparent to program execution.

2.2 Terminal Assignments

Figure 2-1 illustrates the ball locations for the 289-ball ZDY package and Figure 2-2 illustrates the ball locations for the 289-ball ZZG package. Figure 2-1 and Figure 2-2 are used in conjunction with Table 2-1 and Table 2-2, respectively, to locate signal names and ball grid numbers. BGA ball numbers in Table 2-1 and Table 2-2 are read from left-to-right, top-to-bottom.

PRODUCT PREVIEW

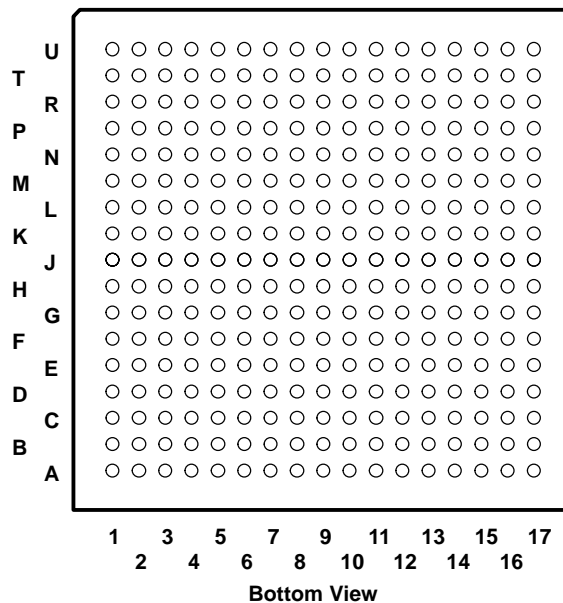


Figure 2-1. OMAP5912 289-Ball ZDY Plastic Ball Grid Array (Bottom View)

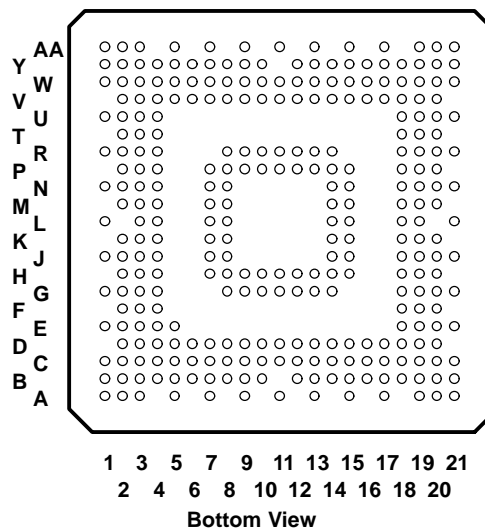


Figure 2–2. OMAP5912 289-Ball ZSG Plastic Ball Grid Array (Bottom View)

In Table 2–1 and Table 2–2, signals with multiplexed functions are highlighted in gray. Signals within a multiplexed pin name are separated with forward slashes as follows:

- **signal1/signal2/signal3** (e.g., MPUIO1/RTCK/SPIF.SCK)

Signals which are associated with specific peripherals are denoted by using the peripheral name, followed by a period, and then the signal name; as follows:

- **peripheral1.signal1** (i.e., MCS11.DOUT)

Table 2–1. ZDY Package Terminal Assignments

ZDY BALL NO.	SIGNAL	ZDY BALL NO.	SIGNAL	ZDY BALL NO.	SIGNAL	ZDY BALL NO.	SIGNAL
A1	SDRAM.A[1]	A2	SDRAM.DQSL	A3	SDRAM.D[6]	A4	SDRAM.D[2]
A5	SDRAM.D[3]	A6	SDRAM.CLKX	A7	SDRAM.CLK	A8	SDRAM.DQMU
A9	CV _{DDLL}	A10	SDRAM.A[7]	A11	SDRAM.D[11]	A12	SDRAM.DQSH
A13	LCD.P[12](0)/ Z_STATE [†] (1)/ SOSSI.D[12](6)/ GPIO33(7)	A14	LCD.PCLK(0)/ Z_STATE [†] (1)/ SOSSI.WR(6)	A15	LCD.P[10](0)/ Z_STATE [†] (1)/ SOSSI.D[10](6)/ GPIO31(7)	A16	LCD.P[6](0)/ Z_STATE [†] (1)/ SOSSI.D6
A17	LCD.P0/ Z_STATE [†] (1)/ SOSSI.D[0](6)	B1	DV _{DD5}	B2	SDRAM.A[0]	B3	SDRAM.D[4]
B4	SDRAM.D[0]	B5	SDRAM.D[1]	B6	SDRAM.D[5]	B7	SDRAM.D[7]
B8	SDRAM.D[10]	B9	SDRAM.D[12]	B10	SDRAM.D[15]	B11	SDRAM.D[13]
B12	SDRAM.D[9]	B13	SDRAM.CKE	B14	LCD.P[11](0)/ Z_STATE [†] (1)/ SOSSI.D[11](6)/ GPIO32(7)	B15	LCD.VS(0)/ Z_STATE [†] (1)/ SOSSI.RD(6)
B16	LCD.P[1](0)/ Z_STATE [†] (1)/ SOSSI.D[1](6)	B17	KB.C[2](0)/ GPIO61(7)	C1	FLASH.A[6](0)	C2	FLASH.A[2](0)
C3	SDRAM.A[3]	C4	SDRAM.BA[1]	C5	SDRAM.BA[0]	C6	SDRAM.A[8]
C7	SDRAM.DQML	C8	SDRAM.A[5]	C9	SDRAM.D[8]	C10	SDRAM.D[14]
C11	CV _{DD}	C12	LCD.P[15](0)/ Z_STATE [†] (1)/ SOSSI.D[15](6)/ GPIO2(7)	C13	LCD.P[8](0)/ Z_STATE [†] (1)/ SOSSI.D[8](6)/ GPIO29(7)	C14	DV _{DD1}
C15	LCD.P[5](0)/ Z_STATE [†] (1)/ SOSSI.D[5](6)	C16	LCD.P[2](0)/ Z_STATE [†] (1)/ SOSSI.D[2](6)	C17	KB.C[1](0)/ MPUIO6(1)	D1	FLASH.A[8](0)
D2	FLASH.A[5](0)	D3	FLASH.A[1](0)	D4	SDRAM.RAS	D5	SDRAM.CAS
D6	DV _{DD4}	D7	DV _{DD4}	D8	DV _{DD4}	D9	SDRAM.A[4]
D10	SDRAM.A[13]	D11	DV _{DD4}	D12	LCD.P[14](0)/ Z_STATE [†] (1)/ SOSSI.D[14](6)/ GPIO35(7)	D13	LCD.P[7](0)/ Z_STATE [†] (1)/ SOSSI.D[7](6)
D14	LCD.P[3](0)/ Z_STATE [†] (1)/ SOSSI.D[3](6)	D15	LCD.HS(0)/ Z_STATE [†] (1)/ SOSSI.CS(6)	D16	KB.C[4](0)/ GPIO27(7)	D17	KB.R[3](0)/ MPUIO13(1)/ VLYNQ.TX0(2)
E1	FLASH.A[9](0)	E2	FLASH.A[7](0)	E3	FLASH.A[4](0)	E4	FLASH.A[3](0)
E5	V _{SS}	E6	SDRAM.WE	E7	SDRAM.CS	E8	SDRAM.A[12]

[†] Z_STATE = high-impedance

[‡] "NC" denotes "No Connect".

[§] LOW_STATE = 0

NOTES: 1. Shading denotes signals with multiplexed functions.

2. The number within parenthesis at the end of a signal name denotes the Pin Mux setting (see the MUX CTRL SETTING column in Table 2–3 and Table 2–4).

Table 2–1. ZDY Package Terminal Assignments (Continued)

ZDY BALL NO.	SIGNAL	ZDY BALL NO.	SIGNAL	ZDY BALL NO.	SIGNAL	ZDY BALL NO.	SIGNAL
E9	SDRAM.A[11]	E10	SDRAM.A[6]	E11	LCD.P[13](0)/ Z_STATE [†] (1)/ SOSSI.D[13](6)/ GPIO34(7)	E12	LCD.P[4](0)/ Z_STATE [†] (1)/ SOSSI.D[4](6)
E13	V _{SS}	E14	NC [‡]	E15	KB.C[3](0)/ GPIO63(6)	E16	KB.R[2](0)/ MPUIO10(1)/ VLYNQ.CLK(2)
E17	KB.R[1](0)/ MPUIO9(1)/ VLYNQ.RX0(2)	F1	FLASH.A[11](0)	F2	FLASH.A[10](0)	F3	FLASH.A[25]
F4	FLASH.A[20]	F5	FLASH.A[12](0)	F6	V _{SS}	F7	SDRAM.A[2]
F8	SDRAM.A[10]	F9	SDRAM.A[9]	F10	LCD.AC(0)/ SYS_CLK_OUT(1)/ Z_STATE [†] (2)/ SOSSI.CMD(6)	F11	LCD.P[9](0)/ Z_STATE [†] (1)/ SOSSI.D[9](6)/ GPIO30(7)
F12	V _{SS}	F13	KB.R[4](0)/ MPUIO15(1)/ VLYNQ.TX1(2)	F14	KB.C0/ MPUIO0(1)	F15	KB.R0/ MPUIO8(1)/ VLYNQ.RX1(2)
F16	MCBSP1.CLKX(0)/ GPIO54(7)	F17	KB.C[5](0)/ GPIO28(7)	G1	DV _{DD5}	G2	FLASH.A[15](0)
G3	FLASH.A[13](0)	G4	FLASH.A[14](0)	G5	FLASH.A[16](0)	G6	FLASH.A[17]
G7	V _{SS}	G8	CV _{DD2}	G9	CV _{DD2}	G10	CV _{DD3}
G11	V _{SS}	G12	DV _{DD1}	G13	MCBSP1.CLKS(0)/ SOSSI.TE(6)/ GPIO62(7)	G14	MCBSP1.DX(0)/ MCBSP1.FSX(1)/ MCBSP1.DXZ(2)/ GPIO52(7)
G15	MCBSP1.FSX(0)/ MCBSP1.DX(1)/ MCBSP1.DXZ(2)/ GPIO53(7)	G16	CAM.LCLK(0)/ ETM.CLK(1)/ UWIRE.SCLK(2)/ GPIO39(7)	G17	MCBSP1.DR(0)/ GPIO51(7)	H1	LDO.FILTER
H2	FLASH.A[22]	H3	FLASH.A[18]	H4	FLASH.A[19]	H5	FLASH.A[21]
H6	FLASH.ADV	H7	CV _{DD2}	H8	V _{SS}	H9	V _{SS}
H10	V _{SS}	H11	CV _{DD3}	H12	CAM.EXCLK(0)/ ETM.SYNC[0](1)/ UWIRE.SDO(2)/ LOW_STATE [§] (6)/ GPIO57(7)	H13	CAM.D[3](0)/ ETM.D[3](1)/ UART3.RX(2)/ GPIO31(7)

[†] Z_STATE = high-impedance

[‡] "NC" denotes "No Connect".

[§] LOW_STATE = 0

NOTES: 1. Shading denotes signals with multiplexed functions.

2. The number within parenthesis at the end of a signal name denotes the Pin Mux setting (see the MUX CTRL SETTING column in Table 2–3 and Table 2–4).

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Table 2–1. ZDY Package Terminal Assignments (Continued)

ZDY BALL NO.	SIGNAL	ZDY BALL NO.	SIGNAL	ZDY BALL NO.	SIGNAL	ZDY BALL NO.	SIGNAL
H14	MPU_BOOT(0)/ USB1.SUSP(2)	H15	CAM.D[6](0)/ ETM.D[6](1)/ UWIRE_CS3(2)/ MMC2.CMD/ SPI.DO(3)/ GPIO34(7)	H16	CAM.D[7](0)/ ETM.D[7](1)/ UWIRE_CS0(2)/ MMC2.DAT2(3)/ GPIO35(7)	H17	CAM.D[5](0)/ ETM.D[5](1)/ UWIRE.SDI(2)/ GPIO33(7)
J1	FLASH_BE0/ FLASH_CS2UOE(1)/ GPIO59(7)	J2	FLASH.A[23]	J3	FLASH_CS1(0)/ FLASH_CS1L(1)	J4	FLASH.A[24]
J5	GPIO62(0)/ FLASH_CS0(1)	J6	FLASH_CS3(0)/ GPIO3(7)	J7	FLASH.D[3]	J8	FLASH_CS2(0)/ FLASH.BAA(1)/ FLASH_CS2L(2)
J9	V _{SS}	J10	CV _{DD3}	J11	CAM.D[4](0)/ ETM.D[4](1)/ UART3.TX(2)/ GPIO32(7)	J12	CAM.HS(0)/ ETM.PSTAT1/ UART2.CTS(2)/ MMC2.DAT0/ SPI.DI(3)/ GPIO38(7)
J13	CAM.VS(0)/ ETM.PSTAT[2](1)/ MPUIO14(2)/ MMC2.DAT1(3)	J14	CAM.D[2](0)/ ETM.D[2](1)/ UART3.CTS(2)/ GPIO30(7)	J15	DV _{DD8}	J16	CAM.D[1](0)/ ETM.D1/ UART3.RTS(2)/ GPIO29(7)
J17	CAM.D0/ ETM.D[0](1)/ MPUIO12(2)/ MMC2.DAT3(3)	K1	FLASH.CLK(0)/ FLASH_CS2UOE(1)	K2	FLASH_BE[1](0)/ FLASH_CS2UWE(1)/ GPIO60(7)	K3	FLASH_CS2U(0)/ GPIO5(1)
K4	NC [‡]	K5	CV _{DD}	K6	FLASH.D[6]	K7	FLASH.D[12]
K8	V _{SS}	K9	V _{SS}	K10	V _{SS}	K11	CV _{DD3}
K12	CAM.RSTZ(0)/ ETM.PSTAT[0](1)/ UART2.RTS(2)/ MMC2.CLK(3)/ LOW_STATE [§] (6)/ GPIO37(7)	K13	GPIO11(0)/ HDQ(1)/ VLYNQ_RX1(4)/ ETM.PSTAT5/ RTDX.D[3](7)	K14	GPIO14(0)/ KB.R[6](1)/ LCD.RED0(2)/ Z_STATE [†] (3)/ VLYNQ_TX0(4)	K15	UART3.RX(0)/ PWL(1)/ UART2.RX(3)/ TIMER.PWM1(4)/ GPIO49(7)
K16	GPIO15(0)/ KB.R[7](1)/ TIMER.PWM2(2)/ VLYNQ_TX1(4)	K17	LOW_STATE [§] (0)/ UART3.TX(1)/ PWT(2)/ UART2.TX(4)/ TIMER.PWM0(5)/ GPIO50(7)	L1	FLASH.D[0]	L2	FLASH.D[2]
L3	DV _{DD5}	L4	FLASH.D[5]	L5	FLASH.D[8]	L6	FLASH.RDY(0)/ GPIO10(1)

[†] Z_STATE = high-impedance

[‡] "NC" denotes "No Connect".

[§] LOW_STATE = 0

NOTES: 1. Shading denotes signals with multiplexed functions.

2. The number within parenthesis at the end of a signal name denotes the Pin Mux setting (see the MUX CTRL SETTING column in Table 2–3 and Table 2–4).

Table 2–1. ZDY Package Terminal Assignments (Continued)

ZDY BALL NO.	SIGNAL	ZDY BALL NO.	SIGNAL	ZDY BALL NO.	SIGNAL	ZDY BALL NO.	SIGNAL
L7	V _{SS}	L8	MCBSP2.DR(0)/ MCBSP2.DX(1)/ MCBSP2.DXZ(2)/ GPIO22(7)	L9	CV _{DDRTC}	L10	BCLK(0)/ UART3.RTS(1)/ CAM.OUTCLK(6)/ GPIO17(7)
L11	V _{SS}	L12	MPUIO2(0)/ EXT_DMA_REQ0(1)/ UWIRE.CS1(2)/ SPIF.CS1(6)	L13	GPIO3(0)/ SPI.CS3(1)/ MCBSP3.FSX(2)/ LED1(3)/ ETM.PSTAT[3](5)/ RTDX.D[1](7)	L14	GPIO6(0)/ SPI.CS1(1)/ MCBSP3.FSX(2)/ TIMER.EVENT3(3)/ MCSI1.DIN(4)/ TMS(5)
L15	GPIO7(0)/ MMC.DAT2(1)/ TCK(3)/ MCSI1.CLK(4)/ ETM.SYNC[1](5)/ RTDX.D[2](7)	L16	GPIO12(0)/ MCBSP3.FSX(1)/ TIMER.EXTCLK(3)/ VLYNQ.RX0[4]	L17	GPIO13(0)/ KB.R[5](1)/ LCD.BLUE0(2)/ Z_STATE†(3)/ VLYNQ.CLK(4)	M1	FLASH.D[1]
M2	FLASH.D[4]	M3	FLASH.D[11]	M4	FLASH.D[10]	M5	FLASH.OE
M6	V _{SS}	M7	CV _{DD}	M8	MMC.CLK(0)/ SSI.CARDY(6)/ GPIO57(7)	M9	UART1.CTS(0)/ UART1.IRSEL(2)/ GPIO38(7)
M10	TMS	M11	I2C.SDA(0)/ GPIO48(7)	M12	V _{SS}	M13	DV _{DD9}
M14	MPUIO4(0)/ EXT_DMA_REQ1(1)/ LED2(2)/ UWIRE.CS2(3)/ SPIF.CS2(4)/ MCBSP3.DR(6)	M15	GPIO1(0)/ UART3.RTS(1)	M16	GPIO2(0)/ SPI.CLK(1)/ ETM.PSTAT[4](5)/ RTDX.D[0](7)	M17	GPIO4(0)/ SPI.CS2(1)/ MCBSP3.FSX(2)/ TIMER.EVENT4(3)/ SPIF.DIN(4)
N1	FLASH.D[7]	N2	FLASH.D[9]	N3	FLASH.RP(0)/ FLASH.CS2UWE(1)	N4	FLASH.D[15]
N5	V _{SS}	N6	MCBSP2.FSX(0)/ VLYNQ.RX1(3)/ GPIO21(7)	N7	MMC.CMD/SPI.DO(0)/ CFLASH.CD2(3)/ SSI.CADATA(6)/ GPIO55(7)	N8	PWRON_RESET
N9	RTC_WAKE_INT(0)/ USB1.SE0(4)/ RST_HOST_OUT(5)/ CCP.CLKM(6)/ GPIO55(7)	N10	MCSI1.SYNC(0)/ MCBSP3.DR(1)/ USB1.VP(2)/ MCBSP3.FSX(4)	N11	EMU1	N12	RST_OUT(0)/ GPIO41(7)
N13	V _{SS}	N14	MPU_RST(0)/ MPUIO14(6)	N15	MPUIO1(0)/ RTCK(1)/ SPIF.SCK(6)	N16	MPUIO5(0)/ LOW_PWR(1)/ UART3.RTS(3)/ UART1.DTR(4)

† Z_STATE = high-impedance

‡ "NC" denotes "No Connect".

§ LOW_STATE = 0

NOTES: 1. Shading denotes signals with multiplexed functions.

2. The number within parenthesis at the end of a signal name denotes the Pin Mux setting (see the MUX CTRL SETTING column in Table 2–3 and Table 2–4).

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Table 2–1. ZDY Package Terminal Assignments (Continued)

ZDY BALL NO.	SIGNAL	ZDY BALL NO.	SIGNAL	ZDY BALL NO.	SIGNAL	ZDY BALL NO.	SIGNAL
N17	GPIO0(0)/ SPI.RDY(1)/ USB.VBUS(2)/ SPIF.DOUT(3)/ MMC2.CLKIN(6)	P1	FLASH.D[13]	P2	OSC1_OUT	P3	FLASH.WE
P4	USB.PUEN(0)/ USB.CLKO(1)/ USB.PUDIS(3)/ Z_STATE†(4)/ LOW_POWER(6)/ GPIO58(7)	P5	UART2.BCLK(0)/ SYS_CLK_IN(6)	P6	UART2.CTS(0)/ USB2.RCV(1)/ GPIO7(2)/ USB0.RCV(5)	P7	GPIO8(0)/ TRST(3)/ MCS1.DOUT(4)/ MMC2.CMD/SPI.DO(6)
P8	MCS12.CLK(0)/ USB2.SUSP(1)/ USB0.SUSP(5)/ MMC2.CLK(6)/ GPIO27(7)	P9	MMC.DAT3(0)/ MPUIO9(1)/ MPUIO6(2)/ CFLASH.CD1(3)/ SSI.ACFLAG(6)	P10	RTC_ON_NOFF(0)/ CCP.CLKP(6)	P11	MCS1.DOUT(0)/ USB1.TXD(1)/ TDO(3)/ MCBSP3.DX(4)/ CCP.DATAP(6)/ GPIO18(7)/ MCBSP3.DOUT_HIZ
P12	MCS11.DIN(0)/ USB1.RCV(1)/ EMU1(3)/ MCBSP3.DR(4)/ SSI.ACWAKE(6)/ GPIO56(7)	P13	TCK	P14	UWIRE.SDI(0)/ UART3.DSR(1)/ UART1.DSR(2)/ MCBSP3.DR(3)/ SPIF.DIN(6)/ GPIO47(7)	P15	UWIRE.SCLK(0)/ KB.C[7](1)/ MPUIO1(2)/ UART3.CTS(4)
P16	I2C.SCL	P17	CVDDA	R1	FLASH.D[14]	R2	OSC1_IN
R3	FLASH.WP	R4	LOW_STATE§(0)/ UART2.TX(1)/ USB2.TXD(2)/ USB0.TXD(5)/ Z_STATE†(6)/ GPIO17(7)	R5	MCBSP2.FSR(0)/ GPIO12(1)/ VLYNQ.RX0(3)	R6	MPUIO3(0)/ MMC2.DAT1(6)
R7	MCS12.DIN(0)/ USB2.VP(1)/ USB0.VP(5)/ GPIO26(7)	R8	MMC.DAT0/SPI.DI(0)/ Z_STATE†(1)/ CFLASH.IOIS16(3)/ SSI.ACRDY(6)/ GPIO58(7)	R9	VSS	R10	DVDDRTC
R11	LOW_STATE§(0)/ UART1.RTS(1)/ UART1.IRSHDN(2)/ VLYNQ.TX0(3)/ Z_STATE†(6)/ GPIO39(7)	R12	BCLKREQ(0)/ UART3.CTS(1)/ MMC2.DAT2(6)/ GPIO40(7)	R13	TRST	R14	CONF

† Z_STATE = high-impedance

‡ "NC" denotes "No Connect".

§ LOW_STATE = 0

NOTES: 1. Shading denotes signals with multiplexed functions.

2. The number within parenthesis at the end of a signal name denotes the Pin Mux setting (see the MUX CTRL SETTING column in Table 2–3 and Table 2–4).

Table 2–1. ZDY Package Terminal Assignments (Continued)

ZDY BALL NO.	SIGNAL	ZDY BALL NO.	SIGNAL	ZDY BALL NO.	SIGNAL	ZDY BALL NO.	SIGNAL
R15	UWIRE.SDO(0)/ UART3.DTR(1)/ UART1.DTR(2)/ MCBSP3.DX(3)/ UART3.RTS(4)/ MCBSP3.DXZ(5)/ SPIF.DOUT(6)/ GPIO46(7)	R16	Z_STATE [†] (0)/ UWIRE.CS3(1)/ KB.C[6](2)/ SPIF.CS3(3)/ UART3.RX(4)/ Z_STATE [†] (6)/ GPIO44(7)	R17	Z_STATE [†] (0)/ UWIRE.CS0(1)/ MCBSP3.CLKX(2)/ UART3.TX(4)/ SPIF.CS0(6)/ GPIO45(7)	T1	FLASH.CS1U(0)/ GPIO16(7)
T2	USB.DP(0)/ I2C.SDA(4) UART1.RX(5)/ USB.PUEN(7)	T3	CV _{DD1}	T4	LOW_STATE [§] (0)/ UART2.RTS(1)/ USB2.SE0(2)/ MPUIO5(3)/ MPUIO12(4)/ USB0.SE0(5)/ LOW_STATE [§] (6)	T5	MCBSP2.DX(0)/ MCBSP2.DR(1)/ MCBSP2.DXZ(2)/ GPIO19(7)
T6	DV _{DD3}	T7	MCLKREQ(0)/ EXT_MASTER_REQ(1)/ UART2.RX(2)/ MMC2.DAT3(6)/ GPIO23(7)	T8	MCSI2.DOUT(0)/ USB2.TXEN(1)/ USB0.TXEN(5)/ Z_STATE [†] (6)/ GPIO25(7)	T9	MMC.DAT2(0)/ Z_STATE [†] (1)/ MPUIO11(2)/ CFLASH.RESET(3)/ SSI.CAFLAG(6)
T10	DV _{DD6}	T11	CLK32K_IN	T12	LOW_STATE [§] (0)/ UART1.TX(1)/ UART1.IRTX(2)/ CCP.DATAM (6)	T13	DV _{DD7}
T14	RTCK	T15	TDO/ VLYNQ.TX0	T16	CV _{DD}	T17	BFAIL/EXT_FIQ(0)/ UART3.CTS(1)/ UART1.DSR(2)/ MMC.DATDIR1(6)
U1	USB.DM(0)/ I2C.SCL(4)/ UART1.TX(5)/ Z_STATE [†] (7)	U2	DV _{DD2}	U3	MCLK(0)/ MMC2.DATDIR0(6)/ GPIO24(7)	U4	UART2.RX(0)/ USB2.VM(1)/ USB0.VM(5)/ GPIO18(7)
U5	MCBSP2.CLKX(0)/ VLYNQ.TX1(3)/ GPIO20(7)	U6	MCBSP2.CLKR(0)/ GPIO11(1)/ VLYNQ.CLK(3)	U7	GPIO9(0)/ EMU0(3)/ MCSI1.SYNC(4)/ MMC2.DAT0/SPI.DI(6)	U8	MCSI2.SYNC(0)/ GIOP7(1)/ USB2.SPEED(2)/ USB0.SPEED(5)/ MMC2.CMDDIR(6)
U9	MMC.DAT1(0)/ MPUIO10(1)/ MPUIO7(2)/ CFLASH.IREQ(3)/ SSI.ACDATA(6)	U10	OSC32K_OUT	U11	OSC32K_IN	U12	CLK32K_OUT(0)/ MPUIO0(4)/ USB1.SPEED(5)/ UART1.TX(6)/ GPIO36(7)

[†] Z_STATE = high-impedance

[‡] "NC" denotes "No Connect".

[§] LOW_STATE = 0

NOTES: 1. Shading denotes signals with multiplexed functions.

2. The number within parenthesis at the end of a signal name denotes the Pin Mux setting (see the MUX CTRL SETTING column in Table 2–3 and Table 2–4).

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Table 2–1. ZDY Package Terminal Assignments (Continued)

ZDY BALL NO.	SIGNAL	ZDY BALL NO.	SIGNAL	ZDY BALL NO.	SIGNAL	ZDY BALL NO.	SIGNAL
U13	UART1.RX(0)/ UART1.IRRX(2)/ GPIO37(7)	U14	Z_STATE [†] (0)/ MCBSP3.CLKX(1)/ USB1.TXEN(2)/ MCSI1.DIN(4)/ Z_STATE [†] (6)/ GPIO42(7)	U15	MCSI1.CLK(0)/ MCBSP3.DX(1)/ USB1.VM(2)/ TDI(3)/ MCBSP3.CLKX(4)/ GPIO43(7)	U16	EMU0
U17	TDI						

[†] Z_STATE = high-impedance

[‡] "NC" denotes "No Connect".

[§] LOW_STATE = 0

NOTES: 1. Shading denotes signals with multiplexed functions.

2. The number within parenthesis at the end of a signal name denotes the Pin Mux setting (see the MUX CTRL SETTING column in Table 2–3 and Table 2–4).

Table 2–2. ZZG Package Terminal Assignments

ZZG BALL NO.	SIGNAL	ZZG BALL NO.	SIGNAL	ZZG BALL NO.	SIGNAL	ZZG BALL NO.	SIGNAL
A1	SDRAM.A[3]	A2	SDRAM.A[0]	A3	CV _{DD2}	A5	DV _{DD4}
A7	DV _{DD4}	A9	CV _{DD2}	A11	CV _{DDLL}	A13	V _{SS}
A15	CV _{DD}	A17	LCD.P[13](0)/ Z_STATE [†] (1)/ SOSSI.D[13](6)/ GPIO34(7)	A19	DV _{DD1}	A20	LCD.P[5](0)/ Z_STATE [†] (1)/ SOSSI.D[5](6)
A21	V _{SS}	B1	V _{SS}	B2	SDRAM.A[1]	B3	SDRAM.BA[0]
B4	SDRAM.CAS	B5	V _{SS}	B6	SDRAM.A[2]	B7	V _{SS}
B8	SDRAM.A[10]	B9	SDRAM.A[5]	B10	DV _{DD4}	B12	SDRAM.A[9]
B13	CV _{DD3}	B14	DV _{DD4}	B15	LCD.AC(0)/ SYS_CLK_OUT(1)/ Z_STATE [†] (2)/ SOSSI.CMD(6)	B16	V _{SS}
B17	LCD.P[11](0)/ Z_STATE [†] (1)/ SOSSI.D[11](6)/ GPIO32(7)	B18	LCD.VS(0)/ Z_STATE [†] (1)/ SOSSI.RD(6)	B19	LCD.P[6](0)/ Z_STATE [†] (1)/ SOSSI.D6	B20	CV _{DD3}
B21	LCD.P[1](0)/ Z_STATE [†] (1)/ SOSSI.D[1](6)	C1	FLASH.A[3](0)	C2	DV _{DD5}	C3	SDRAM.BA[1]
C4	SDRAM.D[6]	C5	SDRAM.D[2]	C6	SDRAM.D[1]	C7	SDRAM.D[5]
C8	SDRAM.DQML	C9	SDRAM.CLK	C10	SDRAM.D[8]	C11	SDRAM.D[12]
C12	SDRAM.D[15]	C13	SDRAM.D[11]	C14	SDRAM.DQSH	C15	LCD.PCLK(0)/ Z_STATE [†] (1)/ SOSSI.WR(6)
C16	LCD.P[14](0)/ Z_STATE [†] (1)/ SOSSI.D[14](6)/ GPIO35(7)	C17	LCD.P[10](0)/ Z_STATE [†] (1)/ SOSSI.D[10](6)/ GPIO31(7)	C18	LCD.P[7](0)/ Z_STATE [†] (1)/ SOSSI.D[7](6)	C19	LCD.P[2](0)/ Z_STATE [†] (1)/ SOSSI.D[2](6)
C20	LCD.HS(0)/ Z_STATE [†] (1)/ SOSSI.CS(6)	C21	KB.C[4](0)/ GPIO27(7)	D2	FLASH.A[5](0)	D3	FLASH.A[2](0)
D4	SDRAM.DQSL	D5	SDRAM.D[4]	D6	SDRAM.D[0]	D7	SDRAM.D[3]
D8	SDRAM.D[7]	D9	SDRAM.CLKX	D10	SDRAM.DQMU	D11	SDRAM.D[10]
D12	SDRAM.D[14]	D13	SDRAM.D[13]	D14	SDRAM.D[9]	D15	LCD.P[15](0)/ Z_STATE [†] (1)/ SOSSI.D[15](6)/ GPIO2(7)

[†] Z_STATE = high-impedance

[‡] "NC" denotes "No Connect".

[§] LOW_STATE = 0

NOTES: 1. Shading denotes signals with multiplexed functions.

2. The number within parenthesis at the end of a signal name denotes the Pin Mux setting (see the MUX CTRL SETTING column in Table 2–3 and Table 2–4).

Table 2–2. ZZG Package Terminal Assignments (Continued)

ZZG BALL NO.	SIGNAL	ZZG BALL NO.	SIGNAL	ZZG BALL NO.	SIGNAL	ZZG BALL NO.	SIGNAL
D16	LCD.P[9](0)/ Z_STATE†(1)/ SOSSI.D[9](6)/ GPIO30(7)	D17	LCD.P[8](0)/ Z_STATE†(1)/ SOSSI.D[8](6)/ GPIO29(7)	D18	LCD.P0/ Z_STATE†(1)/ SOSSI.D[0](6)	D19	KB.C[2](0)/ GPIO61(7)
D20	KB.C[1](0)/ MPUIO6(1)	E1	FLASH.A[25]	E2	CV _{DD2}	E3	FLASH.A[7](0)
E4	FLASH.A[4](0)	E5	NC‡	E18	KB.C[3](0)/ GPIO63(6)	E19	KB.R[4](0)/ MPUIO15(1)/ VLYNQ.TX1(2)
E20	KB.R[3](0)/ MPUIO13(1)/ VLYNQ.TX0(2)	E21	DV _{DD1}	F2	FLASH.A[20]	F3	FLASH.A[9](0)
F4	FLASH.A[6](0)	F18	KB.C0/ MPUIO0(1)	F19	KB.R[1](0)/ MPUIO9(1)/ VLYNQ.RX0(2)	F20	V _{SS}
G1	V _{SS}	G2	FLASH.A[12](0)	G3	FLASH.A[11](0)	G4	FLASH.A[10](0)
G8	SDRAM.CS	G9	SDRAM.A[8]	G10	SDRAM.A[4]	G11	SDRAM.A[7]
G12	SDRAM.A[6]	G13	LCD.P[12](0)/ Z_STATE†(1)/ SOSSI.D[12](6)/ GPIO33(7)	G14	LCD.P[3](0)/ Z_STATE†(1)/ SOSSI.D[3](6)	G18	KB.R0/ MPUIO8(1)/ VLYNQ.RX1(2)
G19	KB.C[5](0)/ GPIO28(7)	G20	MCBSP1.CLKS(0)/ SOSSI.TE(6)/ GPIO62(7)	G21	MCBSP1.CLKX(0)/ GPIO54(7)	H2	DV _{DD5}
H3	FLASH.A[15](0)	H4	FLASH.A[14](0)	H7	SDRAM.RAS	H8	SDRAM.WE
H9	SDRAM.A[12]	H10	SDRAM.A[11]	H11	SDRAM.A[13]	H12	SDRAM.CKE
H13	LCD.P[4](0)/ Z_STATE†(1)/ SOSSI.D[4](6)	H14	KB.R[2](0)/ MPUIO10(1)/ VLYNQ.CLK(2)	H15	MCBSP1.FSX(0)/ MCBSP1.DX(1)/ MCBSP1.DXZ(2) GPIO53(7)	H18	MCBSP1.DX(0)/ MCBSP1.FSX(1)/ MCBSP1.DXZ(2)/ GPIO52(7)
H19	CAM.EXCLK(0)/ ETM.SYNC0(1)/ UWIRE.SDO(2)/ LOW_STATE§(6)/ GPIO57(7)	H20	MCBSP1.DR(0)/ GPIO51(7)	J1	LDO.FILTER	J2	FLASH.A[17]
J3	FLASH.A[19]	J4	FLASH.A[18]	J7	FLASH.A[8](0)	J8	FLASH.A[1](0)
J14	CAM.D[5](0)/ ETM.D[5](1)/ UWIRE.SDI(2)/ GPIO33(7)	J15	CAM.LCLK(0)/ ETM.CLK(1)/ UWIRE.SCLK(2)/ GPIO39(7)	J18	CAM.D[7](0)/ ETM.D[7](1)/ UWIRE.CS0(2)/ MMC2.DAT2(3)/ GPIO35(7)	J19	CAM.D[6](0)/ ETM.D[6](1)/ UWIRE.CS3(2)/ MMC2.CMD SPI.DO(3)/ GPIO34(7)

† Z_STATE = high-impedance

‡ "NC" denotes "No Connect".

§ LOW_STATE = 0

NOTES: 1. Shading denotes signals with multiplexed functions.

2. The number within parenthesis at the end of a signal name denotes the Pin Mux setting (see the MUX CTRL SETTING column in Table 2–3 and Table 2–4).

Table 2–2. ZZG Package Terminal Assignments (Continued)

ZZG BALL NO.	SIGNAL	ZZG BALL NO.	SIGNAL	ZZG BALL NO.	SIGNAL	ZZG BALL NO.	SIGNAL
J20	MPU_BOOT(0)/ USB1.SUSP(2)	J21	CV _{DD3}	K2	V _{SS}	K3	FLASH.A[23]
K4	FLASH.A[22]	K7	FLASH.A[16](0)	K8	FLASH.A[13](0)	K14	CAM.D[1](0)/ ETM.D1/ UART3.RTS(2)/ GPIO29(7)
K15	CAM.D[2](0)/ ETM.D[2](1)/ UART3.CTS(2)/ GPIO30(7)	K18	CAM.D[4](0)/ ETM.D[4](1)/ UART3.TX(2)/ GPIO32(7)	K19	CAM.D[3](0)/ ETM.D[3](1)/ UART3.RX(2)/ GPIO31(7)	K20	V _{SS}
L1	NC [‡]	L3	FLASH.BE0/ FLASH.CS2UOE(1)/ GPIO59(7)	L4	FLASH.ADV	L7	FLASH.A[24]
L8	FLASH.A[21]	L14	UART3.RX(0)/ PWL(1)/ UART2.RX(3)/ TIMER.PWM1(4)/ GPIO49(7)	L15	CAM.HS(0)/ ETM.PSTAT1/ UART2.CTS(2)/ MMC2.DAT0/ SPI.DI(3)/ GPIO38(7)	L18	CAM.VS(0)/ ETM.PSTAT[2](1)/ MPUIO14(2)/ MMC2.DAT1(3)
L19	CAM.D0/ ETM.D[0](1)/ MPUIO12(2)/ MMC2.DAT3(3)	L21	DV _{DD8}	M2	CV _{DD}	M3	FLASH.CS1(0)/ FLASH.CS1L(1)
M4	FLASH.CS2(0)/ FLASH.BAA(1)/ FLASH.CS2L(2)	M7	GPIO62(0)/ FLASH.CS0(1)	M8	FLASH.BE[1](0)/ FLASH.CS2UWE(1)/ GPIO60(7)	M14	GPIO2(0)/ SPI.CLK(1)/ ETM.PSTAT[4](5)/ RTDX.D[0](7)
M15	GPIO7(0)/ MMC.DAT2(1)/ TCK(3)/ MCSI1.CLK(4)/ ETM.SYNC[1](5)/ RTDX.D[2](7)	M18	LOW_STATE [§] (0)/ UART3.TX(1)/ PWT(2)/ UART2.TX(4)/ TIMER.PWM0(5)/ GPIO50(7)	M19	CAM.RSTZ(0)/ ETM.PSTAT[0](1)/ UART2.RTS(2)/ MMC2.CLK(3)/ LOW_STATE [§] (6)/ GPIO37(7)	M20	GPIO15(0)/ KB.R[7](1)/ TIMER.PWM2(2)/ VLYNQ.TX1(4)
N1	V _{SS}	N2	FLASH.D[1]	N3	FLASH.CLK(0)/ FLASH.CS2UOE(1)	N4	FLASH.D[0]
N7	FLASH.D[2]	N8	FLASH.CS3(0)/ GPIO3(7)	N14	Z_STATE [†] (0)/ UWIRE.CS0(1)/ MCBSP3.CLKX(2)/ UART3.TX(4)/ SPIF.CS0(6)/ GPIO45(7)	N15	MPUIO2(0)/ EXT_DMA_REQ0(1)/ UWIRE.CS1(2)/ SPIF.CS1(6)

[†] Z_STATE = high-impedance

[‡] "NC" denotes "No Connect".

[§] LOW_STATE = 0

NOTES: 1. Shading denotes signals with multiplexed functions.

2. The number within parenthesis at the end of a signal name denotes the Pin Mux setting (see the MUX CTRL SETTING column in Table 2–3 and Table 2–4).

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Table 2–2. ZZG Package Terminal Assignments (Continued)

ZZG BALL NO.	SIGNAL	ZZG BALL NO.	SIGNAL	ZZG BALL NO.	SIGNAL	ZZG BALL NO.	SIGNAL
N18	GPIO12(0)/ MCBSP3.FSX(1)/ TIMER.EXTCLK(3)/ VLYNQ.RX0[4]	N19	GPIO13(0)/ KB.R[5](1)/ LCD.BLUE0(2)/ Z_STATE†(3)/ VLYNQ.CLK(4)	N20	GPIO11(0)/ HDQ(1)/ VLYNQ.RX1(4)/ ETM.PSTAT5/ RTDX.D[3](7)	N21	GPIO14(0)/ KB.R[6](1)/ LCD.RED0(2)/ Z_STATE†(3)/ VLYNQ.TX0(4)
P2	FLASH.D[3]	P3	FLASH.CS2U(0)/ GPIO5(1)	P4	FLASH.D[4]	P7	FLASH.D[5]
P8	FLASH.D[11]	P9	USB.DP(0)/ I2C.SDA(4) UART1.RX(5)/ USB.PUEN(7)	P10	MCBSP2.DR(0)/ MCBSP2.DX(1)/ MCBSP2.DXZ(2)/ GPIO22(7)	P11	MMC.CMD/SPI.DO(0)/ CFLASH.CD2(3)/ SSI.CADATA(6)/ GPIO55(7)
P12	V _{SS}	P13	CLK32K_IN	P14	MCS11.CLK(0)/ MCBSP3.DX(1)/ USB1.VM(2)/ TDI(3)/ MCBSP3.CLKX(4)/ GPIO43(7)	P15	Z_STATE†(0)/ UWIRE.CS3(1)/ KB.C[6](2)/ SPIF.CS3(3)/ UART3.RX(4)/ Z_STATE†(6)/ GPIO44(7)
P18	GPIO3(0)/ SPI.CS3(1)/ MCBSP3.FSX(2)/ LED1(3)/ ETM.PSTAT[3](5)/ RTDX.D[1](7)	P19	GPIO6(0)/ SPI.CS1(1)/ MCBSP3.FSX(2)/ TIMER.EVENT3(3)/ MCS11.DIN(4)/ TMS(5)	P20	GPIO4(0)/ SPI.CS2(1)/ MCBSP3.FSX(2)/ TIMER.EVENT4(3)/ SPIF.DIN(4)	R1	DV _{DD5}
R2	FLASH.D[6]	R3	FLASH.D[7]	R4	FLASH.D[8]	R8	USB.DM(0)/ I2C.SCL(4)/ UART1.TX(5)/ Z_STATE†(7)
R9	UART2.RX(0)/ USB2.VM(1)/ USB0.VM(5)/ GPIO18(7)	R10	MCLKREQ(0)/ EXT_MASTER_REQ(1)/ UART2.RX(2)/ MMC2.DAT3(6)/ GPIO23(7)	R11	MMC.DAT0/SPI.DI(0)/ Z_STATE†(1)/ CFLASH.IOIS16(3)/ SSI.ACRDY(6)/ GPIO58(7)	R12	PWRON_RESET
R13	CLK32K_OUT(0)/ MPUIO0(4)/ USB1.SPEED(5)/ UART1.TX(6)/ GPIO36(7)	R14	UART1.CTS(0)/ UART1.IRSEL(2)/ GPIO38(7)	R18	GPIO0(0)/ SPI.RDY(1)/ USB.VBUS(2)/ SPIF.DOUT(3)/ MMC2.CLKIN(6)	R19	GPIO1(0)/ UART3.RTS(1)
R20	CV _{DD3}	R21	V _{SS}	T2	FLASH.D[9]	T3	FLASH.D[10]

† Z_STATE = high-impedance

‡ "NC" denotes "No Connect".

§ LOW_STATE = 0

NOTES: 1. Shading denotes signals with multiplexed functions.

2. The number within parenthesis at the end of a signal name denotes the Pin Mux setting (see the MUX CTRL SETTING column in Table 2–3 and Table 2–4).

Table 2–2. ZZG Package Terminal Assignments (Continued)

ZZG BALL NO.	SIGNAL	ZZG BALL NO.	SIGNAL	ZZG BALL NO.	SIGNAL	ZZG BALL NO.	SIGNAL
T4	FLASH.D[14]	T18	I2C.SCL	T19	MPUIO4(0)/ EXT_DMA_REQ1(1)/ LED2(2)/ UWIRE.CS2(3)/ SPIF.CS2(4)/ MCBSP3.DR(6)	T20	MPUIO5(0)/ LOW_PWR(1)/ UART3.RTS(3)/ UART1.DTR(4)
U1	FLASH.D[12]	U2	V _{SS}	U3	FLASH.D[13]	U4	FLASH.OE
U18	UWIRE.SDI(0)/ UART3.DSR(1)/ UART1.DSR(2)/ MCBSP3.DR(3)/ SPIF.DIN(6)/ GPIO47(7)	U19	MPUIO1(0)/ RTCK(1)/ SPIF.SCK(6)	U20	MPU_RST(0)/ MPUIO14(6)	U21	DV _{DD9}
V2	FLASH.RDY(0)/ GPIO10(1)	V3	FLASH.D[15]	V4	FLASH.WP	V5	MCLK(0)/ MMC2.DATDIR0(6)/ GPIO24(7)
V6	LOW_STATE [§] (0)/ UART2.TX(1)/ USB2.TXD(2)/ USB0.TXD(5)/ Z_STATE [†] (6)/ GPIO17(7)	V7	MCBSP2.CLKR(0)/ GPIO11(1)/ VLYNQ.CLK(3)	V8	MPUIO3(0)/ MMC2.DAT1(6)	V9	MCS12.SYNC(0)/ GIOP7(1)/ USB2.SPEED(2)/ USB0.SPEED(5)/ MMC2.CMDIR(6)
V10	MMC.DAT1(0)/ MPUIO10(1)/ MPUIO7(2)/ CFLASH.IREQ(3)/ SSI.ACDATA(6)	V11	MMC.CLK(0)/ SSI.CARDY(6)/ GPIO57(7)	V12	DV _{DDRTC}	V13	OSC32K_IN
V14	UART1.RX(0)/ UART1.IRRX(2)/ GPIO37(7)	V15	MCS11.DIN(0)/ USB1.RCV(1)/ EMU1(3)/ MCBSP3.DR(4)/ SSI.ACWAKE(6)/ GPIO56(7)	V16	EMU0	V17	TMS
V18	CONF	V19	UWIRE.SCLK(0)/ KB.C[7](1)/ MPUIO1(2)/ UART3.CTS(4)	V20	I2C.SDA(0)/ GPIO48(7)	W1	FLASH.RP(0)/ FLASH.CS2UWE(1)
W2	FLASH.WE	W3	OSC1_OUT	W4	USB.PUEN(0)/ USB.CLKO(1)/ USB.PUDIS(3)/ Z_STATE [†] (4)/ LOW_POWER(6)/ GPIO58(7)	W5	LOW_STATE [§] (0)/ UART2.RTS(1)/ USB2.SE0(2)/ MPUIO5(3)/ MPUIO12(4)/ USB0.SE0(5)/ LOW_STATE [§] (6)

[†] Z_STATE = high-impedance

[‡] "NC" denotes "No Connect".

[§] LOW_STATE = 0

NOTES: 1. Shading denotes signals with multiplexed functions.

2. The number within parenthesis at the end of a signal name denotes the Pin Mux setting (see the MUX CTRL SETTING column in Table 2–3 and Table 2–4).

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Table 2–2. ZZG Package Terminal Assignments (Continued)

ZZG BALL NO.	SIGNAL	ZZG BALL NO.	SIGNAL	ZZG BALL NO.	SIGNAL	ZZG BALL NO.	SIGNAL
W6	MCBSP2.FSR(0)/ GPIO12(1)/ VLYNQ.RX0(3)	W7	MCBSP2.FSX(0)/ VLYNQ.RX1(3)/ GPIO21(7)	W8	GPIO9(0)/ EMU0(3)/ MCSI1.SYNC(4)/ MMC2.DAT0/SPI.DI(6)	W9	MCSI2.DOUT(0)/ USB2.TXEN(1)/ USB0.TXEN(5)/ Z_STATE†(6)/ GPIO25(7)
W10	MMC.DAT2(0)/ Z_STATE†(1)/ MPUIO11(2)/ CFLASH.RESET(3)/ SSI.CAFLAG(6)	W11	MMC.DAT3(0)/ MPUIO9(1)/ MPUIO6(2)/ CFLASH.CD1(3)/ SSI.ACFLAG(6)	W12	CV _{DDR} TC	W13	RTC_WAKE_INT(0)/ USB1.SE0(4)/ RST_HOST_OUT(5)/ CCP.CLKM(6)/ GPIO55(7)
W14	MCSI1.DOUT(0)/ USB1.TXD(1)/ TDO(3)/ MCBSP3.DX(4)/ CCP.DATAP(6)/ GPIO18(7)/ MCBSP3.DOUT_HIZ	W15	BCLKREQ(0)/ UART3.CTS(1)/ MMC2.DAT2(6)/ GPIO40(7)	W16	Z_STATE†(0)/ MCBSP3.CLKX(1)/ USB1.TXEN(2)/ MCSI1.DIN(4)/ Z_STATE†(6)/ GPIO42(7)	W17	EMU1
W18	TCK	W19	BF A IL/EXT_FIQ(0)/ UART3.CTS(1)/ UART1.DSR(2)/ MMC.DATDIR1(6)	W20	V _{SS}	W21	UWIRE.SDO(0)/ UART3.DTR(1)/ UART1.DTR(2)/ MCBSP3.DX(3)/ UART3.RTS(4)/ MCBSP3.DXZ(5)/ SPIF.DOUT(6)/ GPIO46(7)
Y1	FLASH.CS1U(0)/ GPIO16(7)	Y2	OSC1_IN	Y3	V _{SS}	Y4	UART2.BCLK(0)/ SYS_CLK_IN(6)
Y5	UART2.CTS(0)/ USB2.RCV(1)/ GPIO7(2)/ USB0.RCV(5)	Y6	MCBSP2.CLKX(0)/ VLYNQ.TX1(3)/ GPIO20(7)	Y7	DV _{DD3}	Y8	GPIO8(0)/ TRST(3)/ MCSI1.DOUT(4)/ MMC2.CMD/SPI.DO(6)
Y9	CV _{DD}	Y10	MCSI2.CLK(0)/ USB2.SUSP(1)/ USB0.SUSP(5)/ MMC2.CLK(6)/ GPIO27(7)	Y12	RTC_ON_NOFF(0)/ CCP.CLKP(6)	Y13	V _{SS}
Y14	LOW_STATE§(0)/ UART1.TX(1)/ UART1.IRTX(2)/ CCP.DATAM(6)	Y15	BCLK(0)/ UART3.RTS(1)/ CAM.OUTCLK(6)/ GPIO17(7)	Y16	DV _{DD7}	Y17	RTCK
Y18	TRST	Y19	TDI	Y20	CV _{DD}	Y21	CV _{DDA}

† Z_STATE = high-impedance

‡ "NC" denotes "No Connect".

§ LOW_STATE = 0

NOTES: 1. Shading denotes signals with multiplexed functions.

2. The number within parenthesis at the end of a signal name denotes the Pin Mux setting (see the MUX CTRL SETTING column in Table 2–3 and Table 2–4).

Table 2-2. ZZG Package Terminal Assignments (Continued)

ZZG BALL NO.	SIGNAL	ZZG BALL NO.	SIGNAL	ZZG BALL NO.	SIGNAL	ZZG BALL NO.	SIGNAL
AA1	V _{SS}	AA2	DV _{DD2}	AA3	CV _{DD1}	AA5	MCBSP2.DX(0)/ MCBSP2.DR(1)/ MCBSP2.DXZ(2)/ GPIO19(7)
AA7	V _{SS}	AA9	MCSI2.DIN(0)/ USB2.VP(1)/ USB0.VP(5)/ GPIO26(7)	AA11	DV _{DD6}	AA13	OSC32K_OUT
AA15	LOW_STATE [§] (0)/ UART1.RTS(1)/ UART1.IRSHDN(2)/ VLYNQ.TX0(3)/ Z_STATE [†] (6)/ GPIO39(7)	AA17	MCSI1.SYNC(0)/ MCBSP3.DR(1)/ USB1.VP(2)/ MCBSP3.FSX(4)	AA19	TDO/ VLYNQ.TX0	AA20	RST_OUT(0)/ GPIO41(7)
AA21	V _{SS}						

[†] Z_STATE = high-impedance

[‡] "NC" denotes "No Connect".

[§] LOW_STATE = 0

- NOTES: 1. Shading denotes signals with multiplexed functions.
2. The number within parenthesis at the end of a signal name denotes the Pin Mux setting (see the MUX CTRL SETTING column in Table 2-3 and Table 2-4).

2.3 Terminal Characteristics and Multiplexing

Table 2–3 describes terminal characteristics and the signals multiplexed on each ball for the ZDY package. Table 2–4 describes terminal characteristics and the signals multiplexed on each ball for the ZZG package. The table column headers are explained below:

- **BALL NO.:** The package ball number.
- **SIGNAL NAME:** The names of all the signals that are multiplexed on each ball.
- **TYPE:** The signal direction.
- **MUX CTRL SETTING:** Shows control of multiplexing modes.
- **PULLUP/PULLDN:** Denotes the presence of an internal pullup or pulldown. Pullups and pulldowns can be enabled or disabled via software.
- **BUFFER STRENGTH:** Drive strength of the associated output buffer.
- **OTHER:** Contains various terminal information, such as buffer type, boundary scan capability, and gating/inhibit functionality.
- **RESET STATE:** The state of the terminal at reset.
- **SUPPLY:** The voltage supply which powers the terminal's I/O buffers.

NOTE: Care must be taken to avoid assigning multiple balls to the same signal. Violations may cause unexpected results.

Table 2–3. ZDY Package Terminal Characteristics

ZDY BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING	PULLUP/PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
E7	SDRAM.CS	O	NA		3 mA (Lv) 8 mA (Hv)	A	1	DV _{DD4}
A12	SDRAM.DQSH	I/O	NA		3 mA (Lv) 6 mA (Hv)	A, K	0	DV _{DD4}
A2	SDRAM.DQSL	I/O	NA		3 mA (Lv) 6 mA (Hv)	A, K	0	DV _{DD4}
D5	SDRAM.CAS	O	NA		3 mA (Lv) 8 mA (Hv)	A	1	DV _{DD4}
D4	SDRAM.RAS	O	NA		3 mA (Lv) 8 mA (Hv)	A	1	DV _{DD4}
C7	SDRAM.DQML	O	NA		3 mA (Lv) 6 mA (Hv)	A, K	0	DV _{DD4}
A8	SDRAM.DQMU	O	NA		3 mA (Lv) 6 mA (Hv)	A, K	0	DV _{DD4}

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20- μ A internal pulldown, PD100=100- μ A internal pulldown, PU20 = 20- μ A internal pullup, PU100 = 100- μ A internal pullup

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output

B = SUBLVDS input/output

C = USB transceiver input/output

D = I²C input/output buffers

E = Analog oscillator terminals

F = Boundary-scannable terminal

K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

NOTES: 3. NA denotes no multiplexing on the ball

4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

G1 = Terminal may be gated by BFAIL

G2 = Terminal may be gated by GPIO9 and MPUIO3

G3 = Terminal may be gated by BFAIL and OMAP5912 Internal Reset

H1 = Terminal may be 3-stated by BFAIL input

H3 = MCS11.DOUT pin can be forced into a high-impedance

state by the OMAP5912 HIGH_IMP3 control bit

Table 2–3. ZDY Package Terminal Characteristics (Continued)

ZDY BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING	PULLUP/PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
E6	SDRAM.WE	O	NA		3 mA (Lv) 8 mA (Hv)	A	1	DV _{DD4}
D10 E8 E9 F8 F9 C6 A10 E10 B9 C8 C3 F7 A1 B2	SDRAM.A[13:0]	O	NA		3 mA (Lv) 8 mA (Hv)	A	0	DV _{DD4}
C4 C5	SDRAM.BA[1:0]	O	NA		3 mA (Lv) 8 mA (Hv)	A	0	DV _{DD4}
B10 C10 B11 B9 A11 B8 B12 C9 B7 A3 B6 B3 A5 A4 B5 B4	SDRAM.D[15:0]	I/O	NA		3 mA (Lv) 6 mA (Hv)	A, K	0	DV _{DD4}
A7	SDRAM.CLK	O	NA		3 mA (Lv) 6 mA (Hv)	A, K	U	DV _{DD4}
A6	SDRAM.CLKX	O	NA		3 mA (Lv) 6 mA (Hv)	A, K	0	DV _{DD4}
B13	SDRAM.CKE	O	NA		3 mA (Lv) 8 mA (Hv)	A	1	DV _{DD4}
F10	LCD.AC	O	RegD[11:9] = 000		2 mA (Lv) 6 mA (Hv)	A, F, G1	0	DV _{DD1}
	SYS_CLK_OUT	O	RegD[11:9] = 001					
	Z_STATE	Z	RegD[11:9] = 010					
	SOSSI.CMD	O	RegD[11:9] = 110					
A14	LCD.PCLK	O	RegD[17:15] = 000		2 mA (Lv) 6 mA (Hv)	A, F, G1	0	DV _{DD1}
	Z_STATE	Z	RegD[17:15] = 001					
	SOSSI.WR	O	RegD[17:15] = 110					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20- μ A internal pulldown, PD100=100- μ A internal pulldown, PU20 = 20- μ A internal pullup, PU100 = 100- μ A internal pullup

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output

B = SUBLVDS input/output

C = USB transceiver input/output

D = I²C input/output buffers

E = Analog oscillator terminals

F = Boundary-scannable terminal

K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

NOTES: 3. NA denotes no multiplexing on the ball

4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2–3. ZDY Package Terminal Characteristics (Continued)

ZDY BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING	PULLUP/PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
C12	LCD.P[15]	O	RegD[20:18] = 000	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F, G1	0	DV _{DD1}
	Z_STATE	Z	RegD[20:18] = 001					
	SOSSI.D[15]	I/O	RegD[20:18] = 110					
	GPIO2	I/O	RegD[20:18] = 111					
D12	LCD.P[14]	O	RegD[23:21] = 000	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F, G1	0	DV _{DD1}
	Z_STATE	Z	RegD[23:21] = 001					
	SOSSI.D[14]	I/O	RegD[23:21] = 110					
	GPIO35	I/O	RegD[23:21] = 111					
E11	LCD.P[13]	O	RegD[26:24] = 000	PU20, PD20	2 mA (Lv) 6 mA (Hv)	F, A, G1	0	DV _{DD1}
	Z_STATE	Z	RegD[26:24] = 001					
	SOSSI.D[13]	I/O	RegD[26:24] = 110					
	GPIO34	I/O	RegD[26:24] = 111					
A13	LCD.P[12]	O	RegD[29:27] = 000	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F, G1	0	DV _{DD1}
	Z_STATE	Z	RegD[29:27] = 001					
	SOSSI.D[12]	I/O	RegD[29:27] = 110					
	GPIO33	I/O	RegD[29:27] = 111					
B14	LCD.P[11]	O	RegE[2:0] = 000	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F, G1	0	DV _{DD1}
	Z_STATE	Z	RegE[2:0] = 001					
	SOSSI.D[11]	I/O	RegE[2:0] = 110					
	GPIO32	I/O	RegE[2:0] = 111					
A15	LCD.P[10]	O	RegE[5:3] = 000	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F, G1	0	DV _{DD1}
	Z_STATE	Z	RegE[5:3] = 001					
	SOSSI.D[10]	I/O	RegE[5:3] = 110					
	GPIO31	I/O	RegE[5:3] = 111					
F11	LCD.P[9]	O	RegE[8:6] = 000	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F, G1	0	DV _{DD1}
	Z_STATE	Z	RegE[8:6] = 001					
	SOSSI.D[9]	I/O	RegE[8:6] = 110					
	GPIO30	I/O	RegE[8:6] = 111					
B15	LCD.VS	O	RegE[11:9] = 000		2 mA (Lv) 6 mA (Hv)	A, F, G1	0	DV _{DD1}
	Z_STATE	Z	RegE[11:9] = 001					
	SOSSI.RD	O	RegE[11:9] = 110					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20- μ A internal pulldown, PD100=100- μ A internal pulldown, PU20 = 20- μ A internal pullup, PU100 = 100- μ A internal pullup

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVC MOS input/output

B = SUBLVDS input/output

C = USB transceiver input/output

D = I²C input/output buffers

E = Analog oscillator terminals

F = Boundary-scannable terminal

K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

NOTES: 3. NA denotes no multiplexing on the ball

4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2–3. ZDY Package Terminal Characteristics (Continued)

ZDY BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING	PULLUP/PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
C13	LCD.P[8]	O	RegE[14:12] = 000	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F, G1	0	DV _{DD1}
	Z_STATE	Z	RegE[14:12] = 001					
	SOSSI.D[8]	I/O	RegE[14:12] = 110					
	GPIO29	I/O	RegE[14:12] = 111					
D13	LCD.P[7]	O	RegE[17:15] = 000	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F, G1	0	DV _{DD1}
	Z_STATE	Z	RegE[17:15] = 001					
	SOSSI.D[7]	I/O	RegE[17:15] = 110					
A16	LCD.P[6]	O	RegE[20:18] = 000	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F, G1	0	DV _{DD1}
	Z_STATE	Z	RegE[20:18] = 001					
	SOSSI.D[6]	I/O	RegE[20:18] = 110					
C15	LCD.P[5]	O	RegE[23:21] = 000	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F, G1	0	DV _{DD1}
	Z_STATE	Z	RegE[23:21] = 001					
	SOSSI.D[5]	I/O	RegE[23:21] = 110					
E12	LCD.P[4]	O	RegE[26:24] = 000	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F, G1	0	DV _{DD1}
	Z_STATE	Z	RegE[26:24] = 001					
	SOSSI.D[4]	I/O	RegE[26:24] = 110					
D14	LCD.P[3]	O	RegE[29:27] = 000	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F, G1	0	DV _{DD1}
	Z_STATE	Z	RegE[29:27] = 001					
	SOSSI.D[3]	I/O	RegE[29:27] = 110					
C16	LCD.P[2]	O	RegF[2:0] = 000	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F, G1	0	DV _{DD1}
	Z_STATE	Z	RegF[2:0] = 001					
	SOSSI.D[2]	I/O	RegF[2:0] = 110					
B16	LCD.P[1]	O	RegF[5:3] = 000	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F, G1	0	DV _{DD1}
	Z_STATE	Z	RegF[5:3] = 001					
	SOSSI.D[1]	I/O	RegF[5:3] = 110					
A17	LCD.P[0]	O	RegF[8:6] = 000	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F, G1	0	DV _{DD1}
	Z_STATE	Z	RegF[8:6] = 001					
	SOSSI.D[0]	I/O	RegF[8:6] = 110					
D15	LCD.HS	O	RegD[14:12] = 000		4 mA (Lv) 8 mA (Hv)	A, F, G1	0	DV _{DD1}
	Z_STATE	Z	RegD[14:12] = 001					
	SOSSI.CS	O	RegD[14:12] = 110					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20- μ A internal pulldown, PD100=100- μ A internal pulldown, PU20 = 20- μ A internal pullup, PU100 = 100- μ A internal pullup

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output

B = SUBLVDS input/output

C = USB transceiver input/output

D = I²C input/output buffers

E = Analog oscillator terminals

F = Boundary-scannable terminal

K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

NOTES: 3. NA denotes no multiplexing on the ball

4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

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Table 2–3. ZDY Package Terminal Characteristics (Continued)

ZDY BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING	PULLUP/PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
D16	KB.C[4] GPIO27	O I/O	Reg3[5:3] = 000 Reg3[5:3] = 111	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F	0	DV _{DD1}
E15	KB.C[3] GPIO63	O I/O	Reg3[8:6] = 000 Reg3[8:6] = 111	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F	0	DV _{DD1}
B17	KB.C[2] GPIO61	O I/O	Reg3[11:9] = 000 Reg3[11:9] = 111	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F	0	DV _{DD1}
C17	KB.C[1] MPUIO6	O I/O	Reg3[14:12] = 000 Reg3[14:12] = 001	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F	0	DV _{DD1}
F14	KB.C[0] MPUIO0	O I/O	Reg3[17:15] = 000 Reg3[17:15] = 001	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F	0	DV _{DD1}
F13	KB.R[4] MPUIO15 VLYNQ.TX1	I I/O O	Reg3[20:18] = 000 Reg3[20:18] = 001 Reg3[20:18] = 010	PU100, PD20	4 mA (Lv) 11 mA (Hv)	A, F	Z	DV _{DD1}
D17	KB.R[3] MPUIO13 VLYNQ.TX0	I I/O O	Reg3[23:21] = 000 Reg3[23:21] = 001 Reg3[23:21] = 010	PU100, PD20	4 mA (Lv) 11 mA (Hv)	A, F	Z	DV _{DD1}
E16	KB.R[2] MPUIO10 VLYNQ.CLK	I I/O I/O	Reg3[26:24] = 000 Reg3[26:24] = 001 Reg3[26:24] = 010	PU100, PD20	4 mA (Lv) 11 mA (Hv)	A, F	Z	DV _{DD1}
E17	KB.R[1] MPUIO9 VLYNQ.RX0	I I/O I	Reg3[29:27] = 000 Reg3[29:27] = 001 Reg3[29:27] = 010	PU100, PD20	4 mA (Lv) 11 mA (Hv)	A, F	Z	DV _{DD1}
F15	KB.R[0] MPUIO8 VLYNQ.RX1	I I/O I	Reg4[2:0] = 000 Reg4[2:0] = 001 Reg4[2:0] = 010	PU100, PD20	4 mA (Lv) 11 mA (Hv)	A, F	Z	DV _{DD1}
F17	KB.C[5] GPIO28	O I/O	Reg3[2:0] = 000 Reg3[2:0] = 111	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F	0	DV _{DD1}
G13	MCBSP1.CLKS SOSSI.TE GPIO62	I I I/O	Reg4[8:6] = 000 Reg4[8:6] = 110 Reg4[8:6] = 111	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F	–	DV _{DD1}
F16	MCBSP1.CLKX GPIO54	I/O I/O	Reg4[11:9] = 000 Reg4[11:9] = 111	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G1	Z	DV _{DD1}

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20- μ A internal pulldown, PD100=100- μ A internal pulldown, PU20 = 20- μ A internal pullup, PU100 = 100- μ A internal pullup

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output

B = SUBLVDS input/output

C = USB transceiver input/output

D = I²C input/output buffers

E = Analog oscillator terminals

F = Boundary-scannable terminal

K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

NOTES: 3. NA denotes no multiplexing on the ball

4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

G1 = Terminal may be gated by BFAIL

G2 = Terminal may be gated by GPIO9 and MPUIO3

G3 = Terminal may be gated by BFAIL and OMAP5912 Internal Reset

H1 = Terminal may be 3-stated by BFAIL input

H3 = MCS11.DOUT pin can be forced into a high-impedance

state by the OMAP5912 HIGH_IMP3 control bit

Table 2–3. ZDY Package Terminal Characteristics (Continued)

ZDY BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING	PULLUP/PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
G15	MCBSP1.FSX	I/O	Reg4[14:12] = 000	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F, G1	Z	DV _{DD1}
	MCBSP1.DX	O	Reg4[14:12] = 001					
	MCBSP1.DXZ	O/Z	Reg4[14:12] = 010					
	GPIO53	I/O	Reg4[14:12] = 111					
G14	MCBSP1.DX	O	Reg4[17:15] = 000	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F, G1	0	DV _{DD1}
	MCBSP1.ESX	I/O	Reg4[17:15] = 001					
	MCBSP1.DXZ	O/Z	Reg4[17:15] = 010					
	GPIO52	I/O	Reg4[17:15] = 111					
G17	MCBSP1.DR	I	Reg4[20:18] = 000	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F	LZ	DV _{DD1}
	GPIO51	I/O	Reg4[20:18] = 111					
H12	CAM.EXCLK	O	Reg4[23:21] = 000	PU20, PD20	4 mA (Lv) 11 mA (Hv)	A, F, G1	0	DV _{DD8}
	ETM.SYNC[0]	O	Reg4[23:21] = 001					
	UWIRE.SDO	O	Reg4[23:21] = 010					
	LOW_STATE	O	Reg4[23:21] = 110					
	GPIO57	I/O	Reg4[23:21] = 111					
G16	CAM.LCLK	I	Reg4[26:24] = 000	PU20, PD20	4 mA (Lv) 11 mA (Hv)	A, F	Z	DV _{DD8}
	ETM.CLK	O	Reg4[26:24] = 001					
	UWIRE.SCLK	O	Reg4[26:24] = 010					
	GPIO39	I/O	Reg4[26:24] = 111					
H14	MPU_BOOT	I	Reg8[29:27] = 000		2 mA (Lv) 6 mA (Hv)	A, F	–	
	USB1.SUSP	O	Reg8[29:27] = 010					
H16	CAM.D[7]	I	Reg4[29:27] = 000	PU20, PD20	4 mA (Lv) 11 mA (Hv)	A, F	Z	DV _{DD8}
	ETM.D[7]	O	Reg4[29:27] = 001					
	UWIRE.CS0	O	Reg4[29:27] = 010					
	MMC2.DAT2	I/O	Reg4[29:27] = 011					
	GPIO35	I/O	Reg4[29:27] = 111					
H15	CAM.D[6]	I	Reg5[2:0] = 000	PU20, PD20	4 mA (Lv) 11 mA (Hv)	A, F	Z	DV _{DD8}
	ETM.D[6]	O	Reg5[2:0] = 001					
	UWIRE.CS3	O	Reg5[2:0] = 010					
	MMC2.CMD/SPI.DO	I/O	Reg5[2:0] = 011					
	GPIO34	I/O	Reg5[2:0] = 111					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20- μ A internal pulldown, PD100=100- μ A internal pulldown, PU20 = 20- μ A internal pullup, PU100 = 100- μ A internal pullup

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output

B = SUBLVDS input/output

C = USB transceiver input/output

D = I²C input/output buffers

E = Analog oscillator terminals

F = Boundary-scannable terminal

K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

NOTES: 3. NA denotes no multiplexing on the ball

4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2–3. ZDY Package Terminal Characteristics (Continued)

ZDY BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING	PULLUP/PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
H17	CAM.D[5]	I	Reg5[5:3] = 000	PU20, PD20	4 mA (Lv) 11 mA (Hv)	A, F	Z	DV _{DD8}
	ETM.D[5]	O	Reg5[5:3] = 001					
	UWIRE.SDI	I	Reg5[5:3] = 010					
	GPIO33	I/O	Reg5[5:3] = 111					
J11	CAM.D[4]	I	Reg5[8:6] = 000	PU20, PD20	4 mA (Lv) 11 mA (Hv)	A, F	Z	DV _{DD8}
	ETM.D[4]	O	Reg5[8:6] = 001					
	UART3.TX	O	Reg5[8:6] = 010					
	GPIO32	I/O	Reg5[8:6] = 111					
H13	CAM.D[3]	I	Reg5[11:9] = 000	PU20, PD20	4 mA (Lv) 11 mA (Hv)	A, F	Z	DV _{DD8}
	ETM.D[3]	O	Reg5[11:9] = 001					
	UART3.RX	I	Reg5[11:9] = 010					
	GPIO31	I/O	Reg5[11:9] = 111					
J14	CAM.D[2]	I	Reg5[14:12] = 000	PU20, PD20	4 mA (Lv) 11 mA (Hv)	A, F	Z	DV _{DD8}
	ETM.D[2]	O	Reg5[14:12] = 001					
	UART3.CTS	I	Reg5[14:12] = 010					
	GPIO30	I/O	Reg5[14:12] = 111					
J16	CAM.D[1]	I	Reg5[17:15] = 000	PU20, PD20	4 mA (Lv) 11 mA (Hv)	A, F	Z	DV _{DD8}
	ETM.D[1]	O	Reg5[17:15] = 001					
	UART3.RTS	O	Reg5[17:15] = 010					
	GPIO29	I/O	Reg5[17:15] = 111					
J17	CAM.D[0]	I	Reg5[20:18] = 000	PU20, PD20	4 mA (Lv) 11 mA (Hv)	A, F	Z	DV _{DD8}
	ETM.D[0]	O	Reg5[20:18] = 001					
	MPUIO12	I/O	Reg5[20:18] = 010					
	MMC2.DAT3	I/O	Reg5[20:18] = 011					
J13	CAM.VS	I	Reg5[23:21] = 000	PU20, PD20	4 mA (Lv) 11 mA (Hv)	A, F	Z	DV _{DD8}
	ETM.PSTAT[2]	O	Reg5[23:21] = 001					
	MPUIO14	I/O	Reg5[23:21] = 010					
	MMC2.DAT1	I/O	Reg5[23:21] = 011					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20- μ A internal pulldown, PD100=100- μ A internal pulldown, PU20 = 20- μ A internal pullup, PU100 = 100- μ A internal pullup

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output

B = SUBLVDS input/output

C = USB transceiver input/output

D = I²C input/output buffers

E = Analog oscillator terminals

F = Boundary-scannable terminal

K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

G1 = Terminal may be gated by BFAIL

G2 = Terminal may be gated by GPIO9 and MPUIO3

G3 = Terminal may be gated by BFAIL and OMAP5912 Internal Reset

H1 = Terminal may be 3-stated by BFAIL input

H3 = MCS11.DOUT pin can be forced into a high-impedance

state by the OMAP5912 HIGH_IMP3 control bit

NOTES: 3. NA denotes no multiplexing on the ball

4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2–3. ZDY Package Terminal Characteristics (Continued)

ZDY BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING	PULLUP/PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
J12	CAM.HS	I	Reg5[26:24] = 000	PU20, PD20	4 mA (Lv) 11 mA (Hv)	A, F	Z	DV _{DD8}
	ETM.PSTAT[1]	O	Reg5[26:24] = 001					
	UART2.CTS	I	Reg5[26:24] = 010					
	MMC2.DAT0/SPI.DI	I/O	Reg5[26:24] = 011					
	GPIO38	I/O	Reg5[26:24] = 111					
K12	CAM.RSTZ	O	Reg5[29:27] = 000	PU20, PD20	4 mA (Lv) 11 mA (Hv)	A, F, G1	0	DV _{DD8}
	ETM.PSTAT[0]	O	Reg5[29:27] = 001					
	UART2.RTS	O	Reg5[29:27] = 010					
	MMC2.CLK	O	Reg5[29:27] = 011					
	LOW_STATE	O	Reg5[29:27] = 110					
	GPIO37	I/O	Reg5[29:27] = 111					
K17	LOW_STATE	O	Reg6[2:0] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G1	0	DV _{DD9}
	UART3.TX	O	Reg6[2:0] = 001					
	PWT	O	Reg6[2:0] = 010					
	UART2.TX	O	Reg6[2:0] = 100					
	TIMER.PWM0	O	Reg6[2:0] = 110					
	GPIO50	I/O	Reg6[2:0] = 111					
K15	UART3.RX	I	Reg6[5:3] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F	–	DV _{DD9}
	PWL	O	Reg6[5:3] = 001					
	UART2.RX	I	Reg6[5:3] = 011					
	TIMER.PWM1	O	Reg6[5:3] = 100					
	GPIO49	I/O	Reg6[5:3] = 111					
K16	GPIO15	I/O	Reg6[8:6] = 000	PU100, PD20	4 mA (Lv) 11 mA (Hv)	A, F, G1	LZ	DV _{DD9}
	KB.R[7]	I	Reg6[8:6] = 001					
	TIMER.PWM2	O	Reg6[8:6] = 010					
	VLYNQ.TX1	O	Reg6[8:6] = 100					
K14	GPIO14	I/O	Reg6[11:9] = 000	PU100, PD20	4 mA (Lv) 11 mA (Hv)	A, F, G1	LZ	DV _{DD9}
	KB.R[6]	I	Reg6[11:9] = 001					
	LCD.RED0	O	Reg6[11:9] = 010					
	Z_STATE	Z	Reg6[11:9] = 011					
	VLYNQ.TX0	O	Reg6[11:9] = 100					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20- μ A internal pulldown, PD100=100- μ A internal pulldown, PU20 = 20- μ A internal pullup, PU100 = 100- μ A internal pullup

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output

B = SUBLVDS input/output

C = USB transceiver input/output

D = I²C input/output buffers

E = Analog oscillator terminals

F = Boundary-scannable terminal

K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

NOTES: 3. NA denotes no multiplexing on the ball

4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

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Table 2–3. ZDY Package Terminal Characteristics (Continued)

ZDY BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING	PULLUP/PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
L17	GPIO13 KB.R[5] LCD.BLUE0 Z_STATE VLYNQ.CLK	I/O I O Z I/O	Reg6[14:12] = 000 Reg6[14:12] = 001 Reg6[14:12] = 010 Reg6[14:12] = 011 Reg6[14:12] = 100	PU100, PD20	4 mA (Lv) 11 mA (Hv)	A, F, G1	LZ	DV _{DD9}
L16	GPIO12 MCBSP3.FSX TIMER.EXTCLK VLYNQ.RX0	I/O I/O I I	Reg6[17:15] = 000 Reg6[17:15] = 001 Reg6[17:15] = 011 Reg6[17:15] = 100	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G1	LZ	DV _{DD9}
K13	GPIO11 HDQ VLYNQ.RX1 ETM.PSTAT[5]	I/O I/O I O	Reg6[20:18] = 000 Reg6[20:18] = 001 Reg6[20:18] = 100 Reg6[20:18] = 101	PU20, PD20	4 mA (Lv) 11 mA (Hv)	A, F, G1	LZ	DV _{DD9}
L15	GPIO7 MMC.DAT2 TCK MCS11.CLK ETM.SYNC[1]	I/O I/O I I/O O	Reg6[23:21] = 000 Reg6[23:21] = 001 Reg6[23:21] = 011 Reg6[23:21] = 100 Reg6[23:21] = 101	PU20, PD20	4 mA (Lv) 11 mA (Hv)	A, F, G1	LZ	DV _{DD9}
L14	GPIO6 SPI.CS1 MCBSP3.ESX TIMER.EVENT3 MCS11.DIN TMS	I/O O I/O I I I	Reg6[26:24] = 000 Reg6[26:24] = 001 Reg6[26:24] = 010 Reg6[26:24] = 011 Reg6[26:24] = 100 Reg6[26:24] = 101	PD100, PU20	4 mA (Lv) 8 mA (Hv)	A, F, G1	LZ	DV _{DD9}
M17	GPIO4 SPI.CS2 MCBSP3.FSX TIMER.EVENT4	I/O O I/O I	Reg6[29:27] = 000 Reg6[29:27] = 001 Reg6[29:27] = 010 Reg6[29:27] = 011	PD100, PU20	4 mA (Lv) 8 mA (Hv)	A, F, G1	LZ	DV _{DD9}

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20- μ A internal pulldown, PD100=100- μ A internal pulldown, PU20 = 20- μ A internal pullup, PU100 = 100- μ A internal pullup

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output

G1 = Terminal may be gated by BFAIL

B = SUBLVDS input/output

G2 = Terminal may be gated by GPIO9 and MPUIO3

C = USB transceiver input/output

G3 = Terminal may be gated by BFAIL and OMAP5912 Internal Reset

D = I²C input/output buffers

H1 = Terminal may be 3-stated by BFAIL input

E = Analog oscillator terminals

H3 = MCS11.DOUT pin can be forced into a high-impedance

F = Boundary-scannable terminal

state by the OMAP5912 HIGH_IMP3 control bit

K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

NOTES: 3. NA denotes no multiplexing on the ball

4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2–3. ZDY Package Terminal Characteristics (Continued)

ZDY BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING	PULLUP/PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
L13	GPIO3	I/O	Reg7[2:0] = 000	PU100, PD20	4 mA (Lv) 11 mA (Hv)	A, F, G1	LZ	DV _{DD9}
	SPI.CS3	O	Reg7[2:0] = 001					
	MCBSP3.FSX	I/O	Reg7[2:0] = 010					
	LED1	O	Reg7[2:0] = 011					
	ETM.PSTAT[3]	O	Reg7[2:0] = 101					
M16	GPIO2	I/O	Reg7[5:3] = 000	PU100, PD20	4 mA (Lv) 11 mA (Hv)	A, F, G1	LZ	DV _{DD9}
	SPI.CLK	O	Reg7[5:3] = 001					
	ETM.PSTAT[4]	O	Reg7[5:3] = 101					
M15	GPIO1	I/O	Reg7[8:6] = 000	PU100, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G1	LZ	DV _{DD9}
	UART3.RTS	O	Reg7[8:6] = 001					
N17	GPIO0	I/O	Reg7[11:9] = 000	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F, G1	LZ	DV _{DD9}
	SPI.RDY	I	Reg7[11:9] = 001					
	USB.VBUS	I	Reg7[11:9] = 010					
	SPIF.DOUT	O	Reg7[11:9] = 011					
	MMC2.CLKIN	I	Reg7[11:9] = 110					
N16	MPUIO5	I/O	Reg7[14:12] = 000	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F	LZ	DV _{DD9}
	LOW_PWR	O	Reg7[14:12] = 001					
	UART3.RTS	O	Reg7[14:12] = 011					
	UART1.DTR	O	Reg7[14:12] = 100					
M14	MPUIO4	I/O	Reg7[17:15] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G1	LZ	DV _{DD9}
	EXT_DMA_REQ1	I	Reg7[17:15] = 001					
	LED2	O	Reg7[17:15] = 010					
	UWIRE.CS2	O	Reg7[17:15] = 011					
	SPIF.CS2	O	Reg7[17:15] = 100					
	MCBSP3.DR	I	Reg7[17:15] = 110					
L12	MPUIO2	I/O	Reg7[20:18] = 000	PU100, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G1	LZ	DV _{DD9}
	EXT_DMA_REQ0	I	Reg7[20:18] = 001					
	UWIRE.CS1	O	Reg7[20:18] = 010					
	SPIF.CS1	O	Reg7[20:18] = 110					
N14	MPU_RST	I	Reg9[8:6] = 000		2 mA (Lv) 6 mA (Hv)	A, F	–	DV _{DD9}
	MPUIO14	I/O	Reg9[8:6] = 110					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20- μ A internal pulldown, PD100=100- μ A internal pulldown, PU20 = 20- μ A internal pullup, PU100 = 100- μ A internal pullup

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output

B = SUBLVDS input/output

C = USB transceiver input/output

D = I²C input/output buffers

E = Analog oscillator terminals

F = Boundary-scannable terminal

K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

NOTES: 3. NA denotes no multiplexing on the ball

4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

G1 = Terminal may be gated by BFAIL

G2 = Terminal may be gated by GPIO9 and MPUIO3

G3 = Terminal may be gated by BFAIL and OMAP5912 Internal Reset

H1 = Terminal may be 3-stated by BFAIL input

H3 = MCS11.DOUT pin can be forced into a high-impedance

state by the OMAP5912 HIGH_IMP3 control bit

Table 2–3. ZDY Package Terminal Characteristics (Continued)

ZDY BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING	PULLUP/PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
N15	MPUIO1	I/O	Reg7[23:21] = 000	PU100, PD20	4 mA (Lv) 8 mA (Hv)	A, F	Z	DV _{DD9}
	RTCK	I/O	Reg7[23:21] = 001					
	SPIF.SCK	I/O	Reg7[23:21] = 110					
P16	I2C.SCL	I/O/Z	Reg7[26:24] = 000		2 mA (Lv) 6 mA (Hv)	D	Z	DV _{DD9}
M11	I2C.SDA	I/O/Z	Reg7[29:27] = 000		2 mA (Lv) 6 mA (Hv)	D	Z	DV _{DD9}
	GPIO48	I	Reg7[29:27] = 111					
P14	UWIRE.SDI	I	Reg8[2:0] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F	LZ	DV _{DD9}
	UART3.DSR	O	Reg8[2:0] = 001					
	UART1.DSR	I	Reg8[2:0] = 010					
	MCBSP3.DR	I	Reg8[2:0] = 011					
	SPIF.DIN	I/O	Reg8[2:0] = 110					
	GPIO47	I/O	Reg8[2:0] = 111					
R15	UWIRE.SDO	O	Reg8[5:3] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G1	0	DV _{DD9}
	UART3.DTR	O	Reg8[5:3] = 001					
	UART1.DTR	O	Reg8[5:3] = 010					
	MCBSP3.DX	O	Reg8[5:3] = 011					
	UART3.RTS	O	Reg8[5:3] = 100					
	MCBSP3.DXZ	O/Z	Reg8[5:3] = 101					
	SPIF.DOUT	I/O	Reg8[5:3] = 110					
	GPIO46	I/O	Reg8[5:3] = 111					
P15	UWIRE.SCLK	O	Reg8[8:6] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G1	0	DV _{DD9}
	KB.C[7]	O	Reg8[8:6] = 001					
	MPUIO1	I/O	Reg8[8:6] = 010					
	UART3.CTS	I	Reg8[8:6] = 100					
R17	Z_STATE	Z	Reg8[11:9] = 000	PU100, PD20	4 mA (Lv) 8 mA (Hv)	A, F	Z	DV _{DD9}
	UWIRE.CS0	O	Reg8[11:9] = 001					
	MCBSP3.CLKX	I/O	Reg8[11:9] = 010					
	UART3.TX	O	Reg8[11:9] = 100					
	SPIF.CS0	I/O	Reg8[11:9] = 110					
	GPIO45	I/O	Reg8[11:9] = 111					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20- μ A internal pulldown, PD100=100- μ A internal pulldown, PU20 = 20- μ A internal pullup, PU100 = 100- μ A internal pullup

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output

B = SUBLVDS input/output

C = USB transceiver input/output

D = I²C input/output buffers

E = Analog oscillator terminals

F = Boundary-scannable terminal

K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

NOTES: 3. NA denotes no multiplexing on the ball

4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2–3. ZDY Package Terminal Characteristics (Continued)

ZDY BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING	PULLUP/PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
R16	Z_STATE	Z	Reg8[14:12] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F	Z	DV _{DD9}
	UWIRE_CS3	O	Reg8[14:12] = 001					
	KB.C[6]	O	Reg8[14:12] = 010					
	SPIF_CS3	O	Reg8[14:12] = 011					
	UART3.RX	I	Reg8[14:12] = 100					
	Z_STATE	Z	Reg8[14:12] = 110					
	GPIO44	I/O	Reg8[14:12] = 111					
T17	BFAIL/EXT_FIQ	I	Reg8[17:15] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F	Z	DV _{DD9}
	UART3.CTS	I	Reg8[17:15] = 001					
	UART1.DSR	I	Reg8[17:15] = 010					
	MMC2.DATDIR1	O	Reg8[17:15] = 110					
N12	RST_OUT	O	Reg9[11:9] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F	0	DV _{DD9}
	GPIO41	I/O	Reg9[11:9] = 111					
R14	CONF	I	NA	PU20, PD20		A	LZ	DV _{DD9}
U17	TDI	I	NA	PD100, PU20		A	LZ	DV _{DD9}
T15	TDO	O	NA		4 mA (Lv) 8 mA (Hv)		–	DV _{DD9}
	VLYNQ.TX0	TBD	TBD					
M10	TMS	I	NA	PD100, PU20		A	LZ	DV _{DD9}
P13	TCK	I	NA	PD100, PU20		A	LZ	DV _{DD9}
R13	TRST	I	NA	PU20, PD20		A	–	DV _{DD9}
U16	EMU0	I/O	NA	PU100, PD20	4 mA (Lv) 8 mA (Hv)	A	Input	DV _{DD9}
N11	EMU1	I/O	NA	PU100, PD20	4 mA (Lv) 8 mA (Hv)	A	Input	DV _{DD9}
T14	RTCK	I/O	NA		4 mA (Lv) 11 mA (Hv)	A	–	DV _{DD9}

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20- μ A internal pulldown, PD100=100- μ A internal pulldown, PU20 = 20- μ A internal pullup, PU100 = 100- μ A internal pullup

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output

B = SUBLVDS input/output

C = USB transceiver input/output

D = I²C input/output buffers

E = Analog oscillator terminals

F = Boundary-scannable terminal

K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

NOTES: 3. NA denotes no multiplexing on the ball

4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

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Table 2–3. ZDY Package Terminal Characteristics (Continued)

ZDY BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING	PULLUP/PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
N10	MCSI1.SYNC	I/O	RegA[5:3] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G1	LZ	DV _{DD7}
	MCBSP3.DR	I	RegA[5:3] = 001					
	USB1.VP	I	RegA[5:3] = 010					
	MCBSP3.FSX	I/O	RegA[5:3] = 100					
U15	MCSI1.CLK	I/O	RegA[8:6] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G1	LZ	DV _{DD7}
	MCBSP3.DX	O	RegA[5:3] = 001					
	USB1.VM	I	RegA[5:3] = 010					
	TDI	I	RegA[5:3] = 011					
	MCBSP3.CLKX	I/O	RegA[5:3] = 100					
	GPIO43	I/O	RegA[5:3] = 111					
U14	Z_STATE	Z	Reg9[5:3] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G1	Z	DV _{DD7}
	MCBSP3.CLKX	I/O	Reg9[5:3] = 001					
	USB1.TXEN	O	Reg9[5:3] = 010					
	MCSI1.DIN	I	Reg9[5:3] = 100					
	Z_STATE	Z	Reg9[5:3] = 110					
	GPIO42	I/O	Reg9[5:3] = 111					
P12	MCSI1.DIN	I	RegA[11:9] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F	Z	DV _{DD7}
	USB1.RCV	I	RegA[11:9] = 001					
	EMU1	I/O	RegA[11:9] = 011					
	MCBSP3.DR	I	RegA[11:9] = 100					
	SSI.ACWAKE	O	RegA[11:9] = 110					
	GPIO56	I/O	RegA[11:9] = 111					
R12	BCLKREQ	I	Reg9[29:27] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F	LZ	DV _{DD7}
	UART3.CTS	I	Reg9[29:27] = 001					
	MMC2.DAT2	I/O	Reg9[29:27] = 110					
	GPIO40	I/O	Reg9[29:27] = 111					
L10	BCLK	O	RegA[2:0] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G1	0	DV _{DD7}
	UART3.RTS	O	RegA[2:0] = 001					
	CAM.OUTCLK	O	RegA[2:0] = 110					
	GPIO17	I/O	RegA[2:0] = 111					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20- μ A internal pulldown, PD100=100- μ A internal pulldown, PU20 = 20- μ A internal pullup, PU100 = 100- μ A internal pullup

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output

B = SUBLVDS input/output

C = USB transceiver input/output

D = I²C input/output buffers

E = Analog oscillator terminals

F = Boundary-scannable terminal

K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

NOTES: 3. NA denotes no multiplexing on the ball

4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2–3. ZDY Package Terminal Characteristics (Continued)

ZDY BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING	PULLUP/PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
R11	LOW_STATE	O	Reg9[14:12] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G1	0	DV _{DD7}
	UART1.RTS	O	Reg9[14:12] = 001					
	UART1.IRSHDN	O	Reg9[14:12] = 010					
	Z_STATE	Z	Reg9[14:12] = 110					
	GPIO39	I/O	Reg9[14:12] = 111					
M9	UART1.CTS	I	Reg9[17:15] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F	LZ	DV _{DD7}
	UART1.IRSEL	O	Reg9[17:15] = 010					
	GPIO38	I/O	Reg9[17:15] = 111					
U13	UART1.RX	I	Reg9[20:18] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F	LZ	DV _{DD7}
	UART1.IRRX	I	Reg9[20:18] = 010					
	GPIO37	I/O	Reg9[20:18] = 111					
T12	LOW_STATE	O	Reg9[23:21] = 000		2 mA (Lv) 6 mA (Hv)	A, B, F, G1	0	DV _{DD7}
	UART1.TX	O	Reg9[23:21] = 001					
	UART1.IRTX	O	Reg9[23:21] = 010					
	CCP.DATAM	I	Reg9[23:21] = 110					
P11	MCSI1.DOUT	O	Reg9[26:24] = 000		2 mA (Lv) 6 mA (Hv)	A, B, F, G1, H3	0	DV _{DD7}
	USB1.TXD	O	Reg9[26:24] = 001					
	TDO	O	Reg9[26:24] = 011					
	MCBSP3.DX	O	Reg9[26:24] = 100					
	CCP.DATAP	I	Reg9[26:24] = 110					
	GPIO18	I/O	Reg9[26:24] = 111					
U12	CLK32K_OUT	O	RegA[14:12] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A	U	DV _{DDRTC}
	MPUIO0	I/O	RegA[14:12] = 100					
	USB1.SPEED	O	RegA[14:12] = 101					
	UART1.TX	O	RegA[14:12] = 110					
	GPIO36	I/O	RegA[14:12] = 111					
U11	OSC32K_IN	–	NA			E	NA	NA
U10	OSC32K_OUT	–	NA			E	NA	NA

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20- μ A internal pulldown, PD100=100- μ A internal pulldown, PU20 = 20- μ A internal pullup, PU100 = 100- μ A internal pullup

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output

B = SUBLVDS input/output

C = USB transceiver input/output

D = I²C input/output buffers

E = Analog oscillator terminals

F = Boundary-scannable terminal

K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

NOTES: 3. NA denotes no multiplexing on the ball

4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

G1 = Terminal may be gated by BFAIL

G2 = Terminal may be gated by GPIO9 and MPUIO3

G3 = Terminal may be gated by BFAIL and OMAP5912 Internal Reset

H1 = Terminal may be 3-stated by BFAIL input

H3 = MCSI1.DOUT pin can be forced into a high-impedance

state by the OMAP5912 HIGH_IMP3 control bit

Table 2–3. ZDY Package Terminal Characteristics (Continued)

ZDY BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING	PULLUP/PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
N9	RTC_WAKE_INT	O	Reg9[2:0] = 000		2 mA (Lv) 6 mA (Hv)	A, B	0	DV _{DDRTC}
	USB1.SE0	O	Reg9[2:0] = 100					
	RST_HOST_OUT	O	Reg9[2:0] = 101					
	CCP.CLKM	I	Reg9[2:0] = 110					
	GPIO55	I/O	Reg9[2:0] = 111					
P10	RTC_ON_NOFF	I	Reg8[20:18] = 000		2 mA (Lv) 6 mA (Hv)	A, B, G1	Z	DV _{DDRTC}
	CCP.CLKP	I	Reg8[20:18] = 110					
T11	CLK32K_IN	I	RegA[17:15] = 000			A	Input	DV _{DDRTC}
N8	PWRON_RESET	I	NA			A	Input	DV _{DDRTC}
P9	MMC.DAT3	I/O	Reg10[17:15] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G1	Z	DV _{DD6}
	MPUIO9	I/O	Reg10[17:15] = 001					
	MPUIO6	I/O	Reg10[17:15] = 010					
	CFLASH.CD1	I	Reg10[17:15] = 011					
	SSI.ACFLAG	O	Reg10[17:15] = 110					
M8	MMC.CLK	O	RegA[23:21] = 000	PD100, PU20	4 mA (Lv) 8 mA (Hv)	A, F, G1	0	DV _{DD6}
	SSI.CARDY	I	RegA[23:21] = 101					
	GPIO57	I/O	RegA[23:21] = 110					
R8	MMC.DAT0/SPI.DI	I/O	RegB[2:0] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G1	Z	DV _{DD6}
	Z_STATE	Z	RegB[2:0] = 001					
	CFLASH.IOIS16	I	RegB[2:0] = 011					
	SSI.ACRDY	O	RegB[2:0] = 110					
	GPIO58	I/O	RegB[2:0] = 111					
T9	MMC.DAT2	I/O	RegA[20:18] = 000	PD100, PU20	4 mA (Lv) 8 mA (Hv)	A, F, G1	Z	DV _{DD6}
	Z_STATE	Z	RegA[20:18] = 001					
	MPUIO11	I/O	RegA[20:18] = 010					
	CFLASH.RFSFT	O	RegA[20:18] = 011					
	SSI.CAFLAG	I	RegA[20:18] = 110					
U9	MMC.DAT1	I/O	RegA[26:24] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G1	Z	DV _{DD6}
	MPUIO10	I/O	RegA[26:24] = 001					
	MPUIO7	I/O	RegA[26:24] = 010					
	CFLASH.IRFQ	I	RegA[26:24] = 011					
	SSI.ACDATA	O	RegA[26:24] = 110					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20- μ A internal pulldown, PD100=100- μ A internal pulldown, PU20 = 20- μ A internal pullup, PU100 = 100- μ A internal pullup

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output

B = SUBLVDS input/output

C = USB transceiver input/output

D = I²C input/output buffers

E = Analog oscillator terminals

F = Boundary-scannable terminal

K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

NOTES: 3. NA denotes no multiplexing on the ball

4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2–3. ZDY Package Terminal Characteristics (Continued)

ZDY BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING	PULLUP/PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
N7	MMC.CMD/SPI.DO	I/O	RegA[29:27] = 000	PD100, PU20	4 mA (Lv) 8 mA (Hv)	A, F, G1	Z	DV _{DD6}
	CFLASH.CD2	I	RegA[29:27] = 011					
	SSI.CADATA	I	RegA[29:27] = 110					
	GPIO55	I/O	RegA[29:27] = 111					
P8	MCSI2.CLK	I/O	RegB[5:3] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F	LZ	DV _{DD3}
	USB2.SUSP	O	RegB[5:3] = 001					
	USB0.SUSP	O	RegB[5:3] = 101					
	MMC2.CLK	O	RegB[5:3] = 110					
	GPIO27	I/O	RegB[5:3] = 111					
R7	MCSI2.DIN	I	RegB[8:6] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F	LZ	DV _{DD3}
	USB2.VP	I	RegB[8:6] = 001					
	USB0.VP	I	RegB[8:6] = 101					
	GPIO26	I/O	RegB[8:6] = 111					
T8	MCSI2.DOUT	O	RegB[11:9] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G2	0	DV _{DD3}
	USB2.TXEN	O	RegB[11:9] = 001					
	USB0.TXEN	O	RegB[11:9] = 101					
	Z_STATE	Z	RegB[11:9] = 110					
	GPIO25	I/O	RegB[11:9] = 111					
U8	MCSI2.SYNC	I/O	RegB[14:12] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F	LZ	DV _{DD3}
	GPIO7	I/O	RegB[14:12] = 001					
	USB2.SPEED	O	RegB[14:12] = 010					
	USB0.SPEED	O	RegB[14:12] = 110					
	MMC2.CMDDIR	O	RegB[14:12] = 111					
T7	MCLKREQ	I	RegB[20:18] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F	LZ	DV _{DD3}
	EXT_MASTER_REQ	O	RegB[20:18] = 001					
	UART2.RX	I	RegB[20:18] = 010					
	MMC2.DAT3	I/O	RegB[20:18] = 110					
	GPIO23	I/O	RegB[20:18] = 111					
U7	GPIO9	I/O	RegB[23:21] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G3	LZ	DV _{DD3}
	EMU0	I/O	RegB[23:21] = 011					
	MCSI1.SYNC	I/O	RegB[23:21] = 100					
	MMC2.DAT0/SPI.DI	I/O	RegB[23:21] = 110					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20- μ A internal pulldown, PD100=100- μ A internal pulldown, PU20 = 20- μ A internal pullup, PU100 = 100- μ A internal pullup

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output

B = SUBLVDS input/output

C = USB transceiver input/output

D = I²C input/output buffers

E = Analog oscillator terminals

F = Boundary-scannable terminal

K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

NOTES: 3. NA denotes no multiplexing on the ball

4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2–3. ZDY Package Terminal Characteristics (Continued)

ZDY BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING	PULLUP/PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
P7	GPIO8	I/O	RegB[26:24] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G3	LZ	DV _{DD3}
	TRST	I	RegB[26:24] = 011					
	MCSI1.DOUT	O	RegB[26:24] = 100					
	MMC2.CMD/SPI.DO	I/O	RegB[26:24] = 110					
R6	MPUIO3	I/O	RegB[29:27] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G1	LZ	DV _{DD3}
	MMC2.DAT1	I/O	RegB[29:27] = 110					
L8	MCBSP2.DR	I	RegC[2:0] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G2	LZ	DV _{DD3}
	MCBSP2.DX	O	RegC[2:0] = 001					
	MCBSP2.DXZ	O/Z	RegC[2:0] = 010					
	GPIO22	I/O	RegC[2:0] = 111					
N6	MCBSP2.FSX	I/O	RegC[5:3] = 000	PU20, PD20	4 mA (Lv) 11 mA (Hv)	A, F, G2	LZ	DV _{DD3}
	VLYNQ.RX1	I	RegC[5:3] = 011					
	GPIO21	I/O	RegC[5:3] = 111					
U6	MCBSP2.CLKR	I/O	RegC[8:6] = 000	PU20, PD20	4 mA (Lv) 11 mA (Hv)	A, F	Z	DV _{DD3}
	GPIO11	I/O	RegC[8:6] = 001					
	VLYNQ.CLK	I/O	RegC[8:6] = 011					
U5	MCBSP2.CLKX	I/O	RegC[11:9] = 000	PU20, PD20	4 mA (Lv) 11 mA (Hv)	A, F, G2	LZ	DV _{DD3}
	VLYNQ.TX1	O	RegC[11:9] = 011					
	GPIO20	I/O	RegC[11:9] = 111					
R5	MCBSP2.FSR	I/O	RegC[14:12] = 000	PU20, PD20	4 mA (Lv) 11 mA (Hv)	A, F	Z	DV _{DD3}
	GPIO12	I/O	RegC[14:12] = 001					
	VLYNQ.RX0	I	RegC[14:12] = 011					
T5	MCBSP2.DX	O	RegC[17:15] = 000	PU20, PD20	4 mA (Lv) 11 mA (Hv)	A, F, G2	0	DV _{DD3}
	MCBSP2.DR	I	RegC[17:15] = 001					
	MCBSP2.DXZ	O/Z	RegC[17:15] = 010					
	VLYNQ.TX0	O	RegC[17:15] = 011					
	GPIO19	I/O	RegC[17:15] = 111					
U4	UART2.RX	I	RegC[20:18] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F	LZ	DV _{DD3}
	USB2.VM	I	RegC[20:18] = 001					
	USB0.VM	I	RegC[20:18] = 101					
	GPIO18	I/O	RegC[20:18] = 111					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20- μ A internal pulldown, PD100=100- μ A internal pulldown, PU20 = 20- μ A internal pullup, PU100 = 100- μ A internal pullup

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVC MOS input/output

B = SUBLVDS input/output

C = USB transceiver input/output

D = I²C input/output buffers

E = Analog oscillator terminals

F = Boundary-scannable terminal

K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

NOTES: 3. NA denotes no multiplexing on the ball

4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2–3. ZDY Package Terminal Characteristics (Continued)

ZDY BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING	PULLUP/PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
P6	UART2.CTS	I	RegC[23:21] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F	LZ	DV _{DD3}
	USB2.RCV	I	RegC[23:21] = 001					
	GPIO7	I/O	RegC[23:21] = 010					
	USB0.RCV	I	RegC[23:21] = 101					
T4	LOW_STATE	O	RegC[26:24] = 000		4 mA (Lv) 8 mA (Hv)	A, F, G2	0	DV _{DD3}
	UART2.RTS	O	RegC[26:24] = 001					
	USB2.SE0	O	RegC[26:24] = 010					
	MPUIO5	I/O	RegC[26:24] = 011					
	MPUIO12	I/O	RegC[26:24] = 100					
	USB0.SE0	O	RegC[26:24] = 101					
	LOW_STATE	O	RegC[26:24] = 110					
R4	LOW_STATE	O	RegC[29:27] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G2	0	DV _{DD3}
	UART2.TX	O	RegC[29:27] = 001					
	USB2.TXD	O	RegC[29:27] = 010					
	USB0.TXD	O	RegC[29:27] = 101					
	Z_STATE	Z	RegC[29:27] = 110					
	GPIO17	I/O	RegC[29:27] = 111					
P5	UART2.BCLK	O	RegD[2:0] = 000		4 mA (Lv) 8 mA (Hv)	A, F, G2	0	DV _{DD3}
	SYS_CLK_IN	I	RegD[2:0] = 110					
U3	MCLK	O	RegB[17:15] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G1	0	DV _{DD3}
	MMC2.DATDIR0	O	RegB[17:15] = 110					
	GPIO24	I/O	RegB[17:15] = 111					
P4	USB.PUEN	O	RegD[5:3] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G1	1	DV _{DD2}
	USB.CLKO	O	RegD[5:3] = 001					
	USB.PUDIS	O	RegD[5:3] = 011					
	Z_STATE	Z	RegD[5:3] = 100					
	LOW_POWER	O	RegD[5:3] = 110					
	GPIO58	I/O	RegD[5:3] = 111					
T2	USB.DP	I/O	USBTCTL[6:4] = 000		18.3 mA (in USB mode)	C	Z	DV _{DD2}
	I2C.SDA	I/O/Z	USBTCTL[6:4] = 100					
	UART1.RX	I	USBTCTL[6:4] = 101					
	USB.PUEN	O	USBTCTL[6:4] = 111					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20- μ A internal pulldown, PD100=100- μ A internal pulldown, PU20 = 20- μ A internal pullup, PU100 = 100- μ A internal pullup

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

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Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

NOTES: 3. NA denotes no multiplexing on the ball

4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

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Table 2–3. ZDY Package Terminal Characteristics (Continued)

ZDY BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING	PULLUP/PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
U1	USB.DM I2C.SCL UART1.TX Z_STATE	I/O I/O/Z O Z	USBTCTL[6:4] = 100 USBTCTL[6:4] = 101 USBTCTL[6:4] = 111		18.3 mA (in USB mode)	C	Z	DV _{DD2}
R2	OSC1_IN	I	NA			E	NA	NA
P2	OSC1_OUT	O	NA			E	NA	NA
T1	FLASH.CS1U GPIO16	O I/O	RegA[2:0] = 000 RegA[2:0] = 111		4 mA (Lv) 8 mA (Hv)	A, F	1	DV _{DD5}
R3	FLASH.WP	O	NA		4 mA (Lv) 8 mA (Hv)	A	0	DV _{DD5}
P3	FLASH.WE	O	NA		4 mA (Lv) 8 mA (Hv)	A	1	DV _{DD5}
N3	FLASH.RP FLASH.CS2UWE	O O	RegF[23:21] = 000 RegF[23:21] = 001		4 mA (Lv) 8 mA (Hv)	A	0	DV _{DD5}
M5	FLASH.OE	O	NA		4 mA (Lv) 8 mA (Hv)	A	1	DV _{DD5}
F3 J4 J2 H2 H5 F4 H4 C1 G6	FLASH.A[25:17]	O	NA		4 mA (Lv) 8 mA (Hv)	A, G1	0	DV _{DD5}
G5	FLASH.A[16]	O	Reg11[5:3] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, G1	0	DV _{DD5}
G2	FLASH.A[15]	O	Reg11[8:6] = 000		3 mA (Lv) 8 mA (Hv)	A, G1	0	DV _{DD5}
G4	FLASH.A[14]	O	Reg11[11:9] = 000		4 mA (Lv) 8 mA (Hv)	A, G1	0	DV _{DD5}
G3	FLASH.A[13]	O	Reg11[14:12] = 000		3 mA (Lv) 8 mA (Hv)	A, G1	1	DV _{DD5}
F5	FLASH.A[12]	O	Reg11[17:15] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, G1	0	DV _{DD5}
F1	FLASH.A[11]	O	Reg11[20:18] = 000		3 mA (Lv) 8 mA (Hv)	A, G1	0	DV _{DD5}

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20- μ A internal pulldown, PD100=100- μ A internal pulldown, PU20 = 20- μ A internal pullup, PU100 = 100- μ A internal pullup

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output

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K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

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NOTES: 3. NA denotes no multiplexing on the ball

4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2–3. ZDY Package Terminal Characteristics (Continued)

ZDY BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING	PULLUP/PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
F2	FLASH.A[10]	O	Reg11[23:21] = 000		3 mA (Lv) 8 mA (Hv)	A, G1	0	DV _{DD5}
E1	FLASH.A[9]	O	Reg11[26:24] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, G1	0	DV _{DD5}
D1	FLASH.A[8]	O	Reg12[5:3] = 000		4 mA (Lv) 8 mA (Hv)	A, G1	0	DV _{DD5}
E2	FLASH.A[7]	O	Reg12[8:6] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, G1	0	DV _{DD5}
C1	FLASH.A[6]	O	Reg12[11:9] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, G1	0	DV _{DD5}
D2	FLASH.A[5]	O	Reg12[14:12] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, G1	0	DV _{DD5}
E3	FLASH.A[4]	O	Reg12[17:15] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, G1	0	DV _{DD5}
E4	FLASH.A[3]	O	Reg12[20:18] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, G1	0	DV _{DD5}
C2	FLASH.A[2]	O	Reg12[23:21] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, G1	0	DV _{DD5}
D3	FLASH.A[1]	O	Reg12[26:24] = 000		3 mA (Lv) 8 mA (Hv)	A, G1	0	DV _{DD5}
N4 R1 P1 K7 M3 M4 N2 L5 N1 K6 L4 M2 J7 L2 M1 L1	FLASH.D[15:0]	I/O	NA		3 mA (Lv) 6 mA (Hv)	A, K	0	DV _{DD5}
K1	FLASH.CLK FLASH.GS2UOE	O O	Reg10[23:21] = 000 Reg10[23:21] = 001		3 mA (Lv) 6 mA (Hv)	A, K, G1	0	DV _{DD5}
L6	FLASH.RDY GPIO10	I I/O	RegF[29:27] = 000 RegF[29:27] = 001	PU100, PD20	4 mA (Lv) 8 mA (Hv)	A, F	Input	DV _{DD5}
H6	FLASH.ADV	O	NA		4 mA (Lv) 8 mA (Hv)	A	1	DV _{DD5}

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20- μ A internal pulldown, PD100=100- μ A internal pulldown, PU20 = 20- μ A internal pullup, PU100 = 100- μ A internal pullup

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output

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K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

NOTES: 3. NA denotes no multiplexing on the ball

4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

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Table 2–3. ZDY Package Terminal Characteristics (Continued)

ZDY BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING	PULLUP/PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
J8	FLASH.CS2	O	RegD[8:6] = 000		4 mA (Lv) 8 mA (Hv)	A	1	DV _{DD5}
	FLASH.BAA	O	RegD[8:6] = 000					
	FLASH.CS2L	O	RegD[8:6] = 000					
J5	GPIO62	I/O	Reg10[2:0] = 000		4 mA (Lv) 8 mA (Hv)	A, F, G1	Input	DV _{DD5}
	FLASH.CS0	O	Reg10[2:0] = 001					
J3	FLASH.CS1	O	Reg10[29:27] = 000		4 mA (Lv) 8 mA (Hv)	A	1	DV _{DD5}
	FLASH.CS1L	O	Reg10[29:27] = 001					
K3	FLASH.CS2U	O	Reg10[20:18] = 000		4 mA (Lv) 8 mA (Hv)	A, F	1	DV _{DD5}
	GPIO5	I/O	Reg10[20:18] = 001					
J1	FLASH.BE[0]	O	Reg10[8:6] = 000		4 mA (Lv) 8 mA (Hv)	A, F	0	DV _{DD5}
	FLASH.CS2UOE	O	Reg10[8:6] = 001					
	GPIO59	I/O	Reg10[8:6] = 111					
K2	FLASH.BE[1]	O	Reg10[5:3] = 000		4 mA (Lv) 8 mA (Hv)	A, F	0	DV _{DD5}
	FLASH.CS2UWE	O	Reg10[5:3] = 001					
	GPIO60	I/O	Reg10[5:3] = 111					
J6	FLASH.CS3	O	Reg10[26:24] = 000		4 mA (Lv) 8 mA (Hv)	A, F	1	DV _{DD5}
	GPIO3	I/O	Reg10[26:24] = 111					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20- μ A internal pulldown, PD100=100- μ A internal pulldown, PU20 = 20- μ A internal pullup, PU100 = 100- μ A internal pullup

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output

B = SUBLVDS input/output

C = USB transceiver input/output

D = I²C input/output buffers

E = Analog oscillator terminals

F = Boundary-scannable terminal

K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

NOTES: 3. NA denotes no multiplexing on the ball

4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

G1 = Terminal may be gated by BFAIL

G2 = Terminal may be gated by GPIO9 and MPUIO3

G3 = Terminal may be gated by BFAIL and OMAP5912 Internal Reset

H1 = Terminal may be 3-stated by BFAIL input

H3 = MCS11.DOUT pin can be forced into a high-impedance

state by the OMAP5912 HIGH_IMP3 control bit

Table 2–4. ZZG Package Terminal Characteristics

ZZG BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING	PULLUP/PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
G8	SDRAM.CS	O	NA		3 mA (Lv) 8 mA (Hv)	A	1	DV _{DD4}
C14	SDRAM.DQSH	I/O	NA		3 mA (Lv) 6 mA (Hv)	A, K	0	DV _{DD4}
D4	SDRAM.DQSL	I/O	NA		3 mA (Lv) 6 mA (Hv)	A, K	0	DV _{DD4}
B4	SDRAM.CAS	O	NA		3 mA (Lv) 8 mA (Hv)	A	1	DV _{DD4}
H7	SDRAM.RAS	O	NA		3 mA (Lv) 8 mA (Hv)	A	1	DV _{DD4}
C8	SDRAM.DQML	O	NA		3 mA (Lv) 6 mA (Hv)	A, K	0	DV _{DD4}
D10	SDRAM.DQMU	O	NA		3 mA (Lv) 6 mA (Hv)	A, K	0	DV _{DD4}
H8	SDRAM.WE	O	NA		3 mA (Lv) 8 mA (Hv)	A	1	DV _{DD4}
H11 H9 H10 B8 B12 G9 G11 G12 B9 G10 A1 B6 B2 A2	SDRAM.A[13:0]	O	NA		3 mA (Lv) 8 mA (Hv)	A	0	DV _{DD4}
C3 B3	SDRAM.BA[1:0]	O	NA		3 mA (Lv) 8 mA (Hv)	A	0	DV _{DD4}
C12 D12 D13 C11 C13 D11 D14 C10 D8 C4 C7 D5 D7 C5 C6 D6	SDRAM.D[15:0]	I/O	NA		3 mA (Lv) 6 mA (Hv)	A, K	0	DV _{DD4}

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20- μ A internal pulldown, PD100=100- μ A internal pulldown, PU20 = 20- μ A internal pullup, PU100 = 100- μ A internal pullup

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output

B = SUBLVDS input/output

C = USB transceiver input/output

D = I²C input/output buffers

E = Analog oscillator terminals

F = Boundary-scannable terminal

K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

NOTES: 3. NA denotes no multiplexing on the ball

4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

G1 = Terminal may be gated by BFAIL

G2 = Terminal may be gated by GPIO9 and MPUIO3

G3 = Terminal may be gated by BFAIL and OMAP5912 Internal Reset

H1 = Terminal may be 3-stated by BFAIL input

H3 = MCS11.DOUT pin can be forced into a high-impedance

state by the OMAP5912 HIGH_IMP3 control bit

Table 2–4. ZZG Package Terminal Characteristics (Continued)

ZZG BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING	PULLUP/PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
C9	SDRAM.CLK	O	NA		3 mA (Lv) 6 mA (Hv)	A, K	U	DV _{DD4}
D9	SDRAM.CLKX	O	NA		3 mA (Lv) 6 mA (Hv)	A, K	0	DV _{DD4}
H12	SDRAM.CKE	O	NA		3 mA (Lv) 8 mA (Hv)	A	1	DV _{DD4}
B15	LCD.AC	O	RegD[11:9] = 000		2 mA (Lv) 6 mA (Hv)	A, F, G1	0	DV _{DD1}
	SYS_CLK_OUT	O	RegD[11:9] = 001					
	Z_STATE	Z	RegD[11:9] = 010					
	SOSSI.CMD	O	RegD[11:9] = 110					
C15	LCD.PCLK	O	RegD[17:15] = 000		2 mA (Lv) 6 mA (Hv)	A, F, G1	0	DV _{DD1}
	Z_STATE	Z	RegD[17:15] = 001					
	SOSSI.WR	O	RegD[17:15] = 110					
D15	LCD.P[15]	O	RegD[20:18] = 000	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F, G1	0	DV _{DD1}
	Z_STATE	Z	RegD[20:18] = 001					
	SOSSI.D[15]	I/O	RegD[20:18] = 110					
	GPIO2	I/O	RegD[20:18] = 111					
C16	LCD.P[14]	O	RegD[23:21] = 000	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F, G1	0	DV _{DD1}
	Z_STATE	Z	RegD[23:21] = 001					
	SOSSI.D[14]	I/O	RegD[23:21] = 110					
	GPIO35	I/O	RegD[23:21] = 111					
A17	LCD.P[13]	O	RegD[26:24] = 000	PU20, PD20	2 mA (Lv) 6 mA (Hv)	F, A, G1	0	DV _{DD1}
	Z_STATE	Z	RegD[26:24] = 001					
	SOSSI.D[13]	I/O	RegD[26:24] = 110					
	GPIO34	I/O	RegD[26:24] = 111					
G13	LCD.P[12]	O	RegD[29:27] = 000	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F, G1	0	DV _{DD1}
	Z_STATE	Z	RegD[29:27] = 001					
	SOSSI.D[12]	I/O	RegD[29:27] = 110					
	GPIO33	I/O	RegD[29:27] = 111					
B17	LCD.P[11]	O	RegE[2:0] = 000	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F, G1	0	DV _{DD1}
	Z_STATE	Z	RegE[2:0] = 001					
	SOSSI.D[11]	I/O	RegE[2:0] = 110					
	GPIO32	I/O	RegE[2:0] = 111					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20- μ A internal pulldown, PD100=100- μ A internal pulldown, PU20 = 20- μ A internal pullup, PU100 = 100- μ A internal pullup

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output

B = SUBLVDS input/output

C = USB transceiver input/output

D = I²C input/output buffers

E = Analog oscillator terminals

F = Boundary-scannable terminal

K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

NOTES: 3. NA denotes no multiplexing on the ball

4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

G1 = Terminal may be gated by BFAIL

G2 = Terminal may be gated by GPIO9 and MPUIO3

G3 = Terminal may be gated by BFAIL and OMAP5912 Internal Reset

H1 = Terminal may be 3-stated by BFAIL input

H3 = MCS11.DOUT pin can be forced into a high-impedance

state by the OMAP5912 HIGH_IMP3 control bit

Table 2–4. ZZG Package Terminal Characteristics (Continued)

ZZG BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING	PULLUP/PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
C17	LCD.P[10]	O	RegE[5:3] = 000	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F, G1	0	DV _{DD1}
	Z_STATE	Z	RegE[5:3] = 001					
	SOSSI.D[10]	I/O	RegE[5:3] = 110					
	GPIO31	I/O	RegE[5:3] = 111					
D16	LCD.P[9]	O	RegE[8:6] = 000	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F, G1	0	DV _{DD1}
	Z_STATE	Z	RegE[8:6] = 001					
	SOSSI.D[9]	I/O	RegE[8:6] = 110					
	GPIO30	I/O	RegE[8:6] = 111					
B18	LCD.VS	O	RegE[11:9] = 000		2 mA (Lv) 6 mA (Hv)	A, F, G1	0	DV _{DD1}
	Z_STATE	Z	RegE[11:9] = 001					
	SOSSI.RD	O	RegE[11:9] = 110					
D17	LCD.P[8]	O	RegE[14:12] = 000	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F, G1	0	DV _{DD1}
	Z_STATE	Z	RegE[14:12] = 001					
	SOSSI.D[8]	I/O	RegE[14:12] = 110					
	GPIO29	I/O	RegE[14:12] = 111					
C18	LCD.P[7]	O	RegE[17:15] = 000	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F, G1	0	DV _{DD1}
	Z_STATE	Z	RegE[17:15] = 001					
	SOSSI.D[7]	I/O	RegE[17:15] = 110					
B19	LCD.P[6]	O	RegE[20:18] = 000	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F, G1	0	DV _{DD1}
	Z_STATE	Z	RegE[20:18] = 001					
	SOSSI.D[6]	I/O	RegE[20:18] = 110					
A20	LCD.P[5]	O	RegE[23:21] = 000	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F, G1	0	DV _{DD1}
	Z_STATE	Z	RegE[23:21] = 001					
	SOSSI.D[5]	I/O	RegE[23:21] = 110					
H13	LCD.P[4]	O	RegE[26:24] = 000	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F, G1	0	DV _{DD1}
	Z_STATE	Z	RegE[26:24] = 001					
	SOSSI.D[4]	I/O	RegE[26:24] = 110					
G14	LCD.P[3]	O	RegE[29:27] = 000	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F, G1	0	DV _{DD1}
	Z_STATE	Z	RegE[29:27] = 001					
	SOSSI.D[3]	I/O	RegE[29:27] = 110					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20- μ A internal pulldown, PD100=100- μ A internal pulldown, PU20 = 20- μ A internal pullup, PU100 = 100- μ A internal pullup

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output

B = SUBLVDS input/output

C = USB transceiver input/output

D = I²C input/output buffers

E = Analog oscillator terminals

F = Boundary-scannable terminal

K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

NOTES: 3. NA denotes no multiplexing on the ball

4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2–4. ZZG Package Terminal Characteristics (Continued)

ZZG BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING	PULLUP/PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
C19	LCD.P[2]	O	RegF[2:0] = 000	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F, G1	0	DV _{DD1}
	Z_STATE	Z	RegF[2:0] = 001					
	SOSSI.D[2]	I/O	RegF[2:0] = 110					
B21	LCD.P[1]	O	RegF[5:3] = 000	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F, G1	0	DV _{DD1}
	Z_STATE	Z	RegF[5:3] = 001					
	SOSSI.D[1]	I/O	RegF[5:3] = 110					
D18	LCD.P[0]	O	RegF[8:6] = 000	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F, G1	0	DV _{DD1}
	Z_STATE	Z	RegF[8:6] = 001					
	SOSSI.D[0]	I/O	RegF[8:6] = 110					
C20	LCD.HS	O	RegD[14:12] = 000		4 mA (Lv) 8 mA (Hv)	A, F, G1	0	DV _{DD1}
	Z_STATE	Z	RegD[14:12] = 001					
	SOSSI.CS	O	RegD[14:12] = 110					
C21	KB.C[4]	O	Reg3[5:3] = 000	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F	0	DV _{DD1}
	GPIO27	I/O	Reg3[5:3] = 111					
E18	KB.C[3]	O	Reg3[8:6] = 000	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F	0	DV _{DD1}
	GPIO63	I/O	Reg3[8:6] = 111					
D19	KB.C[2]	O	Reg3[11:9] = 000	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F	0	DV _{DD1}
	GPIO61	I/O	Reg3[11:9] = 111					
D20	KB.C[1]	O	Reg3[14:12] = 000	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F	0	DV _{DD1}
	MPUIO6	I/O	Reg3[14:12] = 001					
F18	KB.C[0]	O	Reg3[17:15] = 000	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F	0	DV _{DD1}
	MPUIO0	I/O	Reg3[17:15] = 001					
E19	KB.R[4]	I	Reg3[20:18] = 000	PU100, PD20	4 mA (Lv) 11 mA (Hv)	A, F	Z	DV _{DD1}
	MPUIO15	I/O	Reg3[20:18] = 001					
	VLYNQ.TX1	O	Reg3[20:18] = 010					
E20	KB.R[3]	I	Reg3[23:21] = 000	PU100, PD20	4 mA (Lv) 11 mA (Hv)	A, F	Z	DV _{DD1}
	MPUIO13	I/O	Reg3[23:21] = 001					
	VLYNQ.TX0	O	Reg3[23:21] = 010					
H14	KB.R[2]	I	Reg3[26:24] = 000	PU100, PD20	4 mA (Lv) 11 mA (Hv)	A, F	Z	DV _{DD1}
	MPUIO10	I/O	Reg3[26:24] = 001					
	VLYNQ.CLK	I/O	Reg3[26:24] = 010					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20- μ A internal pulldown, PD100=100- μ A internal pulldown, PU20 = 20- μ A internal pullup, PU100 = 100- μ A internal pullup

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVC MOS input/output

B = SUBLVDS input/output

C = USB transceiver input/output

D = I²C input/output buffers

E = Analog oscillator terminals

F = Boundary-scannable terminal

K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

NOTES: 3. NA denotes no multiplexing on the ball

4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2–4. ZZG Package Terminal Characteristics (Continued)

ZZG BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING	PULLUP/PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
F19	KB.R[1] MPUIO9 VLYNQ.RX0	I I/O I	Reg3[29:27] = 000 Reg3[29:27] = 001 Reg3[29:27] = 010	PU100, PD20	4 mA (Lv) 11 mA (Hv)	A, F	Z	DV _{DD1}
G18	KB.R[0] MPUIO8 VLYNQ.RX1	I I/O I	Reg4[2:0] = 000 Reg4[2:0] = 001 Reg4[2:0] = 010	PU100, PD20	4 mA (Lv) 11 mA (Hv)	A, F	Z	DV _{DD1}
G19	KB.C[5] GPIO28	O I/O	Reg3[2:0] = 000 Reg3[2:0] = 111	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F	0	DV _{DD1}
G20	MCBSP1.CLKS SOSSI.TE GPIO62	I I I/O	Reg4[8:6] = 000 Reg4[8:6] = 110 Reg4[8:6] = 111	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F	–	DV _{DD1}
G21	MCBSP1.CLKX GPIO54	I/O I/O	Reg4[11:9] = 000 Reg4[11:9] = 111	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G1	Z	DV _{DD1}
H15	MCBSP1.FSX MCBSP1.DX MCBSP1.DXZ GPIO53	I/O O O/Z I/O	Reg4[14:12] = 000 Reg4[14:12] = 001 Reg4[14:12] = 010 Reg4[14:12] = 111	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F, G1	Z	DV _{DD1}
H18	MCBSP1.DX MCBSP1.ESX MCBSP1.DXZ GPIO52	O I/O O/Z I/O	Reg4[17:15] = 000 Reg4[17:15] = 001 Reg4[17:15] = 010 Reg4[17:15] = 111	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F, G1	0	DV _{DD1}
H20	MCBSP1.DR GPIO51	I I/O	Reg4[20:18] = 000 Reg4[20:18] = 111	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F	LZ	DV _{DD1}
H19	CAM.EXCLK ETM.SYNC[0] UWIRE.SDO LOW_STATE GPIO57	O O O O I/O	Reg4[23:21] = 000 Reg4[23:21] = 001 Reg4[23:21] = 010 Reg4[23:21] = 110 Reg4[23:21] = 111	PU20, PD20	4 mA (Lv) 11 mA (Hv)	A, F, G1	0	DV _{DD8}
J15	CAM.LCLK ETM.CLK UWIRE.SCLK GPIO39	I O O I/O	Reg4[26:24] = 000 Reg4[26:24] = 001 Reg4[26:24] = 010 Reg4[26:24] = 111	PU20, PD20	4 mA (Lv) 11 mA (Hv)	A, F	Z	DV _{DD8}

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20- μ A internal pulldown, PD100=100- μ A internal pulldown, PU20 = 20- μ A internal pullup, PU100 = 100- μ A internal pullup

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D = I²C input/output buffers

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K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

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NOTES: 3. NA denotes no multiplexing on the ball

4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2–4. ZZG Package Terminal Characteristics (Continued)

ZZG BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING	PULLUP/PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
J20	MPU_BOOT USB1.SUSP	I O	Reg8[29:27] = 000 Reg8[29:27] = 010		2 mA (Lv) 6 mA (Hv)	A, F	–	
J18	CAM.D[7] ETM.D[7] UWIRE.CS0 MMC2.DAT2 GPIO35	I O O I/O I/O	Reg4[29:27] = 000 Reg4[29:27] = 001 Reg4[29:27] = 010 Reg4[29:27] = 011 Reg4[29:27] = 111	PU20, PD20	4 mA (Lv) 11 mA (Hv)	A, F	Z	DV _{DD8}
J19	CAM.D[6] ETM.D[6] UWIRE.CS3 MMC2.CMD/SPI.DO GPIO34	I O O I/O I/O	Reg5[2:0] = 000 Reg5[2:0] = 001 Reg5[2:0] = 010 Reg5[2:0] = 011 Reg5[2:0] = 111	PU20, PD20	4 mA (Lv) 11 mA (Hv)	A, F	Z	DV _{DD8}
J14	CAM.D[5] ETM.D[5] UWIRE.SDI GPIO33	I O I I/O	Reg5[5:3] = 000 Reg5[5:3] = 001 Reg5[5:3] = 010 Reg5[5:3] = 111	PU20, PD20	4 mA (Lv) 11 mA (Hv)	A, F	Z	DV _{DD8}
K18	CAM.D[4] ETM.D[4] UART3.TX GPIO32	I O O I/O	Reg5[8:6] = 000 Reg5[8:6] = 001 Reg5[8:6] = 010 Reg5[8:6] = 111	PU20, PD20	4 mA (Lv) 11 mA (Hv)	A, F	Z	DV _{DD8}
K19	CAM.D[3] ETM.D[3] UART3.RX GPIO31	I O I I/O	Reg5[11:9] = 000 Reg5[11:9] = 001 Reg5[11:9] = 010 Reg5[11:9] = 111	PU20, PD20	4 mA (Lv) 11 mA (Hv)	A, F	Z	DV _{DD8}
K15	CAM.D[2] ETM.D[2] UART3.CTS GPIO30	I O I I/O	Reg5[14:12] = 000 Reg5[14:12] = 001 Reg5[14:12] = 010 Reg5[14:12] = 111	PU20, PD20	4 mA (Lv) 11 mA (Hv)	A, F	Z	DV _{DD8}
K14	CAM.D[1] ETM.D[1] UART3.RTS GPIO29	I O O I/O	Reg5[17:15] = 000 Reg5[17:15] = 001 Reg5[17:15] = 010 Reg5[17:15] = 111	PU20, PD20	4 mA (Lv) 11 mA (Hv)	A, F	Z	DV _{DD8}

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20- μ A internal pulldown, PD100=100- μ A internal pulldown, PU20 = 20- μ A internal pullup, PU100 = 100- μ A internal pullup

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output

B = SUBLVDS input/output

C = USB transceiver input/output

D = I²C input/output buffers

E = Analog oscillator terminals

F = Boundary-scannable terminal

K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

NOTES: 3. NA denotes no multiplexing on the ball

4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

G1 = Terminal may be gated by BFAIL

G2 = Terminal may be gated by GPIO9 and MPUIO3

G3 = Terminal may be gated by BFAIL and OMAP5912 Internal Reset

H1 = Terminal may be 3-stated by BFAIL input

H3 = MCS11.DOUT pin can be forced into a high-impedance

state by the OMAP5912 HIGH_IMP3 control bit

Table 2–4. ZZG Package Terminal Characteristics (Continued)

ZZG BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING	PULLUP/PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
L19	CAM.D[0]	I	Reg5[20:18] = 000	PU20, PD20	4 mA (Lv) 11 mA (Hv)	A, F	Z	DV _{DD8}
	ETM.D[0]	O	Reg5[20:18] = 001					
	MPUIO12	I/O	Reg5[20:18] = 010					
	MMC2.DAT3	I/O	Reg5[20:18] = 011					
L18	CAM.VS	I	Reg5[23:21] = 000	PU20, PD20	4 mA (Lv) 11 mA (Hv)	A, F	Z	DV _{DD8}
	ETM.PSTAT[2]	O	Reg5[23:21] = 001					
	MPUIO14	I/O	Reg5[23:21] = 010					
	MMC2.DAT1	I/O	Reg5[23:21] = 011					
L15	CAM.HS	I	Reg5[26:24] = 000	PU20, PD20	4 mA (Lv) 11 mA (Hv)	A, F	Z	DV _{DD8}
	ETM.PSTAT[1]	O	Reg5[26:24] = 001					
	UART2.CTS	I	Reg5[26:24] = 010					
	MMC2.DAT0/SPI.DI	I/O	Reg5[26:24] = 011					
	GPIO38	I/O	Reg5[26:24] = 111					
M19	CAM.RSTZ	O	Reg5[29:27] = 000	PU20, PD20	4 mA (Lv) 11 mA (Hv)	A, F, G1	0	DV _{DD8}
	ETM.PSTAT[0]	O	Reg5[29:27] = 001					
	UART2.RTS	O	Reg5[29:27] = 010					
	MMC2.CLK	O	Reg5[29:27] = 011					
	LOW_STATE	O	Reg5[29:27] = 110					
	GPIO37	I/O	Reg5[29:27] = 111					
	M18	LOW_STATE	O					
UART3.TX		O	Reg6[2:0] = 001					
PWT		O	Reg6[2:0] = 010					
UART2.TX		O	Reg6[2:0] = 100					
TIMER.PWM0		O	Reg6[2:0] = 110					
GPIO50		I/O	Reg6[2:0] = 111					
L14		UART3.RX	I	Reg6[5:3] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F	–
	PWL	O	Reg6[5:3] = 001					
	UART2.RX	I	Reg6[5:3] = 011					
	TIMER.PWM1	O	Reg6[5:3] = 100					
	GPIO49	I/O	Reg6[5:3] = 111					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20- μ A internal pulldown, PD100=100- μ A internal pulldown, PU20 = 20- μ A internal pullup, PU100 = 100- μ A internal pullup

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output

B = SUBLVDS input/output

C = USB transceiver input/output

D = I²C input/output buffers

E = Analog oscillator terminals

F = Boundary-scannable terminal

K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

NOTES: 3. NA denotes no multiplexing on the ball

4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2–4. ZZG Package Terminal Characteristics (Continued)

ZZG BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING	PULLUP/PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
M20	GPIO15	I/O	Reg6[8:6] = 000	PU100, PD20	4 mA (Lv) 11 mA (Hv)	A, F, G1	LZ	DV _{DD9}
	KB.R[7]	I	Reg6[8:6] = 001					
	TIMER.PWM2	O	Reg6[8:6] = 010					
	VLYNQ.TX1	O	Reg6[8:6] = 100					
N21	GPIO14	I/O	Reg6[11:9] = 000	PU100, PD20	4 mA (Lv) 11 mA (Hv)	A, F, G1	LZ	DV _{DD9}
	KB.R[6]	I	Reg6[11:9] = 001					
	LCD.RED0	O	Reg6[11:9] = 010					
	Z_STATE	Z	Reg6[11:9] = 011					
	VLYNQ.TX0	O	Reg6[11:9] = 100					
N19	GPIO13	I/O	Reg6[14:12] = 000	PU100, PD20	4 mA (Lv) 11 mA (Hv)	A, F, G1	LZ	DV _{DD9}
	KB.R[5]	I	Reg6[14:12] = 001					
	LCD.BLUE0	O	Reg6[14:12] = 010					
	Z_STATE	Z	Reg6[14:12] = 011					
	VLYNQ.CLK	I/O	Reg6[14:12] = 100					
N18	GPIO12	I/O	Reg6[17:15] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G1	LZ	DV _{DD9}
	MCBSP3.FSX	I/O	Reg6[17:15] = 001					
	TIMER.EXTCLK	I	Reg6[17:15] = 011					
	VLYNQ.RX0	I	Reg6[17:15] = 100					
N20	GPIO11	I/O	Reg6[20:18] = 000	PU20, PD20	4 mA (Lv) 11 mA (Hv)	A, F, G1	LZ	DV _{DD9}
	HDQ	I/O	Reg6[20:18] = 001					
	VLYNQ.RX1	I	Reg6[20:18] = 100					
	ETM.PSTAT[5]	O	Reg6[20:18] = 101					
M15	GPIO7	I/O	Reg6[23:21] = 000	PU20, PD20	4 mA (Lv) 11 mA (Hv)	A, F, G1	LZ	DV _{DD9}
	MMC.DAT2	I/O	Reg6[23:21] = 001					
	TCK	I	Reg6[23:21] = 011					
	MCSI1.CLK	I/O	Reg6[23:21] = 100					
	ETM.SYNC[1]	O	Reg6[23:21] = 101					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20- μ A internal pulldown, PD100=100- μ A internal pulldown, PU20 = 20- μ A internal pullup, PU100 = 100- μ A internal pullup

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output

B = SUBLVDS input/output

C = USB transceiver input/output

D = I²C input/output buffers

E = Analog oscillator terminals

F = Boundary-scannable terminal

K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

NOTES: 3. NA denotes no multiplexing on the ball

4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2–4. ZZG Package Terminal Characteristics (Continued)

ZZG BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING	PULLUP/PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
P19	GPIO6	I/O	Reg6[26:24] = 000	PD100, PU20	4 mA (Lv) 8 mA (Hv)	A, F, G1	LZ	DV _{DD9}
	SPI.CS1	O	Reg6[26:24] = 001					
	MCBSP3.ESX	I/O	Reg6[26:24] = 010					
	TIMER.EVENT3	I	Reg6[26:24] = 011					
	MCSI1.DIN	I	Reg6[26:24] = 100					
	TMS	I	Reg6[26:24] = 101					
P20	GPIO4	I/O	Reg6[29:27] = 000	PD100, PU20	4 mA (Lv) 8 mA (Hv)	A, F, G1	LZ	DV _{DD9}
	SPI.CS2	O	Reg6[29:27] = 001					
	MCBSP3.FSX	I/O	Reg6[29:27] = 010					
	TIMER.EVENT4	I	Reg6[29:27] = 011					
P18	GPIO3	I/O	Reg7[2:0] = 000	PU100, PD20	4 mA (Lv) 11 mA (Hv)	A, F, G1	LZ	DV _{DD9}
	SPI.CS3	O	Reg7[2:0] = 001					
	MCBSP3.FSX	I/O	Reg7[2:0] = 010					
	LED1	O	Reg7[2:0] = 011					
	ETM.PSTAT[3]	O	Reg7[2:0] = 101					
M14	GPIO2	I/O	Reg7[5:3] = 000	PU100, PD20	4 mA (Lv) 11 mA (Hv)	A, F, G1	LZ	DV _{DD9}
	SPI.CLK	O	Reg7[5:3] = 001					
	ETM.PSTAT[4]	O	Reg7[5:3] = 101					
R19	GPIO1	I/O	Reg7[8:6] = 000	PU100, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G1	LZ	DV _{DD9}
	UART3.RTS	O	Reg7[8:6] = 001					
R18	GPIO0	I/O	Reg7[11:9] = 000	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F, G1	LZ	DV _{DD9}
	SPI.RDY	I	Reg7[11:9] = 001					
	USB.VBUS	I	Reg7[11:9] = 010					
	SPIF.DOUT	O	Reg7[11:9] = 011					
	MMC2.CLKIN	I	Reg7[11:9] = 110					
T20	MPUIO5	I/O	Reg7[14:12] = 000	PU20, PD20	2 mA (Lv) 6 mA (Hv)	A, F	LZ	DV _{DD9}
	LOW_PWR	O	Reg7[14:12] = 001					
	UART3.RTS	O	Reg7[14:12] = 011					
	UART1.DTR	O	Reg7[14:12] = 100					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20- μ A internal pulldown, PD100=100- μ A internal pulldown, PU20 = 20- μ A internal pullup, PU100 = 100- μ A internal pullup

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output

B = SUBLVDS input/output

C = USB transceiver input/output

D = I²C input/output buffers

E = Analog oscillator terminals

F = Boundary-scannable terminal

K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

NOTES: 3. NA denotes no multiplexing on the ball

4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2–4. ZZG Package Terminal Characteristics (Continued)

ZZG BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING	PULLUP/PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
T19	MPUIO4	I/O	Reg7[17:15] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G1	LZ	DV _{DD9}
	EXT_DMA_REQ1	I	Reg7[17:15] = 001					
	LED2	O	Reg7[17:15] = 010					
	UWIRE_CS2	O	Reg7[17:15] = 011					
	SPIF_CS2	O	Reg7[17:15] = 100					
	MCBSP3.DR	I	Reg7[17:15] = 110					
N15	MPUIO2	I/O	Reg7[20:18] = 000	PU100, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G1	LZ	DV _{DD9}
	EXT_DMA_REQ0	I	Reg7[20:18] = 001					
	UWIRE_CS1	O	Reg7[20:18] = 010					
	SPIF_CS1	O	Reg7[20:18] = 110					
U20	MPU_RST	I	Reg9[8:6] = 000		2 mA (Lv) 6 mA (Hv)	A, F	–	DV _{DD9}
	MPUIO14	I/O	Reg9[8:6] = 110					
U19	MPUIO1	I/O	Reg7[23:21] = 000	PU100, PD20	4 mA (Lv) 8 mA (Hv)	A, F	Z	DV _{DD9}
	RTCK	I/O	Reg7[23:21] = 001					
	SPIF.SCK	I/O	Reg7[23:21] = 110					
T18	I2C.SCL	I/O/Z	Reg7[26:24] = 000		2 mA (Lv) 6 mA (Hv)	D	Z	DV _{DD9}
V20	I2C.SDA	I/O/Z	Reg7[29:27] = 000		2 mA (Lv) 6 mA (Hv)	D	Z	DV _{DD9}
	GPIO48	I	Reg7[29:27] = 111					
U18	UWIRE.SDI	I	Reg8[2:0] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F	LZ	DV _{DD9}
	UART3.DSR	O	Reg8[2:0] = 001					
	UART1.DSR	I	Reg8[2:0] = 010					
	MCBSP3.DR	I	Reg8[2:0] = 011					
	SPIF.DIN	I/O	Reg8[2:0] = 110					
	GPIO47	I/O	Reg8[2:0] = 111					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20- μ A internal pulldown, PD100=100- μ A internal pulldown, PU20 = 20- μ A internal pullup, PU100 = 100- μ A internal pullup

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output

B = SUBLVDS input/output

C = USB transceiver input/output

D = I²C input/output buffers

E = Analog oscillator terminals

F = Boundary-scannable terminal

K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

NOTES: 3. NA denotes no multiplexing on the ball

4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2–4. ZZG Package Terminal Characteristics (Continued)

ZZG BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING	PULLUP/PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
W21	UWIRE.SDO	O	Reg8[5:3] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G1	0	DV _{DD9}
	UART3.DTR	O	Reg8[5:3] = 001					
	UART1.DTR	O	Reg8[5:3] = 010					
	MCBSP3.DX	O	Reg8[5:3] = 011					
	UART3.RTS	O	Reg8[5:3] = 100					
	MCBSP3.DXZ	O/Z	Reg8[5:3] = 101					
	SPIF.DOUT	I/O	Reg8[5:3] = 110					
GPIO46	I/O	Reg8[5:3] = 111						
V19	UWIRE.SCLK	O	Reg8[8:6] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G1	0	DV _{DD9}
	KB.C[7]	O	Reg8[8:6] = 001					
	MPUIO1	I/O	Reg8[8:6] = 010					
	UART3.CTS	I	Reg8[8:6] = 100					
N14	Z_STATE	Z	Reg8[11:9] = 000	PU100, PD20	4 mA (Lv) 8 mA (Hv)	A, F	Z	DV _{DD9}
	UWIRE.CS0	O	Reg8[11:9] = 001					
	MCBSP3.CLKX	I/O	Reg8[11:9] = 010					
	UART3.TX	O	Reg8[11:9] = 100					
	SPIF.CS0	I/O	Reg8[11:9] = 110					
	GPIO45	I/O	Reg8[11:9] = 111					
P15	Z_STATE	Z	Reg8[14:12] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F	Z	DV _{DD9}
	UWIRE.CS3	O	Reg8[14:12] = 001					
	KB.C[6]	O	Reg8[14:12] = 010					
	SPIF.CS3	O	Reg8[14:12] = 011					
	UART3.RX	I	Reg8[14:12] = 100					
	Z_STATE	Z	Reg8[14:12] = 110					
	GPIO44	I/O	Reg8[14:12] = 111					
W19	BFAIL/EXT_FIQ	I	Reg8[17:15] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F	Z	DV _{DD9}
	UART3.CTS	I	Reg8[17:15] = 001					
	UART1.DSR	I	Reg8[17:15] = 010					
	MMC2.DATDIR1	O	Reg8[17:15] = 110					
AA20	RST_OUT	O	Reg9[11:9] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F	0	DV _{DD9}
	GPIO41	I/O	Reg9[11:9] = 111					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20- μ A internal pulldown, PD100=100- μ A internal pulldown, PU20 = 20- μ A internal pullup, PU100 = 100- μ A internal pullup

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output

B = SUBLVDS input/output

C = USB transceiver input/output

D = I²C input/output buffers

E = Analog oscillator terminals

F = Boundary-scannable terminal

K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

NOTES: 3. NA denotes no multiplexing on the ball

4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

G1 = Terminal may be gated by BFAIL

G2 = Terminal may be gated by GPIO9 and MPUIO3

G3 = Terminal may be gated by BFAIL and OMAP5912 Internal Reset

H1 = Terminal may be 3-stated by BFAIL input

H3 = MCS11.DOUT pin can be forced into a high-impedance

state by the OMAP5912 HIGH_IMP3 control bit

Table 2–4. ZZG Package Terminal Characteristics (Continued)

ZZG BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING	PULLUP/PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
V18	CONF	I	NA	PU20, PD20		A	LZ	DV _{DD9}
Y19	TDI	I	NA	PD100, PU20		A	LZ	DV _{DD9}
AA19	TDO VLYNQ.TX0	O TBD	NA TBD		4 mA (Lv) 8 mA (Hv)		–	DV _{DD9}
V17	TMS	I	NA	PD100, PU20		A	LZ	DV _{DD9}
W18	TCK	I	NA	PD100, PU20		A	LZ	DV _{DD9}
Y18	TRST	I	NA	PU20, PD20		A	–	DV _{DD9}
V16	EMU0	I/O	NA	PU100, PD20	4 mA (Lv) 8 mA (Hv)	A	Input	DV _{DD9}
W17	EMU1	I/O	NA	PU100, PD20	4 mA (Lv) 8 mA (Hv)	A	Input	DV _{DD9}
Y17	RTCK	I/O	NA		4 mA (Lv) 11 mA (Hv)	A	–	DV _{DD9}
AA17	MCSI1.SYNC MCBSP3.DR USB1.VP MCBSP3.FSX	I/O I I I/O	RegA[5:3] = 000 RegA[5:3] = 001 RegA[5:3] = 010 RegA[5:3] = 100	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G1	LZ	DV _{DD7}
P14	MCSI1.CLK MCBSP3.DX USB1.VM TDI MCBSP3.CLKX GPIO43	I/O O I I I/O I/O	RegA[8:6] = 000 RegA[5:3] = 001 RegA[5:3] = 010 RegA[5:3] = 011 RegA[5:3] = 100 RegA[5:3] = 111	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G1	LZ	DV _{DD7}
W16	Z_STATE MCBSP3.CLKX USB1.TXEN MCSI1.DIN Z_STATE GPIO42	Z I/O O I Z I/O	Reg9[5:3] = 000 Reg9[5:3] = 001 Reg9[5:3] = 010 Reg9[5:3] = 100 Reg9[5:3] = 110 Reg9[5:3] = 111	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G1	Z	DV _{DD7}

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20- μ A internal pulldown, PD100=100- μ A internal pulldown, PU20 = 20- μ A internal pullup, PU100 = 100- μ A internal pullup

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output

B = SUBLVDS input/output

C = USB transceiver input/output

D = I²C input/output buffers

E = Analog oscillator terminals

F = Boundary-scannable terminal

K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

NOTES: 3. NA denotes no multiplexing on the ball

4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2–4. ZZG Package Terminal Characteristics (Continued)

ZZG BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING	PULLUP/PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
V15	MCSI1.DIN	I	RegA[11:9] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F	Z	DV _{DD7}
	USB1.RCV	I	RegA[11:9] = 001					
	EMU1	I/O	RegA[11:9] = 011					
	MCBSP3.DR	I	RegA[11:9] = 100					
	SSI.ACWAKE	O	RegA[11:9] = 110					
	GPIO56	I/O	RegA[11:9] = 111					
W15	BCLKREQ	I	Reg9[29:27] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F	LZ	DV _{DD7}
	UART3.CTS	I	Reg9[29:27] = 001					
	MMC2.DAT2	I/O	Reg9[29:27] = 110					
	GPIO40	I/O	Reg9[29:27] = 111					
Y15	BCLK	O	RegA[2:0] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G1	0	DV _{DD7}
	UART3.RTS	O	RegA[2:0] = 001					
	CAM.OUTCLK	O	RegA[2:0] = 110					
	GPIO17	I/O	RegA[2:0] = 111					
AA15	LOW_STATE	O	Reg9[14:12] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G1	0	DV _{DD7}
	UART1.RTS	O	Reg9[14:12] = 001					
	UART1.IRSHDN	O	Reg9[14:12] = 010					
	Z_STATE	Z	Reg9[14:12] = 110					
	GPIO39	I/O	Reg9[14:12] = 111					
R14	UART1.CTS	I	Reg9[17:15] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F	LZ	DV _{DD7}
	UART1.IRSEL	O	Reg9[17:15] = 010					
	GPIO38	I/O	Reg9[17:15] = 111					
V14	UART1.RX	I	Reg9[20:18] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F	LZ	DV _{DD7}
	UART1.IRRX	I	Reg9[20:18] = 010					
	GPIO37	I/O	Reg9[20:18] = 111					
Y14	LOW_STATE	O	Reg9[23:21] = 000		2 mA (Lv) 6 mA (Hv)	A, B, F, G1	0	DV _{DD7}
	UART1.TX	O	Reg9[23:21] = 001					
	UART1.IRTX	O	Reg9[23:21] = 010					
	CCP.DATAM	I	Reg9[23:21] = 110					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20- μ A internal pulldown, PD100=100- μ A internal pullup, PU20 = 20- μ A internal pullup, PU100 = 100- μ A internal pullup

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output

B = SUBLVDS input/output

C = USB transceiver input/output

D = I²C input/output buffers

E = Analog oscillator terminals

F = Boundary-scannable terminal

K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

NOTES: 3. NA denotes no multiplexing on the ball

4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2–4. ZYG Package Terminal Characteristics (Continued)

ZYG BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING	PULLUP/PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
W14	MCSI1.DOUT	O	Reg9[26:24] = 000		2 mA (Lv) 6 mA (Hv)	A, B, F, G1, H3	0	DV _{DD7}
	USB1.TXD	O	Reg9[26:24] = 001					
	TDO	O	Reg9[26:24] = 011					
	MCBSP3.DX	O	Reg9[26:24] = 100					
	CCP.DATAP	I	Reg9[26:24] = 110					
	GPIO18	I/O	Reg9[26:24] = 111					
R13	CLK32K_OUT	O	RegA[14:12] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A	U	DV _{DDRTC}
	MPUIO0	I/O	RegA[14:12] = 100					
	USB1.SPEED	O	RegA[14:12] = 101					
	UART1.TX	O	RegA[14:12] = 110					
	GPIO36	I/O	RegA[14:12] = 111					
V13	OSC32K_IN	–	NA			E	NA	NA
AA13	OSC32K_OUT	–	NA			E	NA	NA
W13	RTC_WAKE_INT	O	Reg9[2:0] = 000		2 mA (Lv) 6 mA (Hv)	A, B	0	DV _{DDRTC}
	USB1.SE0	O	Reg9[2:0] = 100					
	RST_HOST_OUT	O	Reg9[2:0] = 101					
	CCP.CLKM	I	Reg9[2:0] = 110					
	GPIO55	I/O	Reg9[2:0] = 111					
Y12	RTC_ON_NOFF	I	Reg8[20:18] = 000		2 mA (Lv) 6 mA (Hv)	A, B, G1	Z	DV _{DDRTC}
	CCP.CLKP	I	Reg8[20:18] = 110					
P13	CLK32K_IN	I	RegA[17:15] = 000			A	Input	DV _{DDRTC}
R12	PWRON_RESET	I	NA			A	Input	DV _{DDRTC}
W11	MMC.DAT3	I/O	Reg10[17:15] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G1	Z	DV _{DD6}
	MPUIO9	I/O	Reg10[17:15] = 001					
	MPUIO6	I/O	Reg10[17:15] = 010					
	CFLASH.CD1	I	Reg10[17:15] = 011					
	SSI.ACFLAG	O	Reg10[17:15] = 110					
V11	MMC.CLK	O	RegA[23:21] = 000	PD100, PU20	4 mA (Lv) 8 mA (Hv)	A, F, G1	0	DV _{DD6}
	SSI.CARDY	I	RegA[23:21] = 101					
	GPIO57	I/O	RegA[23:21] = 110					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20- μ A internal pulldown, PD100=100- μ A internal pulldown, PU20 = 20- μ A internal pullup, PU100 = 100- μ A internal pullup

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output

B = SUBLVDS input/output

C = USB transceiver input/output

D = I²C input/output buffers

E = Analog oscillator terminals

F = Boundary-scannable terminal

K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

NOTES: 3. NA denotes no multiplexing on the ball

4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2–4. ZZG Package Terminal Characteristics (Continued)

ZZG BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING	PULLUP/PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
R11	MMC.DAT0/SPI.DI	I/O	RegB[2:0] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G1	Z	DV _{DD6}
	Z_STATE	Z	RegB[2:0] = 001					
	CFLASH.IOIS16	I	RegB[2:0] = 011					
	SSI.ACRDY	O	RegB[2:0] = 110					
	GPIO58	I/O	RegB[2:0] = 111					
W10	MMC.DAT2	I/O	RegA[20:18] = 000	PD100, PU20	4 mA (Lv) 8 mA (Hv)	A, F, G1	Z	DV _{DD6}
	Z_STATE	Z	RegA[20:18] = 001					
	MPUIO11	I/O	RegA[20:18] = 010					
	CFLASH.RFSFT	O	RegA[20:18] = 011					
	SSI.CAFLAG	I	RegA[20:18] = 110					
V10	MMC.DAT1	I/O	RegA[26:24] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G1	Z	DV _{DD6}
	MPUIO10	I/O	RegA[26:24] = 001					
	MPUIO7	I/O	RegA[26:24] = 010					
	CFLASH.IRFQ	I	RegA[26:24] = 011					
	SSI.ACDATA	O	RegA[26:24] = 110					
P11	MMC.CMD/SPI.DO	I/O	RegA[29:27] = 000	PD100, PU20	4 mA (Lv) 8 mA (Hv)	A, F, G1	Z	DV _{DD6}
	CFLASH.CD2	I	RegA[29:27] = 011					
	SSI.CADATA	I	RegA[29:27] = 110					
	GPIO55	I/O	RegA[29:27] = 111					
Y10	MCSI2.CLK	I/O	RegB[5:3] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F	LZ	DV _{DD3}
	USB2.SUSP	O	RegB[5:3] = 001					
	USB0.SUSP	O	RegB[5:3] = 101					
	MMC2.CLK	O	RegB[5:3] = 110					
	GPIO27	I/O	RegB[5:3] = 111					
AA9	MCSI2.DIN	I	RegB[8:6] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F	LZ	DV _{DD3}
	USB2.VP	I	RegB[8:6] = 001					
	USB0.VP	I	RegB[8:6] = 101					
	GPIO26	I/O	RegB[8:6] = 111					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20- μ A internal pulldown, PD100=100- μ A internal pulldown, PU20 = 20- μ A internal pullup, PU100 = 100- μ A internal pullup

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output

B = SUBLVDS input/output

C = USB transceiver input/output

D = I²C input/output buffers

E = Analog oscillator terminals

F = Boundary-scannable terminal

K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

NOTES: 3. NA denotes no multiplexing on the ball

4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

G1 = Terminal may be gated by BFAIL

G2 = Terminal may be gated by GPIO9 and MPUIO3

G3 = Terminal may be gated by BFAIL and OMAP5912 Internal Reset

H1 = Terminal may be 3-stated by BFAIL input

H3 = MCSI1.DOUT pin can be forced into a high-impedance state by the OMAP5912 HIGH_IMP3 control bit

Table 2–4. ZZG Package Terminal Characteristics (Continued)

ZZG BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING	PULLUP/PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
W9	MCSI2.DOUT	O	RegB[11:9] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G2	0	DV _{DD3}
	USB2.TXEN	O	RegB[11:9] = 001					
	USB0.TXEN	O	RegB[11:9] = 101					
	Z_STATE	Z	RegB[11:9] = 110					
	GPIO25	I/O	RegB[11:9] = 111					
V9	MCSI2.SYNC	I/O	RegB[14:12] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F	LZ	DV _{DD3}
	GPIO7	I/O	RegB[14:12] = 001					
	USB2.SPEED	O	RegB[14:12] = 010					
	USB0.SPEED	O	RegB[14:12] = 110					
	MMC2.CMDDIR	O	RegB[14:12] = 111					
R10	MCLKREQ	I	RegB[20:18] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F	LZ	DV _{DD3}
	EXT_MASTER_REQ	O	RegB[20:18] = 001					
	UART2.RX	I	RegB[20:18] = 010					
	MMC2.DAT3	I/O	RegB[20:18] = 110					
	GPIO23	I/O	RegB[20:18] = 111					
W8	GPIO9	I/O	RegB[23:21] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G3	LZ	DV _{DD3}
	EMU0	I/O	RegB[23:21] = 011					
	MCSI1.SYNC	I/O	RegB[23:21] = 100					
	MMC2.DAT0/SPI.DI	I/O	RegB[23:21] = 110					
Y8	GPIO8	I/O	RegB[26:24] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G3	LZ	DV _{DD3}
	TRST	I	RegB[26:24] = 011					
	MCSI1.DOUT	O	RegB[26:24] = 100					
	MMC2.CMD/SPI.DO	I/O	RegB[26:24] = 110					
V8	MPUIO3	I/O	RegB[29:27] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G1	LZ	DV _{DD3}
	MMC2.DAT1	I/O	RegB[29:27] = 110					
P10	MCBSP2.DR	I	RegC[2:0] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G2	LZ	DV _{DD3}
	MCBSP2.DX	O	RegC[2:0] = 001					
	MCBSP2.DXZ	O/Z	RegC[2:0] = 010					
	GPIO22	I/O	RegC[2:0] = 111					
W7	MCBSP2.FSX	I/O	RegC[5:3] = 000	PU20, PD20	4 mA (Lv) 11 mA (Hv)	A, F, G2	LZ	DV _{DD3}
	VLYNQ.RX1	I	RegC[5:3] = 011					
	GPIO21	I/O	RegC[5:3] = 111					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20- μ A internal pulldown, PD100=100- μ A internal pulldown, PU20 = 20- μ A internal pullup, PU100 = 100- μ A internal pullup

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output

B = SUBLVDS input/output

C = USB transceiver input/output

D = I²C input/output buffers

E = Analog oscillator terminals

F = Boundary-scannable terminal

K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

NOTES: 3. NA denotes no multiplexing on the ball

4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2–4. ZZG Package Terminal Characteristics (Continued)

ZZG BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING	PULLUP/PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
V7	MCBSP2.CLKR	I/O	RegC[8:6] = 000	PU20, PD20	4 mA (Lv) 11 mA (Hv)	A, F	Z	DV _{DD3}
	GPIO11	I/O	RegC[8:6] = 001					
	VLYNQ.CLK	I/O	RegC[8:6] = 011					
Y6	MCBSP2.CLKX	I/O	RegC[11:9] = 000	PU20, PD20	4 mA (Lv) 11 mA (Hv)	A, F, G2	LZ	DV _{DD3}
	VLYNQ.TX1	O	RegC[11:9] = 011					
	GPIO20	I/O	RegC[11:9] = 111					
W6	MCBSP2.FSR	I/O	RegC[14:12] = 000	PU20, PD20	4 mA (Lv) 11 mA (Hv)	A, F	Z	DV _{DD3}
	GPIO12	I/O	RegC[14:12] = 001					
	VLYNQ.RX0	I	RegC[14:12] = 011					
AA5	MCBSP2.DX	O	RegC[17:15] = 000	PU20, PD20	4 mA (Lv) 11 mA (Hv)	A, F, G2	0	DV _{DD3}
	MCBSP2.DR	I	RegC[17:15] = 001					
	MCBSP2.DXZ	O/Z	RegC[17:15] = 010					
	VLYNQ.TX0	O	RegC[17:15] = 011					
	GPIO19	I/O	RegC[17:15] = 111					
R9	UART2.RX	I	RegC[20:18] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F	LZ	DV _{DD3}
	USB2.VM	I	RegC[20:18] = 001					
	USB0.VM	I	RegC[20:18] = 101					
	GPIO18	I/O	RegC[20:18] = 111					
Y5	UART2.CTS	I	RegC[23:21] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F	LZ	DV _{DD3}
	USB2.RCV	I	RegC[23:21] = 001					
	GPIO7	I/O	RegC[23:21] = 010					
	USB0.RCV	I	RegC[23:21] = 101					
W5	LOW_STATE	O	RegC[26:24] = 000		4 mA (Lv) 8 mA (Hv)	A, F, G2	0	DV _{DD3}
	UART2.RTS	O	RegC[26:24] = 001					
	USB2.SE0	O	RegC[26:24] = 010					
	MPUIO5	I/O	RegC[26:24] = 011					
	MPUIO12	I/O	RegC[26:24] = 100					
	USB0.SE0	O	RegC[26:24] = 101					
	LOW_STATE	O	RegC[26:24] = 110					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20- μ A internal pulldown, PD100=100- μ A internal pulldown, PU20 = 20- μ A internal pullup, PU100 = 100- μ A internal pullup

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output

B = SUBLVDS input/output

C = USB transceiver input/output

D = I²C input/output buffers

E = Analog oscillator terminals

F = Boundary-scannable terminal

K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

NOTES: 3. NA denotes no multiplexing on the ball

4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2–4. ZZG Package Terminal Characteristics (Continued)

ZZG BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING	PULLUP/PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
V6	LOW_STATE	O	RegC[29:27] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G2	0	DV _{DD3}
	UART2.TX	O	RegC[29:27] = 001					
	USB2.TXD	O	RegC[29:27] = 010					
	USB0.TXD	O	RegC[29:27] = 101					
	Z_STATE	Z	RegC[29:27] = 110					
	GPIO17	I/O	RegC[29:27] = 111					
Y4	UART2.BCLK	O	RegD[2:0] = 000		4 mA (Lv) 8 mA (Hv)	A, F, G2	0	DV _{DD3}
	SYS_CLK_IN	I	RegD[2:0] = 110					
V5	MCLK	O	RegB[17:15] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G1	0	DV _{DD3}
	MMC2.DATDIR0	O	RegB[17:15] = 110					
	GPIO24	I/O	RegB[17:15] = 111					
W4	USB.PUEN	O	RegD[5:3] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, F, G1	1	DV _{DD2}
	USB.CLKO	O	RegD[5:3] = 001					
	USB.PUDIS	O	RegD[5:3] = 011					
	Z_STATE	Z	RegD[5:3] = 100					
	LOW_POWER	O	RegD[5:3] = 110					
	GPIO58	I/O	RegD[5:3] = 111					
P9	USB.DP	I/O	USBTCTL[6:4] = 000		18.3 mA (in USB mode)	C	Z	DV _{DD2}
	I2C.SDA	I/O/Z	USBTCTL[6:4] = 100					
	UART1.RX	I	USBTCTL[6:4] = 101					
	USB.PUEN	O	USBTCTL[6:4] = 111					
R8	USB.DM	I/O			18.3 mA (in USB mode)	C	Z	DV _{DD2}
	I2C.SCL	I/O/Z	USBTCTL[6:4] = 100					
	UART1.TX	O	USBTCTL[6:4] = 101					
	Z_STATE	Z	USBTCTL[6:4] = 111					
Y2	OSC1_IN	I	NA			E	NA	NA
W3	OSC1_OUT	O	NA			E	NA	NA
Y1	FLASH.CS1U	O	RegA[2:0] = 000		4 mA (Lv) 8 mA (Hv)	A, F	1	DV _{DD5}
	GPIO16	I/O	RegA[2:0] = 111					
V4	FLASH.WP	O	NA		4 mA (Lv) 8 mA (Hv)	A	0	DV _{DD5}
W2	FLASH.WE	O	NA		4 mA (Lv) 8 mA (Hv)	A	1	DV _{DD5}

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20- μ A internal pulldown, PD100=100- μ A internal pulldown, PU20 = 20- μ A internal pullup, PU100 = 100- μ A internal pullup

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output

B = SUBLVDS input/output

C = USB transceiver input/output

D = I²C input/output buffers

E = Analog oscillator terminals

F = Boundary-scannable terminal

K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

NOTES: 3. NA denotes no multiplexing on the ball

4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2–4. ZZG Package Terminal Characteristics (Continued)

ZZG BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING	PULLUP/PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
W1	FLASH.RP	O	RegF[23:21] = 000		4 mA (Lv) 8 mA (Hv)	A	0	DV _{DD5}
	FLASH.CS2UWE	O	RegF[23:21] = 001					
U4	FLASH.OE	O	NA		4 mA (Lv) 8 mA (Hv)	A	1	DV _{DD5}
E1 L7 K3 K4 L8 F2 J3 F4 J2	FLASH.A[25:17]	O	NA		4 mA (Lv) 8 mA (Hv)	A, G1	0	DV _{DD5}
K7	FLASH.A[16]	O	Reg11[5:3] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, G1	0	DV _{DD5}
H3	FLASH.A[15]	O	Reg11[8:6] = 000		3 mA (Lv) 8 mA (Hv)	A, G1	0	DV _{DD5}
H4	FLASH.A[14]	O	Reg11[11:9] = 000		4 mA (Lv) 8 mA (Hv)	A, G1	0	DV _{DD5}
K8	FLASH.A[13]	O	Reg11[14:12] = 000		3 mA (Lv) 8 mA (Hv)	A, G1	1	DV _{DD5}
G2	FLASH.A[12]	O	Reg11[17:15] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, G1	0	DV _{DD5}
G3	FLASH.A[11]	O	Reg11[20:18] = 000		3 mA (Lv) 8 mA (Hv)	A, G1	0	DV _{DD5}
G4	FLASH.A[10]	O	Reg11[23:21] = 000		3 mA (Lv) 8 mA (Hv)	A, G1	0	DV _{DD5}
F3	FLASH.A[9]	O	Reg11[26:24] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, G1	0	DV _{DD5}
J7	FLASH.A[8]	O	Reg12[5:3] = 000		4 mA (Lv) 8 mA (Hv)	A, G1	0	DV _{DD5}
E3	FLASH.A[7]	O	Reg12[8:6] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, G1	0	DV _{DD5}
F4	FLASH.A[6]	O	Reg12[11:9] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, G1	0	DV _{DD5}
D2	FLASH.A[5]	O	Reg12[14:12] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, G1	0	DV _{DD5}

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20- μ A internal pulldown, PD100=100- μ A internal pulldown, PU20 = 20- μ A internal pullup, PU100 = 100- μ A internal pullup

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVC MOS input/output

B = SUBLVDS input/output

C = USB transceiver input/output

D = I²C input/output buffers

E = Analog oscillator terminals

F = Boundary-scannable terminal

K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

NOTES: 3. NA denotes no multiplexing on the ball

4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

G1 = Terminal may be gated by BFAIL

G2 = Terminal may be gated by GPIO9 and MPUIO3

G3 = Terminal may be gated by BFAIL and OMAP5912 Internal Reset

H1 = Terminal may be 3-stated by BFAIL input

H3 = MCS11.DOUT pin can be forced into a high-impedance

state by the OMAP5912 HIGH_IMP3 control bit

Table 2–4. ZZG Package Terminal Characteristics (Continued)

ZZG BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING	PULLUP/PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
E4	FLASH.A[4]	O	Reg12[17:15] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, G1	0	DV _{DD5}
C1	FLASH.A[3]	O	Reg12[20:18] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, G1	0	DV _{DD5}
D3	FLASH.A[2]	O	Reg12[23:21] = 000	PU20, PD20	4 mA (Lv) 8 mA (Hv)	A, G1	0	DV _{DD5}
J8	FLASH.A[1]	O	Reg12[26:24] = 000		3 mA (Lv) 8 mA (Hv)	A, G1	0	DV _{DD5}
V3 T4 U3 U1 P8 T3 T2 R4 R3 R2 P7 P4 P2 N7 N2 N4	FLASH.D[15:0]	I/O	NA		3 mA (Lv) 6 mA (Hv)	A, K	0	DV _{DD5}
N3	FLASH.CLK FLASH.CS2UOE	O O	Reg10[23:21] = 000 Reg10[23:21] = 001		3 mA (Lv) 6 mA (Hv)	A, K, G1	0	DV _{DD5}
V2	FLASH.RDY GPIO10	I I/O	RegF[29:27] = 000 RegF[29:27] = 001	PU100, PD20	4 mA (Lv) 8 mA (Hv)	A, F	Input	DV _{DD5}
L4	FLASH.ADV	O	NA		4 mA (Lv) 8 mA (Hv)	A	1	DV _{DD5}
M4	FLASH.CS2 FLASH.BAA FLASH.CS2L	O O O	RegD[8:6] = 000 RegD[8:6] = 000 RegD[8:6] = 000		4 mA (Lv) 8 mA (Hv)	A	1	DV _{DD5}
M7	GPIO62 FLASH.CS0	I/O O	Reg10[2:0] = 000 Reg10[2:0] = 001		4 mA (Lv) 8 mA (Hv)	A, F, G1	Input	DV _{DD5}
M3	FLASH.CS1 FLASH.CS1L	O O	Reg10[29:27] = 000 Reg10[29:27] = 001		4 mA (Lv) 8 mA (Hv)	A	1	DV _{DD5}
P3	FLASH.CS2U GPIO5	O I/O	Reg10[20:18] = 000 Reg10[20:18] = 001		4 mA (Lv) 8 mA (Hv)	A, F	1	DV _{DD5}
L3	FLASH.BE[0] FLASH.CS2UOE GPIO59	O O I/O	Reg10[8:6] = 000 Reg10[8:6] = 001 Reg10[8:6] = 111		4 mA (Lv) 8 mA (Hv)	A, F	0	DV _{DD5}

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20- μ A internal pulldown, PD100=100- μ A internal pulldown, PU20 = 20- μ A internal pullup, PU100 = 100- μ A internal pullup

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output

B = SUBLVDS input/output

C = USB transceiver input/output

D = I²C input/output buffers

E = Analog oscillator terminals

F = Boundary-scannable terminal

K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

NOTES: 3. NA denotes no multiplexing on the ball

4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

Table 2–4. ZZG Package Terminal Characteristics (Continued)

ZZG BALL NO.	SIGNAL NAME	TYPE†	MUX CTRL SETTING	PULLUP/PULLDN‡	BUFFER STRENGTH§	OTHER¶	RESET STATE#	SUPPLY
M8	FLASH.BE[1]	O	Reg10[5:3] = 000		4 mA (Lv) 8 mA (Hv)	A, F	0	DV _{DD5}
	FLASH.CS2UWE	O	Reg10[5:3] = 001					
	GPIO60	I/O	Reg10[5:3] = 111					
N8	FLASH.CS3	O	Reg10[26:24] = 000		4 mA (Lv) 8 mA (Hv)	A, F	1	DV _{DD5}
	GPIO3	I/O	Reg10[26:24] = 111					

† I = Input, O = Output, Z = High-Impedance

‡ PD20 = 20- μ A internal pulldown, PD100=100- μ A internal pulldown, PU20 = 20- μ A internal pullup, PU100 = 100- μ A internal pullup

§ Lv = Low voltage (1.65 V), Hv = High voltage (2.5 V)

¶ A = Standard LVCMOS input/output

B = SUBLVDS input/output

C = USB transceiver input/output

D = I²C input/output buffers

E = Analog oscillator terminals

F = Boundary-scannable terminal

K = Output buffer includes a serial resistor of 20 Ω to match with PCB line impedance and ensure proper signal integrity

Z = High-Impedance, LZ = Low-Impedance (pin is driven), 1 = Output driven high, 0 = Output driven low

NOTES: 3. NA denotes no multiplexing on the ball

4. 'Regx' denotes the terminal multiplexing register that controls the specified terminal where Regx = FUNC_MUX_CTRL_x

G1 = Terminal may be gated by BFAIL

G2 = Terminal may be gated by GPIO9 and MPUIO3

G3 = Terminal may be gated by BFAIL and OMAP5912 Internal Reset

H1 = Terminal may be 3-stated by BFAIL input

H3 = MCS11.DOUT pin can be forced into a high-impedance

state by the OMAP5912 HIGH_IMP3 control bit

2.4 Signal Description

Table 2–5 provides a description of the signals on OMAP5912. Many signals are available on multiple pins, depending upon the software configuration of the pin multiplexing options.

Table 2–5. Signal Description

SIGNAL	ZDY BALL#	ZZG BALL#	DESCRIPTION	TYPE†
EXTERNAL MEMORY INTERFACE FAST (EMIFF) SDRAM INTERFACE				
SDRAM.CS	E7	G8	SDRAM chip-select	O
SDRAM.DQSH	A12	C14	DDR DQ strobe high	I/O
SDRAM.DQSL	A2	D4	DDR DQ strobe low	I/O
SDRAM.CAS	D5	B4	SDRAM column address strobe. $\overline{\text{SDRAM.CAS}}$ is active (low) during reads, writes, and the REFR and MRS commands to SDRAM memory.	O
SDRAM.DQM $\overline{\text{L}}$	C7	C8	SDRAM lower data mask. Active-low data mask for the lower byte of the SDRAM data bus (SDRAM.D[7:0]). The data mask outputs allow for both 16-bit-wide and 8-bit-wide accesses to SDRAM memory.	O
SDRAM.DQM $\overline{\text{U}}$	A8	D10	SDRAM upper data mask. Active-low data mask for the upper byte of the SDRAM data bus (SDRAM.D[15:8]). The data mask outputs allow for both 16-bit-wide and 8-bit-wide accesses to SDRAM memory.	O
SDRAM.RAS	D4	H7	SDRAM row address strobe. $\overline{\text{SDRAM.RAS}}$ is active (low) during ACTV, DCAB, REFR, and MRS commands to SDRAM memory.	O
SDRAM.WE $\overline{\text{}}$	E6	H8	SDRAM write enable. $\overline{\text{SDRAM.WE}}$ is active (low) during writes, DCAB, and MRS commands to SDRAM memory.	O
SDRAM.A[13:0]	D10 E8 E9 F8 F9 C6 A10 E10 C8 D9 C3 F7 A1 B2	H11 H9 H10 B8 B12 G9 G11 G12 B9 G10 A1 B6 B2 A2	SDRAM address bus. Provides row and column address information to the SDRAM memory as well as MRS command data. SDRAM.A[10] also serves as a control signal to define specific commands to SDRAM memory.	O
SDRAM.BA[1:0]	C4 C5	C3 B3	SDRAM bank address bus. Provides the bank address to SDRAM memories	O
SDRAM.D[15:0]	B10 C10 B11 B9 A11 B8 B12 C9 B7 A3 B6 B3 A5 A4 B5 B4	C12 D12 D13 C11 C13 D11 D14 C10 D8 C4 C7 D5 D7 C5 C6 D6	SDRAM data bus. SDRAM.D[15:0] provides data exchange between the traffic controller and SDRAM memory.	I/O
SDRAM.CLK	A7	C9	SDRAM clock. Clock for synchronization SDRAM memory commands/accesses.	O
SDRAM.CLKX	A6	D9	DDR clock. Inverted clock for synchronization DDR memory commands/accesses	O
SDRAM.CKE	B13	H12	SDRAM clock enable (active-high). Asserting this signal enables the SDRAM clock for normal operation; negating puts SDRAM memory into low-power mode.	O

† I = Input, O = Output, Z = High-Impedance

Table 2–5. Signal Description (Continued)

SIGNAL	ZDY BALL#	ZZG BALL#	DESCRIPTION	TYPE†
EXTERNAL MEMORY INTERFACE SLOW (EMIFS) FLASH AND ASYNCHRONOUS MEMORY INTERFACE				
FLASH.A[25:1]	F3 J4 J2 H2 H5 F4 H4 H3 G6 G5 G2 G4 G3 F5 F1 F2 E1 D1 E2 C1 D2 E3 E4 C2 D3	E1 L7 K3 K4 L8 F2 J3 J4 J2 K7 H3 H4 K8 G2 G3 G4 F3 J7 E3 F4 D2 E4 C1 D3 J8	EMIFS address bus. Address output bus for all EMIFS accesses.	O
FLASH.D[15:0]	N4 R1 P1 K7 M3 M4 N2 L5 N1 K6 L4 M2 J7 L2 M1 L1	V3 T4 U3 U1 P8 T3 T2 R4 R3 R2 P7 P4 P2 N7 N2 N4	EMIFS data bus. Bidirectional 16-bit data bus used to transfer read and write data during EMIFS accesses. The 16-bit data bus becomes address/data in case the EMIFS is configured in address/data multiplexed mode.	I/O
FLASH.CLK	K1	N3	Flash clock. Clock output that is active during synchronous modes of flash operation for synchronous burst flash memories.	O
FLASH.RDY	L6	V2	Flash ready. Active-high ready input used to suspend the flash interface when the external memory or asynchronous device is not ready to continue the current cycle.	I
FLASH.ADV	H6	L4	Flash address valid. Active-low control signal used to indicate a valid address is present on the FLASH.A[25:1] bus.	O
FLASH.BAA	J8	M4	Flash burst advance acknowledge. Active-low control signal used with Advanced Micro Devices™ E burst flash.	O
FLASH.BE[1:0]	K2 J1	M8 L3	Flash byte enables. Active-low byte enable signals used to perform byte-wide accesses to memories or devices that support byte enables.	O
FLASH.CS0	J5	M7	Flash chip-select bit 0	O
FLASH.CS1	J3	M3	Flash chip-select bit 1	O
FLASH.CS1L	J3	M3	Lower half of FLASH.CS1 address range	O
FLASH.CS1U	T1	Y1	Upper half of FLASH.CS1 address range	O
FLASH.CS2	J8	M4	Flash chip-select bit 2	O
FLASH.CS2L	J8	M4	Lower half of FLASH.CS2 address range	O
FLASH.CS2U	K3	P3	Upper half of FLASH.CS2 address range	O

† I = Input, O = Output, Z = High-Impedance

Table 2–5. Signal Description (Continued)

SIGNAL	ZDY BALL#	ZZG BALL#	DESCRIPTION	TYPE†
EXTERNAL MEMORY INTERFACE SLOW (EMIFS) FLASH AND ASYNCHRONOUS MEMORY INTERFACE (CONTINUED)				
FLASH.CS2UOE	J1 K1	L3 N3	FLASH.CS2U gated with FLASH.OE. Output enable if EMIFS is used to interface with external flash.	O
FLASH.CS2UWE	K2 N3	M8 W1	FLASH.CS2U gated with FLASH.WE. Write enable if EMIFS is used to interface with external flash.	O
FLASH.CS3	J6	N8	Flash chip-select bit 3. If MPU_BOOT is high and the device is an emulation device, select external boot memory.	O
FLASH.OE	M5	U4	Flash output enable. Active-low output enable output for Flash or SRAM memories or asynchronous devices.	O
FLASH.RP	N3	W1	Flash power down (TI Flash devices) or reset output (Intel® Flash devices)	O
FLASH.WE	P3	W2	Flash write enable. Active-low write enable output for Flash or SRAM memories or asynchronous devices.	O
FLASH.WP	R3	V4	Flash write protect. Active-low output for hardware write protection feature on standard memory devices.	O
CompactFlash INTERFACE				
CFLASH.IREQ	U9	V10	CompactFlash interrupt request	I
CFLASH.CD1	P9	W11	Card detect	I
CFLASH.CD2	N7	P11	Card detect	I
CFLASH.IOIS16	R8	R11	8/16 bits selection	I
CFLASH.RESET	T9	W10	Reset	O

† I = Input, O = Output, Z = High-Impedance

Table 2–5. Signal Description (Continued)

SIGNAL	ZDY BALL#	ZZG BALL#	DESCRIPTION	TYPE†
MULTIMEDIA CARD/SECURE DIGITAL INPUT/OUTPUT INTERFACES (MMC/SDIOs)				
MMC.CLK	M8	V11	MMC/SDIO1 clock. Clock output to the MMC/SD card.	O
MMC.CMD/SPI.DO	N7	P11	MMC/SDIO1 command/SPI data output. MMC/SD commands are transferred to/from this pin. The pin functions as the data output during SPI mode.	I/O
MMC.DAT0/SPI.DI	R8	R11	MMC/SDIO1 data bit 0/SPI input. MMC.DAT0/SPI.DI functions as data bit 0 during MMC and secure digital operation. The pin functions as the data input in generic SPI mode.	I/O
MMC.DAT1	U9	V10	SD card data bit 1. Data bit 1 is used in 4-bit secure digital mode.	I/O
MMC.DAT2	T9 L15	W10 M15	SD card data bit 2. Data bit 2 is used in 4-bit secure digital mode.	I/O
MMC.DAT3	P9	W11	SD card data bit 3. Data bit 3 is used in 4-bit secure digital mode.	I/O
SPI.CLK	M16	M14	SPI clock. SPI clock output used during generic SPI mode operation.	O
SPI.RDY	N17	R18	SPI ready. SPI ready input from SPI device used only in generic SPI mode operation.	I
SPI.CS1	L14	P19	SPI chip-selects. SPI chip-selects used during generic SPI mode operation.	O
SPI.CS2	M17	P20		
SPI.CS3	L13	P18		
MMC2.CLK	K12 P8	M19 Y10	MMC/SDIO2 clock. Clock output to the MMC/SD card.	O
MMC2.CLKIN	N17	R18	MMC/SDIO2 clock feedback	I
MMC2.CMD/SPI.DO	P7 H15	Y8 J19	MMC/SDIO2 command/SPI data output. MMC/SD commands are transferred to/from this pin. The pin functions as the data output during SPI mode.	I/O
MMC2.CMDDIR	U8	V9	MMC/SDIO2 command direction control	O
MMC2.DAT0/SPI.DI	J12 U7	L15 W8	MMC/SDIO2 data bit 0/SPI serial Input. MMC2.DAT0/SPI.DI functions as data bit 0 during MMC and secure digital operation. The pin functions as the data input in generic SPI mode.	I/O
MMC2.DAT1	J13 R6	L18 V8	MMC/SDIO2 card data bit 1	I/O
MMC2.DAT2	H16 R12	J18 W15	MMC/SDIO2 card data bit 2	I/O
MMC2.DAT3	J17 T7	L19 R10	MMC/SDIO2 card data bit 3	I/O
MMC2.DATDIR0	U3	V5	MMC/SDIO2 data bit 0 direction control	O
MMC2.DATDIR1	T17	W19	MMC/SDIO2 data bit 1, 2, 3 direction control	O

† I = Input, O = Output, Z = High-Impedance

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Table 2–5. Signal Description (Continued)

SIGNAL	ZDY BALL#	ZZG BALL#	DESCRIPTION	TYPE†
MULTICHANNEL BUFFERED SERIAL PORTS (McBSPs)				
MCBSP1.CLKX	F16	G21	McBSP1 bit clock	I/O
MCBSP1.CLKS	G13	G20	McBSP1 clock input	I
MCBSP1.DR	G17	H20	McBSP1 data input	I
MCBSP1.DX	G14	H18	McBSP1 data output	O
	G15	H15		
MCBSP1.DXZ	G15	H15	McBSP1 data output (for multichannel mode)	O/Z
	G14	H18		
MCBSP1.FSX	G15	H15	McBSP1 frame synchronization	I/O
	G14	H18		
MCBSP2.CLKR	U6	V7	McBSP2 receive clock	I/O
MCBSP2.CLKX	U5	Y6	McBSP2 transmit clock	I/O
MCBSP2.DR	L8	P10	McBSP2 data input	I
	T5	AA5		
MCBSP2.DX	L8	P10	McBSP2 data output	O
	T5	AA5		
MCBSP2.DXZ	L8	P10	McBSP2 data output (for multichannel mode)	O/Z
	T5	AA5		
MCBSP2.FSR	R5	W6	McBSP2 receive frame synchronization	I/O
MCBSP2.FSX	N6	W7	McBSP2 transmit frame synchronization	I/O
MCBSP3.CLKX	U14	W16	McBSP3 clock	I/O
	R17	N14		
	U15	P14		
MCBSP3.DR	N10	AA17	McBSP3 data input	I
	P14	U18		
	P12	V15		
	M14	T19		
MCBSP3.DX	U15	P14	McBSP3 data output	O
	R15	W21		
	P11	W14		
MCBSP3.DXZ	R15	W21	McBSP3 data output (for multichannel mode)	O/Z
MCBSP3.FSX	L16	N18	McBSP3 frame synchronization	I/O
	L13	P18		
	L14	P19		
	M17	P20		
	N10	AA17		

† I = Input, O = Output, Z = High-Impedance

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Table 2–5. Signal Description (Continued)

SIGNAL	ZDY BALL#	ZZG BALL#	DESCRIPTION	TYPE†
MULTICHANNEL SERIAL INTERFACES (MCSIs)				
MCSI1.CLK	U15 L15	P14 M15	MCSI1 bit clock	I/O
MCSI1.DIN	L14 P12 U14	P19 V15 W16	MCSI1 data input	I
MCSI1.DOUT	P11 P7	W14 Y8	MCSI1 data output	O
MCSI1.SYNC	N10 U7	AA17 W8	MCSI1 frame synchronization	I/O
MCSI2.CLK	P8	Y10	MCSI2 bit clock	I/O
MCSI2.DIN	R7	AA9	MCSI2 data input	I
MCSI2.DOUT	T8	W9	MCSI2 data output	O
MCSI2.SYNC	U8	V9	MCSI2 frame synchronization	I/O
SERIAL PORT INTERFACE (SPI)				
SPIF.CS ₀	R17	N14	SPI output chip-selects in master mode/input chip-select when SPI is in slave mode.	I/O
SPIF.CS ₁	L12	N15		O
SPIF.CS ₂	M14	T19		
SPIF.CS ₃	R16	P15		
SPIF.SCK	N15	U19	SPI output clock in master mode. SPI input clock in slave mode.	I/O
SPIF.DIN	M17	P20	SPI data-In in master mode. SPI data-out in slave mode.	I/O
	P14	U18		I/O
SPIF.DOUT	N17	R18	SPI data-out in master mode. SPI data-in in slave mode.	I/O
	R15	W21		I/O
SYNCHRONOUS SERIAL INTERCONNECT (SSI)				
SSI.ACDATA	U9	V10	Data transmit (SST)	O
SSI.ACFLAG	P9	W11	Flag associated with transmitting data (SST)	O
SSI.ACRDY	R8	R11	CMT ready signal (SST)	O
SSI.ACWAKE	P12	V15	CMT wake up	O
SSI.CADATA	N7	P11	Data receive (SSR)	I
SSI.CAFLAG	T9	W10	Flag associated with receiving data (SSR)	I
SSI.CARDY	M8	V11	APE ready signal (SSR)	I

† I = Input, O = Output, Z = High-Impedance

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Table 2–5. Signal Description (Continued)

SIGNAL	ZDY BALL#	ZZG BALL#	DESCRIPTION	TYPE†
UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART) INTERFACES				
UART1.CTS	M9	R14	UART1 clear to send	I
UART1.DSR	P14 T17	U18 W19	UART1 data set ready	I
UART1.DTR	R15 N16	W21 T20	UART1 data terminal ready	O
UART1.RTS	R11	AA15	UART1 request to send	O
UART1.RX	U13 T2	V14 P9	UART1 receive data	I
UART1.TX	T12 U1 U12	Y14 R8 R13	UART1 transmit data	O
UART1.IRTX	T12	Y14	UART1 IrDA transmit data	O
UART1.IRRX	U13	V14	UART1 IrDA receive data	I
UART1.IRSEL	M9	R14	UART1 IrDA mode select for external transceiver	O
UART1.IRSHDN	R11	AA15	UART1 IrDA mode select for external transceiver	O
UART2.BCLK	P5	Y4	UART2 baud clock. A clock of 16x	O
UART2.CTS	P6 J12	Y5 L15	UART2 clear to send	I
UART2.RTS	T4 K12	W5 M19	UART2 request to send	O
UART2.RX	U4 T7 K15	R9 R10 L14	UART2 receive data	I
UART2.TX	R4 K17	V6 M18	UART2 transmit data	O
UART3.CTS	R12 T17 J14 P15	W15 W19 K15 V19	UART3 clear to send	I
UART3.DSR	P14	U18	UART3 data set ready	I
UART3.DTR	R15	W21	UART3 data terminal ready	O
UART3.RTS	M15 L10 J16 N16 R15	R19 Y15 K14 T20 W21	UART3 request to send in UART mode SD_MODE in IrDA mode	O

† I = Input, O = Output, Z = High-Impedance

Table 2–5. Signal Description (Continued)

SIGNAL	ZDY BALL#	ZZG BALL#	DESCRIPTION	TYPE†
UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART) INTERFACES (CONTINUED)				
UART3.RX	K15 H13 R16	L14 K19 P15	UART3 receive data	I
UART3.TX	K17 J11 R17	M18 K18 N14	UART3 transmit data	O
USB (INTEGRATED TRANSCEIVER)				
USB.DM	U1	R8	USB differential (–) line	I/O
USB.DP	T2	P9	USB differential (+) line	I/O
USB PORT 0				
USB0.RCV	P6	Y5	USB port 0 receive data	I
USB0.SE0	T4	W5	USB port 0 single-ended zero	O
USB0.SPEED	U8	V9	USB 0 speed	O
USB0.SUSP	P8	Y10	USB 0 suspend	O
USB0.TXD	R4	V6	USB port 0 transmit data	O
USB0.TXEN	T8	W9	USB port 0 transmit enable	O
USB0.VM	U4	R9	USB port 0 V minus receive data	I
USB0.VP	R7	AA9	USB port 0 V plus receive data	I
USB PORT 1				
USB1.RCV	P12	V15	USB port 1 receive data	I
USB1.SE0	N9	W13	USB port 1 single-ended zero	O
USB1.SPEED	U12	R13	USB port 1 bus segment speed control	O
USB1.SUSP	H14	J20	USB port 1 bus segment suspend control	O
USB1.TXD	P11	W14	USB port 1 transmit data	O
USB1.TXEN	U14	W16	USB port 1 transmit enable	O
USB1.VM	U15	P14	USB port 1 V minus receive data	I
USB1.VP	N10	AA17	USB port 1 V plus receive data	I
USB PORT 2				
USB2.RCV	P6	Y5	USB port 2 receive data	I
USB2.SE0	T4	W5	USB port 2 single-ended zero	O
USB2.SPEED	U8	V9	Low-speed USB device or full-speed USB device	O
USB2.SUSP	P8	Y10	USB port 2 bus segment suspend control	O
USB2.TXD	R4	V6	USB port 2 transmit data	O
USB2.TXEN	T8	W9	USB port 2 transmit enable	O
USB2.VM	U4	R9	USB port 2 V minus receive data	I
USB2.VP	R7	AA9	USB port 2 V plus receive data	I

† I = Input, O = Output, Z = High-Impedance

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Table 2–5. Signal Description (Continued)

SIGNAL	ZDY BALL#	ZZG BALL#	DESCRIPTION	TYPE†
UNIVERSAL SERIAL BUS (USB) MISCELLANEOUS SIGNALS				
USB.CLKO	P4	W4	USB clock output. 6-MHz divided clock output of the internal USB DPLL provided for reference. Common for all USB host and function peripherals.	O
USB.VBUS	N17	R18	USB voltage bus enable. USB.VBUS is an input which allows the OMAP5912 device to detect whether the USB cable is connected or not. USB.VBUS must be connected to USB power from the USB cable through a voltage translation buffer to convert the 5-V power from the USB cable to within the 3.3-V nominal range specified for the OMAP device input.	I
USB.PUEN	P4 T2	W4 P9	USB pullup enable	O
USB.PUDIS	P4	W4	USB pullup disable	O
INTER-INTEGRATED CIRCUIT (I²C) MASTER AND SLAVE INTERFACE				
I2C.SCL	P16 U1	T18 R8	I ² C serial clock	I/O
I2C.SDA	M11 T2	V20 P9	I ² C serial data	I/O
HDQ/1-Wire INTERFACE				
HDQ	K13	N20	HDQ/1-Wire interface. HDQ optionally implements one of two serial protocols: HDQ or 1-Wire.	I/O
MICROWIRE™ INTERFACE				
UWIRE.CS ₀	R17 H16	N14 J18	MICROWIRE chip-select 0. The output selects a single MICROWIRE device (configurable as active-high or active-low).	O
UWIRE.CS ₁	L12	N15	MICROWIRE chip-select 1	
UWIRE.CS ₂	M14	T19	MICROWIRE chip-select 2	
UWIRE.CS ₃	R16 H15	P15 J19	MICROWIRE chip-select 3	
UWIRE.SCLK	P15 G16	V19 J15	MICROWIRE serial clock. This pin drives a clock to a MICROWIRE device. The active edge is software-configurable.	O
UWIRE.SDI	P14 H17	U18 J14	MICROWIRE serial data input	I
UWIRE.SDO	R15 H12	W21 H19	MICROWIRE serial data output	O

† I = Input, O = Output, Z = High-Impedance

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Table 2–5. Signal Description (Continued)

SIGNAL	ZDY BALL#	ZZG BALL#	DESCRIPTION	TYPE†
CAMERA INTERFACE				
CAM.OUTCLK	L10	Y15	Camera output clock	O
CAM.D[7:0]	H16 H15 H17 J11 H13 J14 J16 J17	J18 J19 J14 K18 K19 K15 K14 L19	Camera digital image data bits	I
CAM.HS	J12	L15	Camera interface horizontal synchronization. Horizontal synchronization input from external camera sensor.	I
CAM.LCLK	G16	J15	Camera interface line clock. Input clock to provide external timing reference from camera sensor logic	I
CAM.RSTZ	K12	M19	Camera interface reset. Reset output used to reset or Initialize external camera sensor logic.	O
CAM.VS	J13	L18	Camera vertical synchronization	I
COMPACT CAMERA PORT (CCP) INTERFACE				
CCP.CLKM	N9	W13	Camera differential clock. Clock up to 208 MHz.	I
CCP.CLKP	P10	Y12	Camera differential clock	I
CCP.DATAM	T12	Y14	Camera differential data	I
CCP.DATAP	P11	W14	Camera differential data	I
CAM.EXCLK	H12	H19	Camera interface external clock. Output clock used to provide a timing reference to a camera sensor.	O
VLYNQ INTERFACE				
VLYNQ.CLK	E16 U6 L17	H14 V7 N19	VLYNQ clock	I/O
VLYNQ.RX0	E17 R5 L16	F19 W6 N18	VLYNQ receive data 0	I
VLYNQ.RX1	F15 N6 K13	G18 W7 N20	VLYNQ receive data 1	I
VLYNQ.TX0	D17 R11 K14	E20 AA15 N21	VLYNQ transmit data 0	O
VLYNQ.TX1	F13 U5 K16	E19 Y6 M20	VLYNQ transmit data 1	O

† I = Input, O = Output, Z = High-Impedance

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Table 2–5. Signal Description (Continued)

SIGNAL	ZDY BALL#	ZZG BALL#	DESCRIPTION	TYPE†
LCD AND LCDCONV INTERFACE				
LCD.AC	F10	B15	LCD AC-bias. LCD.AC signals the LCD display to switch the polarity of the row and column power supplies to counteract charge buildup causing DC offset. In TFT mode, LCD.AC is used as the output enable to latch LCD pixel data using the pixel clock.	O
LCD.BLUE0	L17	N19	Blue bit 0 in 18-bit LCD output mode	O
LCD.HS	D15	C20	LCD horizontal sync. LCD_HSYNC is the line clock that signals the end of a line of pixels to the LCD display panel. In TFT mode, LCD_HSYNC is the horizontal synchronization signal.	O
LCD.PCLK	A14	C15	LCD pixel clock output. Clock output provided to synchronize pixel data to LCD display panels. In passive mode, LCD_PCLK transitions only when LCD.P[15:0] is valid. In active mode, LCD_PCLK transitions continuously and LCD.AC is used as the output enable when LCD.P[15:0] is valid.	O
LCD.P[15:0]	C12 D12 E11 A13 B14 A15 F11 C13 D13 A16 C15 E12 D14 C16 B16 A17	D15 C16 A17 G13 B17 C17 D16 D17 C18 B19 A20 H13 G14 C19 B21 D18	LCD pixel data bits	O
LCD.RED0	K14	N21	Red bit 0 in 18-bit LCD output mode	O
LCD.VS	B15	B18	LCD vertical synchronization (sync) output. LCD.VS is the frame clock that signals the start of a new frame of pixels to the LCD display panel. In TFT mode, LCD.VS is the vertical synchronization signal.	O
SPECIALLY OPTIMIZED SCREEN INTERFACE (SoSSI)				
SOSSI.CMD	F10	B15	SoSSI command/data control	O
SOSSI.CS	D15	C20	LCD chip-select	O
SOSSI.D[15:0]	C12 D12 E11 A13 B14 A15 F11 C13 D13 A16 C15 E12 D14 C16 B16 A17	D15 C16 A17 G13 B17 C17 D16 D17 C18 B19 A20 H13 G14 C19 B21 D18	SoSSI data bits	I/O
SOSSI.RD	B15	B18	Read enable for SoSSI	O
SOSSI.WR	A14	C15	Write enable for SoSSI	O
SOSSI.TE	G13	G20	Tearing effect removal	I

† I = Input, O = Output, Z = High-Impedance

Table 2–5. Signal Description (Continued)

SIGNAL	ZDY BALL#	ZZG BALL#	DESCRIPTION	TYPE†
JTAG/EMULATION INTERFACE				
TCK	P13 L15	W18 M15	IEEE Standard 1149.1 test clock. TCK is normally a free-running clock signal with a 50% duty cycle. The changes on the test access port (TAP) of input signals TDI and TMS are clocked into the TAP controller, instruction register, or selected test data register on the rising edge of TCK. Changes at the TAP output signal TDO occur on the falling edge of TCK.	I
RTCK	T14 N15	Y17 U19	ARM926EJ-S return clock emulation	I/O
RTDX.D[0]	M16	M14	Emulation data transmit	I/O
RTDX.D[1]	L13	P18	Emulation data transmit	I/O
RTDX.D[2]	L15	M15	Emulation data transmit	I/O
RTDX.D[3]	K13	N20	Emulation data transmit	I/O
TDI	U17 U15	Y19 P14	IEEE Standard 1149.1 test data input. TDI is clocked into the selected register (instruction or data) on the rising edge of TCK.	I
TDO	T15 P11	AA19 W14	IEEE Standard 1149.1 test data output. The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK. TDO is in the high-impedance state except when the scanning of data is in progress.	O
TMS	M10 L14	V17 P19	IEEE Standard 1149.1 test mode select. This serial control input is clocked into the TAP controller on the rising edge of TCK.	I
$\overline{\text{TRST}}$	R13 P7	Y18 Y8	IEEE Standard 1149.1 test reset. $\overline{\text{TRST}}$, when high, gives the IEEE standard 1149.1 scan system control of the operations of the device. If $\overline{\text{TRST}}$ is not connected, or driven low, the device operates in its functional mode, and the IEEE standard 1149.1 signals are ignored.	I
EMU1	N11 P12	W17 V15	Emulation pin 1. When $\overline{\text{TRST}}$ is driven high, EMU1 is used as an interrupt to or from the emulator system and is defined as input/output by way of the IEEE standard 1149.1 scan system.	I/O
EMU0	U16 U7	V16 W8	EMU0 V16 Emulation pin 0. When $\overline{\text{TRST}}$ is driven high, EMU0 is used as an interrupt to or from the emulator system and is defined as input/output by way of the IEEE standard 1149.1 scan system.	I/O

† I = Input, O = Output, Z = High-Impedance

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Table 2–5. Signal Description (Continued)

SIGNAL	ZDY BALL#	ZZG BALL#	DESCRIPTION	TYPE†
SHARED GENERAL-PURPOSE IO MODULES (GPIOs)				
GPIO63	E15	E18	General-Purpose IOs module 4. Each GPIO pin can be used by either the DSP core or the MPU core. Control of each GPIO pin between the two cores is selected by the MPU via control registers. Each GPIO pin may also be configured to cause an interrupt to its respective core processor.	I/O
GPIO62	J5	M7		
	G13	G20		
GPIO61	B17	D19		
GPIO60	K2	M8		
GPIO59	J1	L3		
GPIO58	R8	R11		
	P4	W4		
GPIO57	M8	V11		
	H12	H19		
GPIO56	P12	V15		
GPIO55	N7	P11		
	N9	W13		
GPIO54	F16	G21		
GPIO53	G15	H15		
GPIO52	G14	H18		
GPIO51	G17	H20		
GPIO50	K17	M18		
GPIO49	K15	L14		
GPIO48	M11	V20		

† I = Input, O = Output, Z = High-Impedance

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Table 2–5. Signal Description (Continued)

SIGNAL	ZDY BALL#	ZZG BALL#	DESCRIPTION	TYPE†
SHARED GENERAL-PURPOSE IO MODULES (GPIOs) (CONTINUED)				
GPIO47	P14	U18	General-Purpose IOs module 3. Each GPIO pin can be used by either the DSP core or the MPU core. Control of each GPIO pin between the two cores is selected by the MPU via control registers. Each GPIO pin may also be configured to cause an interrupt to its respective core processor.	I/O
GPIO46	R15	W21		
GPIO45	R17	N14		
GPIO44	R16	P15		
GPIO43	U15	P14		
GPIO42	U14	W16		
GPIO41	N12	AA20		
GPIO40	R12	W15		
GPIO39	R11	AA15		
	G16	J15		
GPIO38	M9	R14		
	J12	L15		
GPIO37	U13	V14		
	K12	M19		
GPIO36	U12	R13		
GPIO35	H16	J18		
	D12	C16		
GPIO34	H15	J19		
	E11	A17		
GPIO33	H17	J14		
	A13	G13		
GPIO32	J11	K18		
	B14	B17		

† I = Input, O = Output, Z = High-Impedance

Table 2–5. Signal Description (Continued)

SIGNAL	ZDY BALL#	ZZG BALL#	DESCRIPTION	TYPE†
SHARED GENERAL-PURPOSE IO MODULES (GPIOs) (CONTINUED)				
GPIO31	H13 A15	K19 C17	General-Purpose IOs module 2. Each GPIO pin can be used by either the DSP core or the MPU core. Control of each GPIO pin between the two cores is selected by the MPU via control registers. Each GPIO pin may also be configured to cause an interrupt to its respective core processor.	I/O
GPIO30	J14 F11	K15 D16		
GPIO29	J16 C13	K14 D17		
GPIO28	F17	G19		
GPIO27	P8 D16	Y10 C21		
GPIO26	R7	AA9		
GPIO25	T8	W9		
GPIO24	U3	V5		
GPIO23	T7	R10		
GPIO22	L8	P10		
GPIO21	N6	W7		
GPIO20	U5	Y6		
GPIO19	T5	AA5		
GPIO18	P11 U4	W14 R9		
GPIO17	L10 R4	Y15 V6		
GPIO16	T1	Y1		

† I = Input, O = Output, Z = High-Impedance

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Table 2–5. Signal Description (Continued)

SIGNAL	ZDY BALL#	ZZG BALL#	DESCRIPTION	TYPE†
SHARED GENERAL-PURPOSE IO MODULES (GPIOs) (CONTINUED)				
GPIO15	K16	M20	General-Purpose IOs module 1. Each GPIO pin can be used by either the DSP core or the MPU core. Control of each GPIO pin between the two cores is selected by the MPU via control registers. Each GPIO pin may also be configured to cause an interrupt to its respective core processor.	I/O
GPIO14	K14	N21		
GPIO13	L17	N19		
GPIO12	L16 R5	N18 W6		
GPIO11	K13 U6	N20 V7		
GPIO10	L6	V2		
GPIO9	U7	W8		
GPIO8	P7	Y8		
GPIO7	L15 U8 P6	M15 V9 Y5		
GPIO6	L14	P19		
GPIO5	K3	P3		
GPIO4	M17	P20		
GPIO3	L13 J6	P18 N8		
GPIO2	M16 C12	M14 D15		
GPIO1	M15	R19		
GPIO0	N17	R18		

† I = Input, O = Output, Z = High-Impedance

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Table 2–5. Signal Description (Continued)

SIGNAL	ZDY BALL#	ZZG BALL#	DESCRIPTION	TYPE†
MPU GENERAL-PURPOSE IO (MPUIOs)				
MPUIO15	F13	E19	MPU general-purpose I/O. MPUIO pins may only be used by the MPU core.	I/O
MPUIO14	J13 N14	L18 U20		
MPUIO13	D17	E20		
MPUIO12	J17 T4	L19 W5		
MPUIO11	T9	W10		
MPUIO10	U9 E16	V10 H14		
MPUIO9	P9 E17	W11 F19		
MPUIO8	F15	G18		
MPUIO7	U9	V10		
MPUIO6	C17 P9	D20 W11		
MPUIO5	N16 T4	T20 W5		
MPUIO4	M14	T19		
MPUIO3	R6	V8		
MPUIO2	L12	N15		
MPUIO1	N15 P15	U19 V19		
MPUIO0	F14 U12	F18 R13		
KEYBOARD MATRIX INTERFACE				
KB.C[7:0]	P15 R16 F17 D16 E15 B17 C17 F14	V19 P15 G19 C21 E18 D19 D20 F18	Keyboard matrix column outputs. KB.Cx column outputs are used in conjunction with the KB.Rx row inputs to implement a 6 x 5 or 8 x 8 keyboard matrix.	O
KB.R[7:0]	K16 K14 L17 F13 D17 E16 E17 F15	M20 N21 N19 E19 E20 H14 F19 G18	Keyboard matrix row inputs. KB.Rx row inputs are used in conjunction with the KB.Cx column outputs to implement a 6 x 5 or 8 x 8 keyboard matrix.	I
LED PULSE GENERATOR (LPG)				
LED1	L13	P18	LED pulse generator output 1. LED1 produces a static or pulsing output used to drive an external LED indicator.	O
LED2	M14	T19	LED pulse generator output 2. LED2 produces a static or pulsing output used to drive an external LED indicator.	O
PULSE-WIDTH TONE (PWT) AND PULSE-WIDTH LIGHT (PWL) INTERFACE				
PWL	K15	L14	Pulse-width light output. The PWL output pin provides a pseudo-random modulated voltage output used for LCD or keypad backlighting.	O
PWT	K17	M18	Pulse-width tone output. The PWT output pin provides a modulated output for use with an external buzzer.	O

† I = Input, O = Output, Z = High-Impedance

Table 2–5. Signal Description (Continued)

SIGNAL	ZDY BALL#	ZZG BALL#	DESCRIPTION	TYPE†
GENERAL-PURPOSE TIMERS				
TIMER.EVENT3	L14	P19	Event capture input signal for GP timer 3	I
TIMER.EVENT4	M17	P20	Event capture input signal for GP timer 4	I
TIMER.EXTCLK	L16	N18	Input clock for the GP timers	I
TIMER.PWM2	K16	M20	PWM output of GP timer 2	O
TIMER.PWM1	K15	L14	PWM output of GP timer 1	O
TIMER.PWM0	K17	M18	PWM output of GP timer 0	O
EMBEDDED TRACE MACROCELL™ (ETM™) INTERFACE				
ETM.CLK	G16	J15	ETM9™ trace clock	O
ETM.PSTAT[5:0]	K13 M16 L13 J13 J12 K12	N20 M14 P18 L18 L15 M19	ETM9 trace pipe state bits	O
ETM.D[7:0]	H16 H15 H17 J11 H13 J14 J16 J17	J18 J19 J14 K18 K19 K15 K14 L19	ETM9 trace packet bits	O
ETM.SYNC[1:0]	L15 H12	M15 H19	ETM9 trace synchronization bits	O
DEVICE CLOCK PINS				
CLK32K_IN	T11	P13	32-kHz clock input. Digital CMOS 32-kHz clock input driven by an external 32-kHz oscillator if the internal 32-kHz oscillator is not used.	I
CLK32K_OUT	U12	R13	32-kHz clock output. Clock output reflecting the internal 32-kHz clock.	O
OSC32K_IN	U11	V13	32-kHz crystal XI connection. Analog clock input to 32-kHz oscillator for use with external crystal.	I
OSC32K_OUT	U10	AA13	32-kHz crystal XO connection. Analog output from 32-kHz oscillator for use with external crystal.	O
SYS_CLK_IN	P5	Y4	System clock main input clock at 19.2-MHz or 12/13-MHz	I
SYS_CLK_OUT	F10	B15	System clock can be output on this pin.	O
OSC1_IN	R2	Y2	Base crystal XI connection. Analog input to base oscillator for use with external crystal or to be driven by external 19.2-MHz or 12/13-MHz oscillator.	I
OSC1_OUT	P2	W3	Base crystal XO connection. Analog output from base oscillator for use with external 19.2-MHz or 12/13-MHz crystal.	O
BCLK	L10	Y15	General-purpose clock output that can be configured to run at 12 or 13 MHz (depending on base oscillator frequency) or 48 MHz. BCLK can be configured to drive constantly or only when the BCLKREQ signal is asserted active-high.	O
BCLKREQ	R12	W15	BCLK clock request. Active-high request input that allows an external device to request that BCLK be driven.	I
MCLK	U3	V5	General-purpose master clock output that may be configured to run at 12 or 13 MHz (depending on base oscillator frequency) or 48 MHz. MCLK can be configured to drive constantly or only when the MCLKREQ signal is asserted active-high.	O
MCLKREQ	T7	R10	MCLK clock request. Active-high request input that allows an external device to request that MCLK be driven.	I

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Table 2–5. Signal Description (Continued)

SIGNAL	ZDY BALL#	ZZG BALL#	DESCRIPTION	TYPE†
RESET LOGIC PINS				
PWRON_RESET	N8	R12	Reset input to device. Active-low asynchronous reset input resets the entire OMAP5912 device.	I
MPU_RST	N14	U20	MPU reset input. Active-low asynchronous reset input resets the MPU core. NOTE: MPU_RST must meet minimum specified pulse width requirements and must be free of glitching to guard against potential operational issues.	I
RST_OUT	N12	AA20	Reset output. Active-low output is asserted when RST_OUT is active (after synchronization).	O
INTERRUPTS AND MISCELLANEOUS CONTROL AND CONFIGURATION PINS				
MPU_BOOT	H14	J20	MPU boot mode. When MPU_BOOT is low, the MPU boots internally from chip-select 0. When MPU_BOOT is high and if the device is an emulation device, the MPU externally boots from chip-select 3 of EMIFS. Protocol (address/data multiplexed or address/data non-multiplexed) is determined by the value on GPIO1.	I
BFAIL/EXT_FIQ	T17	W19	Battery power failure and external FIQ interrupt input. BFAIL can be used to gate certain input pins when battery power is low or failing. The pins that can be gated are configured via software. This pin can also optionally be used as an external FIQ interrupt source to the MPU. The function of this pin is configurable via software.	I
EXT_DMA_REQ0	L12	N15	External DMA request. EXT_DMA_REQ0 provides DMA request inputs which external devices can use to trigger system DMA transfers. The system DMA must be configured in software to respond to these external requests.	I
EXT_DMA_REQ1	M14	T19	External DMA request. EXT_DMA_REQ1 provides DMA request inputs which external devices may use to trigger system DMA transfers. The system DMA must be configured in software to respond to these external requests.	I
LOW_PWR	N16	T20	Low-power request output. This active-high output indicates that the OMAP5912 device is in a LOW_PWR sleep mode. During reset and functional modes, LOW_PWR is driven low. This signal can be used to indicate a low-power state to external power management devices in a system, or it can be used as a chip-select to external SDRAM memory to minimize current consumption while the SDRAM is in self-refresh and the OMAP5912 device is in sleep mode.	O
LOW_POWER	P4	W4	Output from ultra low-power device (ULPD)	O
RTC_ON_NOFF	P10	Y12	Active-low asynchronous reset signal if real-time clock (RTC) is used.	I
RTC_WAKE_INT	N9	W13	RTC wake-up interrupt. RTC periodic interrupt to external power device to restart the main power supplies when RTC times out.	O
EXT_MASTER_REQ	T7	R10	External master request. If the base clock is provided by an external device instead of an on-chip oscillator, a high level on this output indicates to the external device that the clock must be driven. A low level indicates that the OMAP5912 device is in sleep mode and the 12- or 13-MHz external clock source is not necessary.	O
RST_HOST_OUT	N9	W13	A software-controllable reset or shutdown output to an external device	O
CONF	R14	V18	OMAP5912 configuration input	I

† I = Input, O = Output, Z = High-Impedance

Table 2–5. Signal Description (Continued)

SIGNAL	ZDY BALL#	ZZG BALL#	DESCRIPTION	TYPE†
POWER SUPPLIES				
CV _{DD}	C11 K5 M7 T16	A15 M2 Y9 Y20	Core supply voltage. Supplies power to OMAP5912 core logic and low-voltage sections of I/O.	Power
CV _{DD1}	T3	AA3	Core supply voltage 1. Supplies power to OMAP5912 core logic.	Power
CV _{DD2}	H7 G9 G8	A3 A9 E2	Core supply voltage 2. Supplies power to the MPU subsystem logic and memory.	Power
CV _{DD3}	G10 H11 K11 J10	B13 B20 J21 R20	Core supply voltage 3. Supplies power to the DSP subsystem logic and memory. If the DSP system is not used, can be grounded after the isolation control in ULPD is set.	Power
CV _{DDRTC}	L9	W12	Core supply voltage for the RTC. Supplies power to the RTC core logic. Can be connected to CV _{DD} if the RTC is not used as a standalone.	Power
CV _{DDA}	P17	Y21	Analog supply voltage. Supplies power to the analog phase-locked loop (APLL) used to provide 48-MHz clock to peripherals such as USB, UART, or MMC/SD/SDIO peripherals. Note: The voltage to this supply pin must be kept as clean as possible to maximize performance by minimizing clock jitter.	Power
CV _{DDDLL}	A9	A11	Core supply voltage for the digitally controlled delay element (calibration module) used to control read and write timings to external dual data rate (DDR) SDRAM. It is recommended that an RC (R = 10 Ω, C = 100 nF) low-pass filter be implemented externally to filter switching noises.	Power
DV _{DD1}	C14 G12	A19 E21	I/O supply voltage 1. Supplies power to the majority of peripheral I/O buffers. DV _{DD1} can be connected in common with the other DV _{DD} supplies if the same operating voltage is desired.	Power
DV _{DD2}	U2	AA2	I/O supply voltage 2. Supplies power to the internal USB transceiver buffers of USB port 0. DV _{DD2} can optionally be used for USB connect and disconnect detection by connecting DV _{DD2} to the power from the USB bus in the system. DV _{DD2} can be connected in common with the other DV _{DD} supplies if the same operating voltage is desired.	Power
DV _{DD3}	T6	Y7	I/O supply voltage 3. Supplies power to the MCSI2 and McBSP2 peripheral I/O buffers as well as to GPIO[9:8] I/O buffers. The DV _{DD3} supply can operate within a high-voltage or low-voltage range. DV _{DD3} can be connected in common with the other DV _{DD} supplies if the same operating voltage is desired.	Power
DV _{DD4}	D6 D7 D8 D11	A5 A7 B10 B14	I/O supply voltage 4. Supplies power to the DDR/SDRAM interface I/O buffers. The DV _{DD4} supply can operate within a high-voltage or low-voltage range. DV _{DD4} can be connected in common with the other DV _{DD} supplies if the same operating voltage is desired.	Power
DV _{DD5}	B1 G1 L3	C2 H2 R1	I/O supply voltage 5. Supplies power to the flash interface I/O buffers. The DV _{DD5} supply can operate within a high-voltage or low-voltage range. DV _{DD5} can be connected in common with the other DV _{DD} supplies if the same operating voltage is desired.	Power
DV _{DD6}	T10	AA11	I/O supply voltage 6. Supplies power to the MMC/SD1 interface I/O buffers. DV _{DD6} can be connected in common with the other DV _{DD} supplies if the same operating voltage is desired.	Power

† I = Input, O = Output, Z = High-Impedance

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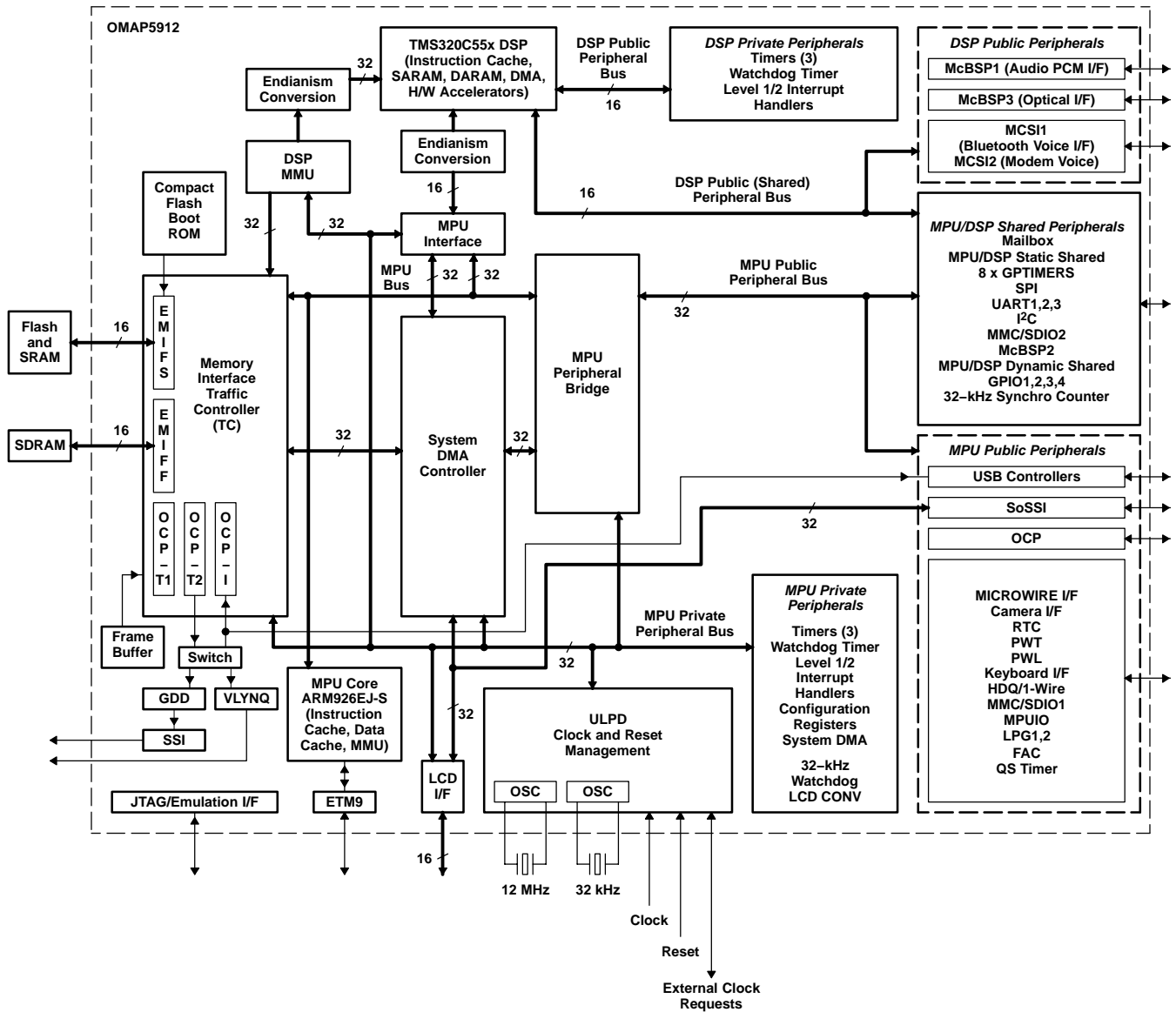
Table 2–5. Signal Description (Continued)

SIGNAL	ZDY BALL#	ZZG BALL#	DESCRIPTION	TYPE†
POWER SUPPLIES (CONTINUED)				
DV _{DD7}	T13	Y16	I/O supply voltage 7. Supplies power to the McBSP3, MCS11, UART, and USB port 1 I/O buffers. DV _{DD7} can be connected in common with the other DV _{DD} supplies if the same operating voltage is desired.	Power
DV _{DD8}	J15	L21	I/O supply voltage 8. Supplies power to the camera interface (I/F) and embedded trace macrocell (ETM) I/O buffers. DV _{DD8} can be connected in common with the other DV _{DD} supplies if the same operating voltage is desired.	Power
DV _{DD9}	M13	U21	I/O supply voltage 9. Supplies power to the GPIO (except GPIO[9:8]), MPUIO, and MICROWIRE I/O buffers. DV _{DD9} can be connected in common with the other DV _{DD} supplies if the same operating voltage is desired.	Power
DV _{DDRTC}	R10	V12	I/O supply voltage for the RTC I/O. (RTC_ON_NOFF, RTC_WAKE_INT, CLK32K_IN, CLK32K_OUT, OSC32K_OUT, OSC32K_IN, PWRON_RESET). DV _{DDRTC} can be connected in common with the other DV _{DD} supplies if the same operating voltage is desired and the RTC is not used in standalone.	Power
LDO.FILTER	H1	J1	A regulated supply is delivered by an embedded LDO to the DPLL macro(s). The regulated supply is available on the bond pad. A decoupling capacitor of 1 μ F must be connected externally between LDO.FILTER and the ground.	Power
V _{SS}	F6 E13 E5 G7 F12 K10 K9 H9 H10 M12 J9 R9 M6 K8 L11 N5 H8 G11 N13 L7	A13 A21 B1 B5 B7 B16 F20 G1 K2 K20 N1 P12 R21 U2 W20 Y3 Y13 AA1 AA7 AA21	Common ground for all core and I/O-Voltage supplies.	Power

† I = Input, O = Output, Z = High-Impedance

3 Functional Overview

The following functional overview is based on the block diagram in Figure 3–1.



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Figure 3–1. OMAP5912 Functional Block Diagram

3.1 Functional Block Diagram Features

The OMAP5912 device includes the following functional blocks:

- ARM9TDMI™-based (ARM926EJ-S) MPU core
 - 16K-byte instruction cache and 8K-byte data cache
 - Memory Management Units (MMUs) with Translation Look-Aside Buffer (TLB)
 - L1 16K-byte, four-way, set-associative instruction cache
 - L1 8K-byte, four-way, set-associative data cache with buffer
- MPU interrupt handler level 1
- Embedded Trace Macrocell module, ETM version 2.a in a 13-bit mode configuration or in a 17-bit demultiplexed mode configuration
- C55x DSP subsystem
 - 48K-word single-access RAM (SARAM) (96K bytes)
 - 32K-word dual-access RAM (DARAM) (64K bytes)
 - 16K-word ROM (32K bytes)
 - 24K-byte instruction cache
 - Six-channel DMA controller
 - Hardware Accelerators for DCT, iDCT, pixel interpolation, and motion estimation
 - L1 cache (24K bytes)
 - DSP interrupt handler level 1 in the C55x DSP core
 - Embedded emulator interface through JTAG port
- DSP Memory Management Unit (MMU) configured by the MPU
- DSP level 2 interrupt handler, which enables connection to 16 additional interrupt lines outside OMAP through the DSP interrupt interface. The priority of each interrupt line is controlled by software.
- Four mailboxes for DSP/MPU communications. Each mailbox is implemented with 2 x 16-bit registers. When a write is done into a register by one processor, it generates an interrupt, released by the read access of the other processor.
 - Two Read/Write accessible by MPU, read-only by the DSP
 - Two Read/Write accessible by the DSP, read-only by the MPU
- External LCD controller support in addition to the OMAP LCD controller
 - LCD controller with its own tearing effect logic
- Memory traffic controller
 - External memory interface slow (EMIFS). Connects to external device memories such as Flash and SRAM. This interface enables 16-bit data accesses and provides four chip-selects, each of which can support up to 128M bytes of address space with a 25-bit address bus.
 - External memory interface fast (EMIFF). Connects to external dual data rate (DDR) SDRAM with 16-bit data accesses. It supports connection to a maximum of 128M bytes of SDRAM. The address width is 16 bits with two bank-selection bits. This provides interfacing with a maximum of 4 banks of 64M x 16-bit SDRAM memory with DDR capability.
- Emulator interface through JTAG port
- Programmable DPLL
- Endianism conversion for DSP. The DSP uses big-endian format. The MPU and OMAP chip use little-endian format.

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- MPU private peripherals (accessible only by the MPU)
 - Three 32-bit general-purpose timers
 - Watchdog timer
 - Level 1/Level 2 interrupt handlers
 - Configuration register for pin-multiplexing and other device-level configurations
 - CompactFlash controller
 - LCD controller supporting monochrome panels or STN and TFT color panels
 - LCDCONV to provide 18-bit (instead of 16-bit) to the LCD interface
- DSP private peripherals (accessible only by the DSP)
 - Three 32-bit general-purpose timers
 - Watchdog timer
 - Level1/Level 2 interrupt handlers
- MPU public peripherals (accessible by the MPU and the system DMA)
 - USB interface
 - Display interface SoSSI
 - Camera interface providing connectivity to CMOS image sensors
 - Compact camera port
 - MICROWIRE serial interface
 - Real-time clock (RTC) module
 - Pulse-width tone (PWT)
 - Pulse-width light (PWL)
 - Keyboard interface (6 x 5 or 8 x 8 matrix)
 - HDQ/1-Wire interface for serial communication to battery management devices
 - Multimedia card/secure digital (MMC/SDIO1) or SPI port
 - Up to 16 MPU general-purpose I/Os (MPUIOs)
 - LED pulse generator (LPG)
 - Frame adjustment counter (FAC)
 - 32-kHz OS timer
- DSP public peripherals (accessible by: DSP, DSP DMA, and the MPU via the MPU interface)
 - Two multichannel buffered serial ports (McBSP1 and 3)
 - Two multichannel serial interfaces (MCSI1 and 2)
- MPU/DSP shared peripherals (controlling processor is selected by the MPU)
 - Four mailboxes for interprocessor communications
 - Eight general-purpose timers
 - Serial port interface (SPI)
 - Three UARTs (UART1 and UART3 have SIR mode for IrDA operation)

- Inter-integrated circuit (I²C) multimode master and slave interface
- Multimedia card/secure digital (MMC/SDIO2)
- Multichannel buffered serial port (McBSP2)
- Up to 64 general-purpose I/O pins with interrupt capability to either processor
- 32-kHz synchro counter
- MPU/DSP shared peripherals (accessible via OCP-T2 Port)
 - VLYNQ interface
 - SSI interface

3.2 MPU Memory Maps

3.2.1 MPU Global Memory Map

The MPU has a unified address space; therefore, the internal and external memories for program and data, as well as peripheral registers and configuration registers, are all accessed within the same address space. The MPU space is always addressed using byte addressing. Table 3–1 provides a high level illustration of the entire MPU addressable space. More details about the peripheral and configuration registers are provided in Section 3.2.2, MPU Subsystem Registers Memory Map.

Table 3–1. OMAP5912 MPU Global Memory Map

DEVICE NAME	START ADDRESS (HEX)	END ADDRESS (HEX)	SIZE	DATA ACCESS TYPE	COMMENT
EMIFS					
CS0	0000 0000	03FF FFFF	64M bytes		
Boot ROM	0000 0000	0000 FFFF	64K bytes	32-bit Ex/R	
Reserved Boot ROM	0001 0000	0003 FFFF	192K bytes	32-bit Ex/R	
Reserved	0004 0000	01FF FFFF			
NOR FLASH	0200 0000	03FF FFFF	32M bytes	8/16/32-bit EX/R/W	16-bit or 32-bit organized
CS1	0400 0000	07FF FFFF	64M bytes		
NOR FLASH	0400 0000	07FF FFFF	64M bytes	8/16/32-bit EX/R/W	16-bit or 32-bit organized
CS2	0800 0000	0BFF FFFF	64M bytes		
NOR FLASH	0800 0000	0BFF FFFF	64M bytes	8/16/32-bit EX/R/W	16-bit or 32-bit organized
CS3	0C00 0000	0FFF FFFF	64M bytes		
NOR FLASH	0C00 0000	0FFF FFFF	64M bytes	8/16/32-bit EX/R/W	16-bit or 32-bit organized
EMIFF					
SDRAM External	1000 0000	17FF FFFF	128M bytes	16-bit EX/R/W	
Reserved	1800 0000	1FFF FFFF			
L3 OCP T1					
Frame Buffer	2000 0000	2003 E7FF	250K bytes	32-bit EX/R/W	
Reserved	2003 E800	2FFF FFFF			
L3 OCP T2					
SSI Mapping	3000 0000	3000 0FFF	4K bytes		
GDD Mapping	3000 1000	3000 1FFF	4K bytes		
VLYNQ Config	3000 2000	3000 21FF	512 bytes		
Reserved	3000 2200	30FF FFFF			Cannot use simultaneously with GDD/SSI
VLYNQ Config	3100 0000	34FF FFFF	64M bytes		
Reserved	3500 0000	7FFF FFFF			

NOTE: CS1 and CS2 can be split to provide up to four chip selects. In this case, each chip select can support 32M bytes of NOR Flash memory.

CS1a	0x0400 0000	0x05FF FFFF	32M bytes
CS1b	0x0600 0000	0x07FF FFFF	32M bytes
CS2a	0x0800 0000	0x09FF FFFF	32M bytes
CS2b	0x0A00 0000	0x0BFF FFFF	32M bytes

Table 3–1. OMAP5912 MPU Global Memory Map (Continued)

DEVICE NAME	START ADDRESS (HEX)	END ADDRESS (HEX)	SIZE	DATA ACCESS TYPE	COMMENT
DSP MPUI Interface					
MPUI memory+ MPUI peripheral	E000 0000	E101 FFFF			Reserved Memory Space
Reserved	E102 0000	FFFF FFFF			
Peripheral and Control Registers					
Reserved	F000 0000	FFFA FFFF			
OMAP5912 Peripherals	FFFB 0000	FFFE FFFF			
Reserved	FFFF 0000	FFFF FFFF			

NOTE: CS1 and CS2 can be split to provide up to four chip selects. In this case, each chip select can support 32M bytes of NOR Flash memory.

CS1a	0x0400 0000	0x05FF FFFF	32M bytes
CS1b	0x0600 0000	0x07FF FFFF	32M bytes
CS2a	0x0800 0000	0x09FF FFFF	32M bytes
CS2b	0x0A00 0000	0x0BFF FFFF	32M bytes

3.2.2 MPU Subsystem Registers Memory Map

The MPU accesses peripheral and configuration registers in the same way that internal and external memory are accessed. The following tables specify the MPU base addresses where each set of registers is accessed. All accesses to these registers must utilize the appropriate access width (8-, 16-, or 32-bit-wide accesses) as indicated in the tables. Accessing registers with the incorrect access width are illegal.

WARNING: Access to Reserved areas is illegal.

3.2.2.1 MPU Private Peripheral Registers

The MPU private peripheral registers include the following:

- MPU Level 2 Interrupt Handler Registers
- LCDCONV Registers
- LCD Controller Registers
- MPU Timer1 Registers
- MPU Timer2 Registers
- MPU Timer3 Registers
- MPU Watchdog Timer Registers
- MPU Level 1 Interrupt Handler Registers
- System DMA Controller Registers

Table 3–2. MPU Level 2 Interrupt Handler Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:0000	MPU_L2_ITR	Interrupt Register	32	R/W	0000 0000h
FFFE:0004	MPU_L2_MIR	Interrupt Mask Register	32	R/W	FFFFFFFFh
FFFE:0008	RESERVED	Reserved			
FFFE:000C	RESERVED	Reserved			
FFFE:0010	MPU_L2_SIR_IRQ	Interrupt Encoded Source (IRQ) Register	32	R	0000 0000h
FFFE:0014	MPU_L2_SIR_FIQ	Interrupt Encoded Source (FIQ) Register	32	R	0000 0000h
FFFE:0018	MPU_L2_CONTROL	Interrupt Control Register	32	R/W	0000 0000h
FFFE:001C	MPU_L2_ILR0	Interrupt Priority Level For IRQ 0 Register	32	R/W	0000 0000h
FFFE:0020	MPU_L2_ILR1	Interrupt Priority Level For IRQ 1 Register	32	R/W	0000 0000h
FFFE:0024	MPU_L2_ILR2	Interrupt Priority Level For IRQ 2 Register	32	R/W	0000 0000h
FFFE:0028	MPU_L2_ILR3	Interrupt Priority Level For IRQ 3 Register	32	R/W	0000 0000h
FFFE:002C	MPU_L2_ILR4	Interrupt Priority Level For IRQ 4 Register	32	R/W	0000 0000h
FFFE:0030	MPU_L2_ILR5	Interrupt Priority Level For IRQ 5 Register	32	R/W	0000 0000h
FFFE:0034	MPU_L2_ILR6	Interrupt Priority Level For IRQ 6 Register	32	R/W	0000 0000h
FFFE:0038	MPU_L2_ILR7	Interrupt Priority Level For IRQ 7 Register	32	R/W	0000 0000h
FFFE:003C	MPU_L2_ILR8	Interrupt Priority Level For IRQ 8 Register	32	R/W	0000 0000h
FFFE:0040	MPU_L2_ILR9	Interrupt Priority Level For IRQ 9 Register	32	R/W	0000 0000h
FFFE:0044	MPU_L2_ILR10	Interrupt Priority Level For IRQ 10 Register	32	R/W	0000 0000h

Table 3–2. MPU Level 2 Interrupt Handler Registers (Continued)

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:0048	MPU_L2_ILR11	Interrupt Priority Level For IRQ 11 Register	32	R/W	0000 0000h
FFFE:004C	MPU_L2_ILR12	Interrupt Priority Level For IRQ 12 Register	32	R/W	0000 0000h
FFFE:0050	MPU_L2_ILR13	Interrupt Priority Level For IRQ 13 Register	32	R/W	0000 0000h
FFFE:0054	MPU_L2_ILR14	Interrupt Priority Level For IRQ 14 Register	32	R/W	0000 0000h
FFFE:0058	MPU_L2_ILR15	Interrupt Priority Level For IRQ 15 Register	32	R/W	0000 0000h
FFFE:005C	MPU_L2_ILR16	Interrupt Priority Level For IRQ 16 Register	32	R/W	0000 0000h
FFFE:0060	MPU_L2_ILR17	Interrupt Priority Level For IRQ 17 Register	32	R/W	0000 0000h
FFFE:0064	MPU_L2_ILR18	Interrupt Priority Level For IRQ 18 Register	32	R/W	0000 0000h
FFFE:0068	MPU_L2_ILR19	Interrupt Priority Level For IRQ 19 Register	32	R/W	0000 0000h
FFFE:006C	MPU_L2_ILR20	Interrupt Priority Level For IRQ 20 Register	32	R/W	0000 0000h
FFFE:0070	MPU_L2_ILR21	Interrupt Priority Level For IRQ 21 Register	32	R/W	0000 0000h
FFFE:0074	MPU_L2_ILR22	Interrupt Priority Level For IRQ 22 Register	32	R/W	0000 0000h
FFFE:0078	MPU_L2_ILR23	Interrupt Priority Level For IRQ 23 Register	32	R/W	0000 0000h
FFFE:007C	MPU_L2_ILR24	Interrupt Priority Level For IRQ 24 Register	32	R/W	0000 0000h
FFFE:0080	MPU_L2_ILR25	Interrupt Priority Level For IRQ 25 Register	32	R/W	0000 0000h
FFFE:0084	MPU_L2_ILR26	Interrupt Priority Level For IRQ 26 Register	32	R/W	0000 0000h
FFFE:0088	MPU_L2_ILR27	Interrupt Priority Level For IRQ 27 Register	32	R/W	0000 0000h
FFFE:008C	MPU_L2_ILR28	Interrupt Priority Level For IRQ 28 Register	32	R/W	0000 0000h
FFFE:0090	MPU_L2_ILR29	Interrupt Priority Level For IRQ 29 Register	32	R/W	0000 0000h
FFFE:0094	MPU_L2_ILR30	Interrupt Priority Level For IRQ 30 Register	32	R/W	0000 0000h
FFFE:0098	MPU_L2_ILR31	Interrupt Priority Level For IRQ 31 Register	32	R/W	0000 0000h
FFFE:009C	MPU_L2_ISR	Software Interrupt Set Register	32	W	0000 0000h
FFFE:00A0	MPU_L2_STATUS	Status Register	32	R	0000 0000h
FFFE:00A4	MPU_L2_OCP_CFG	OCP Configuration Register	32	R/W	0000 0000h
FFFE:00A8	MPU_L2_INTH_REV	Interrupt Controller Revision ID	32	R	0000 0000h

Table 3–3. LCDCONV Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:3000 – FFFE:301F	LCDCONV_R_LOOK_UP	R Look-up Table Register File	32	R/W	undefined
FFFE:3020 – FFFE:303F	LCDCONV_B_LOOK_UP	B Look-up Table Register File	32	R/W	undefined
FFFE:3040 – FFFE:307F	LCDCONV_G_LOOK_UP	G Look-up Table Register File	32	R/W	undefined
FFFE:3080	LCDCONV_CONTROL	Control Register	32	R/W	0000h
FFFE:3084	LCDCONV_DEV_REV	Device Revision Register	32	R	undefined

Table 3–4. LCD Controller Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:C000	LCD_CONTROL	LCD Control Register	32	R/W	xx00 0000h
FFFE:C004	LCD_TIMING0	LCD Timing0 Register	32	R/W	0000 000Fh
FFFE:C008	LCD_TIMING1	LCD Timing1 Register	32	R/W	0000 0000h
FFFE:C00C	LCD_TIMING2	LCD Timing2 Register	32	R/W	xx00 0000h
FFFE:C010	LCD_STATUS	LCD Status Register	32	R/W	xxxx xxx0h
FFFE:C014	LCD_SUBPANEL	LCD Subpanel Display Register	32	R/W	xx00 0000h
FFFE:C018	LCD_LINEINT	LCD Line Interrupt Register	32	R/W	xxxx xx00h
FFFE:C01C	LCD_DISPLAYSTATUS	LCD Display Status Register	32	R/W	xxxx x3FFh

Table 3–5. MPU Timer1 Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:C500	MPU_CNTL_TIMER1	MPU Timer1 Control Register	32	R/W	0000 0000h
FFFE:C504	MPU_LOAD_TIMER1	MPU Timer1 Load Register	32	W	undefined
FFFE:C508	MPU_READ_TIMER1	MPU Timer1 Read Register	32	R	undefined

Table 3–6. MPU Timer2 Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:C600	MPU_CNTL_TIMER2	MPU Timer2 Control Register	32	R/W	0000 0000h
FFFE:C604	MPU_LOAD_TIMER2	MPU Timer2 Load Register	32	W	undefined
FFFE:C608	MPU_READ_TIMER2	MPU Timer2 Read Register	32	R	undefined

Table 3–7. MPU Timer3 Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:C700	MPU_CNTL_TIMER3	MPU Timer3 Control Register	32	R/W	0000 0000h
FFFE:C704	MPU_LOAD_TIMER3	MPU Timer3 Load Register	32	W	undefined
FFFE:C708	MPU_READ_TIMER3	MPU Timer3 Read Register	32	R	undefined

Table 3–8. MPU Watchdog Timer Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:C800	MPU_WDT_CNTL_TIMER	MPU Watchdog Timer Control Register	32	R/W	0000 0E02h
FFFE:C804	MPU_WDT_LOAD_TIMER	MPU Watchdog Timer Load Register	32	W	xxxx FFFFh
FFFE:C804	MPU_WDT_READ_TIMER	MPU Watchdog Timer Read Register	32	R	xxxx FFFFh
FFFE:C808	MPU_WDT_TIMER_MODE	MPU Watchdog Timer Mode Register	32	R/W	0000 8000h

Table 3–9. MPU Level 1 Interrupt Handler Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:CB00	MPU_L1_ITR	Interrupt Register	32	R/W	0000 0000h
FFFE:CB04	MPU_L1_MIR	Interrupt Mask Register	32	R/W	FFFF FFFFh
FFFE:CB08	RESERVED	Reserved			
FFFE:CB0C	RESERVED	Reserved			
FFFE:CB10	MPU_L1_SIR_IRQ_CODE	Interrupt Encoded Source (IRQ) Register	32	R	0000 0000h
FFFE:CB14	MPU_L1_SIR_FIQ_CODE	Interrupt Encoded Source (FIQ) Register	32	R	0000 0000h
FFFE:CB18	MPU_L1_CONTROL	Interrupt Control Register	32	R/W	0000 0000h
FFFE:CB1C	MPU_L1_ILR0	Interrupt Priority Level For IRQ 0 Register	32	R/W	0000 0000h
FFFE:CB20	MPU_L1_ILR1	Interrupt Priority Level For IRQ 1 Register	32	R/W	0000 0000h
FFFE:CB24	MPU_L1_ILR2	Interrupt Priority Level For IRQ 2 Register	32	R/W	0000 0000h
FFFE:CB28	MPU_L1_ILR3	Interrupt Priority Level For IRQ 3 Register	32	R/W	0000 0000h
FFFE:CB2C	MPU_L1_ILR4	Interrupt Priority Level For IRQ 4 Register	32	R/W	0000 0000h
FFFE:CB30	MPU_L1_ILR5	Interrupt Priority Level For IRQ 5 Register	32	R/W	0000 0000h
FFFE:CB34	MPU_L1_ILR6	Interrupt Priority Level For IRQ 6 Register	32	R/W	0000 0000h
FFFE:CB38	MPU_L1_ILR7	Interrupt Priority Level For IRQ 7 Register	32	R/W	0000 0000h
FFFE:CB3C	MPU_L1_ILR8	Interrupt Priority Level For IRQ 8 Register	32	R/W	0000 0000h
FFFE:CB40	MPU_L1_ILR9	Interrupt Priority Level For IRQ 9 Register	32	R/W	0000 0000h
FFFE:CB44	MPU_L1_ILR10	Interrupt Priority Level For IRQ 10 Register	32	R/W	0000 0000h
FFFE:CB48	MPU_L1_ILR11	Interrupt Priority Level For IRQ 11 Register	32	R/W	0000 0000h
FFFE:CB4C	MPU_L1_ILR12	Interrupt Priority Level For IRQ 12 Register	32	R/W	0000 0000h
FFFE:CB50	MPU_L1_ILR13	Interrupt Priority Level For IRQ 13 Register	32	R/W	0000 0000h
FFFE:CB54	MPU_L1_ILR14	Interrupt Priority Level For IRQ 14 Register	32	R/W	0000 0000h
FFFE:CB58	MPU_L1_ILR15	Interrupt Priority Level For IRQ 15 Register	32	R/W	0000 0000h
FFFE:CB5C	MPU_L1_ILR16	Interrupt Priority Level For IRQ 16 Register	32	R/W	0000 0000h
FFFE:CB60	MPU_L1_ILR17	Interrupt Priority Level For IRQ 17 Register	32	R/W	0000 0000h
FFFE:CB64	MPU_L1_ILR18	Interrupt Priority Level For IRQ 18 Register	32	R/W	0000 0000h
FFFE:CB68	MPU_L1_ILR19	Interrupt Priority Level For IRQ 19 Register	32	R/W	0000 0000h
FFFE:CB6C	MPU_L1_ILR20	Interrupt Priority Level For IRQ 20 Register	32	R/W	0000 0000h
FFFE:CB70	MPU_L1_ILR21	Interrupt Priority Level For IRQ 21 Register	32	R/W	0000 0000h
FFFE:CB74	MPU_L1_ILR22	Interrupt Priority Level For IRQ 22 Register	32	R/W	0000 0000h
FFFE:CB78	MPU_L1_ILR23	Interrupt Priority Level For IRQ 23 Register	32	R/W	0000 0000h
FFFE:CB7C	MPU_L1_ILR24	Interrupt Priority Level For IRQ 24 Register	32	R/W	0000 0000h
FFFE:CB80	MPU_L1_ILR25	Interrupt Priority Level For IRQ 25 Register	32	R/W	0000 0000h
FFFE:CB84	MPU_L1_ILR26	Interrupt Priority Level For IRQ 26 Register	32	R/W	0000 0000h
FFFE:CB88	MPU_L1_ILR27	Interrupt Priority Level For IRQ 27 Register	32	R/W	0000 0000h
FFFE:CB8C	MPU_L1_ILR28	Interrupt Priority Level For IRQ 28 Register	32	R/W	0000 0000h
FFFE:CB90	MPU_L1_ILR29	Interrupt Priority Level For IRQ 29 Register	32	R/W	0000 0000h
FFFE:CB94	MPU_L1_ILR30	Interrupt Priority Level For IRQ 30 Register	32	R/W	0000 0000h
FFFE:CB98	MPU_L1_ILR31	Interrupt Priority Level For IRQ 31 Register	32	R/W	0000 0000h
FFFE:C9C	MPU_L1_ISR	Interrupt Priority Level For IRQ 0 Register	32	R/W	0000 0000h
FFFE:CBA0	MPU_L1_ENHANCED_CNTL	Enhanced Control Register	32	R/W	0000 0000h

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Table 3–10. System DMA Controller Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
TBD	TBD	TBD	TBD	TBD	TBD

3.2.2.2 MPU Public Peripheral Registers

The MPU public peripheral registers include the following:

- USB On-the-Go (OTG) Registers
- MICROWIRE Registers
- USB Client Registers
- Real-Time Clock (RTC) Registers
- MPUIO (Keyboard Included) Registers
- Pulse Width Light (PWL) Registers
- Pulse Width Tone (PWT) Registers
- MMC/SDIO1 Registers
- OS Timer 32-kHz Registers
- USB Host Registers
- Frame Adjustment Counter (FAC) Registers
- Specially Optimized Screen Interface (SoSSI) Registers
- HDQ/1-Wire Interface Registers
- LED Pulse Generator 1 (LPG1) Registers
- LED Pulse Generator 2 (LPG2) Registers

Table 3–11. USB On-the-Go (OTG) Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:0700	USB_OTG_REV	USB On The Go Revision Number	32	R	0000 0000h
FFFB:0704	USB_OTG_SYSCON1	USB On The Go Configuration Register 1	32	R/W	0000 0000h
FFFB:0708	USB_OTG_SYSCON2	USB On The Go Configuration Register 2	32	R/W	0000 0000h
FFFB:070C	USB_OTG_CTRL	USB On The Go Control Register	32	R/W	0000 0000h
FFFB:0710	USB_OTG_IRQ_EN	USB On The Go Interrupt Enable Register	32	R/W	0000 0000h
FFFB:0714	USB_OTG_IRQ_SRC	USB On The Go Interrupt Status Register	32	R/W	0000 0000h
FFFB:0718	USB_OTG_OUTCTRL	USB On The Go Output Pins Control Register	32	R/W	0000 0000h
FFFB:0720	USB_OTG_TEST	USB On The Go Test Register	32	R/W	0000 0000h
FFFB:07FC	USB_OTG_VC	USB On The Go Vendor Code Register	32	R	undefined

Table 3–12. MICROWIRE Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:3000	MWIRE_RDR	MICROWIRE Receive Data Register	16	R	undefined
FFFB:3000	MWIRE_TDR	MICROWIRE Transmit Data Register	16	W	undefined
FFFB:3004	MWIRE_CSR	MICROWIRE Control And Status Register	16	R/W	undefined
FFFB:3008	MWIRE_SR1	MICROWIRE Setup Register For CS0 And CS1	16	R/W	undefined
FFFB:300C	MWIRE_SR2	MICROWIRE Setup Register For CS2 And CS3	16	R/W	undefined
FFFB:3010	MWIRE_SR3	MICROWIRE Setup Register For Internal Clock	16	R/W	undefined
FFFB:3014	MWIRE_SR4	MICROWIRE Setup Register For Clock Polarity	16	R/W	undefined
FFFB:3018	MWIRE_SR5	MICROWIRE Setup Register For Transmit Mode	16	R/W	0000h

Table 3–13. USB Client Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
TBD	TBD	TBD	TBD	TBD	TBD

Table 3–14. Real-Time Clock (RTC) Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:4800	SECONDS_REG	RTC Seconds Register	8	R/W	00h
FFFB:4804	MINUTES_REG	RTC Minutes Register	8	R/W	00h
FFFB:4808	HOURS_REG	RTC Hours Register	8	R/W	00h
FFFB:480C	DAYS_REG	RTC Days Register	8	R/W	01h
FFFB:4810	MONTHS_REG	RTC Months Register	8	R/W	01h
FFFB:4814	YEARS_REG	RTC Years Register	8	R/W	00h
FFFB:4818	WEEK_REG	RTC Weeks Register	8	R/W	00h
FFFB:481C		Reserved			
FFFB:4820	ALARM_SECONDS_REG	RTC Alarm Seconds Register	8	R/W	00h
FFFB:4824	ALARM_MINUTES_REG	RTC Alarm Minutes Register	8	R/W	00h
FFFB:4828	ALARM_HOURS_REG	RTC Alarm Hours Register	8	R/W	00h
FFFB:482C	ALARM_DAYS_REG	RTC Alarm Days Register	8	R/W	01h
FFFB:4830	ALARM_MONTHS_REG	RTC Alarm Months Register	8	R/W	01h
FFFB:4834	ALARM_YEARS_REG	RTC Alarm Years Register	8	R/W	00h
FFFB:4838 – FFFB:483F		Reserved			
FFFB:4840	RTC_CTRL_REG	RTC Control Register	8	R/W	00h
FFFB:4844	RTC_STATUS_REG	RTC Status Register	8	R/W	00h
FFFB:4848	RTC_INTERRUPTS_REG	RTC Interrupts Register	8	R/W	00h
FFFB:484C	RTC_COMP_LSB_REG	RTC Compensation LSB Register	8	R/W	00h
FFFB:4850	RTC_COMP_MSB_REG	RTC Compensation MSB Register	8	RW	00h
FFFB:4854	RTC_OSC_REG	RTC Oscillator Register	8	RW	0Bh

Table 3–15. MPUIO (Keyboard) Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:5000	MPUIO_INPUT_LATCH	MPUIO General Purpose Input Register	16	R	0000h
FFFB:5004	MPUIO_OUTPUT	MPUIO General Purpose Output Register	16	R/W	0000h
FFFB:5008	MPUIO_IO_CNTL	MPUIO In/Out Control Register for General-Purpose I/O	16	R/W	FFFFh
FFFB:5010	MPUIO_KBD_LATCH	MPUIO Keyboard Row Input Register	16	R	FFFFh
FFFB:5014	MPUIO_KBC	MPUIO Keyboard Column Output Register	16	R/W	FF00h
FFFB:5018	MPUIO_GPIO_EVENT	MPUIO GPIO Event Mode Register	16	R/W	0FE0h
FFFB:501C	MPUIO_GPIO_EDGE	MPUIO GPIO Interrupt Edge Register	16	R/W	0000h
FFFB:5020	MPUIO_KBD_INT	MPUIO Keyboard Interrupt Register	16	R	FFFFh
FFFB:5024	MPUIO_GPIO_INT	MPUIO GPIO Interrupt Register	16	R	0000h
FFFB:5028	MPUIO_KBD_MASKIT	MPUIO Keyboard Interrupt Mask Register	16	R/W	FFFEh
FFFB:502C	MPUIO_GPIO_MASKIT	MPUIO GPIO Interrupt Mask Register	16	R/W	0000h
FFFB:5030	MPUIO_GPIO_DBNC	MPUIO GPIO Debouncing Register	16	R/W	EF00h
FFFB:5034	MPUIO_GPIO_LATCH	MPUIO GPIO Latch Register	16	R	0000h

Table 3–16. Pulse Width Light (PWL) Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:5800	PWL_LEVEL	PWL Level Register	8	R/W	00h
FFFB:5804	PWL_CONTROL	PWL Control Register	8	R/W	00h

Table 3–17. Pulse Width Tone (PWT) Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:6000	PWT_FRC	PWT Frequency Control Register	8	R/W	00h
FFFB:6004	PWT_VRC	PWT Volume Control Register	8	R/W	00h
FFFB:6008	PWT_GCR	PWT General Control Register	8	R/W	00h

Table 3–18. MMC/SDIO1 Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:7800	MPU_MMC_CMD	MMC Command Register	16	R/W	0000h
FFFB:7804	MPU_MMC_ARGL	MMC Argument Register Low	16	R/W	0000h
FFFB:7808	MPU_MMC_ARGH	MMC Argument Register High	16	R/W	0000h
FFFB:780C	MPU_MMC_CON	MMC Module Configuration Register	16	R/W	0000h
FFFB:7810	MPU_MMC_STAT	MMC Module Status Register	16	R/W	0000h
FFFB:7814	MPU_MMC_IE	MMC System Interrupt Enable Register	16	R/W	0000h
FFFB:7818	MPU_MMC_CTO	MMC Command Time-Out Register	16	R/W	0000h
FFFB:781C	MPU_MMC_DTO	MMC Data Read Time-Out Register	16	R/W	0000h
FFFB:7820	MPU_MMC_DATA	MMC Data Access Register	16	R/W	0000h
FFFB:7824	MPU_MMC_BLEN	MMC Block Length Register	16	R/W	0000h
FFFB:7828	MPU_MMC_NBLK	MMC Number of Blocks Register	16	R/W	0000h
FFFB:782C	MPU_MMC_BUF	MMC Buffer Configuration Register	16	R/W	0000h

Table 3–18. MMC/SDIO1 Registers (Continued)

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:7830	MPU_MMC_SPI	MMC SPI Configuration Register	16	R/W	0000h
FFFB:7834	MPU_MMC_SDIO	MMC SDIO Configuration Register	16	R/W	0000h
FFFB:7838	MPU_MMC_SYST	MMC System Test Register	16	R/W	0000h
FFFB:783C	MPU_MMC_REV	MMC Module Revision Register	16	R	undefined
FFFB:7840	MPU_MMC_RSP0	MMC Command Response Register 0	16	R	0000h
FFFB:7844	MPU_MMC_RSP1	MMC Command Response Register 1	16	R	0000h
FFFB:7848	MPU_MMC_RSP2	MMC Command Response Register 2	16	R	0000h
FFFB:784C	MPU_MMC_RSP3	MMC Command Response Register 3	16	R	0000h
FFFB:7850	MPU_MMC_RSP4	MMC Command Response Register 4	16	R	0000h
FFFB:7854	MPU_MMC_RSP5	MMC Command Response Register 5	16	R	0000h
FFFB:7858	MPU_MMC_RSP6	MMC Command Response Register 6	16	R	0000h
FFFB:785C	MPU_MMC_RSP7	MMC Command Response Register 7	16	R	0000h
FFFB:7860	MPU_MMC_IOSR	MMC Command Response IOSR Register	16	R/W	0000h
FFFB:7864	MPU_MMC_SYSC	MMC System Control Register	16	R/W	0000h
FFFB:7868	MPU_MMC_SYSS	MMC System Status Register	16	R	0000h

Table 3–19. OS Timer 32-kHz Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:9000	OS_TIMER_TICK_VAL	OS Timer 32K Tick Value Register	32	R/W	00FF FFFFh
FFFB:9004	OS_TIMER_TICK_CNTR	OS Timer 32k Tick Counter Register	32	R	00FF FFFFh
FFFB:9008	OS_TIMER_CTRL	OS Timer 32k Timer Control Register	32	R/W	0000 0008h

Table 3–20. USB Host Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
TBD	TBD	TBD	TBD	TBD	TBD

Table 3–21. Frame Adjustment Counter (FAC) Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:A800	FAC_CNT	FAC Frame Adjustment Reference Counter Register	16	R/W	0000h
FFFB:A810	FAC_SYNC_CNT	FAC Sync Counter Register	16	R	0000h
FFFB:A814	FAC_START_CNT	FAC Start Counter Register	16	R	0000h
FFFB:A804	FAC_CNT_RSLT	FAC Frame Starter Count Register	16	R	0000h
FFFB:A808	FAC_CTRL	FAC Control Register	16	R/W	0000h
FFFB:A80C	FAC_STATUS	FAC Status Register	16	R	0000h

Table 3–22. Specially Optimized Screen Interface (SoSSI) Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:AC00	SOSSI_IDENT	SoSSI Identification Register	32	R/W	0000 0000h
FFFB:AC04	SOSSI_INIT1	SoSSI Timing For Display Register	32	R/W	C000 0000h
FFFB:AC08	SOSSI_INIT2	SoSSI Main Control Register	32	R/W	0000 000Ch
FFFB:AC0C	SOSSI_INIT3	SoSSI Main Control Register	32	R/W	0000 0047h
FFFB:AC10	SOSSI_FIFO	SoSSI FIFO Register	32	R/W	0000 0000h
FFFB:AC14	SOSSI_REOTABLE	SoSSI Reordering Table Register	32	R/W	0000 0000h
FFFB:AC18	SOSSI_TEARING	SoSSI Tearing Effect Register	32	R/W	0000 0000h
FFFB:AC1C	SOSSI_INIT1B	SoSSI Part of INIT1 Register	32	R/W	0000 0000h
FFFB:AC20	SOSSI_FIFOB	SoSSI Part of FIFO Register	32	W	0000 0000h

Table 3–23. HDQ/1-Wire Interface Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:C000	HDQ_TX_DATA	HDQ Transmit Register	32	R/W	0000 0000h
FFFB:C004	HDQ_RX_BUF	HDQ Receive Buffer Register	32	R	0000 0000h
FFFB:C008	HDQ_CNTL_STAT	HDQ Control and Status Register	32	R/W	0000 0000h
FFFB:C00C	HDQ_INT_STAT	HDQ Interrupt Status Register	32	R	0000 0000h

Table 3–24. LED Pulse Generator 1 (LPG1) Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:D000	LPG1_CNTL	LPG1 Control Register	8	R/W	00h
FFFB:D004	LPG1_PWR_MNGT	LPG1 Power Management Register	8	R/W	00h

Table 3–25. LED Pulse Generator 2 (LPG2) Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:D800	LPG2_CNTL	LPG2 Control Register	8	R/W	00h
FFFB:D804	LPG2_PWR_MNGT	LPG2 Power Management Register	8	R/W	00h

3.2.2.3 MPU/DSP Shared Peripheral Registers

The MPU public peripheral registers include the following:

- UART1 Registers
- UART2 Registers
- SPI1 Registers
- McBSP2 Registers
- General-Purpose Timer 1 Registers
- General-Purpose Timer 2 Registers
- General-Purpose Timer 3 Registers
- General-Purpose Timer 4 Registers
- General-Purpose Timer 5 Registers
- I²C1 Registers
- General-Purpose Timer 6 Registers
- General-Purpose Timer 7 Registers
- MMC/SDIO2 Registers
- UART 3 Registers
- MPU GPIO3 Registers
- MPU GPIO4 Registers
- 32-kHz Synchro Count Registers
- General-Purpose Timer 8 Registers
- MPU GPIO1 Registers
- MPU GPIO2 Registers
- MPU/DSP Shared Mailbox Registers

Table 3–26. UART1 Registers

DSP WORD ADDRESS	MPU BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 8000h	FFFB:0000	UART1_RHR	UART1 receive holding register	8	R	Undefined
0x00 8000h	FFFB:0000	UART1_THR	UART1 transmit holding register	8	W	Undefined
0x00 8000h	FFFB:0000	UART1_DLL	UART1 divisor latch low register	8	R/W	00h
0x00 8001h	FFFB:0004	UART1_IER	UART1 interrupt enable register	8	R/W	00h
0x00 8001h	FFFB:0004	UART1_DLH	UART1 divisor latch high register	8	R/W	00h
0x00 8002h	FFFB:0008	UART1_IIR	UART1 interrupt identification register	8	R	01h
0x00 8002h	FFFB:0008	UART1_FCR	UART1 FIFO control register	8	W	00h
0x00 8002h	FFFB:0008	UART1_EFR	UART1 enhanced feature register	8	R/W	00h
0x00 8003h	FFFB:000C	UART1_LCR	UART1 line control register	8	R/W	00h
0x00 8004h	FFFB:0010	UART1_MCR	UART1 modem control register	8	R/W	00h
0x00 8004h	FFFB:0010	UART1_XON1	UART1 XON1 register	8	R/W	00h
0x00 8005h	FFFB:0014	UART1_LSR	UART1 mode register	8	R	60h
0x00 8005h	FFFB:0014	UART1_XON2	UART1 XON2 register	8	R/W	00h
0x00 8006h	FFFB:0018	UART1_MSR	UART1 modem status register	8	R	Undefined
0x00 8006h	FFFB:0018	UART1_TCR	UART1 transmission control register	8	R/W	0Fh
0x00 8006h	FFFB:0018	UART1_XOFF1	UART1 XOFF1 register	8	R/W	00h
0x00 8007h	FFFB:001C	UART1_SPR	UART1 scratchpad register	8	R/W	00h
0x00 8007h	FFFB:001C	UART1_TLR	UART1 trigger level register	8	R/W	00h
0x00 8007h	FFFB:001C	UART1_XOFF2	UART1 XOFF2 register	8	R/W	00h
0x00 8008h	FFFB:0020	UART1_MDR1	UART1 mode definition 1 register	8	R/W	07h
0x00 8009h	FFFB:0024	UART1_MDR2	UART1 mode definition register 2	8	R/W	00h
0x00 800Ah	FFFB:0028	UART1_SFLSR	UART1 status FIFO line status register	8	R	00h
0x00 800Ah	FFFB:0028	UART1_TXFLL	UART1 transmit frame length low	8	W	00h
0x00 800Bh	FFFB:002C	UART1_RESUME	UART1 resume register	8	R	00h
0x00 800Bh	FFFB:002C	UART1_TXFLH	UART1 transmit frame length high	8	W	00h
0x00 800Ch	FFFB:0030	UART1_SFREGL	UART1 status FIFO low register	8	R	Undefined
0x00 800Ch	FFFB:0030	UART1_RXFLL	UART1 receive frame length low	8	W	00h
0x00 800Dh	FFFB:0034	UART1_SFREGH	UART1 status FIFO high register	8	R	Undefined
0x00 800Dh	FFFB:0034	UART1_RXFLH	UART1 receive frame length high	8	W	00h
0x00 800Eh	FFFB:0038	UART1_UASR	UART1 autobauding status register	8	R	00h
0x00 800Eh	FFFB:0038	UART1_BLR	UART1 BOF control register	8	R/W	40h
0x00 800Fh	FFFB:003C	UART1_ACREG	UART1 auxiliary control register	8	R/W	00h
0x00 8010h	FFFB:0040	UART1_SCR	UART1 supplementary control register	8	R/W	00h
0x00 8011h	FFFB:0044	UART1_SSR	UART1 supplementary status register	8	R	00h
0x00 8012h	FFFB:0048	UART1_EBLR	UART1 BOF length register	8	R/W	00h
0x00 8013h	FFFB:004C		Reserved			
0x00 8014h	FFFB:0050	UART1_MVR	UART1 module version register	8	R	–
0x00 8015h	FFFB:0054	UART1_SYSC	UART1 system configuration register	8	R/W	00h
0x00 8016h	FFFB:0058	UART1_SYSS	UART1 system status register	8	R/W	00h
0x00 8017h	FFFB:005C	UART1_WER	UART1 wake-up enable register	8	R/W	7Fh

Table 3–27. UART2 Registers

DSP WORD ADDRESS	MPU BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 8400h	FFFB:0800	UART2_RHR	UART2 receive holding register	8	R	Undefined
0x00 8400h	FFFB:0800	UART2_THR	UART2 transmit holding register	8	W	Undefined
0x00 8400h	FFFB:0800	UART2_DLL	UART2 divisor latch low register	8	R/W	00h
0x00 8401h	FFFB:0804	UART2_IER	UART2 interrupt enable register	8	R/W	00h
0x00 8401h	FFFB:0804	UART2_DLH	UART2 divisor latch high register	8	R/W	00h
0x00 8402h	FFFB:0808	UART2_IIR	UART2 interrupt identification register	8	R	01h
0x00 8402h	FFFB:0808	UART2_FCR	UART2 FIFO control register	8	W	00h
0x00 8402h	FFFB:0808	UART2_EFR	UART2 enhanced feature register	8	R/W	00h
0x00 8403h	FFFB:080C	UART2_LCR	UART2 line control register	8	R/W	00h
0x00 8404h	FFFB:0810	UART2_MCR	UART2 modem control register	8	R/W	00h
0x00 8404h	FFFB:0810	UART2_XON1	UART2 XON1 register	8	R/W	00h
0x00 8405h	FFFB:0814	UART2_LSR	UART2 mode register	8	R	60h
0x00 8405h	FFFB:0814	UART2_XON2	UART2 XON2 register	8	R/W	00h
0x00 8406h	FFFB:0818	UART2_MSR	UART2 modem status register	8	R	Undefined
0x00 8406h	FFFB:0818	UART2_TCR	UART2 transmission control register	8	R/W	0Fh
0x00 8406h	FFFB:0818	UART2_XOFF	UART2 XOFF1 register	8	R/W	00h
0x00 8407h	FFFB:081C	UART2_SPR	UART2 scratchpad register	8	R/W	00h
0x00 8407h	FFFB:081C	UART2_TLR	UART2 trigger level register	8	R/W	00h
0x00 8407h	FFFB:081C	UART2_XOFF2	UART2 XOFF2 register	8	R/W	00h
0x00 8408h	FFFB:0820	UART2_MDR1	UART2 mode definition 1 register	8	R/W	07h
0x00 8409h	FFFB:0824	UART2_MDR2	UART2 mode definition register 2	8	R/W	00h
0x00 840Ah	FFFB:0828	UART2_SFLSR	UART2 status FIFO line status register	8	R	00h
0x00 840Ah	FFFB:0828	UART2_TXFLL	UART2 transmit frame length low	8	W	00h
0x00 840Bh	FFFB:082C	UART2_RESUME	UART2 resume register	8	R	00h
0x00 840Bh	FFFB:082C	UART2_TXFLH	UART2 transmit frame length high	8	W	00h
0x00 840Ch	FFFB:0830	UART2_SFREGL	UART2 status FIFO low register	8	R	Undefined
0x00 840Ch	FFFB:0830	UART2_RXFLL	UART2 receive frame length low	8	W	00h
0x00 840Dh	FFFB:0834	UART2_SFREGH	UART2 status FIFO high register	8	R	Undefined
0x00 840Dh	FFFB:0834	UART2_RXFLH	UART2 receive frame length high	8	W	00h
0x00 840Eh	FFFB:0838	UART2_UASR	UART2 autobauding status register	8	R	00h
0x00 840Eh	FFFB:0838	UART2_BLR	UART2 BOF control register	8	R/W	40h
0x00 840Fh	FFFB:083C	UART2_ACREG	UART2 auxiliary control register	8	R/W	00h
0x00 8410h	FFFB:0840	UART2_SCR	UART2 supplementary control register	8	R/W	00h
0x00 8411h	FFFB:0844	UART2_SSR	UART2 supplementary status register	8	R	00h
0x00 8412h	FFFB:0848	UART2_EBLR	UART2 BOF length register	8	R/W	00h
0x00 8413h	FFFB:084C		Reserved			
0x00 8414h	FFFB:0850	UART2_MVR	UART2 module version register	8	R	–
0x00 8415h	FFFB:0854	UART2_SYSC	UART2 system configuration register	8	R/W	00h
0x00 8416h	FFFB:0858	UART2_SYSS	UART2 system status register	8	R/W	00h
0x00 8417h	FFFB:085C	UART2_WER	UART2 wake-up enable register	8	R/W	7Fh

Table 3–28. SPI1 Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:0C00	SPI1_REV	Module Version Register	32	R	0000 00Xh
FFFB:0C04 – FFFB:0C0F		Reserved			
FFFB:0C10	SPI1_SCR	System Configuration Register	32	R/W	0000 0020h
FFFB:0C14	SPI1_SSR	System Status Register	32	R	0000 0000h
FFFB:0C18	SPI1_ISR	Interrupt Status Register	32	R/W	0000 0000h
FFFB:0C1C	SPI1_IER	Interrupt Enable Register	32	R/W	0000 0000h
FFFB:0C20		Reserved			
FFFB:0C24	SPI1_SET1	Setup 1 Register	32	R/W	0000 0000h
FFFB:0C28	SPI1_SET2	Setup 2 Register	32	R/W	0000 0000h
FFFB:0C2C	SPI1_CTRL	Control Register	32	R/W	0000 0000h
FFFB:0C30	SPI1_DSR	Data Status Register	32	R	0000 0002h
FFFB:0C34	SPI1_TX	Transmit Register	32	R/W	0000 0000h
FFFB:0C38	SPI1_RX	Receive Register	32	R	0000 0000h
FFFB:0C3C	SPI1_TEST	Test Register	32	R/W	0000 0000h

Table 3–29. McBSP2 Registers

MPU BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:1000	MCBSP2_DRR2	McBSP2 Data receive register 2	16	R/W	0000h
FFFB:1002	MCBSP2_DRR1	McBSP2 Data receive register 1	16	R/W	0000h
FFFB:1004	MCBSP2_DXR2	McBSP2 Data transmit register 2	16	R/W	0000h
FFFB:1006	MCBSP2_DXR1	McBSP2 Data transmit register 1	16	R/W	0000h
FFFB:1008	MCBSP2_SPCR2	McBSP2 Serial port control register 2	16	R/W	0000h
FFFB:100A	MCBSP2_SPCR1	McBSP2 Serial port control register 1	16	R/W	0000h
FFFB:100C	MCBSP2_RCR2	McBSP2 Receive control register 2	16	R/W	0000h
FFFB:100E	MCBSP2_RCR1	McBSP2 Receive control register 1	16	R/W	0000h
FFFB:1010	MCBSP2_XCR2	McBSP2 Transmit control register 2	16	R/W	0000h
FFFB:1012	MCBSP2_XCR1	McBSP2 Transmit control register 1	16	R/W	0000h
FFFB:1014	MCBSP2_SRGR2	McBSP2 Sample rate generator register 2	16	R/W	2000h
FFFB:1016	MCBSP2_SRGR1	McBSP2 Sample rate generator register 1	16	R/W	0001h
FFFB:1018	MCBSP2_MCR2	McBSP2 Multichannel register 2	16	R/W	0000h
FFFB:101A	MCBSP2_MCR1	McBSP2 Multichannel register 1	16	R/W	0000h
FFFB:101C	MCBSP2_RCERA	McBSP2 Receive channel enable register partition A	16	R/W	0000h
FFFB:101E	MCBSP2_RCERB	McBSP2 Receive channel enable register partition B	16	R/W	0000h
FFFB:1020	MCBSP2_XCERA	McBSP2 Transmit channel enable register partition A	16	R/W	0000h
FFFB:1022	MCBSP2_XCERB	McBSP2 Transmit channel enable register partition B	16	R/W	0000h
FFFB:1024	MCBSP2_PCR0	McBSP2 Pin control register 0	16	R/W	0000h
FFFB:1026	MCBSP2_RCERC	McBSP2 Receive channel enable register partition C	16	R/W	0000h
FFFB:1028	MCBSP2_RCERD	McBSP2 Receive channel enable register partition D	16	R/W	0000h
FFFB:102A	MCBSP2_XCERC	McBSP2 Transmit channel enable register partition C	16	R/W	0000h
FFFB:102C	MCBSP2_XCERD	McBSP2 Transmit channel enable register partition D	16	R/W	0000h
FFFB:102E	MCBSP2_RCERE	McBSP2 Receive channel enable register partition E	16	R/W	0000h
FFFB:1030	MCBSP2_RCERF	McBSP2 Receive channel enable register partition F	16	R/W	0000h

Table 3–29. McBSP2 Registers (Continued)

MPU BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:1032	MCBSP2_XCERE	McBSP2 Transmit channel enable register partition E	16	R/W	0000h
FFFB:1034	MCBSP2_XCERF	McBSP2 Transmit channel enable register partition F	16	R/W	0000h
FFFB:1036	MCBSP2_RCERG	McBSP2 Receive channel enable register partition G	16	R/W	0000h
FFFB:1038	MCBSP2_RCERH	McBSP2 Receive channel enable register partition H	16	R/W	0000h
FFFB:103A	MCBSP2_XCERG	McBSP2 Transmit channel enable register partition G	16	R/W	0000h
FFFB:103C	MCBSP2_XCERH	McBSP2 Transmit channel enable register partition H	16	R/W	0000h
FFFB:103E	MCBSP2_REV	McBSP2 Version register	16	R/W	0011h

Table 3–30. General-Purpose Timer1 Registers

DSP WORD ADDRESS	MPU BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 8A00h	FFFB:1400	GPTMR1_TIDR	GPTimer1 Identification Register	16/32	R	0000 0010h
0x00 8A02h	FFFB:1404		Reserved			
0x00 8A08h	FFFB:1410	GPTMR1_TIOCP_CFG	GPTimer1 OCP Configuration Register	16/32	R/W	0000 0000h
0x00 8A0Ah	FFFB:1414	GPTMR1_TISTAT	GPTimer1 System Status Register	16/32	R	0000 0000h
0x00 8A0Ch	FFFB:1418	GPTMR1_TISR	GPTimer1 Status Register	16/32	R/W	0000 0000h
0x00 8A0Eh	FFFB:141C	GPTMR1_TIER	GPTimer1 Interrupt Enable Register	16/32	R/W	0000 0000h
0x00 8A10h	FFFB:1420	GPTMR1_TWERM	GPTimer1 Wake Up Enable Register	16/32	R/W	0000 0000h
0x00 8A12h	FFFB:1424	GPTMR1_TCLR	GPTimer1 Control Register	16/32	R/W	0000 0000h
0x00 8A14h	FFFB:1428	GPTMR1_TCRR	GPTimer1 Counter Register	16/32	R/W	0000 0000h
0x00 8A16h	FFFB:142C	GPTMR1_TLDR	GPTimer1 Load Register	16/32	R/W	0000 0000h
0x00 8A18h	FFFB:1430	GPTMR1_TTGR	GPTimer1 Trigger Register	16/32	R/W	FFFF FFFFh
0x00 8A1Ah	FFFB:1434	GPTMR1_TWPS	GPTimer1 Write Posted Register	16/32	R	0000 0000h
0x00 8A1Ch	FFFB:1438	GPTMR1_TMAR	GPTimer1 Match Register	16/32	R/W	0000 0000h
0x00 8A1Eh	FFFB:143C	GPTMR1_TCAR	GPTimer1 Capture Register	16/32	R	0000 0000h
0x00 8A20h	FFFB:1440	GPTMR1_TSICR	GPTimer1 Synchronization Interface Control Register	16/32	R/W	0000 0004h

Table 3–31. General-Purpose Timer2 Registers

DSP WORD ADDRESS	MPU BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 8E00h	FFFB:1C00	GPTMR2_TIDR	GPTimer2 Identification Register	16/32	R	0000 0010h
0x00 8E02h	FFFB:1C04		Reserved			
0x00 8E08h	FFFB:1C10	GPTMR2_TIOCP_CFG	GPTimer2 OCP Configuration Register	16/32	R/W	0000 0000h
0x00 8E0Ah	FFFB:1C14	GPTMR2_TISTAT	GPTimer2 System Status Register	16/32	R	0000 0000h
0x00 8E0Ch	FFFB:1C18	GPTMR2_TISR	GPTimer2 Status Register	16/32	R/W	0000 0000h
0x00 8E0Eh	FFFB:1C1C	GPTMR2_TIER	GPTimer2 Interrupt Enable Register	16/32	R/W	0000 0000h
0x00 8E10h	FFFB:1C20	GPTMR2_TWERM	GPTimer2 Wake Up Enable Register	16/32	R/W	0000 0000h
0x00 8E12h	FFFB:1C24	GPTMR2_TCLR	GPTimer2 Control Register	16/32	R/W	0000 0000h
0x00 8E14h	FFFB:1C28	GPTMR2_TCRR	GPTimer2 Counter Register	16/32	R/W	0000 0000h
0x00 8E16h	FFFB:1C2C	GPTMR2_TLDR	GPTimer2 Load Register	16/32	R/W	0000 0000h
0x00 8E18h	FFFB:1C30	GPTMR2_TTGR	GPTimer2 Trigger Register	16/32	R/W	FFFF FFFFh
0x00 8E1Ah	FFFB:1C34	GPTMR2_TWPS	GPTimer2 Write Posted Register	16/32	R	0000 0000h
0x00 8E1Ch	FFFB:1C38	GPTMR2_TMAR	GPTimer2 Match Register	16/32	R/W	0000 0000h

Table 3–31. General-Purpose Timer2 Registers (Continued)

DSP WORD ADDRESS	MPU BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 8E1Eh	FFFB:1C3C	GPTMR2_TCAR	GPTimer2 Capture Register	16/32	R	0000 0000h
0x00 8E20h	FFFB:1C40	GPTMR2_TSICR	GPTimer2 Synchronization Interface Control Register	16/32	R/W	0000 0004h

Table 3–32. General-Purpose Timer3 Registers

DSP WORD ADDRESS	MPU BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 9200h	FFFB:2400	GPTMR3_TIDR	GPTimer3 Identification Register	16/32	R	0000 0010h
0x00 9202h	FFFB:2404		Reserved			
0x00 9208h	FFFB:2410	GPTMR3_TIOCP_CFG	GPTimer3 OCP Configuration Register	16/32	R/W	0000 0000h
0x00 920Ah	FFFB:2414	GPTMR3_TISTAT	GPTimer3 System Status Register	16/32	R	0000 0000h
0x00 920Ch	FFFB:2418	GPTMR3_TISR	GPTimer3 Status Register	16/32	R/W	0000 0000h
0x00 920Eh	FFFB:241C	GPTMR3_TIER	GPTimer3 Interrupt Enable Register	16/32	R/W	0000 0000h
0x00 9210h	FFFB:2420	GPTMR3_TWER	GPTimer3 Wake Up Enable Register	16/32	R/W	0000 0000h
0x00 9212h	FFFB:2424	GPTMR3_TCLR	GPTimer3 Control Register	16/32	R/W	0000 0000h
0x00 9214h	FFFB:2428	GPTMR3_TCRR	GPTimer3 Counter Register	16/32	R/W	0000 0000h
0x00 9216h	FFFB:242C	GPTMR3_TLDR	GPTimer3 Load Register	16/32	R/W	0000 0000h
0x00 9218h	FFFB:2430	GPTMR3_TTGR	GPTimer3 Trigger Register	16/32	R/W	FFFF FFFFh
0x00 921Ah	FFFB:2434	GPTMR3_TWPS	GPTimer3 Write Posted Register	16/32	R	0000 0000h
0x00 921Ch	FFFB:2438	GPTMR3_TMAR	GPTimer3 Match Register	16/32	R/W	0000 0000h
0x00 921Eh	FFFB:243C	GPTMR3_TCAR	GPTimer3 Capture Register	16/32	R	0000 0000h
0x00 9220h	FFFB:2440	GPTMR3_TSICR	GPTimer3 Synchronization Interface Control Register	16/32	R/W	0000 0004h

Table 3–33. General-Purpose Timer4 Registers

DSP WORD ADDRESS	MPU BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 9600h	FFFB:2C00	GPTMR4_TIDR	GPTimer4 Identification Register	16/32	R	0000 0010h
0x00 9602h	FFFB:2C04		Reserved			
0x00 9608h	FFFB:2C10	GPTMR4_TIOCP_CFG	GPTimer4 OCP Configuration Register	16/32	R/W	0000 0000h
0x00 960Ah	FFFB:2C14	GPTMR4_TISTAT	GPTimer4 System Status Register	16/32	R	0000 0000h
0x00 960Ch	FFFB:2C18	GPTMR4_TISR	GPTimer4 Status Register	16/32	R/W	0000 0000h
0x00 960Eh	FFFB:2C1C	GPTMR4_TIER	GPTimer4 Interrupt Enable Register	16/32	R/W	0000 0000h
0x00 9610h	FFFB:2C20	GPTMR4_TWER	GPTimer4 Wake Up Enable Register	16/32	R/W	0000 0000h
0x00 9612h	FFFB:2C24	GPTMR4_TCLR	GPTimer4 Control Register	16/32	R/W	0000 0000h
0x00 9614h	FFFB:2C28	GPTMR4_TCRR	GPTimer4 Counter Register	16/32	R/W	0000 0000h
0x00 9616h	FFFB:2C2C	GPTMR4_TLDR	GPTimer4 Load Register	16/32	R/W	0000 0000h
0x00 9618h	FFFB:2C30	GPTMR4_TTGR	GPTimer4 Trigger Register	16/32	R/W	FFFF FFFFh
0x00 961Ah	FFFB:2C34	GPTMR4_TWPS	GPTimer4 Write Posted Register	16/32	R	0000 0000h
0x00 961Ch	FFFB:2C38	GPTMR4_TMAR	GPTimer4 Match Register	16/32	R/W	0000 0000h
0x00 961Eh	FFFB:2C3C	GPTMR4_TCAR	GPTimer4 Capture Register	16/32	R	0000 0000h
0x00 9620h	FFFB:2C40	GPTMR4_TSICR	GPTimer4 Synchronization Interface Control Register	16/32	R/W	0000 0004h

Table 3–34. General-Purpose Timer5 Registers

DSP WORD ADDRESS	MPU BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 9A00h	FFFB:3400	GPTMR5_TIDR	GPTimer5 Identification Register	16/32	R	0000 0010h
0x00 9A02h	FFFB:3404		Reserved			
0x00 9A08h	FFFB:3410	GPTMR5_TIOCP_CFG	GPTimer5 OCP Configuration Register	16/32	R/W	0000 0000h
0x00 9A0Ah	FFFB:3414	GPTMR5_TISTAT	GPTimer5 System Status Register	16/32	R	0000 0000h
0x00 9A0Ch	FFFB:3418	GPTMR5_TISR	GPTimer5 Status Register	16/32	R/W	0000 0000h
0x00 9A0Eh	FFFB:341C	GPTMR5_TIER	GPTimer5 Interrupt Enable Register	16/32	R/W	0000 0000h
0x00 9A10h	FFFB:3420	GPTMR5_TWER	GPTimer5 Wake Up Enable Register	16/32	R/W	0000 0000h
0x00 9A12h	FFFB:3424	GPTMR5_TCLR	GPTimer5 Control Register	16/32	R/W	0000 0000h
0x00 9A14h	FFFB:3428	GPTMR5_TCRR	GPTimer5 Counter Register	16/32	R/W	0000 0000h
0x00 9A16h	FFFB:342C	GPTMR5_TLDR	GPTimer5 Load Register	16/32	R/W	0000 0000h
0x00 9A18h	FFFB:3430	GPTMR5_TTGR	GPTimer5 Trigger Register	16/32	R/W	FFFF FFFFh
0x00 9A1Ah	FFFB:3434	GPTMR5_TWPS	GPTimer5 Write Posted Register	16/32	R	0000 0000h
0x00 9A1Ch	FFFB:3438	GPTMR5_TMAR	GPTimer5 Match Register	16/32	R/W	0000 0000h
0x00 9A1Eh	FFFB:343C	GPTMR5_TCAR	GPTimer5 Capture Register	16/32	R	0000 0000h
0x00 9A20h	FFFB:3440	GPTMR5_TSICR	GPTimer5 Synchronization Interface Control Register	16/32	R/W	0000 0004h

Table 3–35. I²C1 Registers

MPU BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:3800	I2C1_REV	I ² C1 Module Version Register	16	R/W	0022h
FFFB:3804	I2C1_IE	I ² C1 Interrupt Enable Register	16	R/W	0000h
FFFB:3808	I2C1_STAT	I ² C1 Status Register	16	R	0000h
FFFB:380C		Reserved			
FFFB:3810	I2C1_SYSS	I ² C1 System Status Register	16	R	0000h
FFFB:3814	I2C1_BUF	I ² C1 Buffer Configuration Register	16	R/W	0000h
FFFB:3818	I2C1_CNT	I ² C1 Data Counter Register	16	R/W	0000h
FFFB:381C	I2C1_DATA	I ² C1 Data Access Register	16	R/W	0000h
FFFB:3820	I2C1_SYSC	I ² C1 System Configuration Register	16	R/W	0000h
FFFB:3824	I2C1_CON	I ² C1 Configuration Register	16	R/W	0000h
FFFB:3828	I2C1_OA	I ² C1 Own Address Register	16	R/W	0000h
FFFB:382C	I2C1_SA	I ² C1 Slave Address Register	16	R/W	03FFh
FFFB:3830	I2C1_PSC	I ² C1 Clock Prescaler Register	16	R/W	0000h
FFFB:3834	I2C1_SCLL	I ² C1 SCL Low Timer Register	16	R/W	0000h
FFFB:3838	I2C1_SCLH	I ² C1 SCL High Timer Register	16	R/W	0000h
FFFB:383C	I2C1_SYSTEST	I ² C1 System Test Register	16	R/W	0000h

Table 3–36. General-Purpose Timer6 Registers

DSP WORD ADDRESS	MPU BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 9E00h	FFFB:3C00	GPTMR6_TIDR	GPTimer6 Identification Register	16/32	R	0000 0010h
0x00 9E02h	FFFB:3C04		Reserved			
0x00 9E08h	FFFB:3C10	GPTMR6_TIOCP_CFG	GPTimer6 OCP Configuration Register	16/32	R/W	0000 0000h
0x00 9E0Ah	FFFB:3C14	GPTMR6_TISTAT	GPTimer6 System Status Register	16/32	R	0000 0000h
0x00 9E0Ch	FFFB:3C18	GPTMR6_TISR	GPTimer6 Status Register	16/32	R/W	0000 0000h
0x00 9E0Eh	FFFB:3C1C	GPTMR6_TIER	GPTimer6 Interrupt Enable Register	16/32	R/W	0000 0000h
0x00 9E10h	FFFB:3C20	GPTMR6_TWER	GPTimer6 Wake Up Enable Register	16/32	R/W	0000 0000h
0x00 9E12h	FFFB:3C24	GPTMR6_TCLR	GPTimer6 Control Register	16/32	R/W	0000 0000h
0x00 9E14h	FFFB:3C28	GPTMR6_TCRR	GPTimer6 Counter Register	16/32	R/W	0000 0000h
0x00 9E16h	FFFB:3C2C	GPTMR6_TLDR	GPTimer6 Load Register	16/32	R/W	0000 0000h
0x00 9E18h	FFFB:3C30	GPTMR6_TTGR	GPTimer6 Trigger Register	16/32	R/W	FFFF FFFFh
0x00 9E1Ah	FFFB:3C34	GPTMR6_TWPS	GPTimer6 Write Posted Register	16/32	R	0000 0000h
0x00 9E1Ch	FFFB:3C38	GPTMR6_TMAR	GPTimer6 Match Register	16/32	R/W	0000 0000h
0x00 9E1Eh	FFFB:3C3C	GPTMR6_TCAR	GPTimer6 Capture Register	16/32	R	0000 0000h
0x00 9E20h	FFFB:3C40	GPTMR6_TSICR	GPTimer6 Synchronization Interface Control Register	16/32	R/W	0000 0004h

Table 3–37. General-Purpose Timer7 Registers

DSP WORD ADDRESS	BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 BA00h	FFFB:7400	GPTMR7_TIDR	GPTimer7 Identification Register	16/32	R	0000 0010h
0x00 BA02h	FFFB:7404		Reserved			
0x00 BA08h	FFFB:7410	GPTMR7_TIOCP_CFG	GPTimer7 OCP Configuration Register	16/32	R/W	0000 0000h
0x00 BA0Ah	FFFB:7414	GPTMR7_TISTAT	GPTimer7 System Status Register	16/32	R	0000 0000h
0x00 BA0Ch	FFFB:7418	GPTMR7_TISR	GPTimer7 Status Register	16/32	R/W	0000 0000h
0x00 BA0Eh	FFFB:741C	GPTMR7_TIER	GPTimer7 Interrupt Enable Register	16/32	R/W	0000 0000h
0x00 BA10h	FFFB:7420	GPTMR7_TWER	GPTimer7 Wake Up Enable Register	16/32	R/W	0000 0000h
0x00 BA12h	FFFB:7424	GPTMR7_TCLR	GPTimer7 Control Register	16/32	R/W	0000 0000h
0x00 BA14h	FFFB:7428	GPTMR7_TCRR	GPTimer7 Counter Register	16/32	R/W	0000 0000h
0x00 BA16h	FFFB:742C	GPTMR7_TLDR	GPTimer7 Load Register	16/32	R/W	0000 0000h
0x00 BA18h	FFFB:7430	GPTMR7_TTGR	GPTimer7 Trigger Register	16/32	R/W	FFFF FFFFh
0x00 BA1Ah	FFFB:7434	GPTMR7_TWPS	GPTimer7 Write Posted Register	16/32	R	0000 0000h
0x00 BA1Ch	FFFB:7438	GPTMR7_TMAR	GPTimer7 Match Register	16/32	R/W	0000 0000h
0x00 BA1Eh	FFFB:743C	GPTMR7_TCAR	GPTimer7 Capture Register	16/32	R	0000 0000h
0x00 BA20h	FFFB:7440	GPTMR7_TSICR	GPTimer7 Synchronization Interface Control Register	16/32	R/W	0000 0004h

Table 3–38. MMC/SDIO2 Registers

MPU BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:7C00	MMC2_CMD	MMC2 Command Register	16	R/W	0000h
FFFB:7C04	MMC2_ARGL	MMC2 Argument Register Low	16	R/W	0000h
FFFB:7C08	MMC2_ARGH	MMC2 Argument Register High	16	R/W	0000h
FFFB:7C0C	MMC2_CON	MMC2 Module Configuration Register	16	R/W	0000h
FFFB:7C10	MMC2_STAT	MMC2 Module Status Register	16	R/W	0000h
FFFB:7C14	MMC2_IE	MMC2 System Interrupt Enable Register	16	R/W	0000h
FFFB:7C18	MMC2_CTO	MMC2 Command Time-Out Register	16	R/W	0000h
FFFB:7C1C	MMC2_DTO	MMC2 Data Read Time-Out Register	16	R/W	0000h
FFFB:7C20	MMC2_DATA	MMC2 Data Access Register	16	R/W	0000h
FFFB:7C24	MMC2_BLEN	MMC2 Block Length Register	16	R/W	0000h
FFFB:7C28	MMC2_NBLK	MMC2 Number of Blocks Register	16	R/W	0000h
FFFB:7C2C	MMC2_BUF	MMC2 Buffer Configuration Register	16	R/W	0000h
FFFB:7C30	MMC2_SPI	MMC2 SPI Configuration Register	16	R/W	0000h
FFFB:7C34	MMC2_SDIO	MMC2 SDIO Configuration Register	16	R/W	0000h
FFFB:7C38	MMC2_SYST	MMC2 System Test Register	16	R/W	0000h
FFFB:7C3C	MMC2_REV	MMC2 Module Revision Register	16	R	undefined
FFFB:7C40	MMC2_RSP0	MMC2 Command Response Register 0	16	R	0000h
FFFB:7C44	MMC2_RSP1	MMC2 Command Response Register 1	16	R	0000h
FFFB:7C48	MMC2_RSP2	MMC2 Command Response Register 2	16	R	0000h
FFFB:7C4C	MMC2_RSP3	MMC2 Command Response Register 3	16	R	0000h
FFFB:7C50	MMC2_RSP4	MMC2 Command Response Register 4	16	R	0000h
FFFB:7C54	MMC2_RSP5	MMC2 Command Response Register 5	16	R	0000h
FFFB:7C58	MMC2_RSP6	MMC2 Command Response Register 6	16	R	0000h
FFFB:7C5C	MMC2_RSP7	MMC2 Command Response Register 7	16	R	0000h
FFFB:7C60	MMC2_IOSR	MMC2 Command Response IOSR Register	16	R/W	0000h
FFFB:7C64	MMC2_SYSC	MMC2 System Control Register	16	R/W	0000h
FFFB:7C68	MMC2_SYSS	MMC2 System Status Register	16	R	0000h

Table 3–39. UART3 Registers

DSP WORD ADDRESS	MPU BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 CC00h	FFFB:9800	UART3_RHR	UART3 receive holding register	8	R	Undefined
0x00 CC00h	FFFB:9800	UART3_THR	UART3 transmit holding register	8	W	Undefined
0x00 CC00h	FFFB:9800	UART3_DLL	UART3 divisor latch low register	8	R/W	00h
0x00 CC01h	FFFB:9804	UART3_IER	UART3 interrupt enable register	8	R/W	00h
0x00 CC01h	FFFB:9804	UART3_DLH	UART3 divisor latch high register	8	R/W	00h
0x00 CC02h	FFFB:9808	UART3_IIR	UART3 interrupt identification register	8	R	01h
0x00 CC02h	FFFB:9808	UART3_FCR	UART3 FIFO control register	8	W	00h
0x00 CC02h	FFFB:9808	UART3_EFR	UART3 enhanced feature register	8	R/W	00h
0x00 CC03h	FFFB:980C	UART3_LCR	UART3 line control register	8	R/W	00h
0x00 CC04h	FFFB:9810	UART3_MCR	UART3 modem control register	8	R/W	00h
0x00 CC04h	FFFB:9810	UART1_XON1	UART3 XON1 register	8	R/W	00h
0x00 CC05h	FFFB:9814	UART3_LSR	UART3 mode register	8	R	60h

Table 3–39. UART3 Registers (Continued)

DSP WORD ADDRESS	MPU BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 CC05h	FFFB:9814	UART3_XON2	UART3 XON2 register	8	R/W	00h
0x00 CC06h	FFFB:9818	UART3_MSR	UART3 modem status register	8	R	Undefined
0x00 CC06h	FFFB:9818	UART3_TCR	UART3 transmission control register	8	R/W	0Fh
0x00 CC06h	FFFB:9818	UART3_XOFF1	UART3 XOFF1 register	8	R/W	00h
0x00 CC07h	FFFB:981C	UART3_SPR	UART3 scratchpad register	8	R/W	00h
0x00 CC07h	FFFB:981C	UART3_TLR	UART3 trigger level register	8	R/W	00h
0x00 CC07h	FFFB:981C	UART3_XOFF2	UART3 XOFF2 register	8	R/W	00h
0x00 CC08h	FFFB:9820	UART3_MDR1	UART3 mode definition 1 register	8	R/W	07h
0x00 CC09h	FFFB:9824	UART3_MDR2	UART3 mode definition register 2	8	R/W	00h
0x00 CC0Ah	FFFB:9828	UART3_SFLSR	UART3 status FIFO line status register	8	R	00h
0x00 CC0Ah	FFFB:9828	UART3_TXFLL	UART3 transmit frame length low	8	W	00h
0x00 CC0Bh	FFFB:982C	UART3_RESUME	UART3 resume register	8	R	00h
0x00 CC0Bh	FFFB:982C	UART3_TXFLH	UART3 transmit frame length high	8	W	00h
0x00 CC0Ch	FFFB:9830	UART3_SFREGL	UART3 status FIFO low register	8	R	Undefined
0x00 CC0Ch	FFFB:9830	UART3_RXFLL	UART3 receive frame length low	8	W	00h
0x00 CC0Dh	FFFB:9834	UART3_SFREGH	UART3 status FIFO high register	8	R	Undefined
0x00 CC0Dh	FFFB:9834	UART3_RXFLH	UART3 receive frame length high	8	W	00h
0x00 CC0Eh	FFFB:9838	UART3_UASR	UART3 autobauding status register	8	R	00h
0x00 CC0Eh	FFFB:9838	UART3_BLR	UART3 BOF control register	8	R/W	40h
0x00 CC0Fh	FFFB:983C	UART3_ACREG	UART3 auxiliary control register	8	R/W	00h
0x00 CC10h	FFFB:9840	UART3_SCR	UART3 supplementary control register	8	R/W	00h
0x00 CC11h	FFFB:9844	UART3_SSR	UART3 supplementary status register	8	R	00h
0x00 CC12h	FFFB:9848	UART3_EBLR	UART3 BOF length register	8	R/W	00h
0x00 CC13h	FFFB:984C		Reserved			
0x00 CC14h	FFFB:9850	UART3_MVR	UART3 module version register	8	R	–
0x00 CC15h	FFFB:9854	UART3_SYSC	UART3 system configuration register	8	R/W	00h
0x00 CC16h	FFFB:9858	UART3_SYSS	UART3 system status register	8	R/W	00h
0x00 CC17h	FFFB:985C	UART3_WER	UART3 wake-up enable register	8	R/W	7Fh

Table 3–40. MPU GPIO3 Registers

MPU BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:B400	GPIO3_REVISION	GPIO3 Revision Register	16/32	R	0000 00xxh
FFFB:B410	GPIO3_SYSCONFIG	GPIO3 System Configuration Register	16/32	R/W	0000 0000h
FFFB:B414	GPIO3_SYSSTATUS	GPIO3 System Status Register	16/32	R	0000 0000h
FFFB:B418	GPIO3_IRQSTATUS1	GPIO3 Interrupt Status1 Register	16/32	R/W	0000 0000h
FFFB:B41C	GPIO3_IRQENABLE1	GPIO3 Interrupt Enable1 Register	16/32	R/W	0000 0000h
FFFB:B420	GPIO3_IRQSTATUS2	GPIO3 Interrupt Status2 Register	16/32	R/W	0000 0000h
FFFB:B424	GPIO3_IRQENABLE2	GPIO3 Interrupt Enable2 Register	16/32	R/W	0000 0000h
FFFB:B428	GPIO3_WAKEUPENABLE	GPIO3 Wake-up Enable Register	16/32	R/W	0000 0000h
FFFB:B42C	GPIO3_DATAIN	GPIO3 Data Input Register	16/32	R	0000 0000h
FFFB:B430	GPIO3_DATAOUT	GPIO3 Data Output Register	16/32	R/W	0000 0000h
FFFB:B434	GPIO3_DIRECTION	GPIO3 Direction Control Register	16/32	R/W	0000 FFFFh

Table 3–40. MPU GPIO3 Registers (Continued)

MPU BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:B438	GPIO3_EDGE_CTRL1	GPIO3 Edge Control 1 Register	16/32	R/W	0000 0000h
FFFB:B43C	GPIO3_EDGE_CTRL2	GPIO3 Edge Control 2 Register	16/32	R/W	0000 0000h
FFFB:B49C	GPIO3_CLEAR_IRQENABLE1	GPIO3 Clear Interrupt Enable1 Register	16/32	R/W	0000 0000h
FFFB:B4A4	GPIO3_CLEAR_IRQENABLE2	GPIO3 Clear Interrupt Enable2 Register	16/32	R/W	0000 0000h
FFFB:B4A8	GPIO3_CLEAR_WAKEUPENA	GPIO3 Clear Wake-up Enable Register	16/32	R/W	0000 0000h
FFFB:B4B0	GPIO3_CLEAR_DATAOUT	GPIO3 Clear Data Output Register	16/32	R/W	0000 0000h
FFFB:B4DC	GPIO3_SET_IRQENABLE1	GPIO3 Set Interrupt Enable1 Register	16/32	R/W	0000 0000h
FFFB:B4E4	GPIO3_SET_IRQENABLE2	GPIO3 Set Interrupt Enable2 Register	16/32	R/W	0000 0000h
FFFB:B4E8	GPIO3_SET_WAKEUPENA	GPIO3 Set Wake-up Enable Register	16/32	R/W	0000 0000h
FFFB:B4F0	GPIO3_SET_DATAOUT	GPIO3 Set Data Output Register	16/32	R/W	0000 0000h

Table 3–41. MPU GPIO4 Registers

MPU BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:BC00	GPIO4_REVISION	GPIO4 Revision Register	16/32	R	0000 00xxh
FFFB:BC10	GPIO4_SYSCONFIG	GPIO4 System Configuration Register	16/32	R/W	0000 0000h
FFFB:BC14	GPIO4_SYSSTATUS	GPIO4 System Status Register	16/32	R	0000 0000h
FFFB:BC18	GPIO4_IRQSTATUS1	GPIO4 Interrupt Status1 Register	16/32	R/W	0000 0000h
FFFB:BC1C	GPIO4_IRQENABLE1	GPIO4 Interrupt Enable1 Register	16/32	R/W	0000 0000h
FFFB:BC20	GPIO4_IRQSTATUS2	GPIO4 Interrupt Status2 Register	16/32	R/W	0000 0000h
FFFB:BC24	GPIO4_IRQENABLE2	GPIO4 Interrupt Enable2 Register	16/32	R/W	0000 0000h
FFFB:BC28	GPIO4_WAKEUPENABLE	GPIO4 Wake-up Enable Register	16/32	R/W	0000 0000h
FFFB:BC2C	GPIO4_DATAIN	GPIO4 Data Input Register	16/32	R	0000 0000h
FFFB:BC30	GPIO4_DATAOUT	GPIO4 Data Output Register	16/32	R/W	0000 0000h
FFFB:BC34	GPIO4_DIRECTION	GPIO4 Direction Control Register	16/32	R/W	0000 FFFFh
FFFB:BC38	GPIO4_EDGE_CTRL1	GPIO4 Edge Control 1 Register	16/32	R/W	0000 0000h
FFFB:BC3C	GPIO4_EDGE_CTRL2	GPIO4 Edge Control 2 Register	16/32	R/W	0000 0000h
FFFB:BC9C	GPIO4_CLEAR_IRQENABLE1	GPIO4 Clear Interrupt Enable1 Register	16/32	R/W	0000 0000h
FFFB:BCA4	GPIO4_CLEAR_IRQENABLE2	GPIO4 Clear Interrupt Enable2 Register	16/32	R/W	0000 0000h
FFFB:BCA8	GPIO4_CLEAR_WAKEUPENA	GPIO4 Clear Wake-up Enable Register	16/32	R/W	0000 0000h
FFFB:BCB0	GPIO4_CLEAR_DATAOUT	GPIO4 Clear Data Output Register	16/32	R/W	0000 0000h
FFFB:BCDC	GPIO4_SET_IRQENABLE1	GPIO4 Set Interrupt Enable1 Register	16/32	R/W	0000 0000h
FFFB:BCE4	GPIO4_SET_IRQENABLE2	GPIO4 Set Interrupt Enable2 Register	16/32	R/W	0000 0000h
FFFB:BCE8	GPIO4_SET_WAKEUPENA	GPIO4 Set Wake-up Enable Register	16/32	R/W	0000 0000h
FFFB:BCF0	GPIO4_SET_DATAOUT	GPIO4 Set Data Output Register	16/32	R/W	0000 0000h

Table 3–42. 32-kHz Synchro Count Registers

MPU BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:D400	32K_SYNC_CNT_REV	32k Synchro Count CID Revision Register	32	R	0000 0010h
FFFB:D410	32K_SYNC_CNT_CR	32k Synchro Count Counter Register	32	R	0000 0003h

Table 3–43. General-Purpose Timer8 Registers

DSP WORD ADDRESS	MPU BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 C200h	FFFB:D400	GPTMR8_TIDR	GPTimer8 Identification Register	16/32	R	0000 0010h
0x00 C202h	FFFB:D404		Reserved			
0x00 C208h	FFFB:D410	GPTMR8_TIOCP_CFG	GPTimer8 OCP Configuration Register	16/32	R/W	0000 0000h
0x00 C20Ah	FFFB:D414	GPTMR8_TISTAT	GPTimer8 System Status Register	16/32	R	0000 0000h
0x00 C20Ch	FFFB:D418	GPTMR8_TISR	GPTimer8 Status Register	16/32	R/W	0000 0000h
0x00 C20Eh	FFFB:D41C	GPTMR8_TIER	GPTimer8 Interrupt Enable Register	16/32	R/W	0000 0000h
0x00 C210h	FFFB:D420	GPTMR8_TWER	GPTimer8 Wake Up Enable Register	16/32	R/W	0000 0000h
0x00 C212h	FFFB:D424	GPTMR8_TCLR	GPTimer8 Control Register	16/32	R/W	0000 0000h
0x00 C214h	FFFB:D428	GPTMR8_TCRR	GPTimer8 Counter Register	16/32	R/W	0000 0000h
0x00 C216h	FFFB:D42C	GPTMR8_TLDR	GPTimer8 Load Register	16/32	R/W	0000 0000h
0x00 C218h	FFFB:D430	GPTMR8_TTGR	GPTimer8 Trigger Register	16/32	R/W	FFFF FFFFh
0x00 C21Ah	FFFB:D434	GPTMR8_TWPS	GPTimer8 Write Posted Register	16/32	R	0000 0000h
0x00 C21Ch	FFFB:D438	GPTMR8_TMAR	GPTimer8 Match Register	16/32	R/W	0000 0000h
0x00 C21Eh	FFFB:D43C	GPTMR8_TCAR	GPTimer8 Capture Register	16/32	R	0000 0000h
0x00 C220h	FFFB:D440	GPTMR8_TSICR	GPTimer8 Synchronization Interface Control Register	16/32	R/W	0000 0004h

Table 3–44. MPU GPIO1 Registers

MPU BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:E400	GPIO1_REVISION	GPIO1 Revision Register	16/32	R	0000 00xxh
FFFB:E410	GPIO1_SYSCONFIG	GPIO1 System Configuration Register	16/32	R/W	0000 0000h
FFFB:E414	GPIO1_SYSSTATUS	GPIO1 System Status Register	16/32	R	0000 0000h
FFFB:E418	GPIO1_IRQSTATUS1	GPIO1 Interrupt Status1 Register	16/32	R/W	0000 0000h
FFFB:E41C	GPIO1_IRQENABLE1	GPIO1 Interrupt Enable1 Register	16/32	R/W	0000 0000h
FFFB:E420	GPIO1_IRQSTATUS2	GPIO1 Interrupt Status2 Register	16/32	R/W	0000 0000h
FFFB:E424	GPIO1_IRQENABLE2	GPIO1 Interrupt Enable2 Register	16/32	R/W	0000 0000h
FFFB:E428	GPIO1_WAKEUPENABLE	GPIO1 Wake-up Enable Register	16/32	R/W	0000 0000h
FFFB:E42C	GPIO1_DATAIN	GPIO1 Data Input Register	16/32	R	0000 0000h
FFFB:E430	GPIO1_DATAOUT	GPIO1 Data Output Register	16/32	R/W	0000 0000h
FFFB:E434	GPIO1_DIRECTION	GPIO1 Direction Control Register	16/32	R/W	0000 FFFFh
FFFB:E438	GPIO1_EDGE_CTRL1	GPIO1 Edge Control 1 Register	16/32	R/W	0000 0000h
FFFB:E43C	GPIO1_EDGE_CTRL2	GPIO1 Edge Control 2 Register	16/32	R/W	0000 0000h
FFFB:E49C	GPIO1_CLEAR_IRQENABLE1	GPIO1 Clear Interrupt Enable1 Register	16/32	R/W	0000 0000h
FFFB:E4A4	GPIO1_CLEAR_IRQENABLE2	GPIO1 Clear Interrupt Enable2 Register	16/32	R/W	0000 0000h
FFFB:E4A8	GPIO1_CLEAR_WAKEUPENA	GPIO1 Clear Wake-up Enable Register	16/32	R/W	0000 0000h
FFFB:E4B0	GPIO1_CLEAR_DATAOUT	GPIO1 Clear Data Output Register	16/32	R/W	0000 0000h
FFFB:E4DC	GPIO1_SET_IRQENABLE1	GPIO1 Set Interrupt Enable1 Register	16/32	R/W	0000 0000h
FFFB:E4E4	GPIO1_SET_IRQENABLE2	GPIO1 Set Interrupt Enable2 Register	16/32	R/W	0000 0000h
FFFB:E4E8	GPIO1_SET_WAKEUPENA	GPIO1 Set Wake-up Enable Register	16/32	R/W	0000 0000h
FFFB:E4F0	GPIO1_SET_DATAOUT	GPIO1 Set Data Output Register	16/32	R/W	0000 0000h

Table 3–45. MPU GPIO2 Registers

MPU BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:EC00	GPIO2_REVISION	GPIO2 Revision Register	16/32	R	0000 00xxh
FFFB:EC10	GPIO2_SYSCONFIG	GPIO2 System Configuration Register	16/32	R/W	0000 0000h
FFFB:EC14	GPIO2_SYSSTATUS	GPIO2 System Status Register	16/32	R	0000 0000h
FFFB:EC18	GPIO2_IRQSTATUS1	GPIO2 Interrupt Status1 Register	16/32	R/W	0000 0000h
FFFB:EC1C	GPIO2_IRQENABLE1	GPIO2 Interrupt Enable1 Register	16/32	R/W	0000 0000h
FFFB:EC20	GPIO2_IRQSTATUS2	GPIO2 Interrupt Status2 Register	16/32	R/W	0000 0000h
FFFB:EC24	GPIO2_IRQENABLE2	GPIO2 Interrupt Enable2 Register	16/32	R/W	0000 0000h
FFFB:EC28	GPIO2_WAKEUPENABLE	GPIO2 Wake-up Enable Register	16/32	R/W	0000 0000h
FFFB:EC2C	GPIO2_DATAIN	GPIO2 Data Input Register	16/32	R	0000 0000h
FFFB:EC30	GPIO2_DATAOUT	GPIO2 Data Output Register	16/32	R/W	0000 0000h
FFFB:EC34	GPIO2_DIRECTION	GPIO2 Direction Control Register	16/32	R/W	0000 FFFFh
FFFB:EC38	GPIO2_EDGE_CTRL1	GPIO2 Edge Control 1 Register	16/32	R/W	0000 0000h
FFFB:EC3C	GPIO2_EDGE_CTRL2	GPIO2 Edge Control 2 Register	16/32	R/W	0000 0000h
FFFB:EC9C	GPIO2_CLEAR_IRQENABLE1	GPIO2 Clear Interrupt Enable1 Register	16/32	R/W	0000 0000h
FFFB:ECA4	GPIO2_CLEAR_IRQENABLE2	GPIO2 Clear Interrupt Enable2 Register	16/32	R/W	0000 0000h
FFFB:ECA8	GPIO2_CLEAR_WAKEUPENA	GPIO2 Clear Wake-up Enable Register	16/32	R/W	0000 0000h
FFFB:ECB0	GPIO2_CLEAR_DATAOUT	GPIO2 Clear Data Output Register	16/32	R/W	0000 0000h
FFFB:ECDC	GPIO2_SET_IRQENABLE1	GPIO2 Set Interrupt Enable1 Register	16/32	R/W	0000 0000h
FFFB:ECE4	GPIO2_SET_IRQENABLE2	GPIO2 Set Interrupt Enable2 Register	16/32	R/W	0000 0000h
FFFB:ECE8	GPIO2_SET_WAKEUPENA	GPIO2 Set Wake-up Enable Register	16/32	R/W	0000 0000h
FFFB:ECF0	GPIO2_SET_DATAOUT	GPIO2 Set Data Output Register	16/32	R/W	0000 0000h

Table 3–46. MPU/DSP Shared Mailbox Registers

DSP WORD ADDRESS	MPU BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	MPU ACCESS TYPE	DSP ACCESS TYPE	RESET VALUE
0x00 F800h	FFFC:F000	ARM2DSP1	MPU to DSP 1 Data Register	16	R/W	R	0000h
0x00 F802h	FFFC:F004	ARM2DSP1B	MPU to DSP 1 Command Register	16	R/W	R	0000h
0x00 F804h	FFFC:F008	DSP2ARM1	DSP to MPU 1 Data Register	16	R	R/W	0000h
0x00 F806h	FFFC:F00C	DSP2ARM1B	DSP to MPU 1 Command Register	16	R	R/W	0000h
0x00 F808h	FFFC:F010	DSP2ARM2	DSP to MPU 2 Data Register	16	R	R/W	0000h
0x00 F80Ah	FFFC:F014	DSP2ARM2B	DSP to MPU 2 Command Register	16	R	R/W	0000h
0x00 F80Ch	FFFC:F018	ARM2DSP1_FLAG	MPU to DSP 1 Flag Register	16	R	R	undef
0x00 F80Eh	FFFC:F01C	DSP2ARM1_FLAG	DSP to MPU 1 Flag Register	16	R	R	undef
0x00 F810h	FFFC:F020	DSP2ARM2_FLAG	DSP to MPU 2 Flag Register	16	R	R	undef
0x00 F812h	FFFC:F024	ARM2DSP2	MPU to DSP 2 Data Register	16	R/W	R	0000h
0x00 F814h	FFFC:F028	ARM2DSP2B	MPU to DSP 2 Command Register	16	R/W	R	0000h
0x00 F816h	FFFC:F02C	ARM2DSP2_FLAG	MPU to DSP 2 Flag Register	16	R	R	undef

3.2.2.4 DSP Public Peripheral Registers (Accessible Via MPUI Port)

The MPU public peripheral registers include the following:

- McBSP1 Registers
- MCS11 Registers
- MCS12 Registers
- McBSP3 Registers

Table 3–47. McBSP1 Registers

DSP WORD ADDRESS	MPU BYTE ADDRESS (VIA MPUI)	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 8C00h	E101:1800	MCBSP1_DRR2	McBSP1 Data receive register 2	16	R/W	0000h
0x00 8C01h	E101:1802	MCBSP1_DRR1	McBSP1 Data receive register 1	16	R/W	0000h
0x00 8C02h	E101:1804	MCBSP1_DXR2	McBSP1 Data transmit register 2	16	R/W	0000h
0x00 8C03h	E101:1806	MCBSP1_DXR1	McBSP1 Data transmit register 1	16	R/W	0000h
0x00 8C04h	E101:1808	MCBSP1_SPCR2	McBSP1 Serial port control register 2	16	R/W	0000h
0x00 8C05h	E101:180A	MCBSP1_SPCR1	McBSP1 Serial port control register 1	16	R/W	0000h
0x00 8C06h	E101:180C	MCBSP1_RCR2	McBSP1 Receive control register 2	16	R/W	0000h
0x00 8C07h	E101:180E	MCBSP1_RCR1	McBSP1 Receive control register 1	16	R/W	0000h
0x00 8C08h	E101:1810	MCBSP1_XCR2	McBSP1 Transmit control register 2	16	R/W	0000h
0x00 8C09h	E101:1812	MCBSP1_XCR1	McBSP1 Transmit control register 1	16	R/W	0000h
0x00 8C0Ah	E101:1814	MCBSP1_SRGR2	McBSP1 Sample rate generator register 2	16	R/W	2000h
0x00 8C0Bh	E101:1816	MCBSP1_SRGR1	McBSP1 Sample rate generator register 1	16	R/W	0001h
0x00 8C0Ch	E101:1818	MCBSP1_MCR2	McBSP1 Multichannel register 2	16	R/W	0000h
0x00 8C0Dh	E101:181A	MCBSP1_MCR1	McBSP1 Multichannel register 1	16	R/W	0000h
0x00 8C0Eh	E101:181C	MCBSP1_RCERA	McBSP1 Receive channel enable register partition A	16	R/W	0000h
0x00 8C10h	E101:181E	MCBSP1_RCERB	McBSP1 Receive channel enable register partition B	16	R/W	0000h
0x00 8C11h	E101:1820	MCBSP1_XCERA	McBSP1 Transmit channel enable register partition A	16	R/W	0000h
0x00 8C12h	E101:1822	MCBSP1_XCERB	McBSP1 Transmit channel enable register partition B	16	R/W	0000h
0x00 8C13h	E101:1824	MCBSP1_PCR0	McBSP1 Pin control register 0	16	R/W	0000h
0x00 8C14h	E101:1826	MCBSP1_RCERC	McBSP1 Receive channel enable register partition C	16	R/W	0000h
0x00 8C15h	E101:1828	MCBSP1_RCERD	McBSP1 Receive channel enable register partition D	16	R/W	0000h
0x00 8C16h	E101:182A	MCBSP1_XCERC	McBSP1 Transmit channel enable register partition C	16	R/W	0000h
0x00 8C17h	E101:182C	MCBSP1_XCERD	McBSP1 Transmit channel enable register partition D	16	R/W	0000h
0x00 8C18h	E101:182E	MCBSP1_RCERE	McBSP1 Receive channel enable register partition E	16	R/W	0000h
0x00 8C19h	E101:1830	MCBSP1_RCERF	McBSP1 Receive channel enable register partition F	16	R/W	0000h
0x00 8C1Ah	E101:1832	MCBSP1_XCERE	McBSP1 Transmit channel enable register partition E	16	R/W	0000h

Table 3–47. McBSP1 Registers (Continued)

DSP WORD ADDRESS	MPU BYTE ADDRESS (VIA MPU)	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 8C1Bh	E101:1834	MCBSP1_XCERF	McBSP1 Transmit channel enable register partition F	16	R/W	0000h
0x00 8C1Ch	E101:1836	MCBSP1_RCERG	McBSP1 Receive channel enable register partition G	16	R/W	0000h
0x00 8C1Dh	E101:1838	MCBSP1_RCERH	McBSP1 Receive channel enable register partition H	16	R/W	0000h
0x00 8C1Eh	E101:183A	MCBSP1_XCERG	McBSP1 Transmit channel enable register partition G	16	R/W	0000h
0x00 8C1Fh	E101:183C	MCBSP1_XCERH	McBSP1 Transmit channel enable register partition H	16	R/W	0000h
0x00 8C20h	E101:183E	MCBSP1_REV	McBSP1 Version register	16	R/W	0011h

Table 3–48. MCS11 Registers

DSP WORD ADDRESS	MPU BYTE ADDRESS (VIA MPU)	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 9400h	E101:2800	MCS11_CONTROL_REG	MCS11 control register	16	R/W	0000h
0x00 9401h	E101:2802	MCS11_MAIN_PARAMETERS_REG	MCS11 main parameters register	16	R/W	0000h
0x00 9402h	E101:2804	MCS11_INTERRUPTS_REG	MCS11 interrupts register	16	R/W	0000h
0x00 9403h	E101:2806	MCS11_CHANNEL_USED_REG	MCS11 channel used register	16	R/W	0000h
0x00 9404h	E101:2808	MCS11_OVER_CLOCK_REG	MCS11 over-clock register	16	R/W	0000h
0x00 9405h	E101:280A	MCS11_CLOCK_FREQUENCY_REG	MCS11 clock frequency register	16	R/W	0000h
0x00 9406h	E101:280C	MCS11_STATUS_REG	MCS11 status register	16	R/W	0000h
0x00 9407h– 0x00 941Fh		Reserved				
0x00 9420h	E101:2840	MCS11_TX0	MCS11 transmit word register 0	16	R/W	Undefined
0x00 9421h	E101:2842	MCS11_TX1	MCS11 transmit word register 1	16	R/W	Undefined
0x00 9422h	E101:2844	MCS11_TX2	MCS11 transmit word register 2	16	R/W	Undefined
0x00 9423h	E101:2846	MCS11_TX3	MCS11 transmit word register 3	16	R/W	Undefined
0x00 9424h	E101:2848	MCS11_TX4	MCS11 transmit word register 4	16	R/W	Undefined
0x00 9425h	E101:284A	MCS11_TX5	MCS11 transmit word register 5	16	R/W	Undefined
0x00 9426h	E101:284C	MCS11_TX6	MCS11 transmit word register 6	16	R/W	Undefined
0x00 9427h	E101:284E	MCS11_TX7	MCS11 transmit word register 7	16	R/W	Undefined
0x00 9428h	E101:2850	MCS11_TX8	MCS11 transmit word register 8	16	R/W	Undefined
0x00 9429h	E101:2852	MCS11_TX9	MCS11 transmit word register 9	16	R/W	Undefined
0x00 942Ah	E101:2854	MCS11_TX10	MCS11 transmit word register 10	16	R/W	Undefined
0x00 942Bh	E101:2856	MCS11_TX11	MCS11 transmit word register 11	16	R/W	Undefined
0x00 942Ch	E101:2858	MCS11_TX12	MCS11 transmit word register 12	16	R/W	Undefined
0x00 942Dh	E101:285A	MCS11_TX13	MCS11 transmit word register 13	16	R/W	Undefined
0x00 942Eh	E101:285C	MCS11_TX14	MCS11 transmit word register 14	16	R/W	Undefined
0x00 942Fh	E101:285E	MCS11_TX15	MCS11 transmit word register 15	16	R/W	Undefined
0x00 9430h	E101:2860	MCS11_RX0	MCS11 receive word register 0	16	R	Undefined
0x00 9431h	E101:2862	MCS11_RX1	MCS11 receive word register 1	16	R	Undefined
0x00 9432h	E101:2864	MCS11_RX2	MCS11 receive word register 2	16	R	Undefined

Table 3–48. MCSI1 Registers (Continued)

DSP WORD ADDRESS	MPU BYTE ADDRESS (VIA MPU)	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 9433h	E101:2866	MCSI1_RX3	MCSI1 receive word register 3	16	R	Undefined
0x00 9434h	E101:2868	MCSI1_RX4	MCSI1 receive word register 4	16	R	Undefined
0x00 9435h	E101:286A	MCSI1_RX5	MCSI1 receive word register 5	16	R	Undefined
0x00 9436h	E101:286C	MCSI1_RX6	MCSI1 receive word register 6	16	R	Undefined
0x00 9437h	E101:286E	MCSI1_RX7	MCSI1 receive word register 7	16	R	Undefined
0x00 9438h	E101:2870	MCSI1_RX8	MCSI1 receive word register 8	16	R	Undefined
0x00 9439h	E101:2872	MCSI1_RX9	MCSI1 receive word register 9	16	R	Undefined
0x00 943Ah	E101:2874	MCSI1_RX10	MCSI1 receive word register 10	16	R	Undefined
0x00 943Bh	E101:2876	MCSI1_RX11	MCSI1 receive word register 11	16	R	Undefined
0x00 943Ch	E101:2878	MCSI1_RX12	MCSI1 receive word register 12	16	R	Undefined
0x00 943Dh	E101:287A	MCSI1_RX13	MCSI1 receive word register 13	16	R	Undefined
0x00 943Eh	E101:287C	MCSI1_RX14	MCSI1 receive word register 14	16	R	Undefined
0x00 943Fh	E101:287E	MCSI1_RX15	MCSI1 receive word register 15	16	R	Undefined

Table 3–49. MCSI2 Registers

DSP WORD ADDRESS	MPU BYTE ADDRESS (VIA MPU)	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 9000h	E101:2000	MCSI2_CONTROL_REG	MCSI2 control register	16	R/W	0000h
0x00 9001h	E101:2002	MCSI2_MAIN_PARAMETERS_REG	MCSI2 main parameters register	16	R/W	0000h
0x00 9002h	E101:2004	MCSI2_INTERRUPTS_REG	MCSI2 interrupts register	16	R/W	0000h
0x00 9003h	E101:2006	MCSI2_CHANNEL_USED_REG	MCSI2 channel used register	16	R/W	0000h
0x00 9004h	E101:2008	MCSI2_OVER_CLOCK_REG	MCSI2 over-clock register	16	R/W	0000h
0x00 9005h	E101:200A	MCSI2_CLOCK_FREQUENCY_REG	MCSI2 clock frequency register	16	R/W	0000h
0x00 9006h	E101:200C	MCSI2_STATUS_REG	MCSI2 status register	16	R/W	0000h
0x00 9007h – 0x00 901Fh		Reserved				
0x00 9020h	E101:2040	MCSI2_TX0	MCSI2 transmit word register 0	16	R/W	Undefined
0x00 9021h	E101:2042	MCSI2_TX1	MCSI2 transmit word register 1	16	R/W	Undefined
0x00 9022h	E101:2044	MCSI2_TX2	MCSI2 transmit word register 2	16	R/W	Undefined
0x00 9023h	E101:2046	MCSI2_TX3	MCSI2 transmit word register 3	16	R/W	Undefined
0x00 9024h	E101:2048	MCSI2_TX4	MCSI2 transmit word register 4	16	R/W	Undefined
0x00 9025h	E101:204A	MCSI2_TX5	MCSI2 transmit word register 5	16	R/W	Undefined
0x00 9026h	E101:204C	MCSI2_TX6	MCSI2 transmit word register 6	16	R/W	Undefined
0x00 9027h	E101:204E	MCSI2_TX7	MCSI2 transmit word register 7	16	R/W	Undefined
0x00 9028h	E101:2050	MCSI2_TX8	MCSI2 transmit word register 8	16	R/W	Undefined
0x00 9029h	E101:2052	MCSI2_TX9	MCSI2 transmit word register 9	16	R/W	Undefined
0x00 902Ah	E101:2054	MCSI2_TX10	MCSI2 transmit word register 10	16	R/W	Undefined
0x00 902Bh	E101:2056	MCSI2_TX11	MCSI2 transmit word register 11	16	R/W	Undefined
0x00 902Ch	E101:2058	MCSI2_TX12	MCSI2 transmit word register 12	16	R/W	Undefined
0x00 902Dh	E101:205A	MCSI2_TX13	MCSI2 transmit word register 13	16	R/W	Undefined
0x00 902Eh	E101:205C	MCSI2_TX14	MCSI2 transmit word register 14	16	R/W	Undefined
0x00 902Fh	E101:205E	MCSI2_TX15	MCSI2 transmit word register 15	16	R/W	Undefined

Table 3–49. MCSI2 Registers (Continued)

DSP WORD ADDRESS	MPU BYTE ADDRESS (VIA MPU)	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 9030h	E101:2060	MCSI2_RX0	MCSI2 receive word register 0	16	R	Undefined
0x00 9031h	E101:2062	MCSI2_RX1	MCSI2 receive word register 1	16	R	Undefined
0x00 9032h	E101:2064	MCSI2_RX2	MCSI2 receive word register 2	16	R	Undefined
0x00 9033h	E101:2066	MCSI2_RX3	MCSI2 receive word register 3	16	R	Undefined
0x00 9034h	E101:2068	MCSI2_RX4	MCSI2 receive word register 4	16	R	Undefined
0x00 9035h	E101:206A	MCSI2_RX5	MCSI2 receive word register 5	16	R	Undefined
0x00 9036h	E101:206C	MCSI2_RX6	MCSI2 receive word register 6	16	R	Undefined
0x00 9037h	E101:206E	MCSI2_RX7	MCSI2 receive word register 7	16	R	Undefined
0x00 9038h	E101:2070	MCSI2_RX8	MCSI2 receive word register 8	16	R	Undefined
0x00 9039h	E101:2072	MCSI2_RX9	MCSI2 receive word register 9	16	R	Undefined
0x00 903Ah	E101:2074	MCSI2_RX10	MCSI2 receive word register 10	16	R	Undefined
0x00 903Bh	E101:2076	MCSI2_RX11	MCSI2 receive word register 11	16	R	Undefined
0x00 903Ch	E101:2078	MCSI2_RX12	MCSI2 receive word register 12	16	R	Undefined
0x00 903Dh	E101:207A	MCSI2_RX13	MCSI2 receive word register 13	16	R	Undefined
0x00 903Eh	E101:207C	MCSI2_RX14	MCSI2 receive word register 14	16	R	Undefined
0x00 903Fh	E101:207E	MCSI2_RX15	MCSI2 receive word register 15	16	R	Undefined

Table 3–50. McBSP3 Registers

DSP WORD ADDRESS	MPU BYTE ADDRESS (VIA MPU)	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 B800h	E101:7000	MCBSP3_DRR2	McBSP3 Data receive register 2	16	R/W	0000h
0x00 B801h	E101:7002	MCBSP3_DRR1	McBSP3 Data receive register 1	16	R/W	0000h
0x00 B802h	E101:7004	MCBSP3_DXR2	McBSP3 Data transmit register 2	16	R/W	0000h
0x00 B803h	E101:7006	MCBSP3_DXR1	McBSP3 Data transmit register 1	16	R/W	0000h
0x00 B804h	E101:7008	MCBSP3_SPCR2	McBSP3 Serial port control register 2	16	R/W	0000h
0x00 B805h	E101:700A	MCBSP3_SPCR1	McBSP3 Serial port control register 1	16	R/W	0000h
0x00 B806h	E101:700C	MCBSP3_RCR2	McBSP3 Receive control register 2	16	R/W	0000h
0x00 B807h	E101:700E	MCBSP3_RCR1	McBSP3 Receive control register 1	16	R/W	0000h
0x00 B808h	E101:7010	MCBSP3_XCR2	McBSP3 Transmit control register 2	16	R/W	0000h
0x00 B809h	E101:7012	MCBSP3_XCR1	McBSP3 Transmit control register 1	16	R/W	0000h
0x00 B80Ah	E101:7014	MCBSP3_SRGR2	McBSP3 Sample rate generator register 2	16	R/W	2000h
0x00 B80Bh	E101:7016	MCBSP3_SRGR1	McBSP3 Sample rate generator register 1	16	R/W	0001h
0x00 B80Ch	E101:7018	MCBSP3_MCR2	McBSP3 Multichannel register 2	16	R/W	0000h
0x00 B80Dh	E101:701A	MCBSP3_MCR1	McBSP3 Multichannel register 1	16	R/W	0000h
0x00 B80Eh	E101:701C	MCBSP3_RCERA	McBSP3 Receive channel enable register partition A	16	R/W	0000h
0x00 B810h	E101:701E	MCBSP3_RCERB	McBSP3 Receive channel enable register partition B	16	R/W	0000h
0x00 B811h	E101:7020	MCBSP3_XCERA	McBSP3 Transmit channel enable register partition A	16	R/W	0000h
0x00 B812h	E101:7022	MCBSP3_XCERB	McBSP3 Transmit channel enable register partition B	16	R/W	0000h
0x00 B813h	E101:7024	MCBSP3_PCR0	McBSP3 Pin control register 0	16	R/W	0000h

Table 3–50. McBSP3 Registers (Continued)

DSP WORD ADDRESS	MPU BYTE ADDRESS (VIA MPUI)	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 B814h	E101:7026	MCBSP3_RCERC	McBSP3 Receive channel enable register partition C	16	R/W	0000h
0x00 B815h	E101:7028	MCBSP3_RCERD	McBSP3 Receive channel enable register partition D	16	R/W	0000h
0x00 B816h	E101:702A	MCBSP3_XCERC	McBSP3 Transmit channel enable register partition C	16	R/W	0000h
0x00 B817h	E101:702C	MCBSP3_XCERD	McBSP3 Transmit channel enable register partition D	16	R/W	0000h
0x00 B818h	E101:702E	MCBSP3_RCERE	McBSP3 Receive channel enable register partition E	16	R/W	0000h
0x00 B819h	E101:7030	MCBSP3_RCERF	McBSP3 Receive channel enable register partition F	16	R/W	0000h
0x00 B81Ah	E101:7032	MCBSP3_XCERE	McBSP3 Transmit channel enable register partition E	16	R/W	0000h
0x00 B81Bh	E101:7034	MCBSP3_XCERF	McBSP3 Transmit channel enable register partition F	16	R/W	0000h
0x00 B81Ch	E101:7036	MCBSP3_RCERG	McBSP3 Receive channel enable register partition G	16	R/W	0000h
0x00 B81Dh	E101:7038	MCBSP3_RCERH	McBSP3 Receive channel enable register partition H	16	R/W	0000h
0x00 B81Eh	E101:703A	MCBSP3_XCERG	McBSP3 Transmit channel enable register partition G	16	R/W	0000h
0x00 B81Fh	E101:703C	MCBSP3_XCERH	McBSP3 Transmit channel enable register partition H	16	R/W	0000h
0x00 B820h	E101:703E	MCBSP3_REV	McBSP3 Version register	16	R/W	0011h

3.2.2.5 MPU Configuration Registers

The MPU public peripheral registers include the following:

- MPU UART TIPB Bus Switch Registers
- Ultra Low-Power Device Peripheral Registers
- OMAP5912 Configuration Registers
- Device Die Identification Registers
- Production Identification Registers
- L3 OCP Initiator Registers
- MPU Interface (MPUI) Registers
- TIPB (Private) Bridge 1 Configuration Registers
- Traffic Controller Registers
- MPU Clock/Reset/Power Mode Control Registers
- DPLL1 Configuration Register
- DSP MMU Registers
- TIPB (Public) Bridge2 Configuration Registers

Table 3–51. MPU UART TIPB Bus Switch Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFB:C800	UART1_SSW_CONF	UART1 Peripheral Ownership Register	32	R/W	0000 0001h
FFFB:C820	UART2_SSW_CONF	UART2 Peripheral Ownership Register	32	R/W	0000 0001h
FFFB:C840	UART3_SSW_CONF	UART3 Peripheral Ownership Register	32	R/W	0000 0001h
FFFB:C890	MCBSP2_SSW_CONF	McBSP2 Peripheral Ownership Register	32	R/W	0000 0001h
FFFB:C8A0	I2C_SSW_CONF	I2C Peripheral Ownership Register	32	R/W	0000 0001h
FFFB:C8B0	SPI_SSW_CONF	SPI Peripheral Ownership Register	32	R/W	0000 0001h
FFFB:C8C0	DUALMODETIMER1_SSW_CONF	Dual Mode Timer1 Ownership Register	32	R/W	0000 0001h
FFFB:C8D0	DUALMODETIMER2_SSW_CONF	Dual Mode Timer2 Ownership Register	32	R/W	0000 0001h
FFFB:C8E0	DUALMODETIMER3_SSW_CONF	Dual Mode Timer3 Ownership Register	32	R/W	0000 0001h
FFFB:C8F0	DUALMODETIMER4_SSW_CONF	Dual Mode Timer4 Ownership Register	32	R/W	0000 0001h
FFFB:C900	DUALMODETIMER5_SSW_CONF	Dual Mode Timer5 Ownership Register	32	R/W	0000 0001h
FFFB:C910	DUALMODETIMER6_SSW_CONF	Dual Mode Timer6 Ownership Register	32	R/W	0000 0001h
FFFB:C930	DUALMODETIMER7_SSW_CONF	Dual Mode Timer7 Ownership Register	32	R/W	0000 0001h
FFFB:C940	DUALMODETIMER8_SSW_CONF	Dual Mode Timer8 Ownership Register	32	R/W	0000 0001h
FFFB:C960	MMCS2_SSW_CONF	MMCS2 Ownership Register	32	R/W	0000 0001h

Table 3–52. Ultra Low-Power Device Peripheral Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:0800	COUNTER_32_LSB	ULPD 32-kHz Counter Register LSB	16	R	0001h
FFFE:0804	COUNTER_32_MSB	ULPD 32-kHz Counter Register MSB	16	R	0001h
FFFE:0808	COUNTER_HIGH_FREQ_LSB	ULPD High-Frequency Counter LSB Register	16	R	0001h
FFFE:080C	COUNTER_HIGH_FREQ_MSB	ULPD High-Frequency Counter MSB Register	16	R	0000h
FFFE:0810	GAUGING_CTRL_REG	ULPD Gauging Control Register	16	R/W	0000h
FFFE:0814	IT_STATUS_REG	ULPD Interrupt Status Register	16	R	0000h
FFFE:0818 – FFFE:0820		Reserved			
FFFE:0824	SETUP_ULPD1_REG	ULPD Wakeup Time Setup Register	16	R/W	03FFh
FFFE:0828 – FFFE:082C		Reserved			
FFFE:0830	CLOCK_CTRL_REG	ULPD Clock Control Register	16	R/W	0000h
FFFE:0834	SOFT_REQ_REG	ULPD Soft Clock Request Register	16	R/W	0000h
FFFE:0838	COUNTER_32_FIQ_REG	ULPD Modem Shutdown Delay Register	16	R/W	0001h
FFFE:083C	DPLL_CTRL_REG	ULPD USB DPLL Control Register	16	R/W	2211h
FFFE:0840	STATUS_REQ_REG	ULPD Hardware Request Status Register	16	R/W	undef
FFFE:0844		Reserved			
FFFE:0848	LOCK_TIME_REG	ULPD APLL Lock Time Register	16	R/W	0960h
FFFE:084C	APLL_CTRL_REG	ULPD APLL Control Register	16	R/W	undef
FFFE:0850	POWER_CTRL_REG	ULPD Power Control Register	16	R/W	0008h

Table 3–53. OMAP5912 Configuration Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:1000	FUNC_MUX_CTRL_0	Functional Mux Control Register 0	32	R/W	0000 0000h
FFFE:1004	FUNC_MUX_CTRL_1	Functional Mux Control Register 1	32	R/W	0000 0000h
FFFE:1008	FUNC_MUX_CTRL_2	Functional Mux Control Register 2	32	R/W	0000 0000h
FFFE:100C	COMP_MODE_CTRL_0	I/O Multiplex Enable Register 0	32	R/W	0000 0000h
FFFE:1010	FUNC_MUX_CTRL_3	Functional Mux Control Register 3	32	R/W	0000 0000h
FFFE:1014	FUNC_MUX_CTRL_4	Functional Mux Control Register 4	32	R/W	0000 0000h
FFFE:1018	FUNC_MUX_CTRL_5	Functional Mux Control Register 5	32	R/W	0000 0000h
FFFE:101C	FUNC_MUX_CTRL_6	Functional Mux Control Register 6	32	R/W	0000 0000h
FFFE:1020	FUNC_MUX_CTRL_7	Functional Mux Control Register 7	32	R/W	0000 0000h
FFFE:1024	FUNC_MUX_CTRL_8	Functional Mux Control Register 8	32	R/W	0000 0000h
FFFE:1028	FUNC_MUX_CTRL_9	Functional Mux Control Register 9	32	R/W	0000 0000h
FFFE:102C	FUNC_MUX_CTRL_A	Functional Mux Control Register A	32	R/W	0000 0000h
FFFE:1030	FUNC_MUX_CTRL_B	Functional Mux Control Register B	32	R/W	0000 0000h
FFFE:1034	FUNC_MUX_CTRL_C	Functional Mux Control Register C	32	R/W	0000 0000h
FFFE:1038	FUNC_MUX_CTRL_D	Functional Mux Control Register D	32	R/W	0000 0000h
FFFE:1040	PULL_DWN_CTRL_0	Pull Down Control Register 0	32	R/W	0000 0000h
FFFE:1044	PULL_DWN_CTRL_1	Pull Down Control Register 1	32	R/W	0000 0000h
FFFE:1048	PULL_DWN_CTRL_2	Pull Down Control Register 2	32	R/W	0000 0000h
FFFE:104C	PULL_DWN_CTRL_3	Pull Down Control Register 3	32	R/W	0000 0000h
FFFE:1050	GATE_INH_CTRL_0	Gate Inhibit Control Register 0	32	R/W	0000 0000h
FFFE:1058	CONF_REV	Configuration Revision	32	R	0000 0002h
FFFE:1060	VOLTAGE_CTRL_0	Voltage Control Register 0	32	R/W	0000 0000h
FFFE:1064	USB_TRANSCEIVER_CTRL	USB Transceiver Control Register	32	R/W	0000 0006h
FFFE:1068	LDO_PWRDN_CTRL	LDO Power Down Control Register	32	R/W	0000 0000h
FFFE:1080	MOD_CONF_CTRL_0	Module Configuration Register 0	32	R/W	0000 0000h
FFFE:1090	FUNC_MUX_CTRL_E	Function Mux Control Register E	32	R/W	0000 0000h
FFFE:1094	FUNC_MUX_CTRL_F	Function Mux Control Register F	32	R/W	0000 0000h
FFFE:1098	FUNC_MUX_CTRL_10	Function Mux Control Register 10	32	R/W	0000 0000h
FFFE:109C	FUNC_MUX_CTRL_11	Function Mux Control Register 11	32	R/W	0000 0000h
FFFE:10A0	FUNC_MUX_CTRL_12	Function Mux Control Register 12	32	R/W	0000 0000h
FFFE:10AC	PULL_DWN_CTRL_4	Pull Down Control Register 4	32	R/W	0000 0000h
FFFE:10B4	PU_PD_SEL_0	Pull Up Pull Down Slection Register 0	32	R/W	0000 0000h
FFFE:10B8	PU_PD_SEL_1	Pull Up Pull Down Slection Register 1	32	R/W	0000 0000h
FFFE:10B8	PU_PD_SEL_2	Pull Up Pull Down Slection Register 2	32	R/W	0000 0000h
FFFE:10C0	PU_PD_SEL_3	Pull Up Pull Down Slection Register 3	32	R/W	0000 0000h
FFFE:10C4	PU_PD_SEL_4	Pull Up Pull Down Slection Register 4	32	R/W	0000 0000h
FFFE:10D0	FUNC_MUX_DSP_DMA_A	DSP DMA Functional Mux Register A	32	R/W	undef
FFFE:10D4	FUNC_MUX_DSP_DMA_B	DSP DMA Functional Mux Register B	32	R/W	undef
FFFE:10D8	FUNC_MUX_DSP_DMA_C	DSP DMA Functional Mux Register C	32	R/W	undef
FFFE:10DC	FUNC_MUX_DSP_DMA_D	DSP DMA Functional Mux Register D	32	R/W	undef
FFFE:10EC	FUNC_MUX_ARM_DMA_A	ARM DMA Functional Mux Register A	32	R/W	undef
FFFE:10F0	FUNC_MUX_ARM_DMA_B	ARM DMA Functional Mux Register B	32	R/W	undef
FFFE:10F4	FUNC_MUX_ARM_DMA_C	ARM DMA Functional Mux Register C	32	R/W	undef

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Table 3–53. OMAP5912 Configuration Registers (Continued)

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:10F8	FUNC_MUX_ARM_DMA_D	ARM DMA Functional Mux Register D	32	R/W	undef
FFFE:10FC	FUNC_MUX_ARM_DMA_E	ARM DMA Functional Mux Register E	32	R/W	undef
FFFE:1100	FUNC_MUX_ARM_DMA_F	ARM DMA Functional Mux Register F	32	R/W	undef
FFFE:1104	FUNC_MUX_ARM_DMA_G	ARM DMA Functional Mux Register G	32	R/W	undef
FFFE:1110	MOD_CONF_CTRL_1	Module Configuration Control Register 1	32	R/W	undef
FFFE:1120	SECCTRL	Secure Mode Control Register	32	R/W	0000 0D1Ah
FFFE:1130	CONF_STATUS	Configuration Status Register	32	R	0000 0000h
FFFE:1140	RESET_CTRL	Reset Control Register	32	R/W	0000 007Fh
FFFE:1150	MOD_CONF_CTRL_2	Configuration Control Register 2	32	R/W	0000 0002h

Table 3–54. Device Die Identification Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:1800	DIE_ID_LSB	Device Die Identification Register (LSB)	32	R	undef
FFFE:1804	DIE_ID_MSB	Device Die Identification Register (MSB)	32	R	undef

Table 3–55. Production Identification Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:2000	PROD_ID_REG0	Production Identification Register0	32	R	undef
FFFE:2004	PROD_ID_REG1	Production Identification Register1	32	R	undef

Table 3–56. L3 OCP Initiator Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:C320	ADDR_FAULT	Address Fault Register	32	R	0000 0000h
FFFE:C324	MCMD_FAULT	Master Command Fault Register	32	R	0000 0000h
FFFE:C328	S_INTERRUPT0	Interrupt Sensitivity Register0	32	R/W	0000 0003h
FFFE:C330	S_INTERRUPT1	Interrupt Sensitivity Register1	32	R/W	0000 0003h
FFFE:C334	PROTECT	Memory Protect Register	32	R/W	0000 0000h
FFFE:C338	SECURE_MODE	Secure Mode Register	32	R/W	0000 007Fh
FFFE:C32C	ABORT_TYPE	Abort Type Register	32	R	0000 0000h

Table 3–57. MPU Interface (MPUI) Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:C900	CTRL_REG	MPUI Control Register	32	R/W	0003 FFFFh
FFFE:C904	DEBUG_ADDR	MPUI Debug Address Register	32	R	00FF FFFFh
FFFE:C908	DEBUG_DATA	MPUI Debug Data Register	32	R	FFFF FFFFh
FFFE:C90C	DEBUG_FLAG	MPUI Debug Flag Register	32	R	0000 1800h
FFFE:C910	STATUS_REG	MPUI Status Register	32	R	0000 1FFFh
FFFE:C914	DSP_STATUS_REG	MPUI DSP Status Register	32	R	0000 0000h
FFFE:C918	DSP_BOOT_CONFIG	MPUI Boot Configuration Register	32	R/W	0000 0000h
FFFE:C91C	DSP_API_CONFIG	MPUI DSP AP Configuration Register	32	R/W	0000 FFFFh
FFFE:C920	DSP_MISC_CONFIG	MPUI Miscellaneous Configuration Register	32	R/W	0000 0000h
FFFE:C924	ENHANCED_CTL	Enhanced Control Register	32	R/W	0000 0000h

Table 3–58. TIPB (Private) Bridge 1 Configuration Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:CA00	TIPB_CNTL	Private TIPB Control Register	16	R/W	FF11h
FFFE:CA04	TIPB_BUS_ALLOC	Private TIPB Bus Allocation Register	16	R/W	0009h
FFFE:CA08	MPU_TIPB_CNTL	Private MPU TIPB Control Register	16	R/W	0000h
FFFE:CA0C	ENHANCED_TIPB_CNTL	Private Enhanced TIPB Control Register	16	R/W	000Fh
FFFE:CA10	ADDRESS_DBG	Private Debug Address Register	16	R	FFFFh
FFFE:CA14	DATA_DEBUG_LOW	Private Debug Data LSB Register	16	R	FFFFh
FFFE:CA18	DATA_DEBUG_HIGH	Private Debug Data MSB Register	16	R	FFFFh
FFFE:CA1C	DEBUG_CNTR_SIG	Private Debug Control Signals Register	16	R	00FCh
FFFE:CA20	ACCESS_CNTL	Private Access Control Register	16	R/W	0001h

Table 3–59. Traffic Controller EMIFS Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:CC0C	EMIFS_CONFIG_REG	EMIFS Configuration Register	32	R/W	undef
FFFE:CC10	EMIFS_CS0_CONFIG	EMIFS nCS0 Configuration Register	32	R/W	undef
FFFE:CC14	EMIFS_CS1_CONFIG	EMIFS nCS1 Configuration Register	32	R/W	undef
FFFE:CC18	EMIFS_CS2_CONFIG	EMIFS nCS2 Configuration Register	32	R/W	undef
FFFE:CC1C	EMIFS_CS3_CONFIG	EMIFS nCS3 Configuration Register	32	R/W	undef
FFFE:CC28	EMIFS_TIMEOUT1	EMIFS Dynamic Priority Timeout 1 Register	32	R/W	0000 0000h
FFFE:CC2C	EMIFS_TIMEOUT2	EMIFS Dynamic Priority Timeout 2 Register	32	R/W	0000 0000h
FFFE:CC30	EMIFS_TIMEOUT3	EMIFS Dynamic Priority Timeout 3 Register	32	R/W	0000 0000h
FFFE:CC34	ENDIANISM	Endianism Register	32	R/W	0000 0000h
FFFE:CC38		Reserved			
FFFE:CC40	EMIFS_CFG_DYN_WAIT	EMIFS Dynamic Wait-States Register	32	R/W	0000 0000h
FFFE:CC44	EMIFS_ABORT_ADDR	EMIFS Abort Address Register	32	R	0000 0000h
FFFE:CC48	EMIFS_ABORT_TYPE	EMIFS Abort Type Register	32	R	0000 0000h
FFFE:CC4C	EMIFS_ABORT_TIMEOUT	EMIFS Abort Timeout Register	32	R/W	0000 01FFh
FFFE:CC50	EMIFS_ADV_CS0_CONFIG	Advanced EMIFS Chip Select Configuration Register nCS0	32	R/W	0000 0000h
FFFE:CC54	EMIFS_ADV_CS1_CONFIG	Advanced EMIFS Chip Select Configuration Register nCS1	32	R/W	0000 0000h

Table 3–59. Traffic Controller EMIFS Registers (Continued)

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:CC58	EMIFS_ADV_CS2_CONFIG	Advanced EMIFS Chip Select Configuration Register nCS2	32	R/W	0000 0000h
FFFE:CC5C	EMIFS_ADV_CS3_CONFIG	Advanced EMIFS Chip Select Configuration Register nCS3	32	R/W	0000 0000h

Table 3–60. Traffic Controller OCP–T1/OCP–T2 Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:CC00	OCP_T1_PRIO	OCP–T1 LRU Priority Register	32	R/W	0000 0000h
FFFE:CCA0	OCP_T1_TIMEOUT1	OCP–T1 Dynamic Priority Time-out Register 1	32	R/W	0000 0000h
FFFE:CCA4	OCP_T1_TIMEOUT2	OCP–T1 Dynamic Priority Time-out Register 2	32	R/W	0000 0000h
FFFE:CCA8	OCP_T1_TIMEOUT3	OCP–T1 Dynamic Priority Time-out Register 3	32	R/W	0000 0000h
FFFE:CCAC	OCP_T1_ABORT_TIMEOUT	OCP–T1 Abort Time-out Register	32	R/W	0000 01FFh
FFFE:CCB0	OCP_T1_ABORT_ADDR	OCP–T1 Abort Address Register	32	R	0000 0000h
FFFE:CCB4	OCP_T1_ABORT_TYPE	OCP–T1 Abort Type Register	32	R	0000 0000h
FFFE:CCB8	CONFIG_REG	OCP Target Configuration Register	32	R/W	0000 0000h
FFFE:CCD0	OCP_T2_PRIO	OCP–T2 LRU Priority Register	32	R/W	0000 0000h
FFFE:CCD4	OCP_T2_TIMEOUT1	OCP–T2 Dynamic Priority Time-out Register 1	32	R/W	0000 0000h
FFFE:CCD8	OCP_T2_TIMEOUT2	OCP–T2 Dynamic Priority Time-out Register 2	32	R/W	0000 0000h
FFFE:CCDC	OCP_T2_TIMEOUT3	OCP–T2 Dynamic Priority Time-out Register 3	32	R/W	0000 0000h
FFFE:CCE0	OCP_T2_ABORT_TIMEOUT	OCP–T2 Abort Time-out Register	32	R/W	0000 01FFh
FFFE:CCE4	OCP_T2_ABORT_ADDR	OCP–T2 Abort Address Register	32	R	0000 0000h
FFFE:CCE8	OCP_T2_ABORT_TYPE	OCP–T2 Abort Type Register	32	R	0000 0000h

Table 3–61. Traffic Controller OCPI Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:C320	OCP_ADDR_FAULT	OCPI Address Fault Register	32	R	0000 0000h
FFFE:C324	OCP_MCMD_FAULT	OCP Master Command Fault Register	32	R	0000 0000h
FFFE:C328	OCP_SINT0	OCP Sinterrupt 0 Register	32	R/W	0000 0003h
FFFE:C32C	OCP_ABORT_TYPE	OCP Abort Type Register	32	R/W	0000 0000h
FFFE:C330	OCP_SINT1	OCP Sinterrupt 1 Register	32	R/W	0000 0003h
FFFE:C334	OCP_PROT	OCP Protection Register	32	R/W	0000 0000h
FFFE:C338	OCP_SMOD	OCPI Secure Mode Register	32	R/W	0000 003Fh

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Table 3–62. Traffic Controller EMIFF Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:CC08	EMIFF_PRIO_REG	EMIFF Priority Register	32	R/W	0000 0000h
FFFE:CC20	EMIFF_SDRAM_CONFIG	EMIFF SDRAM Configuration Register	32	R/W	0061 8800h
FFFE:CC24	EMIFF_MRS	EMIFF SDRAM MRS Register	32	R/W	0000 0037h
FFFE:CC3C	EMIFF_SDRAM_CONFIG_2	EMIFF SDRAM Configuration Register 2	32	R/W	0000 0003h
FFFE:CC64	DLL_WRT_CTL	DLL WRT Control Register (write byte)	32	R/W	0000 0000h
FFFE:CC68	DLL_WRT_STAT	DLL WRT Status Register (read lower byte)	32	R	0000 0000h
FFFE:CC70	EMIFF_MRS_NEW	EMIFF SDRAM MRS Register (duplicate)	32	R/W	0000 0037h
FFFE:CC74	EMIFF_EMRS0	EMIFF SDRAM EMRS 0 Register	32	R/W	0000 0000h
FFFE:CC78	EMIFF_EMRS1	EMIFF SDRAM EMRS 1 Register	32	R/W	0000 0000h
FFFE:CC80	EMIFF_OP	EMIFF SDRAM Operation Register	32	R/W	0000 0004h
FFFE:CC84	EMIFF_MCMD	EMIFF SDRAM Manual Command Register	32	R/W	0000 0000h
FFFE:CC8C	EMIFF_TIMEOUT1	EMIFF Dynamic Arb. Priority Timeout 1 Register	32	R/W	0000 0000h
FFFE:CC90	EMIFF_TIMEOUT2	EMIFF Dynamic Arb. Priority Timeout 2 Register	32	R/W	0000 0000h
FFFE:CC94	EMIFF_TIMEOUT3	EMIFF Dynamic Arb. Priority Timeout 3 Register	32	R/W	0000 0000h
FFFE:CC98	EMIFF_ABORT_ADDR	EMIFF Abort Address Register	32	R	0000 0000h
FFFE:CC9C	EMIFF_ABORT_TYPE	EMIFF Abort Type Register	32	R	0000 0000h
FFFE:CCC0	DLL_URD_CTL	DLL URD Control Register (read upper byte)	32	R/W	0000 0000h
FFFE:CCC4	DLL_URD_STAT	DLL URD Status Register (read upper byte)	32	R	0000 0000h
FFFE:CCC8	EMIFF_EMRS2	EMIFF SDRAM EMRS 2 Register	32	R/W	0000 0000h
FFFE:CCCC	DLL_LRD_CTL	DLL LRD Control Register (read lower byte)	32	R/W	0000 0000h
FFFE:CCBC	DLL_LRD_STAT	DLL LRD Status Register (read lower byte)	32	R	0000 0000h

Table 3–63. MPU Clock/Reset/Power Mode Control Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:CE00	ARM_CKCTL	MPU Clock Control Register	32	R/W	3000h
FFFE:CE04	ARM_IDLECT1	MPU Idle Control 1 Register	32	R/W	0400h
FFFE:CE08	ARM_IDLECT2	MPU Idle Control 2 Register	32	R/W	0100h
FFFE:CE0C	ARM_EWUPCT	MPU External Wakeup Control Register	32	R/W	003Fh
FFFE:CE10	ARM_RSTCT1	MPU Reset Control 1 Register	32	R/W	0000h
FFFE:CE14	ARM_RSTCT2	MPU Reset Control 2 Register	32	R/W	0000h
FFFE:CE18	ARM_SYSST	MPU System Status Register	32	R/W	0038h
FFFE:CE1C	ARM_CKOUT1	MPU Clock Out Definition Register 1	32	R/W	0015h
FFFE:CE20	ARM_CKOUT2	MPU Clock Out Definition Register 2	32	R/W	0000h
FFFE:CE24	ARM_IDLECT3	MPU Idle Enable Control Register 3	32	R/W	0015h

Table 3–64. DPLL1 Configuration Register

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:CF00	DPLL1_CTL_REG	DPLL1 Control Register	32	R/W	0000 2002h

Table 3–65. DSP MMU Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:D200	DSP_MMU_PREFETCH_REG	DSP MMU Prefetch Register	16	R/W	0000h
FFFE:D204	DSP_MMU_WALKING_ST_REG	DSP MMU Prefetch Status Register	16	R	0000h
FFFE:D208	DSP_MMU_CNTL_REG	DSP MMU Control Register	16	R/W	0000h
FFFE:D20C	DSP_MMU_FAULT_AD_H_REG	DSP MMU Fault Address Register MSB	16	R	0000h
FFFE:D210	DSP_MMU_FAULT_AD_L_REG	DSP MMU Fault Address Register LSB	16	R	0000h
FFFE:D214	DSP_MMU_F_ST_REG	DSP MMU Fault Status Register	16	R	0000h
FFFE:D218	DSP_MMU_IT_ACK_REG	DSP MMU IT Acknowledge Register	16	W	0000h
FFFE:D21C	DSP_MMU_TTB_H_REG	DSP MMU TTB Register MSB	16	R/W	0000h
FFFE:D220	DSP_MMU_TTB_L_REG	DSP MMU TTB Register LSB	16	R/W	0000h
FFFE:D224	DSP_MMU_LOCK_REG	DSP MMU Lock Counter Register	16	R/W	0000h
FFFE:D228	DSP_MMU_LD_TLB_REG	DSP MMU Load Entry TLB Register	16	R/W	0000h
FFFE:D22C	DSP_MMU_CAM_H_REG	DSP MMU CAM Entry Register MSB	16	R/W	0000h
FFFE:D230	DSP_MMU_CAM_L_REG	DSP MMU CAM Entry Register LSB	16	R/W	0000h
FFFE:D234	DSP_MMU_RAM_H_REG	DSP MMU RAM Entry Register MSB	16	R/W	0000h
FFFE:D238	DSP_MMU_RAM_L_REG	DSP MMU RAM Entry Register LSB	16	R/W	0000h
FFFE:D23C	DSP_MMU_GFLUSH_REG	DSP MMU Global Flush Register	16	R/W	0000h
FFFE:D240	DSP_MMU_FLUSH_ENTRY_REG	DSP MMU Individual Flush Register	16	R/W	0000h
FFFE:D244	DSP_MMU_READ_CAM_H_REG	DSP MMU Read CAM Register MSB	16	R/W	0000h
FFFE:D248	DSP_MMU_READ_CAM_L_REG	DSP MMU Read CAM Register LSB	16	R/W	0000h
FFFE:D24C	DSP_MMU_READ_RAM_H_REG	DSP MMU Read RAM Register MSB	16	R/W	0000h
FFFE:D250	DSP_MMU_READ_RAM_L_REG	DSP MMU Read RAM Register LSB	16	R/W	0000h

Table 3–66. TIPB (Public) Bridge 2 Configuration Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
FFFE:D300	TIPB_CNTL	Public TIPB Control Register	16	R/W	FF11h
FFFE:D304	TIPB_BUS_ALLOC	Public TIPB Bus Allocation Register	16	R/W	0009h
FFFE:D308	MPU_TIPB_CNTL	Public MPU TIPB Control Register	16	R/W	0000h
FFFE:D30C	ENHANCED_TIPB_CNTL	Public Enhanced TIPB Control Register	16	R/W	0007h
FFFE:D310	ADDRESS_DBG	Public Debug Address Register	16	R	FFFFh
FFFE:D314	DATA_DEBUG_LOW	Public Debug Data LSB Register	16	R	FFFFh
FFFE:D318	DATA_DEBUG_HIGH	Public Debug Data MSB Register	16	R	FFFFh
FFFE:D31C	DEBUG_CNTR_SIG	Public Debug Control Signals Register	16	R	00F8h

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3.3 DSP Memory Maps

The DSP supports a unified program/data memory map (program and data accesses are made to the same physical space); however, peripheral registers are located in a separate I/O space which is accessed via the DSP's port instructions.

3.3.1 DSP Global Memory Map

The DSP Subsystem contains 160K bytes of on-chip SRAM (64K bytes of DARAM and 96K bytes of SARAM). The MPU also has access to these memories via the MPUI (MPU Interface) port. The DSP also has access to the shared system SRAM (250K bytes) and both EMIF spaces (EMIFF and EMIFS) via the DSP Memory Management Unit (MMU) which is configured by the MPU.

Table 3–67 shows the high-level program/data memory map for the DSP subsystem. DSP data accesses utilize 16-bit word addresses while DSP program fetches utilize byte addressing.

Table 3–67. DSP Global Memory Map

BYTE ADDRESS RANGE	WORD ADDRESS RANGE	INTERNAL MEMORY	EXTERNAL MEMORY†
0x00 0000 – 0x00 FFFF	0x00 0000 – 0x00 7FFF	DARAM 64K bytes	
0x01 0000 – 0x02 7FFF	0x00 8000 – 0x01 3FFF	SARAM 96K bytes	
0x02 8000 – 0x04 FFFF	0x01 4000 – 0x02 7FFF	Reserved	
0x05 0000 – 0xFF 7FFF	0x02 8000 – 0x7F BFFF		Managed by DSP MMU
0xFF 8000 – 0xFF FFFF	0x7F C000 – 0x7F FFFF	PDRAM (MPNMC = 0)	Managed by DSP MMU (MPNMC =1)

† This space could be external memory or internal shared system memory, depending on the DSP MMU configuration.

3.3.2 On-Chip Dual-Access RAM (DARAM)

The DARAM is located in the byte address range 000000h–00FFFFh and is composed of eight blocks of 8K bytes each (see Table 3–68). Each DARAM block can perform two accesses per cycle (two reads, two writes, or a read and a write).

Table 3–68. DARAM Blocks

DSP BYTE ADDRESS RANGE	DSP WORD ADDRESS RANGE	MEMORY BLOCK
0x00 0000 – 0x00 1FFF	0x00 0000 – 0x00 0FFF	DARAM 0
0x00 2000 – 0x00 3FFF	0x00 1000 – 0x001FFF	DARAM 1
0x00 4000 – 0x00 5FFF	0x00 2000 – 0x00 2FFF	DARAM 2
0x00 6000 – 0x00 7FFF	0x00 3000 – 0x00 3FFF	DARAM 3
0x00 8000 – 0x00 9FFF	0x00 4000 – 0x00 4FFF	DARAM 4
0x00 A000 – 0x00 BFFF	0x00 5000 – 0x00 5FFF	DARAM 5
0x00 C000 – 0x00 DFFF	0x00 6000 – 0x00 6FFF	DARAM 6
0x00 E000 – 0x00 FFFF	0x00 7000 – 0x00 7FFF	DARAM 7

3.3.3 On-Chip Single-Access RAM (SARAM)

The SARAM is located at the byte address range 010000h–027FFFh and is composed of 12 blocks of 8K bytes each (see Table 3–69). Each SARAM block can perform one access per cycle (one read or one write).

Table 3–69. SARAM Blocks

DSP BYTE ADDRESS RANGE	DSP WORD ADDRESS RANGE	MEMORY BLOCK
0x01 0000 – 0x01 1FFF	0x00 8000 – 0x00 8FFF	SARAM 0
0x01 2000 – 0x01 3FFF	0x00 9000 – 0x00 9FFF	SARAM 1
0x01 4000 – 0x01 5FFF	0x00 A000 – 0x00 AFFF	SARAM 2
0x01 6000 – 0x01 7FFF	0x00 B000 – 0x00 BFFF	SARAM 3
0x01 8000 – 0x01 9FFF	0x00 C000 – 0x00 CFFF	SARAM 4
0x01 A000 – 0x01 BFFF	0x00 D000 – 0x00 DFFF	SARAM 5
0x01 C000 – 0x01 DFFF	0x00 E000 – 0x00 EFFF	SARAM 6
0x01 E000 – 0x01 FFFF	0x00 F000 – 0x00 FFFF	SARAM 7
0x02 0000 – 0x02 1FFF	0x01 0000 – 0x01 0FFF	SARAM 8
0x02 2000 – 0x02 3FFF	0x01 1000 – 0x01 1FFF	SARAM 9
0x02 4000 – 0x02 5FFF	0x01 2000 – 0x01 2FFF	SARAM 10
0x02 6000 – 0x02 7FFF	0x01 3000 – 0x01 3FFF	SARAM 11

3.3.4 DSP I/O Space Memory Map

The DSP I/O space is a separate address space from the data/program memory space. The I/O space is accessed via the DSP's port instructions. The DSP I/O space is accessed using 16-bit word addresses. Table 3–70 to Table 3–82 specify the DSP base addresses where each set of registers is accessed. All accesses to these registers must utilize the appropriate access width as indicated in the tables. Accessing registers with the incorrect access width may cause unexpected results, including a TI Peripheral Bus (TIPB) bus error and associated TIPB interrupt.

3.3.4.1 DSP Private Peripheral Registers

The DSP Private Registers include the following:

- DSP DMA Controller Registers
- DSP Timer1 Registers
- DSP Timer2 Registers
- DSP Timer3 Registers
- DSP Watchdog Timer Registers
- DSP Level 2.0 Interrupt Handler Registers
- DSP Interrupt Interface Registers
- DSP Level 2.1 Interrupt Handler Registers

Table 3–70. DSP DMA Controller Registers

DSP WORD ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 0C00h	DSP_DMA_CSDP0	Channel 0 Source/Destination Parameters Register	16	R/W	0000h
0x00 0C01h	DSP_DMA_CCR0	Channel 0 Control Register	16	R/W	0000h
0x00 0C02h	DSP_DMA_CICR0	Channel 0 Interrupt Control Register	16	R/W	0003h
0x00 0C03h	DSP_DMA_CSR0	Channel 0 Status Register	16	R	0000h
0x00 0C04h	DSP_DMA_CSSA_L0	Channel 0 Source Start Address Register LSB	16	R/W	undef
0x00 0C05h	DSP_DMA_CSSA_U0	Channel 0 Source Start Address Register MSB	16	R/W	undef
0x00 0C06h	DSP_DMA_CDSA_L0	Channel 0 Destination Start Address Register LSB	16	R/W	undef
0x00 0C07h	DSP_DMA_CDSA_U0	Channel 0 Destination Start Address Register MSB	16	R/W	undef
0x00 0C08h	DSP_DMA_CEN0	Channel 0 Element Number Register	16	R/W	undef
0x00 0C09h	DSP_DMA_CFN0	Channel 0 Frame Number Register	16	R/W	undef
0x00 0C0Ah	DSP_DMA_CSFIO	Channel 0 Frame Index Register	16	R/W	undef
0x00 0C0Bh	DSP_DMA_CSEIO	Channel 0 Element Index Register	16	R/W	undef
0x00 0C0Ch	DSP_DMA_CSAC0	Channel 0 Source Address Counter Register	16	R/W	undef
0x00 0C0Dh	DSP_DMA_CDAC0	Channel 0 Destination Address Counter Register	16	R/W	undef
0x00 0C0Eh	DSP_DMA_CDFIO	Channel 0 Destination Frame Index	16	R/W	undef
0x00 0C0Fh	DSP_DMA_CDEIO	Channel 0 Destination Element Index	16	R/W	undef
0x00 0C10h – 0x00 0C1Fh		Reserved			
0x00 0C20h	DSP_DMA_CSDP1	Channel 1 Source/Destination Parameters Register	16	R/W	0000h
0x00 0C21h	DSP_DMA_CCR1	Channel 1 Control Register	16	R/W	0000h
0x00 0C22h	DSP_DMA_CICR1	Channel 1 Interrupt Control Register	16	R/W	0003h
0x00 0C23h	DSP_DMA_CSR1	Channel 1 Status Register	16	R	0000h
0x00 0C24h	DSP_DMA_CSSA_L1	Channel 1 Source Start Address Register LSB	16	R/W	undef
0x00 0C25h	DSP_DMA_CSSA_U1	Channel 1 Source Start Address Register MSB	16	R/W	undef
0x00 0C26h	DSP_DMA_CDSA_L1	Channel 1 Destination Start Address Register LSB	16	R/W	undef
0x00 0C27h	DSP_DMA_CDSA_U1	Channel 1 Destination Start Address Register MSB	16	R/W	undef
0x00 0C28h	DSP_DMA_CEN1	Channel 1 Element Number Register	16	R/W	undef
0x00 0C29h	DSP_DMA_CFN1	Channel 1 Frame Number Register	16	R/W	undef
0x00 0C2Ah	DSP_DMA_CSF11	Channel 1 Frame Index Register	16	R/W	undef
0x00 0C2Bh	DSP_DMA_CSE11	Channel 1 Element Index Register	16	R/W	undef
0x00 0C2Ch	DSP_DMA_CSAC1	Channel 1 Source Address Counter Register	16	R/W	undef
0x00 0C2Dh	DSP_DMA_CDAC1	Channel 1 Destination Address Counter Register	16	R/W	undef
0x00 0C2Eh	DSP_DMA_CDF11	Channel 1 Destination Frame Index	16	R/W	undef
0x00 0C2Fh	DSP_DMA_CDE11	Channel 1 Destination Element Index	16	R/W	undef
0x00 0C30h – 0x00 0C3Fh		Reserved			
0x00 0C40h	DSP_DMA_CSDP2	Channel 2 Source/Destination Parameters Register	16	R/W	0000h
0x00 0C41h	DSP_DMA_CCR2	Channel 2 Control Register	16	R/W	0000h
0x00 0C42h	DSP_DMA_CICR2	Channel 2 Interrupt Control Register	16	R/W	0003h
0x00 0C43h	DSP_DMA_CSR2	Channel 2 Status Register	16	R	0000h
0x00 0C44h	DSP_DMA_CSSA_L2	Channel 2 Source Start Address Register LSB	16	R/W	undef
0x00 0C45h	DSP_DMA_CSSA_U2	Channel 2 Source Start Address Register MSB	16	R/W	undef
0x00 0C46h	DSP_DMA_CDSA_L2	Channel 2 Destination Start Address Register LSB	16	R/W	undef
0x00 0C47h	DSP_DMA_CDSA_U2	Channel 2 Destination Start Address Register MSB	16	R/W	undef

Table 3–70. DSP DMA Controller Registers (Continued)

DSP WORD ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 0C48h	DSP_DMA_CEN2	Channel 2 Element Number Register	16	R/W	undef
0x00 0C49h	DSP_DMA_CFN2	Channel 2 Frame Number Register	16	R/W	undef
0x00 0C4Ah	DSP_DMA_CSF12	Channel 2 Frame Index Register	16	R/W	undef
0x00 0C4Bh	DSP_DMA_CSE12	Channel 2 Element Index Register	16	R/W	undef
0x00 0C4Ch	DSP_DMA_CSAC2	Channel 2 Source Address Counter Register	16	R/W	undef
0x00 0C4Dh	DSP_DMA_CDAC2	Channel 2 Destination Address Counter Register	16	R/W	undef
0x00 0C4Eh	DSP_DMA_CDF12	Channel 2 Destination Frame Index	16	R/W	undef
0x00 0C4Fh	DSP_DMA_CDE12	Channel 2 Destination Element Index	16	R/W	undef
0x00 0C50h – 0x00 0C5Fh		Reserved			
0x00 0C60h	DSP_DMA_CSDP3	Channel 3 Source/Destination Parameters Register	16	R/W	0000h
0x00 0C61h	DSP_DMA_CCR3	Channel 3 Control Register	16	R/W	0000h
0x00 0C62h	DSP_DMA_CICR3	Channel 3 Interrupt Control Register	16	R/W	0003h
0x00 0C63h	DSP_DMA_CSR3	Channel 3 Status Register	16	R	0000h
0x00 0C64h	DSP_DMA_CSSA_L3	Channel 3 Source Start Address Register LSB	16	R/W	undef
0x00 0C65h	DSP_DMA_CSSA_U3	Channel 3 Source Start Address Register MSB	16	R/W	undef
0x00 0C66h	DSP_DMA_CDSA_L3	Channel 3 Destination Start Address Register LSB	16	R/W	undef
0x00 0C67h	DSP_DMA_CDSA_U3	Channel 3 Destination Start Address Register MSB	16	R/W	undef
0x00 0C68h	DSP_DMA_CEN3	Channel 3 Element Number Register	16	R/W	undef
0x00 0C69h	DSP_DMA_CFN3	Channel 3 Frame Number Register	16	R/W	undef
0x00 0C6Ah	DSP_DMA_CSF13	Channel 3 Frame Index Register	16	R/W	undef
0x00 0C6Bh	DSP_DMA_CSE13	Channel 3 Element Index Register	16	R/W	undef
0x00 0C6Ch	DSP_DMA_CSAC3	Channel 3 Source Address Counter Register	16	R/W	undef
0x00 0C6Dh	DSP_DMA_CDAC3	Channel 3 Destination Address Counter Register	16	R/W	undef
0x00 0C6Eh	DSP_DMA_CDF13	Channel 3 Destination Frame Index	16	R/W	undef
0x00 0C6Fh	DSP_DMA_CDE13	Channel 3 Destination Element Index	16	R/W	undef
0x00 0C70h – 0x00 0C7Fh		Reserved			
0x00 0C80h	DSP_DMA_CSDP4	Channel 4 Source/Destination Parameters Register	16	R/W	0000h
0x00 0C81h	DSP_DMA_CCR4	Channel 4 Control Register	16	R/W	0000h
0x00 0C82h	DSP_DMA_CICR4	Channel 4 Interrupt Control Register	16	R/W	0003h
0x00 0C83h	DSP_DMA_CSR4	Channel 4 Status Register	16	R	0000h
0x00 0C84h	DSP_DMA_CSSA_L4	Channel 4 Source Start Address Register LSB	16	R/W	undef
0x00 0C85h	DSP_DMA_CSSA_U4	Channel 4 Source Start Address Register MSB	16	R/W	undef
0x00 0C86h	DSP_DMA_CDSA_L4	Channel 4 Destination Start Address Register LSB	16	R/W	undef
0x00 0C87h	DSP_DMA_CDSA_U4	Channel 4 Destination Start Address Register MSB	16	R/W	undef
0x00 0C88h	DSP_DMA_CEN4	Channel 4 Element Number Register	16	R/W	undef
0x00 0C89h	DSP_DMA_CFN4	Channel 4 Frame Number Register	16	R/W	undef
0x00 0C8Ah	DSP_DMA_CSF14	Channel 4 Frame Index Register	16	R/W	undef
0x00 0C8Bh	DSP_DMA_CSE14	Channel 4 Element Index Register	16	R/W	undef
0x00 0C8Ch	DSP_DMA_CSAC4	Channel 4 Source Address Counter Register	16	R/W	undef
0x00 0C8Dh	DSP_DMA_CDAC4	Channel 4 Destination Address Counter Register	16	R/W	undef
0x00 0C8Eh	DSP_DMA_CDF14	Channel 4 Destination Frame Index	16	R/W	undef
0x00 0C8Fh	DSP_DMA_CDE14	Channel 4 Destination Element Index	16	R/W	undef

Table 3–70. DSP DMA Controller Registers (Continued)

DSP WORD ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 0C90h – 0x00 0C9Fh		Reserved			
0x00 0CA0h	DSP_DMA_CSDP5	Channel 5 Source/Destination Parameters Register	16	RW	0000h
0x00 0CA1h	DSP_DMA_CCR5	Channel 5 Control Register	16	R/W	0000h
0x00 0CA2h	DSP_DMA_CICR5	Channel 5 Interrupt Control Register	16	R/W	0003h
0x00 0CA3h	DSP_DMA_CSR5	Channel 5 Status Register	16	R	0000h
0x00 0CA4h	DSP_DMA_CSSA_L5	Channel 5 Source Start Address Register LSB	16	R/W	undef
0x00 0CA5h	DSP_DMA_CSSA_U5	Channel 5 Source Start Address Register MSB	16	R/W	undef
0x00 0CA6h	DSP_DMA_CDSA_L5	Channel 5 Destination Start Address Register LSB	16	R/W	undef
0x00 0CA7h	DSP_DMA_CDSA_U5	Channel 5 Destination Start Address Register MSB	16	R/W	undef
0x00 0CA8h	DSP_DMA_CEN5	Channel 5 Element Number Register	16	R/W	undef
0x00 0CA9h	DSP_DMA_CFN5	Channel 5 Frame Number Register	16	R/W	undef
0x00 0CAAh	DSP_DMA_CSF15	Channel 5 Frame Index Register	16	R/W	undef
0x00 0CABh	DSP_DMA_CSEI5	Channel 5 Element Index Register	16	R/W	undef
0x00 0CACh	DSP_DMA_CSAC5	Channel 5 Source Address Counter Register	16	R/W	undef
0x00 0CADh	DSP_DMA_CDAC5	Channel 5 Destination Address Counter Register	16	R/W	undef
0x00 0CAEh	DSP_DMA_CDFI5	Channel 5 Destination Frame Index	16	R/W	undef
0x00 0CAFh	DSP_DMA_CDEI5	Channel 5 Destination Element Index	16	R/W	undef
0x00 0CB0h – 0x00 0DFFh		Reserved			
0x00 0E00h	DSP_DMA_GCR	Global Control Register	16	R/W	0008h
0x00 0E01h	DSP_DMA_GTCR	Global Timeout Control Register	16	R/W	0000h
0x00 0E02h	DSP_DMA_GSCR	Global Software Incompatible Control Register	16	R/W	0000h

Table 3–71. DSP Timer1 Registers

DSP WORD ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 2800h	DSP_TMR1_CNTL	DSP Timer1 Control Register	16	R/W	0000h
0x00 2802h	DSP_TMR1_LOAD_LO	DSP Timer1 Load Register Low	16	W	undef
0x00 2803h	DSP_TMR1_LOAD_HI	DSP Timer1 Load Register High	16	W	undef
0x00 2804h	DSP_TMR1_READ_LO	DSP Timer1 Read Register Low	16	R	undef
0x00 2805h	DSP_TMR1_READ_HI	DSP Timer1 Read Register High	16	R	undef

Table 3–72. DSP Timer2 Registers

DSP WORD ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 2C00h	DSP_TMR2_CNTL	DSP Timer2 Control Register	16	R/W	0000h
0x00 2C02h	DSP_TMR2_LOAD_LO	DSP Timer2 Load Register Low	16	W	undef
0x00 2C03h	DSP_TMR2_LOAD_HI	DSP Timer2 Load Register High	16	W	undef
0x00 2C04h	DSP_TMR2_READ_LO	DSP Timer2 Read Register Low	16	R	undef
0x00 2C05h	DSP_TMR2_READ_HI	DSP Timer2 Read Register High	16	R	undef

Table 3–73. DSP Timer3 Registers

DSP WORD ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 3000h	DSP_TMR3_CNTL	DSP Timer3 Control Register	16	R/W	0000h
0x00 3002h	DSP_TMR3_LOAD_LO	DSP Timer3 Load Register Low	16	W	undef
0x00 3003h	DSP_TMR3_LOAD_HI	DSP Timer3 Load Register High	16	W	undef
0x00 3004h	DSP_TMR3_READ_LO	DSP Timer3 Read Register Low	16	R	undef
0x00 3005h	DSP_TMR3_READ_HI	DSP Timer3 Read Register High	16	R	undef

Table 3–74. DSP Watchdog Timer Registers

DSP WORD ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 3400h	DSP_WD_CNTL_TIMER	DSP Watchdog Control Timer	16	R/W	0E02h
0x00 3402h	DSP_WD_LOAD_TIMER	DSP Watchdog Load Timer	16	W	FFFFh
0x00 3402h	DSP_WD_READ_TIMER	DSP Watchdog Read Timer	16	R	FFFFh
0x00 3404h	DSP_WD_TIMER_MODE	DSP Watchdog Timer Mode	16	R/W	8000h

Table 3–75. DSP Level 2.0 Interrupt Handler Registers

DSP WORD ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
TBD	TBD	TBD	TBD	TBD	TBD

Table 3–76. DSP Interrupt Interface Registers

DSP WORD ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 3800h	ET_LS_CTRL_HI	Edge Triggered/Level Sensitive Control Register High	16	R/W	007Fh
0x00 3801h	ET_LS_CTRL_LO	Edge Triggered/Level Sensitive Control Register Low	16	R/W	FFFFh
0x00 3800h	RST_LVL_HI	Reset Level Control Register High	16	R/W	0000h
0x00 3801h	RST_LVL_LO	Reset Level Control Register Low	16	R/W	0000h

Table 3–77. DSP Level 2.1 Interrupt Handler Registers

DSP WORD ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 4C00h	DSP_L21_ITR	Interrupt Register	16	R/W	0000h
0x00 4C02h	DSP_L21_MIR	Mask Interrupt Register	16	R/W	FFFFh
0x00 4C04h	DSP_L21_SIR_IRQ_CODE	IRQ Interrupt Encoded Source Register	16	R	0000h
0x00 4C06h	DSP_L21_SIR_FIQ_CODE	FIQ Interrupt Encoded Source Register	16	R	0000h
0x00 4C08h	DSP_L21_CONTROL_REG	Interrupt Control Register	16	R/W	0000h
0x00 4C0Ah	DSP_L21_ISR	Software Interrupt Set Register	16	R/W	0000h
0x00 4C0Ch	DSP_L21_ILR0	Interrupt 0 Priority Level Register	16	R/W	0000h
0x00 4C0Eh	DSP_L21_ILR1	Interrupt 1 Priority Level Register	16	R/W	0000h
0x00 4C10h	DSP_L21_ILR2	Interrupt 2 Priority Level Register	16	R/W	0000h
0x00 4C12h	DSP_L21_ILR3	Interrupt 3 Priority Level Register	16	R/W	0000h
0x00 4C14h	DSP_L21_ILR4	Interrupt 4 Priority Level Register	16	R/W	0000h
0x00 4C16h	DSP_L21_ILR5	Interrupt 5 Priority Level Register	16	R/W	0000h
0x00 4C18h	DSP_L21_ILR6	Interrupt 6 Priority Level Register	16	R/W	0000h
0x00 4C1Ah	DSP_L21_ILR7	Interrupt 7 Priority Level Register	16	R/W	0000h

Table 3–77. DSP Level 2.1 Interrupt Handler Registers (Continued)

DSP WORD ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 4C1Ch	DSP_L21_ILR8	Interrupt 8 Priority Level Register	16	R/W	0000h
0x00 4C1Eh	DSP_L21_ILR9	Interrupt 9 Priority Level Register	16	R/W	0000h
0x00 4C20h	DSP_L21_ILR10	Interrupt 10 Priority Level Register	16	R/W	0000h
0x00 4C22h	DSP_L21_ILR11	Interrupt 11 Priority Level Register	16	R/W	0000h
0x00 4C24h	DSP_L21_ILR12	Interrupt 12 Priority Level Register	16	R/W	0000h
0x00 4C26h	DSP_L21_ILR13	Interrupt 13 Priority Level Register	16	R/W	0000h
0x00 4C28h	DSP_L21_ILR14	Interrupt 14 Priority Level Register	16	R/W	0000h
0x00 4C2Ah	DSP_L21_ILR15	Interrupt 15 Priority Level Register	16	R/W	0000h

3.3.4.2 DSP Configuration Registers

The DSP Private Registers include the following:

- DSP TIPB Bridge Configuration Registers
- DSP EMIF Configuration Registers
- DSP I-CACHE Registers
- DSP Clock Mode Registers
- DSP TIPB Bus Switch Registers

Table 3–78. DSP TIPB Bridge Configuration Registers

DSP WORD ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 0000	DSP_ID	Identification Register	32	R/W	5555 5555h
0x00 0002	DSP_MODE	Mode Register	32	R/W	0000 0000h
0x00 0004	DSP_FRAME_SIZE	Frame Size Register	32	R/W	0000 0000h
0x00 0006	DSP_RXSTATE	Receive State Register	32	R/W	0000 0000h
0x00 0008	DSP_BUFSTATE	Receive Buffer State Register	32	R/W	0000 0000h
0x00 000E	DSP_BREAK	Break Detection State Register	32	R/W	0000 0000h
0x00 0010	DSP_ERROR	Error Detection State Register	32	R/W	0000 0000h
0x00 0012	DSP_ERRORACK	Error Acknowledge Register	32	R/W	0000 0000h
0x00 0014	DSP_CHANNELS	Channels Register	32	R/W	0000 0000h
0x00 0016	DSP_OVERRUN	Overflow Register	32	R/W	0000 0000h
0x00 0018	DSP_OVERRUNACK	Overflow Acknowledge Register	32	R/W	0000 0000h
0x00 001A	DSP_TIMEOUT	Timeout Period Register	32	R/W	0000 0000h
0x00 0040	DSP_BUFFER_CH0	Reception Buffer Channel 0 Register	32	R/W	0000 0000h
0x00 0042	DSP_BUFFER_CH1	Reception Buffer Channel 1 Register	32	R/W	0000 0000h
0x00 0044	DSP_BUFFER_CH2	Reception Buffer Channel 2 Register	32	R/W	0000 0000h
0x00 0046	DSP_BUFFER_CH3	Reception Buffer Channel 3 Register	32	R/W	0000 0000h
0x00 0048	DSP_BUFFER_CH4	Reception Buffer Channel 4 Register	32	R/W	0000 0000h
0x00 004A	DSP_BUFFER_CH5	Reception Buffer Channel 5 Register	32	R/W	0000 0000h
0x00 004C	DSP_BUFFER_CH6	Reception Buffer Channel 6 Register	32	R/W	0000 0000h
0x00 004E	DSP_BUFFER_CH7	Reception Buffer Channel 7 Register	32	R/W	0000 0000h
0x00 0060	DSP_SWAPBUFFER_CH0	Byte Swapping Receive Buffer Channel 0 Register	32	R/W	0000 0000h

Table 3–78. DSP TIPB Bridge Configuration Registers (Continued)

DSP WORD ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 0062	DSP_SWAPBUFFER_CH1	Byte Swapping Receive Buffer Channel 1 Register	32	R/W	0000 0000h
0x00 0064	DSP_SWAPBUFFER_CH2	Byte Swapping Receive Buffer Channel 2 Register	32	R/W	0000 0000h
0x00 0066	DSP_SWAPBUFFER_CH3	Byte Swapping Receive Buffer Channel 3 Register	32	R/W	0000 0000h
0x00 0068	DSP_SWAPBUFFER_CH4	Byte Swapping Receive Buffer Channel 4 Register	32	R/W	0000 0000h
0x00 006A	DSP_SWAPBUFFER_CH5	Byte Swapping Receive Buffer Channel 5 Register	32	R/W	0000 0000h
0x00 006C	DSP_SWAPBUFFER_CH6	Byte Swapping Receive Buffer Channel 6 Register	32	R/W	0000 0000h
0x00 006E	DSP_SWAPBUFFER_CH7	Byte Swapping Receive Buffer Channel 7 Register	32	R/W	0000 0000h

Table 3–79. DSP EMIF Configuration Registers

DSP WORD ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
TBD	TBD	TBD	TBD	TBD	TBD

Table 3–80. DSP I-Cache Registers

DSP WORD ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
TBD	TBD	TBD	TBD	TBD	TBD

Table 3–81. DSP Clock Mode Registers

DSP WORD ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 4000	DSP_CKTL	DSP Clock Control Register	16	R/W	0190h
0x00 4002	DSP_IDLCT1	DSP Idle Control 1 Register	16	R/W	0040h
0x00 4004	DSP_IDLCT2	DSP Idle Control 2 Register	16	R/W	0000h
0x00 4006		Reserved			
0x00 4008		Reserved			
0x00 400A	DSP_RSTCT2	DSP Reset Control 2 Register	16	R/W	0000h
0x00 400C	DSP_SYSST	DSP System Information Register	16	R/W	0000h

Table 3–82. DSP TIPB Bus Switch Registers

DSP WORD ADDRESS	REGISTER NAME	DESCRIPTION	ACCESS WIDTH	ACCESS TYPE	RESET VALUE
0x00 E400	DSP_UART1_SSW_CONF	UART1 Peripheral Ownership Register	32	R/W	0000 00001h
0x00 E410	DSP_UART2_SSW_CONF	UART2 Peripheral Ownership Register	32	R/W	0000 00001h
0x00 E420	DSP_UART3_SSW_CONF	UART3 Peripheral Ownership Register	32	R/W	0000 00001h
0x00 E448	DSP_MCBSP2_SSW_CONF	MCBSP2 Peripheral Ownership Register	32	R/W	0000 00001h
0x00 E450	DSP_I2C_SSW_CONF	I2C Peripheral Ownership Register	32	R/W	0000 00001h
0x00 E458	DSP_SPI_SSW_CONF	SPI Peripheral Ownership Register	32	R/W	0000 00001h
0x00 E460	DSP_GPTIMER1_SSW_CONF	GPTIMER1 Peripheral Ownership Register	32	R/W	0000 00001h
0x00 E468	DSP_GPTIMER2_SSW_CONF	GPTIMER2 Peripheral Ownership Register	32	R/W	0000 00001h
0x00 E470	DSP_GPTIMER3_SSW_CONF	GPTIMER3 Peripheral Ownership Register	32	R/W	0000 00001h
0x00 E478	DSP_GPTIMER4_SSW_CONF	GPTIMER4 Peripheral Ownership Register	32	R/W	0000 00001h
0x00 E480	DSP_GPTIMER5_SSW_CONF	GPTIMER5 Peripheral Ownership Register	32	R/W	0000 00001h
0x00 E488	DSP_GPTIMER6_SSW_CONF	GPTIMER6 Peripheral Ownership Register	32	R/W	0000 00001h
0x00 E498	DSP_GPTIMER7_SSW_CONF	GPTIMER7 Peripheral Ownership Register	32	R/W	0000 00001h
0x00 E4A0	DSP_GPTIMER8_SSW_CONF	GPTIMER8 Peripheral Ownership Register	32	R/W	0000 00001h
0x00 E4A8		Reserved			
0x00 E4B0	DSP_MMCS2_SSW_CONF	MMC/SDIO 2 Peripheral Ownership Register	32	R/W	0000 00001h

3.4 DSP External Memory (Managed by MMU)

When the DSP MMU is off, the 24 address lines are directly copied to the traffic controller without any modification. There is no virtual-to-physical address translation. All the addresses between 0x05 0000 and 0x00FF 8000 (0x00FF FFFF if DSP bit MP/MC = 1) are redirected to the first sector of Flash (CS0) in the shared memory space (shared by MPU and DSP). See Figure 3–2.

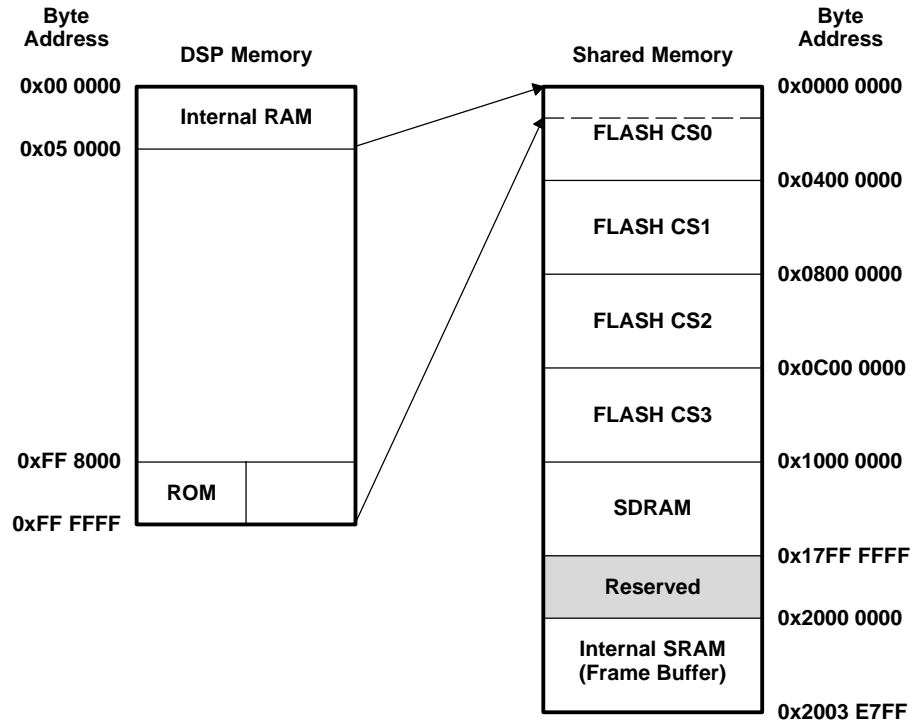


Figure 3–2. DSP MMU Off

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When the DSP MMU is on, the 24 address lines (virtual address) are relocated within a physical 32-bit address by the DSP MMU. The DSP MMU is controlled by the MPU. See Figure 3–3.

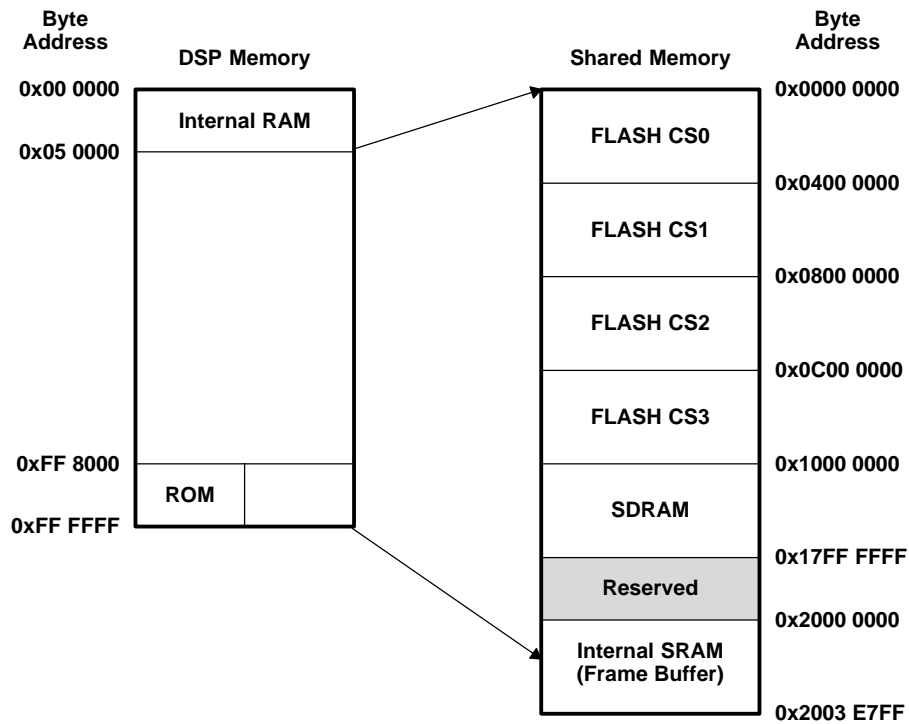


Figure 3–3. DSP MMU On

3.5 MPU and DSP Private Peripherals

The MPU and DSP each have their own separate private peripheral bus. Peripherals on each of these private buses may only be accessed by their respective processors. For instance, the DSP timers on the DSP private peripheral bus are not accessible by the MPU or the system DMA controller.

3.5.1 Timers

The MPU and DSP each have their own three 32-bit timers available on their respective private TI Peripheral Bus (TIPB). These timers may be configured either in auto-reload or one-shot mode with on-the-fly read capability. The timers generate an interrupt to the respective processor (MPU or DSP) when the timer's down-counter is equal to zero.

3.5.2 Watchdog Timer

The MPU and DSP each have a single watchdog timer. Each watchdog timer can be configured as either a watchdog timer or a general-purpose timer.

A watchdog timer requires that the MPU or DSP software or OS periodically write to the appropriate WDT count register before the counter underflows. If the counter underflows, the WDT generates a reset to the appropriate processor (MPU or DSP). The DSP WDT resets only the DSP processor while the MPU WDT resets both processors (MPU and DSP). The watchdog timers are useful for detecting user programs that are stuck in an infinite loop, resulting in loss of program control or in a runaway condition.

When used as a general-purpose timer, the WDT is a 16-bit timer configurable either in autoreload or one-shot mode with on-the-fly read capability. The timer generates an interrupt to the respective processor (MPU or DSP) when the timer's down-counter is equal to zero.

3.5.3 Interrupt Handlers

The MPU and DSP have two levels of interrupt handling each, allowing up to 160 interrupts on the MPU and 98 interrupts on the DSP. This is necessary because of the large number of integrated peripherals on the OMAP5912 device. Some peripherals can generate interrupts to both processors.

3.5.4 CompactFlash Controller (MPU Only)

The CompactFlash controller interfaces a CompactFlash and a classical memory interface. Control signals from the memory interface are processed through the CompactFlash controller to drive a CompactFlash, and control signals from CompactFlash are processed to perform a data transfer to the memory interface. Some pins are shared with common flash memory such as address bus, data bus, and control pins. The CompactFlash controller includes a bypass mode used when common flash memory is connected instead of a CompactFlash card. The CompactFlash module supports the following access modes:

- Common Memory
- Attribute Memory
- I/O

NOTE: True IDE mode is not supported.

3.5.5 LCD Controller (MPU Only)

The OMAP5912 device includes an LCD controller that interfaces with most industry-standard LCD displays. The LCD controller is configured by the MPU and utilizes a dedicated channel on the system DMA to transfer data from the frame buffer. The frame buffer can be implemented using external SDRAM via the EMIF. Using the frame buffer as its data source, the system DMA must provide data to the FIFO at the front end of the LCD controller data path at a rate sufficient to support the chosen display mode and resolution. Optimal performance is achieved when using the internal SRAM as the frame buffer.

The panel size is programmable, and can be any width (line length) from 16 to 1024 pixels in 16-pixel increments. The number of lines is set by programming the total number of pixels in the LCD. The total frame size is programmable up to 1024 x 1024; however, clock rate and frame size may be limited by memory bandwidth, which is shared with the MPU and DSP.

The screen is intended to be mapped to the frame buffer as one contiguous block where each horizontal line of pixels is mapped to a set of consecutive bytes of words in the frame memory.

The principle features of the LCD controller are:

- Dedicated 64-entry x 16-bit FIFO
- Dedicated LCD DMA channel for LCD display
- Programmable display including support for 2-, 4-, 8-, 12-, and 16-bit graphics modes
- Programmable display resolutions up to 1024 pixels by 1024 lines (assuming sufficient system bandwidth)
- Support for passive monochrome (STN) displays
- Support for passive color (STN) displays
- Support for active color (TFT) displays
- Patented dithering algorithm, providing:
 - 15 grayscale levels for monochrome passive displays
 - 3375 colors for color passive displays
 - 65536 colors for active color displays
 - 256-entry x 12-bit palette
- Programmable pixel rate
- Pixel clock plus horizontal and vertical synchronization signals
- AC-bias drive signal
- Active display enable signal

3.5.6 LCDCONV (MPU Only)

This module enables to provide a 16-bit to 18-bit LCD data conversion to the LCD interface. It supports two operating modes:

- 16-bit LCD mode
- 18-bit LCD mode

The mode switching is done by software by setting a dedicated bit in its control register. The software is also able to know which mode is currently in use by looking in a status register. When 16-bit LCD mode is used, the module operates in bypass mode, where all the 16-bit LCD pixel data coming from the frame buffer is directly provided to an external LCD interface. When the 18-bit LCD mode is used, the 16-bit LCD pixel signal is converted to an 18-bit LCD pixel signal through a Red, Green, Blue color (RGB) lookup table. Then the 18-bit LCD pixel format adds a LSB bit to the R (coding Red color) and B (Blue color) signals.

3.5.7 Random Number Generator (RNG)

The Random Number Generator (RNG) module provides a true, non-deterministic noise source for the purpose of generating keys, Initialization Vectors (IVs), and other random number requirements. It is designed for FIPS 140-1 compliance. It also includes Built-In Self-Test (BIST) logic that allows testing of the randomness of the module output and its compliance with the FIPS 140-1 standard.

Initial Latency After Reset

To make sure that sufficient entropy has been built up in the RNG, it takes 2^{25} (33554432) system clock cycles after RNG reset to produce the first random output. Reading the Random Number Output Register (RNG_OUT) triggers the generation of the next random number, and the busy status bit is set to 1.

Generate Random Number

It takes only 160 system clock cycles to produce each subsequent 32-bit random number once the initial reset latency has been completed. The random numbers are accessible to the application in a 32-bit read-only register (RNG_OUT). Once the register is read, the RNG module immediately generates a new value, which is available after 160 system clock cycles and is then shifted into the output register.

3.5.8 DES/3DES

The DES3DES security module provides hardware-accelerated data encryption/decryption functions. It can run either the single DES algorithm or the triple DES (TDES or 3DES) algorithm in compliance with the FIPS 46-3 standard. It supports ECB (Electronic Codebook) and CBC (Cipher Block Chaining) modes of operation. It does not support the CFB (Cipher Feedback) and the OFB (Output Feedback) modes of operation in hardware.

3.5.9 SHA1/MD5

The SHA1MD5 security module provides hardware-accelerated hash functions. It can run either the SHA-1 algorithm in compliance with the FIPS 180-1 standard or the MD5 Message-Digest Algorithm developed by R. Rivest in 1991. Up to 2^{27} bytes (128 Mbytes) of data can be hashed in a single operation and will produce a 160-bit signature in the case of SHA-1, and a 128-bit signature in the case of MD5.

3.6 MPU Public Peripherals

Peripherals on the MPU Public Peripheral bus may only be accessed by the MPU and the system DMA controller, which is configured by the MPU. This bus is called a public bus because it is accessible by the system DMA controller. The DSP cannot access peripherals on this bus.

3.6.1 USB Interface

The OMAP5912 processor provides several varieties of USB functionality, including:

- USB host: OMAP5912 provides a three-port USB Specification Revision 1.1-compliant host controller, which is based on the OHCI Specification for USB Release 1.0a.
- USB device: OMAP5912 provide a full-speed USB device.
- USB On-The-Go (OTG): OMAP5912 acts as an OTG dual-role device; the USB device functionality and one port of the USB host controller act in concert to provide an OTG port.

Flexible multiplexing of signals from the OMAP5912 USB host controller, USB function controller, and other peripherals allows for a wide variety of system-level USB capabilities. Many of the OMAP5912 pins can be used for USB-related signals or for signals from other peripherals. The top-level pin multiplexing controls each pin individually and allows for the selection of one of several possible internal pin signal interconnections.

When these shared pins are programmed for use as USB signals, the OMAP5912 USB signal multiplexing selects how the signals associated with the three OMAP5912 USB host ports and the OMAP5912 USB function controller can be brought out to OMAP5912 pins.

The USB host controller (HC) is a three-port controller that communicates with USB devices at low-speed (1.5M bit-per-second maximum) and full-speed (12M bit-per-second maximum) data rates. It is compatible with the Universal Serial Bus Specification Revision 2.0 and the OpenHCI – Open Host Controller Interface Specification for USB, Release 1.0a, which is available on the Internet, and is hereafter called the OHCI Specification for USB. It is assumed that users of the OMAP5912 USB host controller are already familiar with the USB Specification and OHCI Specification for USB.

The OMAP5912 OTG controller can use one of the USB host controller ports as part of a USB OTG-capable connection. When used for an OTG connection, the host controller port acts as the upstream device when OMAP5912 controls the OTG link, and the USB function controller acts as the downstream device when OMAP5912 acts as an OTG downstream device.

The USB host controller implements the register set and makes use of the memory data structures defined in the OHCI Specification for USB. These registers and data structures are the mechanism by which a USB host controller driver software package can control the USB host controller. The OHCI Specification for USB also defines how the USB host controller implementation must interact with those registers and data structures in system memory. The OMAP5912 MPU accesses these registers via the MPU public peripheral bus.

NOTE: USB 2.0 hi-speed is not supported.

3.6.2 Display Interface SoSSI

The SoSSI peripheral supports the medium speed screen interface (MeSSI) display interface standard. This peripheral includes a VIA-bus interface converted into TIPB interface connected on the MPU shared peripheral bus, and an interface with the system DMA which enables connection of an extended LCD display to the OMAP5912 device.

This peripheral supports multiple frequencies for different displays (maximum output data frequency is 20 MHz). It also provides the capability to program the number of bytes sent to the LCD display.

The display interface is a bidirectional parallel interface. It consists of a display data I/O bus (DispDataOut[15:0]), write enable (WRX), read enable (RDX), chip-select (CS), and command/pixel data (A0) signals.

3.6.3 Camera Interface

The camera interface is an 8-bit external port that can be used to accept data from an external camera sensor. This interface can handle multiple image formats synchronized on vertical and horizontal synchronization signals.

The camera interface module converts the 8-bit data transfers into 32-bit words and utilizes a 128-word buffer to facilitate efficient data transfer to memory. Data may be transferred from the camera interface buffer to internal memory by the system DMA controller or directly by the MPU. The interface provides an output reference clock at rates of 6 MHz to 24 MHz from the internal clock (ARM peripheral clock).

3.6.4 Compact Camera Port (CCP)

In addition to the parallel camera interface, OMAP5912 includes a 2-pin differential pair compact camera port interface.

This interface is a synchronous serial bus, one data and one clock line. The camera provides one clock, another clock is provided by OMAP5912 to the camera. The CCP interface uses differential signalling, and subLVDS I/Os are needed for that. The CCP is a unidirectional interface. Control information to the camera is transmitted via an I²C Bus™.

¹I²C Bus is a trademark of Philips Electronics N.V.

3.6.5 MICROWIRE Serial Interface

The MICROWIRE interface is a serial synchronous interface that can drive up to four serial external components. This interface is compatible with the MICROWIRE standard and is seen as the master.

MICROWIRE is typically used to transmit control and status information to external peripheral devices or to transmit data to or from small nonvolatile memories such as serial EEPROMs or serial flash devices.

3.6.6 Real-Time Clock (RTC)

The RTC peripheral provides an embedded real-time clock module that can be directly accessible from the MPU. The RTC peripheral is powered independently of the OMAP5912 MPU core power.

The RTC module has the following features:

- Time information (seconds/minutes/hours) directly in BCD code
- Calendar information (day/month/year/day of the week) directly in BCD code up to year 2099
- Interrupts generation, periodically (1s/1m/1h/1d period) or at a precise time of the day (alarm function)
- 30-s time correction
- Oscillator frequency calibration

3.6.7 Pulse-Width Tone (PWT)

The pulse-width tone (PWT) peripheral generates a modulated frequency signal for use with an external buzzer. The frequency is programmable between 349 Hz and 5276 Hz with 12 half-tone frequencies per octave. The volume level of the output is also programmable.

3.6.8 Pulse-Width Light (PWL)

The pulse-width light (PWL) peripheral allows the control of the backlight of the LCD and the keypad by employing a 4096-bit random sequence. This voltage level control technique decreases the spectral power at the modulator harmonic frequencies. The block uses a switchable 32-kHz clock, independent of UPS.

3.6.9 Keyboard Interface

Keyboard is composed of specific MPUIOs dedicated for 8 x 8 keyboard connection:

- Eight inputs (KB.R[7:0]) for row lines
- Eight outputs (KB.C[7:0]) for column lines

The keyboard feature allows communication with a keyboard. The MPUIO or keyboard interface supports keyboards with up to eight rows and eight columns and has the capability to detect multiple key presses. A keyboard event is signaled to the host by an interrupt.

3.6.10 HDQ/1-Wire Interface

This module allows implementation of both HDQ and 1-Wire protocols. These protocols use a single wire to communicate between a master and a slave. The HDQ/1-Wire pin is open-drain and requires an external pullup resistor.

HDQ and 1-Wire interfaces can be found on commercially available battery and power management devices. The interface can be used to send command and monitor its status between OMAP5912 and such devices.

3.6.11 Multimedia Card/Secure Digital (MMC/SDIO1) Interface

The MMC/SDIO1 host controller provides an interface between the MPU and MMC/SD/SDIO memory cards plus up to four serial flash cards, and it also handles MMC/SDIO or SPI transactions with minimum local host intervention. The following combinations of external devices are supported:

- One or more MMC memory cards sharing the same bus and up to four devices with 8-bit SPI protocol interface (serial flash memories, etc.)
- One single SD memory card or SDIO card and up to four devices with 8-bit SPI protocol interface

The application interface is responsible for managing transaction semantics; the MMC/SDIO1 host controller deals with MMC/SDIO protocol at transmission level, packing data, adding CRC, start/end bit and checking for syntactical correctness. SD mode wide bus width is also supported (1- or 4-bit data lines).

The application interface can send every MMC/SDIO command and either poll for the status of the adapter or wait for an interrupt request, which is sent back in case of exceptions or to notify for end of operations. The application interface can read card responses or flag register. It can also mask individually interrupt sources. All these operations can be performed reading and writing control registers. The MMC/SDIO1 peripheral also supports two DMA channels. The main features of the MMC/SDIO1 module are:

- Full compliance with MMC command/response sets as defined in the MMC standard specifications v.3.1
- Full compliance with SD command/response sets as defined in the SD physical layer specifications v.1.0
- Full compliance with SDIO command/response sets as defined in the SDIO card specification v1.0
- Flexible architecture, allowing support for new command structure
- Built-in 64-byte FIFO for buffered read or write
- 16-bit-wide access bus to maximize bus throughput
- Designed for low power
- Wide interrupt capability
- Programmable clock generation
- Two DMA channels

NOTE:

The MMC/SDIO1 interface includes all the MMC/SDIO pins except the direction controls (data and control).

3.6.12 MPUIO Interface

The MPUIO feature allows communication with an external device through as many as 16 MPUIOs. These MPUIOs can be configured on a pin-by-pin basis as inputs or outputs. When configured as input, each MPUIO can be individually selected to generate interrupts on a level change (rising or falling edge). In normal operation, the MPUIO inputs are latched at the falling edge of 32 kHz. In event capture mode, one of the MPUIO inputs can be assigned a clock source, and all the other inputs are latched on its falling edge.

The MPUIO module functional clock domain is clocked by the OMAP5912 32-kHz clock. This clock is always fed into the block, regardless of the state of the chip (awake, asleep, or idle). This allows external event latching and interrupt generation even when the system is in idle mode, to wake up the system via interrupt.

The MPUIO module interfaces with the host through a TIPB bus. The MPU peripheral clock resynchronizes register access to the module and avoids time-out on the TIPB bus caused by the functional clock being too slow.

3.6.13 LED Pulse Generators (LPG)

There are two separate LED pulse generator (LPG) modules. Each LPG module provides an output for an indication LED. The blinking period is programmable between 152 ms and 4 s or the LED can be switched on or off permanently.

3.6.14 Frame Adjustment Counter (FAC)

The frame adjustment counter (FAC) is a simple peripheral that counts the number of rising edges of one signal (start of frame interrupt of the USB function) during a programmable number of rising edges of a second signal (transmit frame synchronization of McBSP2). The FAC may only be used with these specific USB Function and McBSP2 signals. The count value can be used by system-level software to adjust the duration of the two time domains with respect to each other to reduce overflow and underflow. If the data being transferred is audio data, this module can be part of a solution that reduces pops and clicks. The FAC module generates one second-level interrupt to the MPU.

3.6.15 Operating System (OS) Timer

A programmable interval timer is required to generate a periodic interrupt, also called system clock tick, to the OS. This is used to keep track of the current time and to control the operation of device drivers.

Key functions are:

- Read current value of the timer
- Generate interrupt as the timer down-counts to zero
- Reset the interrupt by writing an 1 to the interrupt bit in the control register
- Timer interrupt period: $Irq_rate = (Tick_value_reg + 1) / 32768$
- Maximum tick value register is 0xFFFF, so maximum timer interrupt period is 2 sec.

3.7 DSP Public Peripherals

Peripherals on the DSP Public Peripheral bus are directly accessible by the DSP and DSP DMA. These peripherals may also be accessed by the MPU and System DMA Controller via the MPUI interface. The MPUI interface must be properly configured to allow this access.

3.7.1 Multichannel Buffered Serial Ports (McBSP1 and 3)

The multichannel buffered serial port (McBSP) provides a high-speed, full-duplex synchronous serial port that allows direct interface to audio codecs and various other system devices. The DSP public peripheral bus has access to two McBSPs: McBSP1 and McBSP3.

NOTE: All of the standard McBSP pins are not necessarily available on every McBSP on the OMAP5912 devices. In the case of the two DSP McBSPs, the following pins are available:

McBSP1 pins:

- CLKX (data bit clock)
- FSX (data bit frame sync)
- DX and DR (transmit and receive data)
- CLKS (external reference to sample rate generator)

McBSP3 pins:

- CLKX (transmit clock)
- FSX (transmit frame sync)
- DX and DR (transmit and receive data)

CLKX and FSX of McBSP1 and McBSP3 are used for both transmitting and receiving.

The functional clock to the McBSP1 and McBSP3 is fixed at the OMAP5912 base operating frequency (12, 13, or 19.2 MHz). The bit-clock rate for these McBSPs is therefore limited to 6, 6.5, or 9.6 MHz (one half the base frequency).

Only McBSP1 has the CLKS pin available. If the sample rate generator (SRG) is used on McBSP1, the reference clock to the SRG can be configured to be either an external reference provided on the CLKS pin, or the internal base (12, 13, or 19.2-MHz) device clock. However, if the SRG is used on McBSP3, the only reference clock available to this SRG is the base device clock as clock reference.

3.7.2 Multichannel Serial Interfaces (MCSI1 and 2)

The MCSI provides a flexible serial interface with multichannel transmission capability. The MCSI allows the DSP to access a variety of external devices, such as audio codecs and other types of analog converters. The DSP public peripheral bus has access to two MCSIs: MCSI1 and MCSI2. These MCSIs provide full-duplex transmission and master or slave clock control. All transmission parameters are configurable to cover the maximum number of operating conditions. The MCSIs have the following features:

- Master or slave clock control (transmitter clock and frame synchronization pulse)
 - Programmable transmitter clock frequency in master mode of up to one half the OMAP5912 base frequency (12,13, or 19.2 MHz)
 - Receiver clock frequency in slave mode of up to the base frequency (12,13, or 19.2 MHz)
- Single-channel or multichannel (x16) frame structure
- Programmable word length: 3 to 16 bits
- Full-duplex transmission
- Programmable frame configuration
 - Continuous or burst transmission
 - Normal or alternate framing
 - Normal or inverted frame and clock polarities
 - Short or long frame pulse
 - Programmable oversize frame length
 - Programmable frame length
- Programmable interrupt occurrence time (TX and RX)
 - Error detection with interrupt generation on wrong frame length
 - System DMA support for both TX and RX data transfers

3.8 Shared Peripherals

The shared peripherals are connected to both the MPU Public Peripheral bus and the DSP Public Peripheral bus. Connections are achieved via a TI Peripheral Bus Switch, which must be configured to allow MPU or DSP access. The other shared peripherals have permanent connections to both public peripheral buses, although read and write accesses to each peripheral register may differ.

3.8.1 Mailboxes

Four sets of shared mailbox registers are available for communication between the DSP and MPU:

- Two read/write accessible by MPU, read-only by the DSP
- Two read/write accessible by the DSP, read-only by the MPU

3.8.2 General-Purpose Timers

OMAP5912 consists of eight 32-bit timers with the following features:

- Counter timer with compare and capture modes
- Autoreload mode
- Start-stop mode
- Programmable divider clock source
- 16-/32-bit addressing
- On-the-fly read/write registers
- Interrupts generated on overflow, compare, and capture
- Interrupt enable
- Wake-up enable
- Write posted mode
- Dedicated input trigger for capture mode and dedicated output trigger/PWM signal

Each timer module contains a free-running upward counter with autoreload capability on overflow. The timer counter can be read and written on-the-fly (while counting). The timer module includes compare logic to allow interrupt event on programmable counter matching value. A dedicated output signal can be pulsed or toggled on overflow and match event. This offers timing stamp trigger signal or PWM (pulse width modulation) signal sources. A dedicated input signal can be used to trigger automatic timer counter capture and interrupt event, on programmable input signal transition type. A programmable clock divider (prescaler) allows reduction of the timer input clock frequency. All internal timer interrupt sources are merged into one module interrupt line and one wake-up line. Each internal interrupt sources can be independently enabled/disabled with a dedicated bit of the TIER register for the interrupt features and a dedicated bit of TWER for the wake-up.

Each timer has three possible clock sources:

- the 32-kHz clock
- the system clock
- an external clock source

NOTE:

- Three of the eight dual-mode timer PWM outputs are connected at OMAP5912 I/Os. Two of the eight dual-mode timer input capture are connected at OMAP5912 I/Os. The system clock can come either from OMAP or directly from the input clock.
- Can wake up the system when the clock is configured as 32-kHz through its own interrupt through a general-purpose timer

3.8.3 Serial Port Interface (SPI)

The serial port interface is a bidirectional, four-line interface dedicated to the transfer of data to and from external devices offering a four-line serial interface. The four-line interfaces are:

- the clock used to shift-in and shift-out data
- the device enable
- the data input
- the data output

This serial port interface is based on a looped shift-register, thus allowing both transmit and receive modes. It can operate either in master or slave mode, using MPU or DMA control.

In master mode, the SPI provides up to five chip-selects; four of them are for external devices. In slave mode, the SPI has its own chip-select.

In master mode, the maximum SPI data rate is the same as the system clock frequency; in slave mode, the clock of the serial data out is provided by an external device at lower data rate.

3.8.4 Universal Asynchronous Receiver/Transmitter (UART)

The OMAP5912 includes three universal asynchronous receiver/transmitter (UART) peripherals which are accessible on the DSP public and MPU public peripheral buses. The MPU configures the UART's owner processor (MPU or DSP). All three UARTs are standard 16C750-compatible UARTs implementing an asynchronous transfer protocol with various flow control options. UART1 and UART3 can function as general UART or can optionally function as IrDA interface.

The clock source for the UART1 and UART3 is:

- APLL output

The clock source for the UART2 can be:

- system clock or the sleep clock
- APLL output

The main features of the UART peripherals include:

- Selectable UART/autobaud modes
- Dual 64-entry FIFOs for received and transmitted data payload
- Programmable and selectable transmit and receive FIFO trigger levels for DMA and interrupt generation

- Programmable sleep mode
- Complete status-reporting capabilities in both normal and sleep mode
- Frequency prescaler values from 0 to 65535 to generate the appropriate baud rates
- Interrupt request generated if multiple system DMA requests
- Baud rate from 300 bits/s up to 1.5M bits/s
- Autobauding between 1200 bits/s and 115.2K bits/s
- Software/hardware flow control
 - Programmable XON/XOFF characters
 - Programmable auto-RTS and auto-CTS
- Programmable serial interface characteristics
 - 5-, 6-, 7-, or 8-bit characters
 - Even-, odd-, or no-parity bit generation and detection
 - 1, 1.5, or 2 stop-bit generation
 - False start bit detection
 - Line break generation and detection
- Internal test and loopback capabilities
- Modem control functions (CTS, RTS, DSR, DTR)
NOTE: DSR and DTR are not available on UART2.

The key features of the IrDA mode (UART1 and 3) are:

- Support of slow infrared (SIR) configuration (baud rate up to 115.2Kbauds)
- Support of medium infrared (MIR) configuration (baud rate 0.576Mbits/s, and 1.152Mbits/s in the following range [1.1508Mbits/s to 1.1532Mbits/s])
- Support of fast infrared (FIR) configuration (baud rate at 4Mbauds, the effective frequency baud rate is 8Mbits/s in the following range [7.9992Mbits/s to 8.0008Mbits/s])
- Frame formatting: addition of variable xBOF characters and EOF characters
- Uplink/downlink CRC generation/detection
- Asynchronous transparency (automatic insertion of break character)
- 8-entry status FIFO available to monitor frame length and frame errors

3.8.5 I²C Master/Slave Interface

The multimaster I²C peripheral provides an interface between a local host (LH), such as an MPU or DSP processor, and any I²C bus compatible device that connects via the I²C serial bus. External components attached to the I²C bus can serially transmit/receive up to 8 bits of data to/from the LH device or a DMA through the I²C interface. This I²C peripheral supports any slave or master I²C-compatible device.

The I²C bus is a multimaster bus. The I²C controller supports the multimaster mode, which allows more than one device capable of controlling the bus to be connected to it. Each I²C device is recognized by a unique address and can operate as either transmitter or receiver, depending on the function of the device. In addition to being a transmitter or receiver, the device connected to the I²C bus can also be considered a master or a slave when performing data transfers. Note that a master device is the device which initiates a data transfer on the bus and generates the clock signals to enable that transfer. During the latter, any device addressed by this master is considered a slave.

The I²C interface with the local host is compliant with 8-/16-bit OCP protocol. The interface clock and the functional clock are independent. The I²C master/slave interface supports the following features:

- Compliant to Philips I²C-bus specification version 2.1
- Support standard mode (up to 100K bits/s) and fast mode (up to 400K bits/s)
- In the master only I²C operating mode of OMAP5912, standard mode is supported up to 83K bits/s.
- 7-bit and 10-bit device addressing modes
- General call
- Start/restart/stop
- Multimaster transmitter/slave receiver mode
- Multimaster receiver/slave transmitter mode
- Combined master transmit/receive and receive/transmit mode
- Built-in FIFO for buffered read or write
- Module enable/disable capability
- Programmable clock generation
- Supports use of two DMA channels

The I²C master/slave interface does not support the following features:

- High-speed (HS) mode for transfer rates up to 3.4M bits
- C-bus compatibility mode

3.8.6 Multichannel Buffered Serial Port (McBSP2)

The multichannel buffered serial port (McBSP) provides a high-speed, full-duplex serial port that allows direct interface to audio codecs, and various other system devices. The McBSP provides:

- Full-duplex communication
- Double-buffer data registers, which allow a continuous data stream
- Independent framing and clocking for receive and transmit

In addition, the McBSP has the following capabilities:

- Direct interface to:
 - T1/E1 framers
 - MVIP switching-compatible and ST-BUS compliant devices
 - IOM-2 compliant device
 - AC97-compliant device
 - I2S-compliant device
 - Serial peripheral interface (SPI)
- Multichannel transmit and receive of up to 128 channels per frame
- A variety of data sizes, including: 8, 12, 16, 20, 24, or 32 bits
- μ -law and A-law companding
- Programmable polarity for both frame synchronization and data clocks
- Programmable internal clock and frame generation

NOTE: All of the standard McBSP signals are not necessarily available on every McBSP on the OMAP5912 device.

In the case of the MPU McBSP2, the following pins are available:

- CLKX and CLKR (transmit and receive clocks)
- FSX and FSR (transmit and receive frame syncs)
- DX and DR (transmit and receive data)

The functional clock to the McBSP2 peripheral is configurable to the DPLL clock rate with a divider of 1, 2, 4, or 8. McBSP2 does not have a CLKS external clock reference pin. Therefore, if the McBSP2 sample rate generator (SRG) is used, the only reference clock available to the SRG is a programmable clock from the MPU domain.

3.8.7 Multimedia Card/Secure Digital (MMC/SDIO2) Interface

The MMC/SDIO2 host controller provides an interface between a local host (such as the MPU/DSP and MMC/SD/SDIO memory cards) plus up to four serial flash cards, and handles MMC/SDIO or SPI transactions with minimum local host intervention. The following combinations of external devices are supported:

- One or more MMC memory cards sharing the same bus and up to four devices with 8-bit SPI protocol interface (serial flash memories, etc.)
- One single SD memory card or SDIO card and up to four devices with 8-bit SPI protocol interface

The application interface is responsible for managing transaction semantics; the MMC/SDIO2 host controller deals with MMC/SDIO protocol at transmission level, packing data, adding CRC, start/end bit and checking for syntactical correctness. SD mode wide bus width is also supported (1- or 4-bit data lines).

The application interface can send every MMC/SDIO command and either poll for the status of the adapter or wait for an interrupt request, which is sent back in case of exceptions or to warn for end of operations. The application interface can read card responses or flag register. It can also mask individually interrupt sources. All these operations can be performed reading and writing control registers. The MMC/SDIO2 peripheral also supports two DMA channels.

The main features of the MMC/SDIO2 module are:

- Full compliance with MMC command/response sets as defined in the MMC standard specifications v.3.1
- Full compliance with SD command/response sets as defined in the SD physical layer specifications v.1.0
- Full compliance with SDIO command/response sets as defined in the SDIO card specification v1.0
- Flexible architecture, allowing support for new command structure
- Built-in 64-byte FIFO for buffered read or write
- 16-bit-wide access bus between MMC/SDIO2 interface and the local hosts to maximize bus throughput
- Designed for low power
- Wide interrupt capability
- Programmable clock generation
- Two DMA channels
- OMAP5912 also support control signals to external level shifters. These signals are derived from the direction control of the MMC_DAT0 and MMC_CMD I/O pads (one direction control per data bit line and one direction control for the command line).

NOTE:

- The MMC/SDIO2 clock is multiplexed between the 48-MHz clock (APLL output) and the system clock (19.2 MHz or 12 MHz).
- At reset, the MMC/SDIO2 clock selection is the system clock.
- The MMC/SDIO2 module is routed at the OMAP5912 level. The OMAP5912 configuration selects only the part of the interface which is required.

3.8.8 General-Purpose I/O (GPIO)

OMAP5912 includes 4 GPIO peripherals of 16 GPIO pins each. There are up to 64 shared GPIO pins. Each GPIO pin is independently configurable as either input or output. If configured as input, each pin can be configurable to generate an interrupt upon detection of its signal level change. As both the MPU and the DSP can access the GPIO, consideration must be taken for its arbitration.

The general-purpose input/output (GPIO) peripheral can be used for the following types of applications:

- Input/output data
- Generation of an interrupt in active mode upon the detection of external events
- Generation of a wake-up request in idle mode upon the detection of external events

3.8.9 32-kHz Synchro Counter

This is a 32-bit ordinary counter, clocked by the falling edge of the 32-kHz clock. It is reset while the Power Up Reset (PWRON_RESET) primary I/O is active (main OMAP5912 reset), then on the rising edge of PWRON_RESET (PWRON_RESET release), it starts to count indefinitely. When the highest value is reached, it wraps back to zero and starts running again.

MPU and DSP have the capability to read the count value at higher frequency from the peripheral interface. The MPU can read it from a 32-bit peripheral access, whereas the DSP can only access it through two consecutive 16-bit accesses.

3.8.10 VLYNQ Interface

VLYNQ is a serial (that is, low pin count) communications interface that enables the extension of an internal bus segment to one or more external physical devices. The external devices are mapped into local, physical address space and appear as if they are on the internal bus of the OMAP5912. The external devices must also have a VLYNQ interface. The VLYNQ module serializes bus transactions in one device, transfers the serialized data between devices via a VLYNQ port, and de-serializes the transaction in the external device.

OMAP5912 includes one VLYNQ module connected on OCPT2 target port and OCPI initiator port. These connections are configured via a static switch, which selects either SSI or VLYNQ module. This switch forbids the simultaneous use of GDD/SSI and VLYNQ.

One typical VLYNQ application of OMAP processors is to open a communication channel with TI wireless LAN 802.11.x base band processors like TNET1130 and TNET1230.

NOTE:

The OMAP5912 VLYNQ channel with TNET1130 or TNET1230 is optimized if OMAP5912 generates the serial clock :

- Maximum serial clock frequency if received as external signal is 80 MHz.
- Maximum serial clock frequency if transmitted and internally generated is 100 MHz.

3.9 System DMA Controller

The system direct memory access (DMA) controller transfers data between points in the memory space without intervention by the MPU. The system DMA allows movements of data to and from internal memory, external memory, and peripherals to occur in the background of MPU operation. It is designed to off-load the block data transfer function from the MPU processor. The system DMA is configured by the MPU via the MPU private peripheral bus.

System DMA consists of:

- Seventeen logical channels
- Seven physical ports + one for configuration
- Four physical channels

The ports are connected to the L3 OCP targets, the external memory, the TIPB bridge, the MPUI, and one dedicated port connected to an LCD controller. The system DMA controller can be controlled via the MPU private TIPB or by an external host via the OCP-I port. The system DMA controller is designed for low-power operation. It is partitioned into several clock domains where each clock domain is enabled only when it is used. All clocks are disabled when no DMA transfers are active (synchronous to the MPU TIPB, this feature is totally under hardware control; no specific programming is needed). Five different logical channels types are supported; each one represents a specific feature set:

- LCh-2D for memory-to-memory transfers, 1D and 2D
- LCh-P for peripheral transfers
- LCh-PD for peripheral transfers on a dedicated channel
- LCh-G for graphical transfers/operations
- LCh-D for display transfers

The available features are:

- Support for up to four address modes:
 - Constant
 - Post-increment
 - Single indexing
 - Double indexing
- Different indexing for source-respective destination
- Logical channel chaining
- Software enabling
- Hardware enabling
- Logical channel interleaving
- Logical channel preemption
- Two choices of logical channel arbitration of physical resources: round robin or fixed
- Two levels of logical channel priority
- Constant fill
- Transparent copy
- Rotation 0, 90, 180, and 270

There are seven ports enabling:

- Memory-to-memory transfers
- Peripheral-to-memory transfers
- Memory-to-peripheral transfers
- Peripheral-to-peripheral transfers
- Binary backward-compatible by default configuration
- Up to four logical channels active in parallel

The logical channel dedicated to the display, LCh-D, has several additional features:

- Channel can be shared by two LCD controllers
- Supports both single- and dual-block modes
- Supports separate indexing and numbering for dual-block mode for both elements and frames

3.10 DSP DMA Controller

The DSP subsystem has its own dedicated DMA controller, which is entirely independent of the MPU or the system DMA controller. The DSP DMA controller has many of the same major features as the system DMA controller.

The DSP DMA Controller has six generic channels and five physical ports available for source or destination data. These five ports are the SARAM port, DARAM port, EMIF (external memory port), DSP TIPB port, and MPUI port. The DSP may configure the DSP DMA controller to transfer data between the SARAM, DARAM, EMIF, and TIPB ports; but the MPUI port is a dedicated port used for MPU or system DMA initiated transfers to DSP subsystem resources. The SARAM and DARAM ports are used to access local DSP memories and the TIPB port is used to access the registers of the DSP peripherals. The EMIF port of the DSP DMA controller is used to access the Traffic Controller via the DSP MMU (Memory Management Unit).

3.11 Traffic Controller (Memory Interfaces)

The traffic controller (TC) manages all accesses by the MPU, DSP, system DMA, and local bus to the OMAP5912 system memory resources. The TC provides access to three different memory interfaces: external memory interface slow (EMIFS), external memory interface fast (EMIFF), and internal memory interface (OCP T1). The OCP T1 allows access to the 250K bytes of on-chip frame buffer. The EMIFS provides 16-bit-wide access to asynchronous or synchronous memories or devices, including the following:

- Intel fast boot block flash (23FxxxF3)
- AMD™ simultaneous read/write boot sector flash (AM29DLxxxG)
- AMD burst-mode flash (AM29BLxxxC)
- Intel StrataFlash® memory (28FxxxJ3A)
- Intel synchronous StrataFlash memory (28FxxxK3/K18)
- Intel wireless flash memory (28FxxxW18)
- Samsung™ NAND Flash (K9F56xxQ0M)
- Asynchronous SRAM

The EMIFF provides access to 16-bit-wide access to mobile SDRAM and DDR memories, including the following:

- Mobile SDRAM (Elpida™ EDLxxxCBB, Infineon™ HYExxLxxx, Samsung K4Mxxxxxx)
- Mobile DDR (Elpida EDKxxxCBB, Samsung K4Xxxxxx)

The TC provides the functions of arbitrating contending accesses to the same memory interface from different initiators (MPU, DSP, system DMA, local bus), synchronization of accesses due to the initiators and the memory interfaces running at different clock rates, and the buffering of data allowing burst access for more efficient multiplexing of transfers from multiple initiators to the memory interfaces.

The TC architecture allows simultaneous transfers between initiators and different memory interfaces without penalty. For instance, if the MPU is accessing the EMIFF at the same time the DSP is accessing the IMIF, transfers may occur simultaneously since there is no contention for resources. There are three separate ports to the TC from the system DMA (one for each of the memory interfaces), allowing for greater bandwidth capability between the system DMA and the TC.

AMD is a trademark of Advanced Micro Devices, Inc.
Intel StrataFlash is a registered trademark of Intel Corporation.
Samsung is a trademark of Samsung Corporation.
Elpida is a trademark of Elpida Memory, Inc.
Infineon is a trademark of Infineon Technologies AG Corporation.

3.12 Interprocessor Communication

Several mechanisms allow for communication between the MPU and the DSP on the OMAP5912 device. These include mailbox registers, MPU Interface, and shared memory space.

3.12.1 MPU/DSP Mailbox Registers

The MPU and DSP processors can communicate with each other via a mailbox-interrupt mechanism. This mechanism provides a very flexible software protocol between the processors. There are four sets of mailbox registers located in public TIPB space. The registers are shared between the two processors, so the MPU and DSP may both access these registers within their own public TIPB space, but read/write accessibility of each register is different for each processor.

There are four sets of mailbox registers: two for the MPU to send messages and issue an interrupt to the DSP, the other two for the DSP to send messages and issue an interrupt to the MPU. Each set of mailbox registers consists of two 16-bit registers and a 1-bit flag register. The interrupting processor can use one 16-bit register to pass a data word to the interrupted processor and the other 16-bit register to pass a command word.

Communication is achieved when one processor writes to the appropriate command word register, which causes an interrupt to the other processor and sets the appropriate flag register. The interrupted processor acknowledges by reading the command word, which causes the flag register to be cleared. An additional data-word register is also available in each mailbox register set to optionally communicate two words of data between the processors for each interrupt instead of just communicating the command word.

The information communicated by the command and data words are entirely user-defined. The data word can be optionally used to indicate an address pointer or status word.

3.12.2 MPU Interface (MPUI)

The MPU interface (MPUI) allows the MPU and the system DMA controller to communicate with the DSP and its peripherals. The MPUI allows access to the full memory space (16M bytes) of the DSP and the DSP public peripheral bus. Thus, the MPU and system DMA controller both have read and write access to the complete DSP I/O space (128K bytes), including the control registers of the DSP public peripherals.

The MPUI port supports the following features:

- Four access modes:
 - Single-access mode (SAM) for MPU access of DSP SARAM, DARAM, and external memory interface
 - Single-access mode (SAM) for peripheral bus access
 - Host-only mode (HOM) for SARAM access
 - Host-only mode (HOM) for peripheral bus access
- Interrupt to MPU if access time-out occurs
- Programmable priority scheme (MPU versus DMA)
- Packing and unpacking of data (16 bits to 32 bits, and vice versa)
- 32-bit single-access support
- Software control endianism conversion
- System DMA capability to full memory space (16M bytes)
- System DMA capability to the DSP public TIPB peripherals (up to 128K bytes space)

This port can be used for many functions, such as: MPU loading of program code into DSP program memory space, sharing of data between MPU and DSP, implementing interprocessing communication protocols via shared memory, or allowing MPU to use and control DSP public TIPB peripherals.

3.12.3 MPU/DSP Shared Memory

The OMAP5912 implements a shared memory architecture via the traffic controller. Therefore, the MPU and DSP both have access to the same shared SRAM memory (frame buffer of 250K bytes) as well as to the EMIFF and EMIFS memory space. Through the DSP memory management unit (MMU), the MPU controls which regions of shared memory space the DSP is allowed to access. By setting up regions of shared memory, and defining a protocol for the MPU and DSP to access this shared memory, an interprocessor communication mechanism may be implemented. This method can be used in conjunction with the mailbox registers to create handshaking interrupts that properly synchronize the MPU and DSP accesses to shared memory. Utilizing the shared memory in this fashion may be useful when the desired data to be passed between the MPU and DSP is larger than the two 16-bit words provided by each set of mailbox command and data registers.

For example, the MPU may need to provide the DSP with a list of pointers to perform a specific task as opposed to a single command and single pointer. Using shared memory and the mailboxes, the DSP can read the list of pointers from shared memory after receiving the interrupt caused by an MPU write to the mailbox command register.

3.13 DSP Hardware Accelerators

The TMS320C55x DSP core within the OMAP5912 device utilizes three powerful hardware accelerator modules which assist the DSP core in implementing specific algorithms that are commonly used in video compression applications such as MPEG4 encoders/decoders. These accelerators allow implementation of such algorithms using fewer DSP instruction cycles and dissipating less power than implementations using only the DSP core. The hardware accelerators are utilized via functions from the TMS320C55x Image/Video Processing Library available from Texas Instruments.

Utilizing the hardware accelerators, the Texas Instruments Image/Video Processing Library implements many useful functions, which include the following:

- Forward and Inverse Discrete Cosine Transform (DCT) (used for video compression/decompression)
- Motion Estimation (used for compression standards such as MPEG video encoding and H.26x encoding)
- Pixel Interpolation (enabling high-performance fractal-pixel motion estimation)
- Quantization/Dequantization (useful for JPEG, MPEG, H.26x Encoding/Decoding)
- Flexible 1D/2D Wavelet Processing (useful for JPEG2000, MPEG4, and other compression standards)
- Boundary and Perimeter Computation (useful for Machine Vision applications)
- Image Threshold and Histogram Computations (useful for various Image Analysis applications)

3.13.1 DCT/iDCT Accelerator

The DCT/iDCT hardware accelerator is used to implement Forward and Inverse DCT (Discrete Cosine Transform) algorithms. These DCT/iDCT algorithms can be used to implement a wide range of video compression standards including JPEG Encode/Decode, MPEG Video Encode/Decode, and H.26x Encode/Decode.

3.13.2 Motion Estimation Accelerator

The Motion Estimation hardware accelerator implements a high-performance motion estimation algorithm, enabling MPEG Video encoder or H.26x encoder applications. Motion estimation is typically one of the most computation-intensive operations in video-encoding systems.

3.13.3 Pixel Interpolation Accelerator

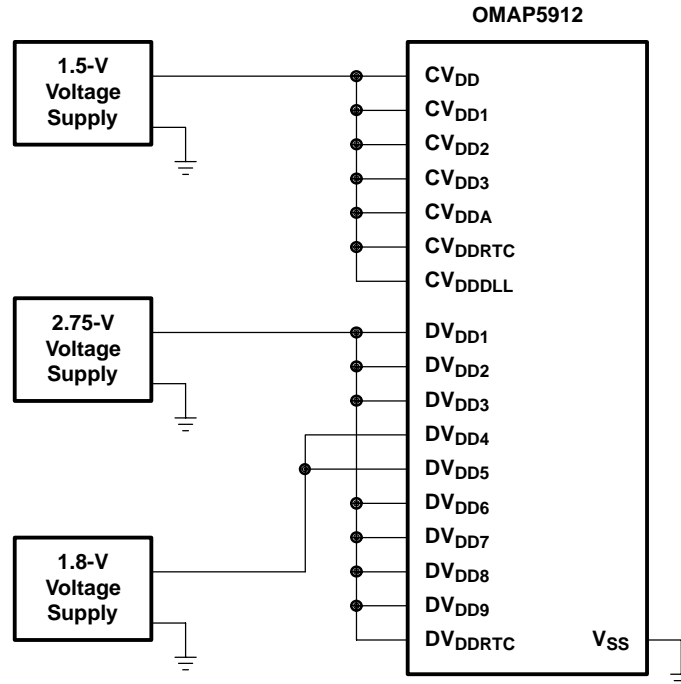
The Pixel Interpolation Accelerator enables high-performance pixel-interpolation algorithms, which allows for powerful fractal pixel motion estimation when used in conjunction with the Motion Estimation Accelerator. Such algorithms provide significant improvement to video-encoding applications.

3.14 Power Supply Connection Examples

3.14.1 Core and I/O Voltage Supply Connections

The OMAP5912 device is extremely flexible regarding the implementation of the core and I/O voltage supplies of the device.

In a typical system, all of the core voltage supplies (CV_{DDx}) may be connected together and powered from one common supply. Likewise, all of the I/O voltage supplies (DV_{DDx}) may be connected together and powered from a common supply. Figure 3–4 illustrates this common system configuration.



NOTE: In this example, SDRAM (DV_{DD4}) and FLASH (DV_{DD5}) I/O voltage supplies are connected to 1.8 V and the other I/O voltage supplies are connected to 2.75 V. But all the I/O voltage supplies (DV_{DDx}) are dual-voltage capable and all power combinations are possible.

Figure 3–4. Supply Connections for a Typical System

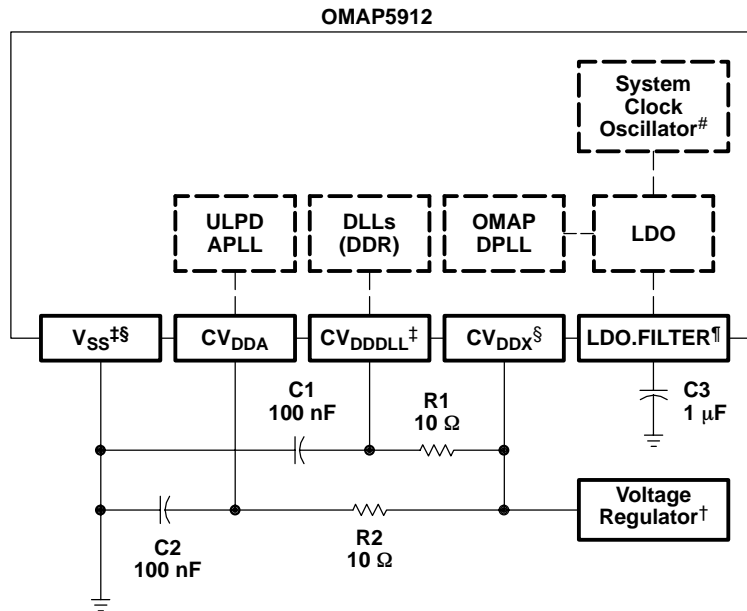
In the previous example, all CV_{DDx} pins are connected in common. However, the OMAP5912 has dedicated CV_{DD} pins that supply power to different sections of the chip. This feature can be useful in prototyping phases to troubleshoot power management features and perform advanced power analysis. By isolating each CV_{DDx} bus from the power source through isolation jumpers or current sense resistors, the current draw into different domains may be measured separately. This type of supply isolation must only be done during prototyping as production system designs should connect all the CV_{DDx} pins together, preferably to a common board plane.

NOTE:

There is no specific power sequencing for the different voltage supplies as long as all CV_{DDx} and DV_{DDx} voltages are ramped to valid operating levels within 500 ms of one another. Additionally, if certain I/O pins are unused in a specific system application, the DV_{DDx} supply pins that power these I/O must still be connected to valid operating voltage levels.

3.14.2 Core Voltage Noise Isolation

Two CV_{DD} pins on OMAP5912, CV_{DDA} and CV_{DDDLL} , are dedicated to supply power for the ULPD APLL and for the DLL elements of the DDR interface, respectively. In addition to using sound board design principles, these dedicated pins allow for added supply noise isolation circuitry to enable maximum performance. An example circuit is shown in Figure 3–5.



- NOTES: A. This circuit is provided only as an example. Specific board layout implementation must minimize noise on the OMAP5912 voltage supply pins.
- B. Unless otherwise noted in this document, all V_{SS} pins on the OMAP5912 are common and must be connected directly to a common ground; however, the discrete capacitor in the RC filter circuit should be placed as close as possible to the V_{SS} pins [ZZG balls AA21 (or W20) and A13; ZDY balls L7 (or L11) and F6].
- C. For special consideration with respect to the connection of V_{SS} pin (ZZG ball Y13; ZDY ball H8), refer to Section 5.6.1, 32-kHz Oscillator and Input Clock.

[†] The voltage regulator must be selected to provide a voltage source with minimal low frequency noise.

[‡] If a dedicated voltage regulator is not available for CV_{DDDLL} in the system, a simple low-pass RC filter can be used to isolate the cells from the switching noise of other digital circuits.

[§] Common CV_{DD} for rest of chip.

[¶] A regulated supply is delivered to DPPLL macro(s) and available on unique bond pad. A decoupling capacitor of 1 μF must be connected externally between the pin called LDO. FILTER (ZZG ball J1; ZDY ball H1) and the ground.

[#] System clock oscillator frequency = 12, 13, or 19.2 MHz.

Figure 3–5. External RC Circuits for Noise Isolation

4 Documentation Support

Extensive documentation supports all OMAP platform of devices from product announcement through applications development. The following types of documentation are available to support the design and use of the OMAP platform of applications processor devices:

- Device-specific data sheets
- Development-support tools
- Hardware and software application reports

A series of DSP textbooks is published by Prentice-Hall and John Wiley & Sons to support digital signal processing research and education. The TMS320 DSP newsletter, *Details on Signal Processing*, is published quarterly and distributed to update TMS320 DSP customers on product information.

Information regarding Texas Instruments (TI) OMAP and DSP products is also available on the Worldwide Web at <http://www.ti.com> uniform resource locator (URL).

4.1 Device and Development-Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all TMS320™ DSP devices and support tools. Each TMS320™ DSP commercial family member has one of three prefixes: TMX, TMP, or TMS. Texas Instruments recommends two of three possible prefix designators for support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

Device development evolutionary flow:

- TMX** Experimental device that is not necessarily representative of the final device's electrical specifications
- TMP** Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification
- TMS** Fully qualified production device

Support tool development evolutionary flow:

- TMDX** Development-support product that has not yet completed Texas Instruments internal qualification testing.
- TMDS** Fully qualified development-support product

TMX and TMP devices and TMDX development-support tools are shipped with appropriate disclaimers describing their limitations and intended uses. Experimental devices (TMX) may not be representative of a final product and Texas Instruments reserves the right to change or discontinue these products without notice.

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

5 Electrical Specifications

This section provides the absolute maximum ratings and the recommended operating conditions for the OMAP5912 device.

All electrical and switching characteristics in this data manual are valid over the recommended operating conditions unless otherwise specified.

5.1 Absolute Maximum Ratings

The list of absolute maximum ratings are specified over operating ambient temperature. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Section 5.2, Recommended Operating Conditions, is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All supply voltage values (core and I/O) are with respect V_{SS} .

This section provides the absolute maximum ratings for the OMAP5912 device.

Supply voltage range (core), CV_{DD} , $CV_{DD1/2/3/A}$, CV_{DDRTC} , CV_{DDLL}	-0.5 V to 1.8 V
Supply voltage range (I/O), $DV_{DD1/2/3/4/5/6/7/8/9/RTC}$	-0.5 V to $DV_{DD} + 0.5$ V
Input voltage range, V_I (12,13, or 19.2-MHz and 32-kHz oscillator)	-0.5 V to $DV_{DD} + 0.5$ V
Input voltage range, V_I (Standard LVCMOS)	-0.5 V to $DV_{DD} + 0.5$ V
Input voltage range, V_I (USB Transceivers)	-0.5 V to $DV_{DD} + 0.5$ V
Input voltage range, V_I (I ² C)	-0.5 V to 4.5 V
Output voltage range, V_O (Standard LVCMOS)	-0.5 V to $DV_{DD} + 0.5$ V
Output voltage range, V_O (USB Transceivers)	-0.5 V to $DV_{DD} + 0.5$ V
Output voltage range, V_O (I ² C)	-0.5 V to 4.5 V
Operating ambient temperature range, T_A	-40°C to 85°C
Storage temperature range, T_{stg}	-65°C to 150°C

5.2 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT	
CV _{DD1/2/3/RTC}	OMAP5912 supply voltage, core††	Low-power standby mode§	1.05	1.1	1.21	V
		Active mode	1.52	1.6	1.65	
CV _{DDA}	Supply voltage for analog PLL	1.35	1.6	1.65	V	
CV _{DDDLL}	Core supply voltage for the DDR interface digitally controlled delay element (DCDL)¶	1.43	1.6	1.65	V	
DV _{DD1/2/3/4/5/6/7/8/9/RTC}	Device supply voltage, I/O‡	Low-voltage range#	1.65	1.8	1.95	V
		High-voltage range#	2.5	2.75 or 3.3	3.6	
DV _{DD2}	Device supply voltage, I/O	Internal USB transceiver not used	1.65	1.8	1.95	V
		Internal USB transceiver used	3	3.3	3.6	
CV _{DD} – DV _{DD}	Device supply voltage difference			TBD	V	
DV _{DD} – CV _{DD}	Device supply voltage difference			TBD	V	
LDO.FILTER*	Internal DPLL and 12, 13, or 19.2-MHz oscillator supply voltage□	Low-power standby mode§	1.05	1.1	1.21	V
		Active mode	1.43	1.5	1.65	
V _{SS}	Device supply voltage, GND		0		V	
V _{IH}	High-level input voltage, I/O	Standard LVCMOS	0.7 DV _{DD}		V	
		ZZG balls P9 and R8 (ZDY balls T2 and U1) are not used for USB differential voltage	2			
		ZZG balls W13, W14, Y12, and Y14 (ZDY balls N9, P11, P10, and T12) are not used for CCP differential voltage	0.7 DV _{DD}			
V _{IL}	Low-level input voltage, I/O	Standard LVCMOS	0.3 DV _{DD}		V	
		ZZG balls P9 and R8 (ZDY balls T2 and U1) are not used for USB differential voltage	0.8			
		ZZG balls W13, W14, Y12, and Y14 (ZDY balls N9, P11, P10, and T12) are not used for CCP differential voltage	0.3 DV _{DD}			

† All core voltage supplies must be tied to the same voltage level (within 50 mV).

‡ In Split-power mode (CV_{DDx} and DV_{DDx} = 0), RTC has to be supplied with CV_{DDRTC} = 1.05 V min and DV_{DDRTC} = 1.65 V min.

§ Low-power standby is defined as follows: the device is in deep-sleep mode and LOW_PWR = 1. The device runs from 32-kHz clock in this mode.

¶ To filter switching noises, it is recommended that an RC (R = 10 Ω, C = 100 nF) low-pass filter be implemented externally.

Corresponding DV_{DD} mode bit must be configured in the Voltage_control_0 register.

|| In systems where the CV_{DDx} and DV_{DDx} power supplies are ramped at generally the same time (within 500 ms of one another), there are no specific power sequencing requirements for the supplies. The only sequencing requirement is that the maximum voltage difference between CV_{DD} and DV_{DD} is not exceeded for greater than 500 ms. Likewise, if different voltages are used for the separate DV_{DDx} supplies, all DV_{DDx} supplies should be ramped up to valid voltage levels within 500 ms of one another.

* An external capacitor (C = 1 μF ± 10%) must be connected between LDO.FILTER and V_{SS} to provide decoupling capacitance for the regulator.

□ LDO has to be powered down by setting LDO_PWRDN_CNTL[0] in OMAP5912 configuration.

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5.2 Recommended Operating Conditions (Continued)

		MIN	NOM	MAX	UNIT
V _I	Input voltage	ZZG balls P9 and R8 (ZDY balls T2 and U1) are used for USB	0.8	2.5	V
		OSC1 and OSC32K pins		C _{VDD}	
V _{ID}	Differential input voltage	ZZG balls P9 and R8 (ZDY balls T2 and U1) are used for USB	±200		mV
		ZZG balls W13, W14, Y12, and Y14 (ZDY balls N9, P11, P10, and T12) are used for CCP	±25		
I _{OH}	High-level output current	Low-voltage range DV _{DDmin} = 1.65 V	2-mA drive strength buffers	-2	mA
			3-mA drive strength buffers	-3	
			4-mA drive strength buffers	-4	
		High-voltage range DV _{DDmin} = 2.5 V	6-mA drive strength buffers	-6	
			8-mA drive strength buffers	-8	
			11-mA drive strength buffers	-11	
		18.3-mA drive strength buffers		-18.3	
I _{OL}	Low-level output current	Low-voltage range DV _{DDmin} = 1.65 V	2-mA drive strength buffers	2	mA
			3-mA drive strength buffers	3	
			4-mA drive strength buffers	4	
		High-voltage range DV _{DDmin} = 2.5 V	6-mA drive strength buffers	6	
			8-mA drive strength buffers	8	
			11-mA drive strength buffers	11	
		18.3-mA drive strength buffers		18.3	
T _A	Operating ambient temperature	-40		85	°C

† All core voltage supplies must be tied to the same voltage level (within 50 mV).

‡ In Split-power mode (C_{VDDx} and DV_{DDx} = 0), RTC has to be supplied with C_{VDDRTC} = 1.05 V min and DV_{DDRTC} = 1.65 V min.

§ Low-power standby is defined as follows: the device is in deep-sleep mode and LOW_PWR = 1. The device runs from 32-kHz clock in this mode.

¶ To filter switching noises, it is recommended that an RC (R = 10 Ω, C = 100 nF) low-pass filter be implemented externally.

Corresponding DV_{DD} mode bit must be configured in the Voltage_control_0 register.

|| In systems where the C_{VDDx} and DV_{DDx} power supplies are ramped at generally the same time (within 500 ms of one another), there are no specific power sequencing requirements for the supplies. The only sequencing requirement is that the maximum voltage difference between C_{VDD} and DV_{DD} is not exceeded for greater than 500 ms. Likewise, if different voltages are used for the separate DV_{DDx} supplies, all DV_{DDx} supplies should be ramped up to valid voltage levels within 500 ms of one another.

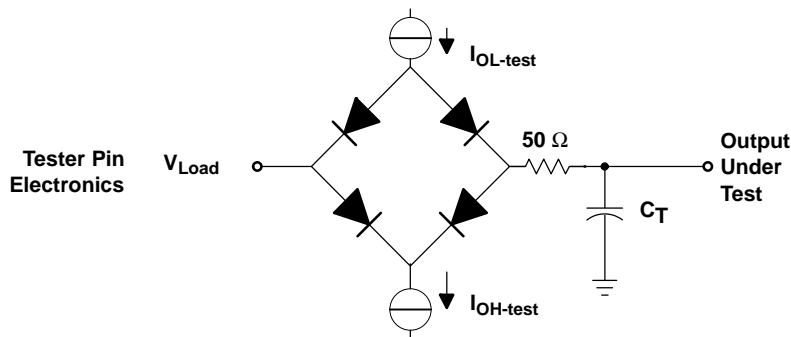
★ An external capacitor (C = 1 μF ± 10%) must be connected between LDO.FILTER and V_{SS} to provide decoupling capacitance for the regulator.

□ LDO has to be powered down by setting LDO_PWRDN_CNTL[0] in OMAP5912 configuration.

5.3 Electrical Characteristics Over Recommended Operating Ambient Temperature Range (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT		
V _{OH}	High-level output voltage	Standard LVCMOS	I _O = rated, DV _{DD} = 3.3 V, dual-supply outputs	0.8 DV _{DD}			V		
		ZZG balls P9 and R8 (ZDY balls T2 and U1) are not used for USB differential voltage	I _O = -18.3 mA	DV _{DD} - 0.5					
V _{OL}	Low-level output voltage	Standard LVCMOS	I _O = rated, DV _{DD} = 3.3 V, dual-supply outputs	0.22 DV _{DD}			V		
		ZZG balls P9 and R8 (ZDY balls T2 and U1) are not used for USB differential voltage	I _O = 18.3 mA	0.28					
		I ² C	Fast mode at 6-mA load	0	0.6				
			Fast mode at 3-mA load	0	0.4				
Standard mode at 3-mA load	0	0.4							
I _I	Input current	Inputs without internal pullups/pulldowns enabled	V _I = V _I MAX to V _I MIN	Low-voltage range	-1		1	μA	
				High-voltage range	-1		1		
		Input pins with 20-μA pulldowns enabled	DV _{DD} = MAX, V _I = V _{SS} to V _{DD}	Low-voltage range	5	10	20		
				High-voltage range	15	30	60		
		Input pins with 100-μA pulldowns enabled	DV _{DD} = MAX, V _I = V _{SS} to V _{DD}	Low-voltage range	55	100	170		
				High-voltage range	35	67	110		
	Input pins with 20-μA pullups enabled	CV _{DD} = MAX, V _I = V _{SS} to V _{DD}	Low-voltage range	-20	-10	-5			
			High-voltage range	-60	-30	-15			
	Input pins with 100-μA pullups enabled	CV _{DD} = MAX, V _I = V _{SS} to V _{DD}	Low-voltage range	-170	-100	-55			
			High-voltage range	-110	-67	-35			
	I _{OZ}	Input current for outputs in high-impedance			-20		20		μA
	C _i	Input capacitance	ZZG balls P9 and R8 (ZDY balls T2 and U1) (USB)		7				pF
All other I/O pins			4						
C _o	Output capacitance	ZZG balls P9 and R8 (ZDY balls T2 and U1) (USB)		7			pF		
		All other I/O pins		4					

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Where: $I_{OL-test} = 5 \text{ mA}$ (all outputs)
 $I_{OH-test} = 300 \mu\text{A}$ (all outputs)
 $V_{Load} = [(V_{OH} - V_{OL})/2] + V_{OL}$
 $C_T = 10 \text{ pF}$ maximum and 5 pF minimum for EMIFF (50 pF maximum and 5 pF minimum for EMIFS and all other I/O pads).

Figure 5–1. 3.3-V Test Load Circuit

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5.4 Package Thermal Resistance Characteristics

Table 5–1 provides the thermal resistance characteristics for the recommended package types used on the OMAP5912 device.

Table 5–1. Thermal Resistance Characteristics

$R_{\theta JA}$ (°C/W)	$R_{\theta JC}$ (°C/W)	Board Type
TBD	TBD	High-K
TBD	TBD	Low-K

Board Types are as defined by JEDEC. Reference JEDEC Standard JESD51-9, Test Boards For Area Array Surface Mount Package Thermal Measurements.

5.5 Timing Parameter Symbolology

Timing parameter symbols used in the timing requirements and switching characteristics tables are created in accordance with JEDEC Standard 100. To shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

Lowercase subscripts and their meanings:

- a access time
- c cycle time (period)
- d delay time
- dis disable time
- en enable time
- f fall time
- h hold time
- r rise time
- su setup time
- t transition time
- v valid time
- w pulse duration (width)
- X Unknown, changing, or don't care level

Letters and symbols and their meanings:

- H High
- L Low
- V Valid
- Z High impedance

5.6 Clock Specifications

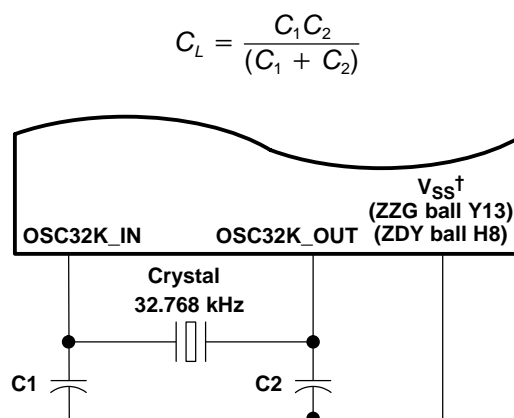
This section provides the timing requirements and switching characteristics for the OMAP5912 system clock signals.

5.6.1 32-kHz Oscillator and Input Clock

The 32.768-kHz clock signal (often abbreviated to 32-kHz) may be supplied by either the on-chip 32-kHz oscillator (requiring an external crystal) or an external CMOS signal.

The on-chip oscillator requires an external 32.768-kHz crystal connected across the OSC32K_IN and OSC32K_OUT pins. The connection of the required circuit, consisting of the crystal and two load capacitors, is shown in Figure 5–2. The load capacitors, C_1 and C_2 , should be chosen such that the equation below is satisfied (recommended values are $C_1 = C_2 = 10$ pF). C_L in the equation is the load specified for the crystal. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator pins (OSC32K_IN and OSC32K_OUT) and to the V_{SS} pin closest to the oscillator pins (ZZG ball Y13; ZDY ball H8).

NOTE 1: Do not connect V_{SS} (ZZG ball Y13; ZDY ball H8) to the common board ground but only to the oscillator circuit as shown.

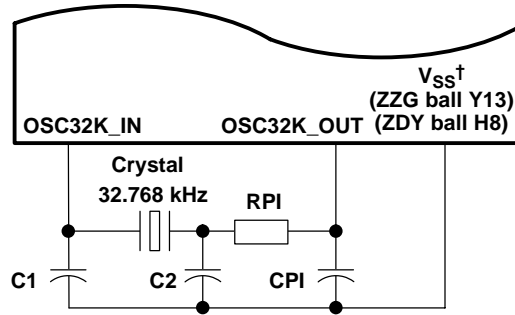


† Do not connect V_{SS} (ZZG ball Y13; ZDY ball H8) to the common board ground but only to the oscillator circuit as shown.

Figure 5–2. 32-kHz Oscillator External Crystal

NOTE 2: Recommended maximum series resistance specification of the crystal is 100 k Ω or less at 32 kHz. Series resistance at any other parasitic resonance of the crystal should be greater than 100 k Ω . For crystals whose parasitic resonance has maximum series resistor less than 100 k Ω , a PI-network (Figure 5–3) is needed between the OSC32K_OUT pin and the crystal to suppress oscillation at frequencies other than 32 kHz. The PI-network creates a pole to reduce the negative resistance at frequencies greater than 32 kHz.

The recommended PI-network for use with these crystals is $C_{PI} = 10$ pF total and $R_{PI} = 390$ k $\Omega \pm 5\%$



† Do not connect V_{SS} (ZYG ball Y13; ZDY ball H8) to the common board ground but only to the oscillator circuit as shown.

Figure 5–3. 32-kHz Oscillator External Crystal With PI-Network

NOTE 3: When the internal oscillator is used to generate the 32-kHz clock, the CLK32K_IN pin must be tied to V_{SS} . Otherwise, the 32-kHz clock is corrupted and the device fails. If the external CMOS clock is used to provide the 32-kHz clock, the OSC32K_IN (XI) pin must be tied to CV_{DD} . The OSC32K_OUT (XO) pin must be tied to V_{SS} .

Table 5–2 shows the switching characteristics of the 32-kHz oscillator and Table 5–3 shows the input requirements of the 32-kHz clock input.

Table 5–2. 32-kHz Oscillator Switching Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start-up time (from power up until oscillating at stable frequency of 32.768 kHz)	$C1 = C2 = 10 \text{ pF}$, $CV_{DD} = 1.35 \text{ V}$		200	800	ms
I_{DDA} , active current consumption			4		μA
Oscillation frequency			32.768		kHz

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Table 5–3. 32-kHz Input Clock Timing Requirements

NO.		MIN	NOM	MAX	UNIT
CK1	t_{cyc} Frequency		32.768		kHz
CK2	t_f Fall time			25	ns
CK3	t_r Rise time			25	ns
CK4	Duty cycle (high-to-low ratio)	30		70	%
CK5	Frequency stability	-70		70	ppm

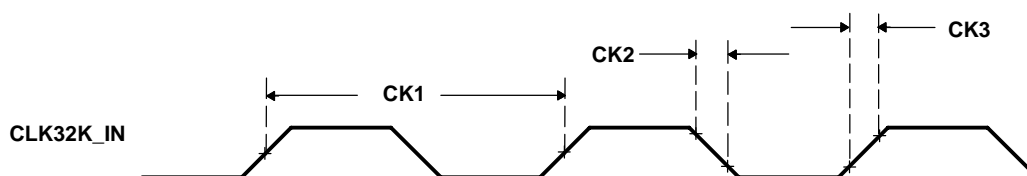


Figure 5–4. 32-kHz Input Clock

5.6.2 Base Oscillator (12, 13, or 19.2 MHz) and Input Clock

The internal base system oscillator is enabled following a device reset. The oscillator requires an external crystal to be connected across the OSC1_IN and OSC1_OUT pins. If the internal oscillator is not used (configured in software), an external clock source (12,13, 19.2 MHz) must be applied to the OSC1_IN pin, and the OSC1_OUT pin must be left unconnected. Because the internal oscillator can be used as a clock source to the OMAP DPLL, the 12-,13-, or 19.2-MHz crystal oscillation frequency can be multiplied to generate the DSP clock, MPU clock, traffic controller clock.

The crystal must be in fundamental-mode operation, and parallel resonant, with a maximum effective series resistance of 30 Ω maximum. The connection of the required circuit, consisting of the crystal and two load capacitors, is shown in Figure 5–5. The load capacitors, C_1 and C_2 , must be chosen such that the equation below is satisfied (recommended values are $C_1 = C_2 = 2C_L$). C_L in the equation is the load specified for the crystal. All discrete components used to implement the oscillator circuit must be placed as close as possible to the associated oscillator pins (OSC1_IN and OSC1_OUT) and to the V_{SS} pins closest to the oscillator pins (ZYG balls AA1 and Y3; ZDY balls G11 and N5).

NOTE: The base oscillator is powered by the embedded LDO. If an external clock source is used instead of using the on-chip oscillator, care must be taken that the voltage level driven onto the OSC1_IN pin is no greater than the LDO voltage level.

$$C_1 = C_2 = 2C_L \quad (C_L = \text{Crystal Load Capacitance})$$

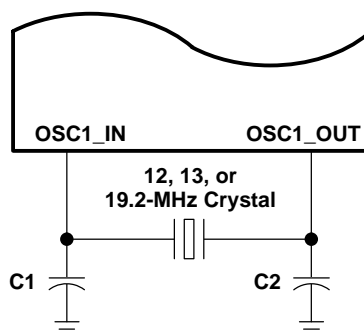


Figure 5–5. Internal System Oscillator External Crystal

If USB host function is used, it is recommended that a very low PPM crystal (≤ 50 ppm) be used for the 12,13, or 19.2 MHz oscillator circuit. If the USB host function is not used, then a crystal of ≤ 180 ppm is recommended. When selecting a crystal, the system design must take into account the temperature and aging characteristics of a crystal versus the user environment and expected lifetime of the system.

Table 5–4 shows the switching characteristics of the base oscillator.

Table 5–4. Base Oscillator Switching Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start-up time (from power up until oscillating at stable frequency of 12,13, or 19.2 MHz)	C1 = C2 = 10 pF, CV _{DD} = 1.3V		1.7	3	ms
I _{DDA} , active current consumption	C1 = C2 = 10 pF, CV _{DD} = 1.5V		220		μA
Oscillation frequency			12 to 19.2		MHz

5.7 Reset Timings

This section provides the timing requirements for the OMAP5912 hardware reset signals.

5.7.1 OMAP5912 Device Reset

The $\overline{\text{PWRON_RESET}}$ signal is the active-low asynchronous reset input responsible for the reset of the entire OMAP5912 device. When using an external crystal to supply the 32-kHz system clock, $\overline{\text{PWRON_RESET}}$ must be asserted low a minimum of two 32-kHz clock cycles longer than the worst-case start-up time of the 32-kHz oscillator after stable power supplies (see Figure 5–6). If an external CMOS input signal is used to source 32 kHz, $\overline{\text{PWRON_RESET}}$ must be asserted low a minimum of two 32-kHz clock cycles after stable power supplies. See Table 5–5 and Table 5–6.

Table 5–5. OMAP5912 Device Reset Timing Requirements

NO.		MIN	MAX	UNIT
RS1	$t_{w(\text{PWRON_RST})}$ Pulse duration, $\overline{\text{PWRON_RESET}}$ low	800		ms

Table 5–6. OMAP5912 Device Reset Switching Characteristics†

NO.	PARAMETER	MIN	MAX	UNIT
RS2	$t_{d(\text{PWRONH-RSTH})}$ Delay time, $\overline{\text{PWRON_RESET}}$ high to $\overline{\text{RST_OUT}}$ high		$T + 10^\dagger$	μs

† $T = P*(C + 7)$, P = period of 32-kHz clock, C = Value of ULPD wakeup time setup register, SETUP_ULPD1_REG (Default 03FFh)

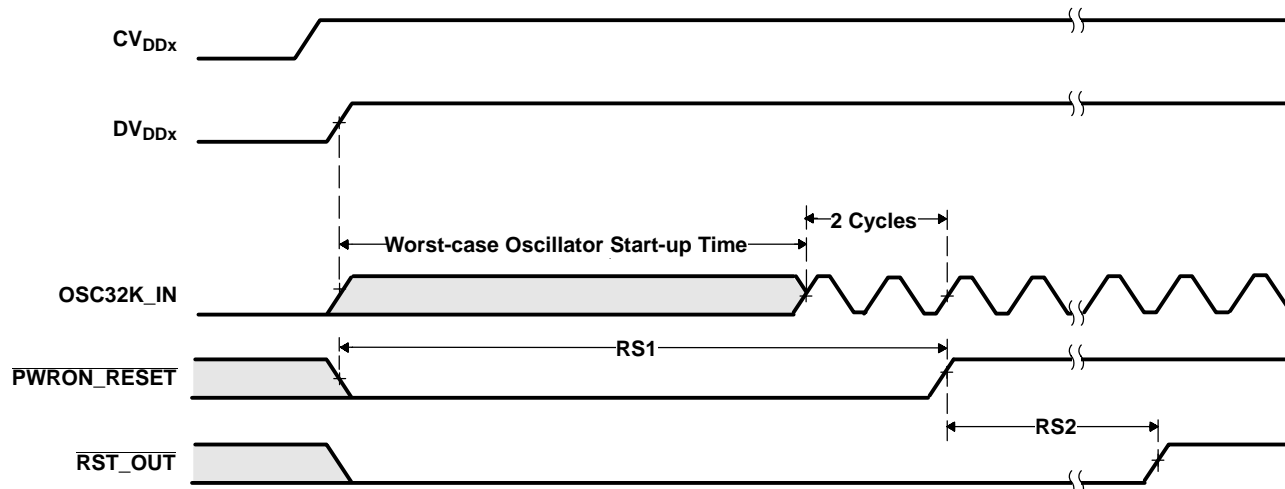


Figure 5–6. Device Reset Timings

5.7.2 OMAP5912 MPU Core Reset

The MPU_RST signal is the active-low asynchronous input responsible for the reset of the OMAP5912 MPU core. Stable power supplies are assumed prior to MPU_RST assertion. Figure 5–7 illustrates the behavior of MPU_RST and RST_OUT. In Figure 5–7, a logic-high level is assumed on the PWRON_RESET input. In the case where an application ties the PWRON_RESET and MPU_RST together, the behavior described in Section 5.7.1, OMAP5912 Device Reset, will override. See Table 5–7 and Table 5–8.

Table 5–7. MPU_RST Timing Requirements

NO.		MIN	MAX	UNIT
M3	$t_w(\overline{\text{MPU_RST}})$ Pulse duration, $\overline{\text{MPU_RST}}$ low	50		μs

Table 5–8. MPU_RST Switching Characteristics†

NO.	PARAMETER	MIN	MAX	UNIT
M1	$t_d(\overline{\text{MPUL-RSTL}})$ Delay time, $\overline{\text{MPU_RST}}$ low to $\overline{\text{RST_OUT}}$ low		1	μs
M2	$t_d(\overline{\text{MPUH-RSTH}})$ Delay time, $\overline{\text{MPU_RST}}$ high to $\overline{\text{RST_OUT}}$ high	MPU_RST asserted during OMAP5912 awake state	10	μs
		MPU_RST asserted during OMAP5912 deep-sleep state	$T + 10^\dagger$	

† $T = P \cdot (C + 7)$, P = period of 32-kHz clock, C = Value of ULPD wakeup time setup register, SETUP_ULPD1_REG (Default 03FFh)

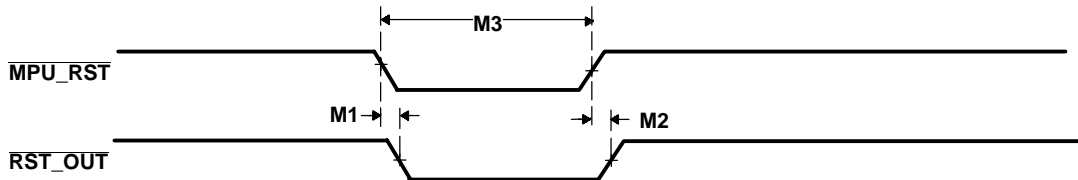


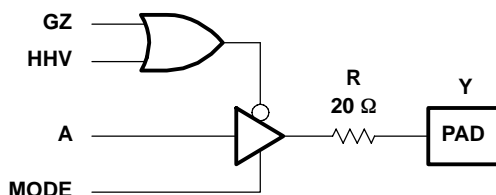
Figure 5–7. MPU Core Reset Timings

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5.8 External Memory Interface Timing

Some EMIFF and EMIFS output terminals have the following particularity:

A serial resistor of 20 Ω is included at the output of the terminal to match with PCB line impedance and ensure proper signal integrity. See Table 2–3 (ZDY Package Terminal Characteristics) and Table 2–4 (ZZG Package Terminal Characteristics) for the list of terminals, which are concerned.



5.8.1 EMIFS/Flash Interface Timing

Table 5–9 and Table 5–10 assume testing over recommended operating conditions (see Figure 5–8 through Figure 5–12).

Table 5–9. EMIFS/Flash Interface Timing Requirements

NO.			DV _{DD5} = 1.8 V Nominal		DV _{DD5} = 2.75 V Nominal		DV _{DD5} = 3.3 V Nominal		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
F6	$t_{su}(RDV-CLKH)$	Setup time, read data valid before FLASH.CLK high	Async modes (RT = 0) [†]		2	2	2	2	ns
			Sync Modes (RT = 1) [†]		2	2	2	2	ns
F7	$t_h(CLKH-RDV)$	Hold time, read data valid after FLASH.CLK high	Async modes (RT = 0) [†]		4	4	4	4	ns
			Sync Modes (RT = 1) [†]		3	3	3	3	ns
F10	$t_{su}(RDY-CLKH)$	Setup time, FLASH.RDY valid before FLASH.CLK high	Async modes (RT = 0) [†]		7	7	7	7	ns
			Sync modes (RT = 1) [†]		2	2	2	2	ns
F11	$t_h(CLKH-RDY)$	Hold time, FLASH.RDY valid after FLASH.CLK high	Async modes (RT = 0) [†]		0,5	0,5	0,5	0,5	ns
			Sync modes (RT = 1) [†]		3	3	3	3	ns

[†] When the RT field in the EMIFS configuration register is set, input data is retimed to the external FLASH.CLK signal. RT=1 setting is only valid in synchronous modes (protocols 1 and 2). For asynchronous modes, $t_{d}(CLKH-CSV)$ with respect to internal FLASH.CLK is given as 0 to allow for other signals reference to $\overline{FLASH.CSx}$. The external FLASH.CLK is disabled for async modes

The EMIFS/Flash Clock is limited by the maximum traffic controller clock rate for OMAP5912, provided that all EMIFS/Flash timing constraints are met.

Timing values are given for the CONF_VOLTAGE_FLASH_R bit of the VOLTAGE_CTRL_0 register programmed as follows: 0 for 1.8 V, 1 for 2.75/3.3 V.

Table 5–10. EMIFS/NOR Flash Interface Switching Characteristics†

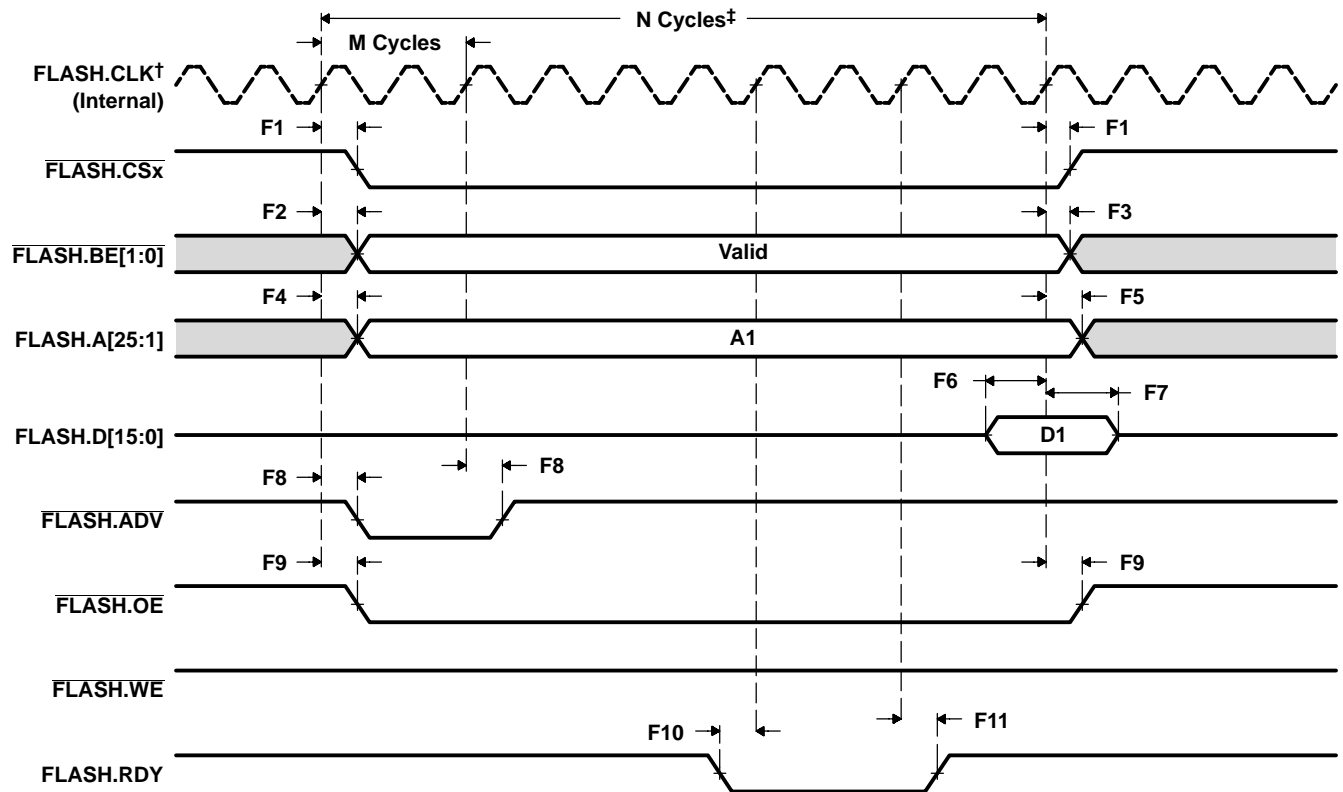
NO.	PARAMETER		DV _{DD5} = 1.8 V Nominal‡		DV _{DD5} = 2.75 V Nominal‡		DV _{DD5} = 3.3 V Nominal‡		UNIT			
			MIN	MAX	MIN	MAX	MIN	MAX				
F1	t _d (CLKH-CSV)	Delay time, FLASH.CLK high to FLASH.CSx transition	async modes	2	19	2.5	17	2.5	16	ns		
			sync modes	0	9.5	0	8.5	0	8.5			
F2	t _d (CLKH-BEV)	Delay time, FLASH.CLK high to FLASH.BEX valid	async modes		14.5		12.5		11.5	ns		
			sync modes		5		4.5		4			
F3	t _d (CLKH-BEIV)	Delay time, FLASH.CLK high to FLASH.BEX invalid	async modes	3.5		3.5		3.5		ns		
			sync modes	1.5		1.5		1.5				
F4	t _d (CLKH-AV)	Delay time, FLASH.CLK high to address valid	async modes		18.5		16.5		15.5	ns		
			sync modes		9		8.5		8			
F5	t _d (CLKH-AIV)	Delay time, FLASH.CLK high to address invalid	async modes	2		2.5		2.5		ns		
			sync modes	0		0		0				
F8	t _d (CLKH-ADV)	Delay time, FLASH.CLK high to FLASH.ADV transition	async modes	2	11.5	2.5	9.5	2.5	8.5	ns		
			sync modes	0	2	0.5	1	0	1			
F9	t _d (CLKH-OEV)	Delay time, FLASH.CLK high to FLASH.OE transition	async modes	3	14	3	12	3	11	ns		
			sync modes	1	4.5	1	4	1	3.5			
F12	t _d (CLKH-WEV)	Delay time, FLASH.CLK high to FLASH.WE transition		3	13.5		3.5	12	3	11	ns	
F13	t _d (CLKH-WDV)	Delay time, FLASH.CLK high to write data valid§			10			9		8	ns	
F14	t _d (CLKH-WDIV)	Delay time, FLASH.CLK high to write data invalid§		2			2		2		ns	
F15	t _d (CLKH-DHZ)	Delay time, FLASH.CLK high to data bus high-impedance§			10			9		8.5	ns	
F16	t _d (CLKH-DLZ)	Delay time, FLASH.CLK high to data bus driven§		6			4.5		4.5		ns	
F17	t _d (CLKH-BAAV)§	Delay time, FLASH.CLK high to FLASH.BAA transition¶		1 + 0.5P	4 + 0.5P		1 + 0.5P	3.5 + 0.5P		1 + 0.5P	3.5 + 0.5P	ns

† The EMIFS/flash clock rate can be limited only by the maximum traffic controller clock rate for the OMAP5912, provided all EMIFS/flash timing constraints are met.

‡ Timing values are given for the CONF_VOLTAGE_FLASH_R bit of the VOLTAGE_CTRL_0 register programmed as follows: 0 for 1.8 V, 1 for 2.75/3.3 V.

§ Data is referenced to the internal FLASH.CLK.

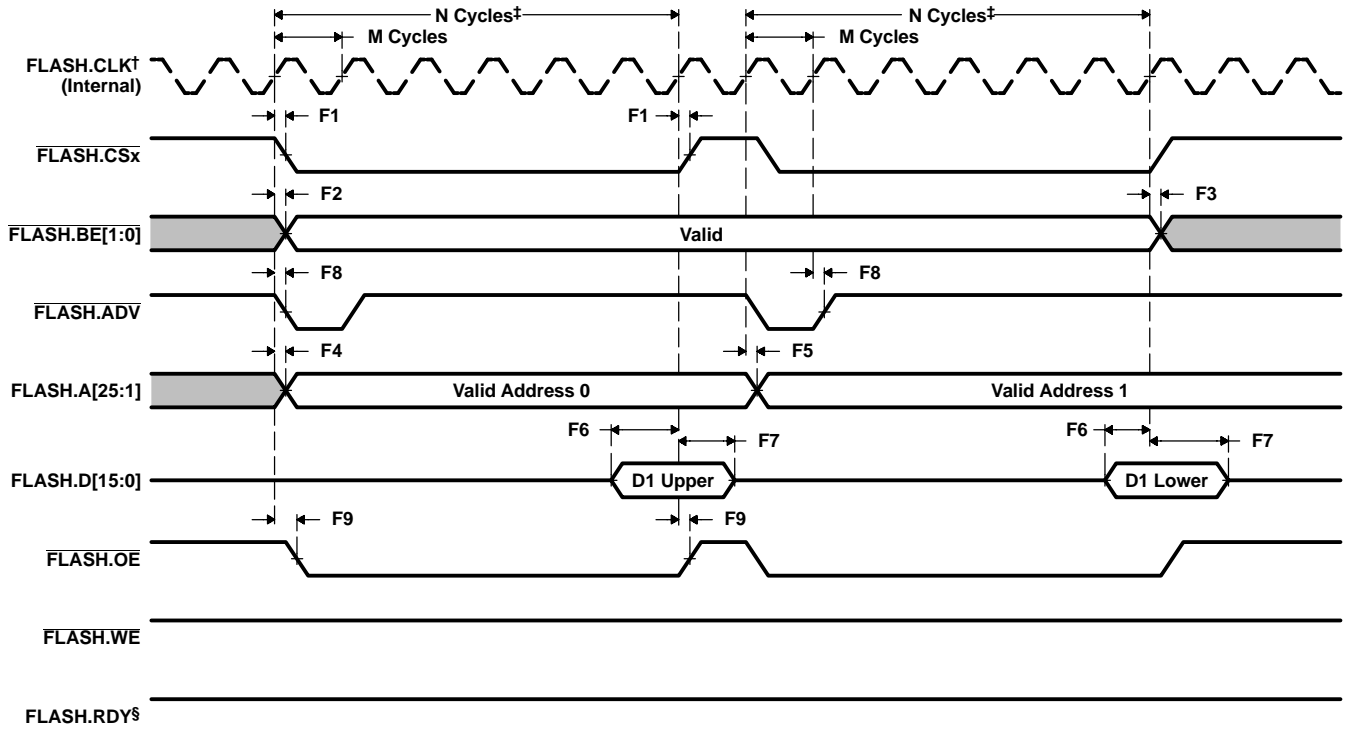
¶ P = period of undivided traffic controller clock regardless of FLASH.CLK divider configuration.



† FLASH.CLK is not driven during this mode of operation. The signal shown represents the internal FLASH.CLK signal given as a reference to express relative timings.

‡ Number of cycles is configurable via EMIFS setup registers.

Figure 5–8. EMIFS/NOR Flash – Asynchronous Memory Read Timing



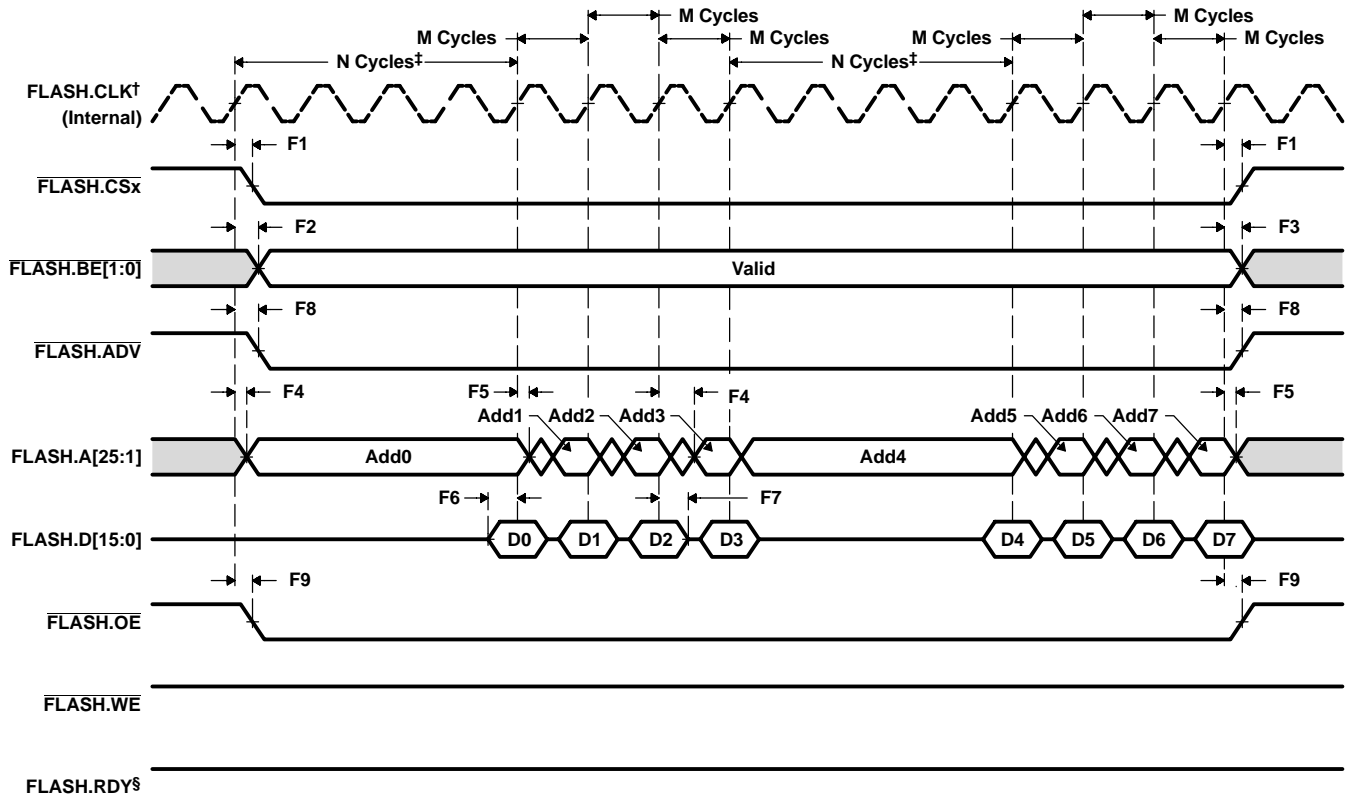
† FLASH.CLK is not driven during this mode of operation. The signal shown represents the internal FLASH.CLK signal given as a reference to express relative timings.

‡ Number of cycles is configurable via EMIFS setup registers.

§ Although shown as always high in this timing diagram, FLASH.RDY may be used to insert wait-states at any time during the cycle.

Figure 5–9. EMIFS/NOR Flash – Asynchronous 32-Bit Read

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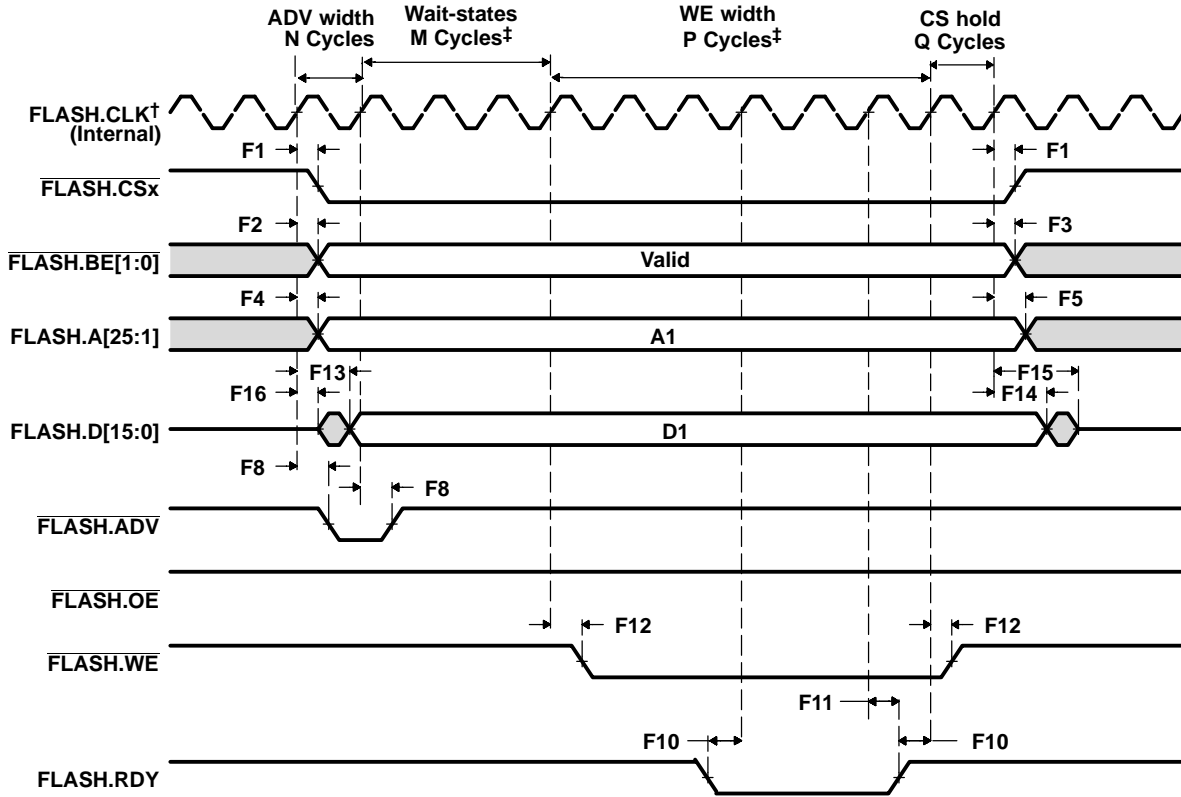


† FLASH.CLK is not driven during this mode of operation. The signal shown represents the internal FLASH.CLK signal given as a reference to express relative timings.

‡ Number of cycles is configurable via EMIFS setup registers.

§ Although shown as always high in this timing diagram, FLASH.RDY may be used to insert wait-states at any time during the cycle.

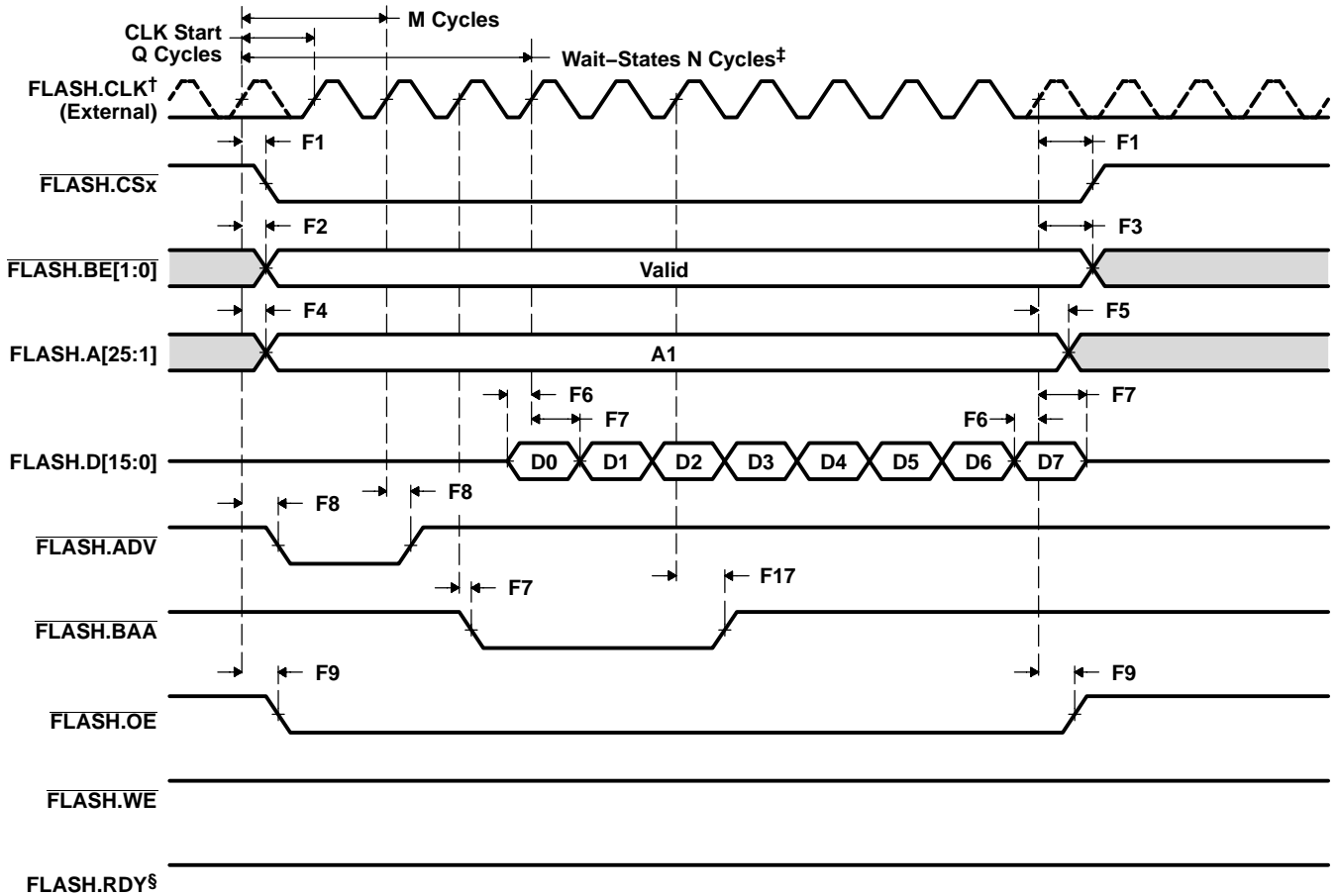
Figure 5–10. EMIFS/NOR Flash – Asynchronous Read – Page Mode 8 x 16 Bit



† FLASH.CLK is not driven during this mode of operation. The signal shown represents the internal FLASH.CLK signal given as a reference to express relative timings.

‡ Number of cycles is configurable via EMIFS setup registers.

Figure 5–11. EMIFS/NOR Flash – Asynchronous Memory Write Timing



† FLASH.CLK is only driven during the active portion of the cycle. For reference, the dashed line shows FLASH.CLK as if it were continuous.
 ‡ Number of cycles is configurable via EMIFS setup registers.
 § Although shown as always high in this timing diagram, FLASH.RDY may be used to insert wait-states at any time during the cycle.

Figure 5–12. EMIFS/NOR Flash – Synchronous Burst Read

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5.8.2 EMIFS/Multiplexed NOR Flash Interface Timings

Table 5–11 and Table 5–12 assume testing over recommended operating conditions (see Figure 5–13 through Figure 5–15).

Table 5–11. EMIFS/Mux NOR Flash Interface Timing Requirements†

NO.			DV _{DD5} = 1.8 V Nominal‡		DV _{DD5} = 2.75 V Nominal‡		DV _{DD5} = 3.3 V Nominal‡		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
MF8	t _{su} (DV-CLKH)	Setup time, input data valid before FLASH.CLK high	Async modes (RT = 0)§		2		2		ns
			Sync modes (RT = 1)§		2		2		
MF9	t _h (CLKH-DV)	Hold time, input data valid after FLASH.CLK high	Async modes (RT = 0)§		4		4		ns
			Sync modes (RT = 1)§		3		3		
MF10	t _{su} (RDYV-CLKH)	Setup time, FLASH.RDY valid before FLASH.CLK high	Async modes (RT = 0)§		7		7		ns
			Sync modes (RT = 1)§		2		2		
MF11	t _h (CLKH-RDYV)	Hold time, FLASH.RDY valid after FLASH.CLK high	Async modes (RT = 0)§		0.5		0.5		ns
			Sync modes (RT = 1)§		3		3		

† The EMIFS/flash clock rate can be limited only by the maximum traffic controller clock rate for the OMAP5912, provided all EMIFS/flash timing constraints are met.

‡ Timing values are given for the CONF_VOLTAGE_FLASH_R bit of the VOLTAGE_CTRL_0 register programmed as follows: 0 for 1.8 V, 1 for 2.75/3.3 V.

§ When the RT field in the EMIFS configuration register is set, input data is retimed to the external FLASH.CLK signal. The RT = 1 setting is only valid in synchronous modes (protocols 1 and 2). The RT = 0 setting in synchronous modes is ensured only for traffic controller clock frequencies of 50 MHz and lower.

Table 5–12. EMIFS/MUX NOR Flash Interface Switching Characteristics†

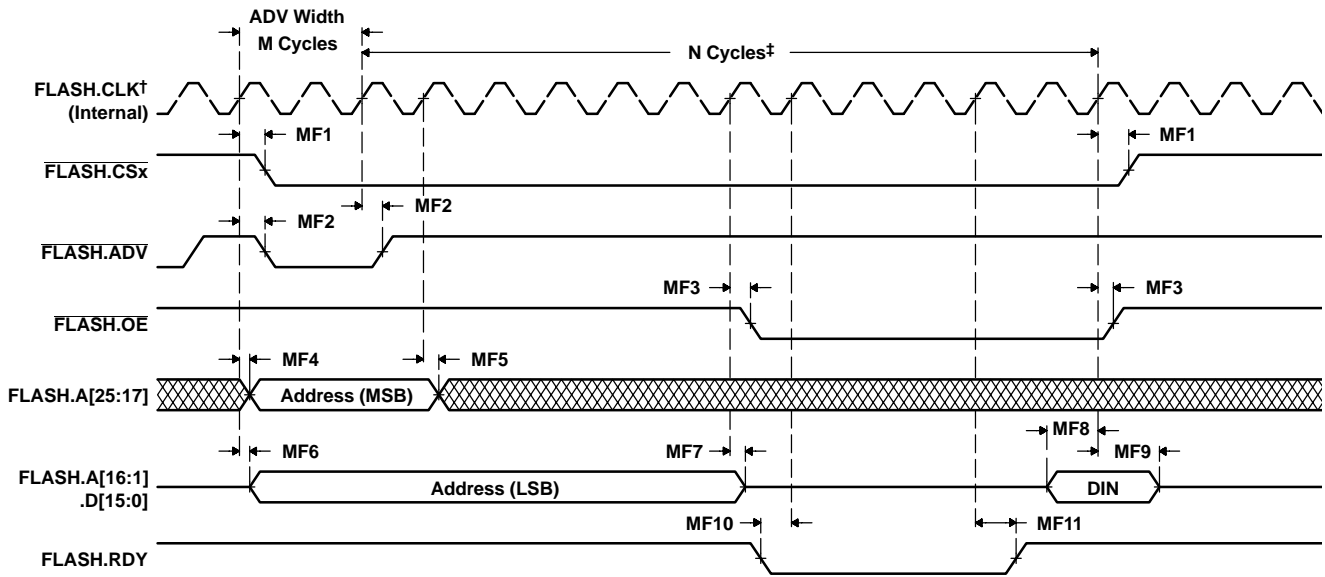
NO.	PARAMETER		DV _{DD5} = 1.8 V Nominal‡		DV _{DD5} = 2.75 V Nominal‡		DV _{DD5} = 3.3 V Nominal‡		UNIT		
			MIN	MAX	MIN	MAX	MIN	MAX			
MF1	t _d (CLKH-CSV)	Delay time, FLASH.CLK high to FLASH.CSx transition	async modes	2	19	2.5	17	2.5	16	ns	
			sync modes	0	9.5	0	8.5	0	8.5		
MF2	t _d (CLKH-ADV)	Delay time, FLASH.CLK high to FLASH.ADV transition	async modes	2	11.5	2.5	9.5	2.5	8.5	ns	
			sync modes	0	2	0.5	1	0	1		
MF3	t _d (CLKH-OEV)	Delay time, FLASH.CLK high to FLASH.OE transition	async modes	3	14	3	12	3	11	ns	
			sync modes	1	4.5	1	4	1	3.5		
MF4	t _d (CLKH-AV)	Delay time, FLASH.CLK high to address valid (FLASH.A[25:17])	async modes		11		9.5		8.5	ns	
			sync modes		1.5		1		0.5		
MF5	t _d (CLKH-AIV)	Delay time, FLASH.CLK high to address invalid (FLASH.A[25:17])	async modes	2		2.5		2.5	ns		
			sync modes	0		0		0			
MF6	t _d (CLKH-DAV)	Delay time, FLASH.CLK high to address valid (FLASH.A[16:1].D[15:0])	async modes		10.5		9		8.5	ns	
			sync modes		0.5		0.5		0.5		
MF7	t _d (CLKH-DAIV)	Delay time, FLASH.CLK high to address invalid (FLASH.A[16:1].D[15:0])	async modes	2.5		2.5		2.5	ns		
			sync modes	0		0		0			
MF12	t _d (CLKH-WEV)	Delay time, FLASH.CLK high to FLASH.WE transition		3	13.5		3.5	12	3	11	ns
MF13	t _d (CLKH-DV)	Delay time, FLASH.CLK high to write data valid§			10			9		8	ns
MF14	t _d (CLKH-DIV)	Delay time, FLASH.CLK high to write data invalid§		2			2		2		ns

† The EMIFS/flash clock rate can be limited only by the maximum traffic controller clock rate for the OMAP5912, provided all EMIFS/flash timing constraints are met.

‡ Timing values are given for the CONF_VOLTAGE_FLASH_R bit of the VOLTAGE_CTRL_0 register programmed as follows: 0 for 1.8 V, 1 for 2.75/3.3 V.

§ Data is referenced to the internal FLASH.CLK.

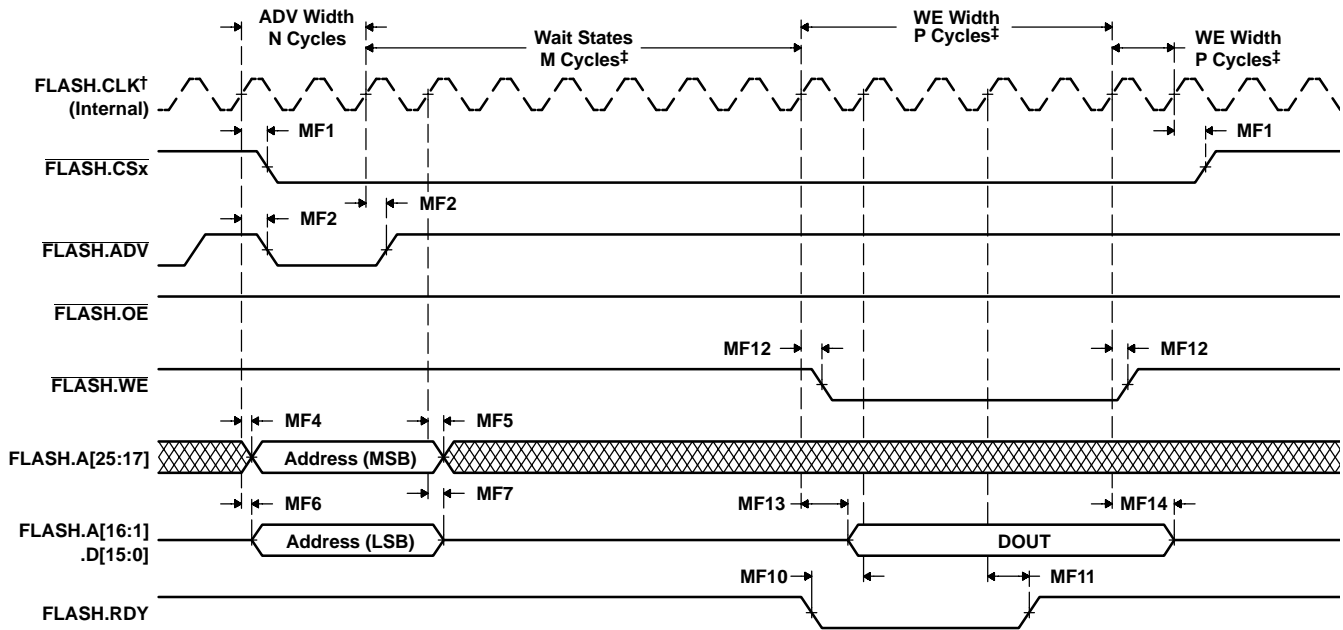
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† FLASH.CLK is not driven during this mode of operation. The signal shown represents the internal FLASH.CLK signal given as a reference to express relative timings.

‡ Number of cycles is configurable via EMIFS setup registers.

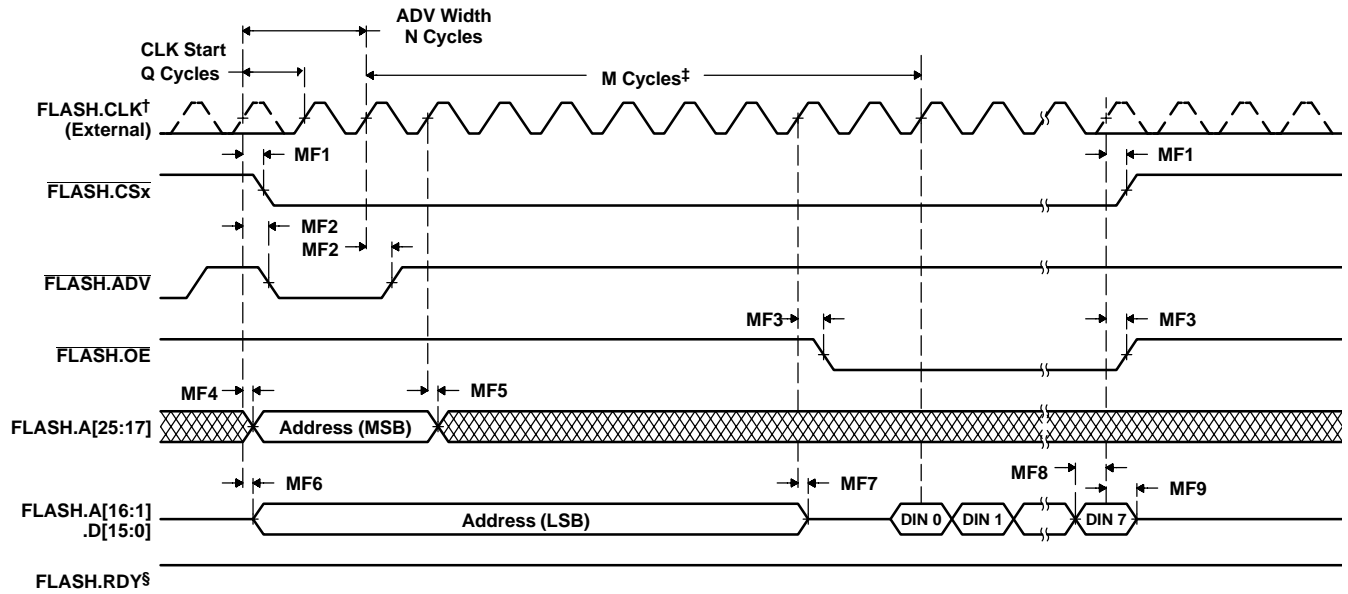
Figure 5–13. EMIFS/MUX NOR Flash – Single Word Asynchronous Read



† FLASH.CLK is not driven during this mode of operation. The signal shown represents the internal FLASH.CLK signal given as a reference to express relative timings.

‡ Number of cycles is configurable via EMIFS setup registers.

Figure 5–14. EMIFS/MUX NOR Flash – Single Word Asynchronous Write



† FLASH.CLK is only driven during the active portion of the cycle. For reference, the dashed line shows FLASH.CLK as if it were continuous.
 ‡ Number of cycles is configurable via EMIFS setup registers.
 § Although shown as always high in this timing diagram, FLASH. RDY may be used to insert wait-states at any time during the cycle.

Figure 5–15. EMIFS/MUX NOR Flash – Synchronous Four-Word Burst Read

5.8.3 EMIFS/NAND Flash Timings

Table 5–13 and Table 5–14 assume testing over operating conditions (see Figure 5–16 through Figure 5–19).

Table 5–13. EMIFS/NAND Flash Timing Requirements

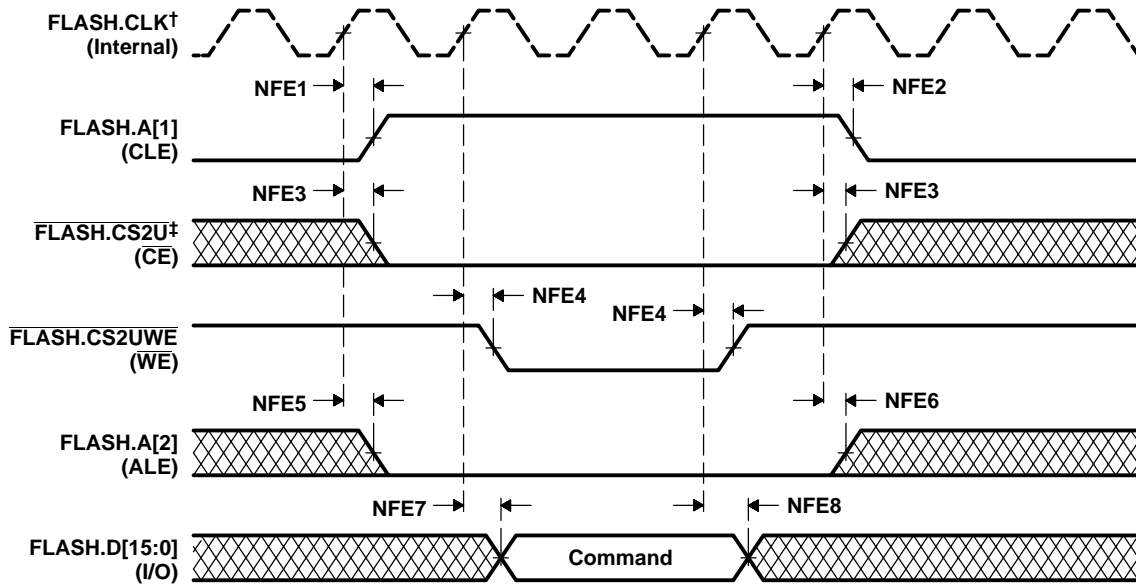
NO.		DV _{DD5} = 1.8 V Nominal [†]		DV _{DD5} = 2.75 V Nominal [†]		DV _{DD5} = 3.3 V Nominal [†]		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
NFE10	t _{su} (DV-CLKH) Setup time, input FLASH.D[15:0] valid before FLASH.CLK high	2		2		2		ns
NFE11	t _h (CLKH-DV) Hold time, input FLASH.D[15:0] valid after FLASH.CLK high	3		3		3		ns

[†] Timing values are given for the CONF_VOLTAGE_FLASH_R bit of the VOLTAGE_CTRL_0 register programmed as follows: 0 for 1.8 V, 1 for 2.75/3.3 V.

Table 5–14. EMIFS/NAND Flash Switching Characteristics

NO.	PARAMETER	DV _{DD5} = 1.8 V Nominal [†]		DV _{DD5} = 2.75 V Nominal [†]		DV _{DD5} = 3.3 V Nominal [†]		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
NFE1	t _d (CLKH-CLEV) Delay time, FLASH.CLK high to FLASH.A[1] (CLE) valid		13.5		12		11	ns
NFE2	t _d (CLKH-CLEIV) Delay time, FLASH.CLK high to FLASH.A[1] (CLE) invalid	3.5		3.5		3.5		ns
NFE3	t _d (CLKH-CEV) Delay time, FLASH.CLK high to $\overline{\text{FLASH.CS2U}}$ ($\overline{\text{CE}}$) transition		14.5		14.5		14.5	ns
NFE4	t _d (CLKH-WEV) Delay time, FLASH.CLK high to $\overline{\text{FLASH.CS2UWE}}$ ($\overline{\text{WE}}$) transition	3	13.5	3	12	3	11	ns
NFE5	t _d (CLKH-ALEV) Delay time, FLASH.CLK high to FLASH.A[2] (ALE) valid		13		11.5		10	ns
NFE6	t _d (CLKH-ALEIV) Delay time, FLASH.CLK high to FLASH.A[2] (ALE) invalid	3		3.5		3.5		ns
NFE7	t _d (CLKH-DV) Delay time, FLASH.CLK high to FLASH.D[15:0] valid		10		9		8	ns
NFE8	t _d (CLKH-DIV) Delay time, FLASH.CLK high to FLASH.D[15:0] invalid	2		2		2		ns
NFE9	t _d (CLKH-REV) Delay time, FLASH.CLK high to $\overline{\text{FLASH.CS2UOE}}$ ($\overline{\text{RE}}$) transition		14.5		14.5		14.5	ns

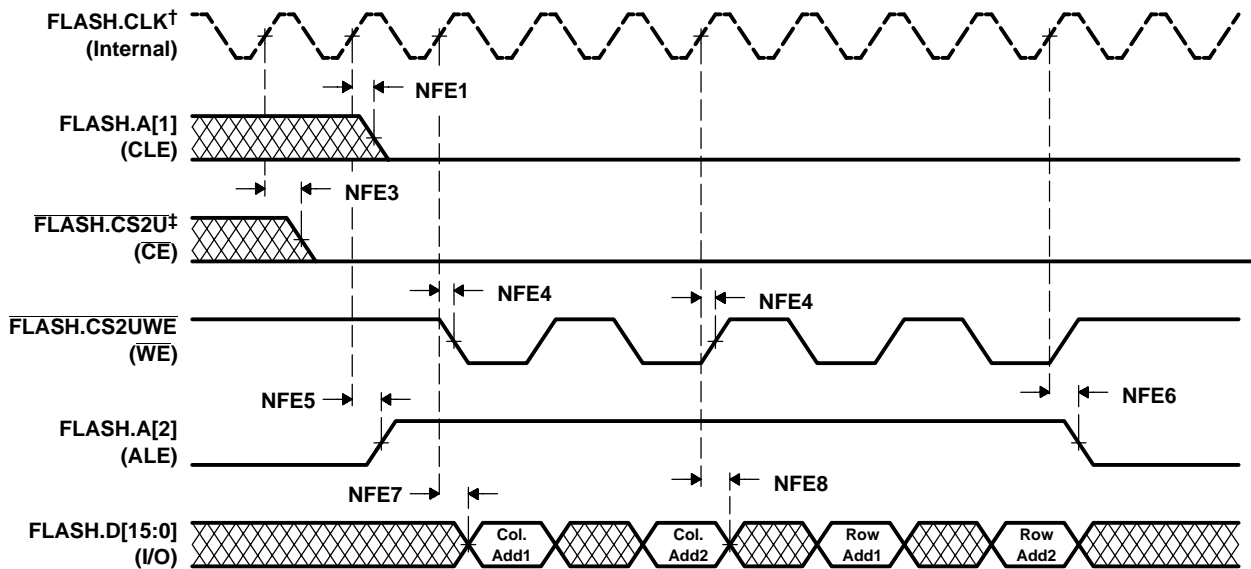
[†] Timing values are given for the CONF_VOLTAGE_FLASH_R bit of the VOLTAGE_CTRL_0 register programmed as follows: 0 for 1.8 V, 1 for 2.75/3.3 V.



† FLASH.CLK is not driven during this mode of operation. The signal shown represents the internal FLASH.CLK signal given as a reference to express relative timings.

‡ When a NAND CE care Flash type is used, FLASH.CS2U is a combination of a GPIO (controlled by software—no timing) and CS2U (internal).

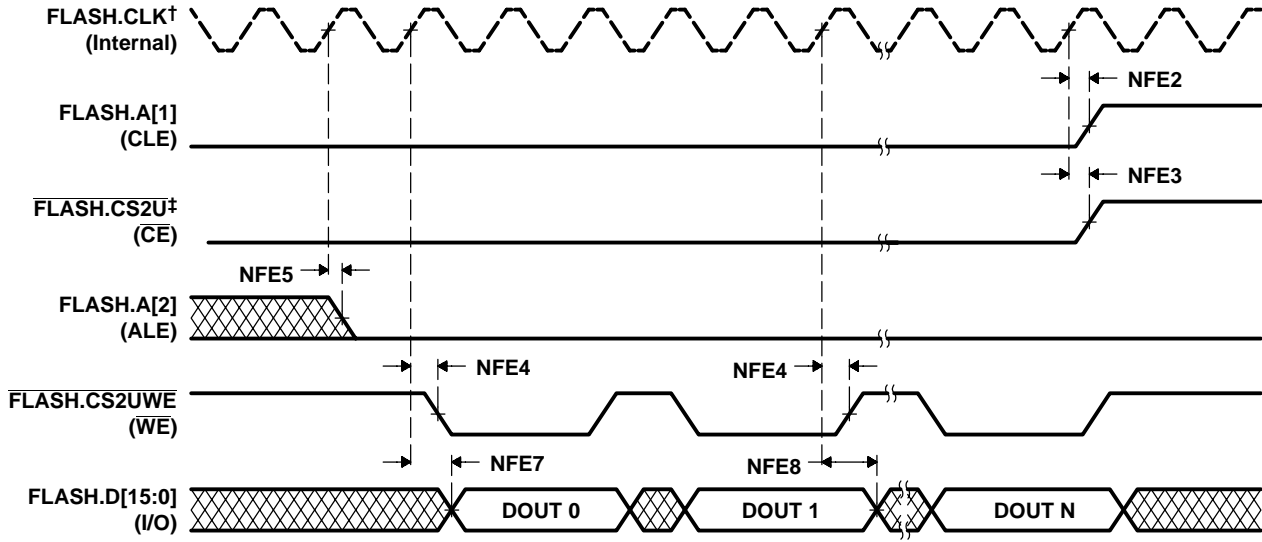
Figure 5–16. EMIFS/NAND Flash – Command Latch Timing



† FLASH.CLK is not driven during this mode of operation. The signal shown represents the internal FLASH.CLK signal given as a reference to express relative timings.

‡ When a NAND CE care Flash type is used, FLASH.CS2U is a combination of a GPIO (controlled by software—no timing) and CS2U (internal).

Figure 5–17. EMIFS/NAND Flash – Address Latch Timing

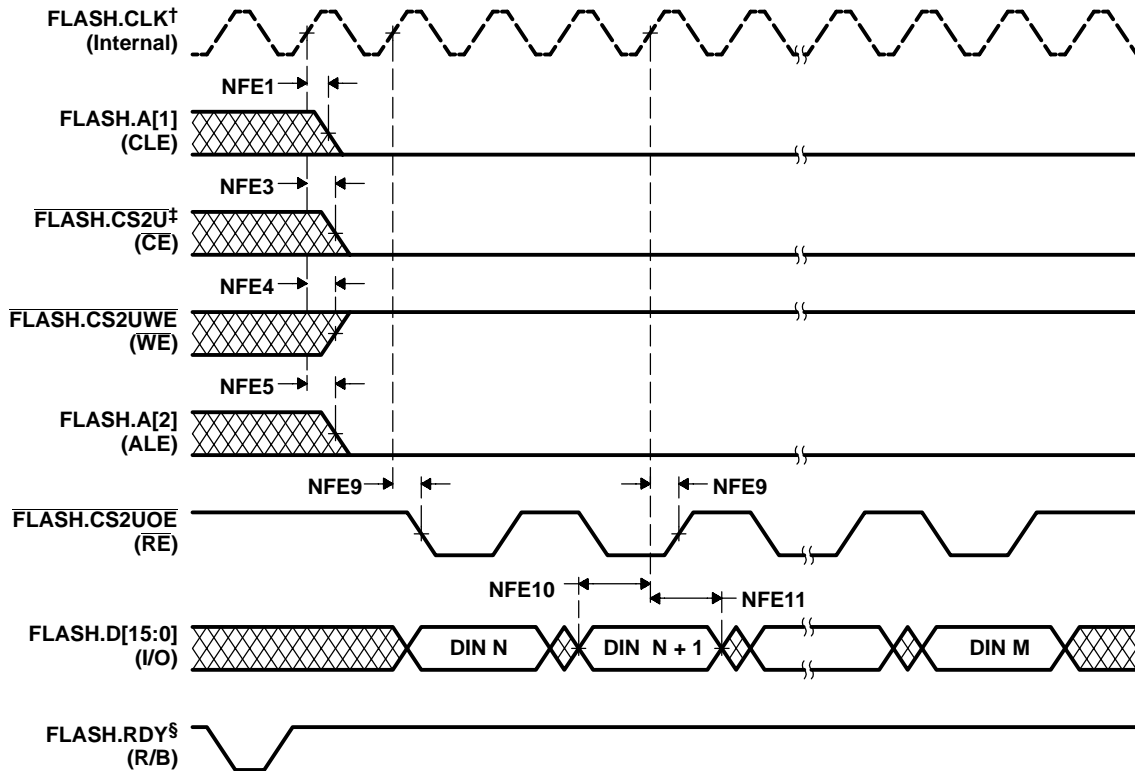


† FLASH.CLK is not driven during this mode of operation. The signal shown represents the internal FLASH.CLK signal given as a reference to express relative timings.

‡ When a NAND CE care Flash type is used, $\overline{\text{FLASH.CS2U}}$ is a combination of a GPIO (controlled by software—no timing) and CS2U (internal).

Figure 5–18. EMIFS/NAND Flash – Memory Write Timing

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† FLASH.CLK is not driven during this mode of operation. The signal shown represents the internal FLASH.CLK signal given as a reference to express relative timings.

‡ When a NAND CE care Flash type is used, FLASH.CS2U is a combination of a GPIO (controlled by software—no timing) and CS2U (internal).

§ The flash Ready/Busy input is monitored by software.

Figure 5–19. EMIFS/NAND Flash – Memory Read Timing

5.9 CompactFlash Interface Timings

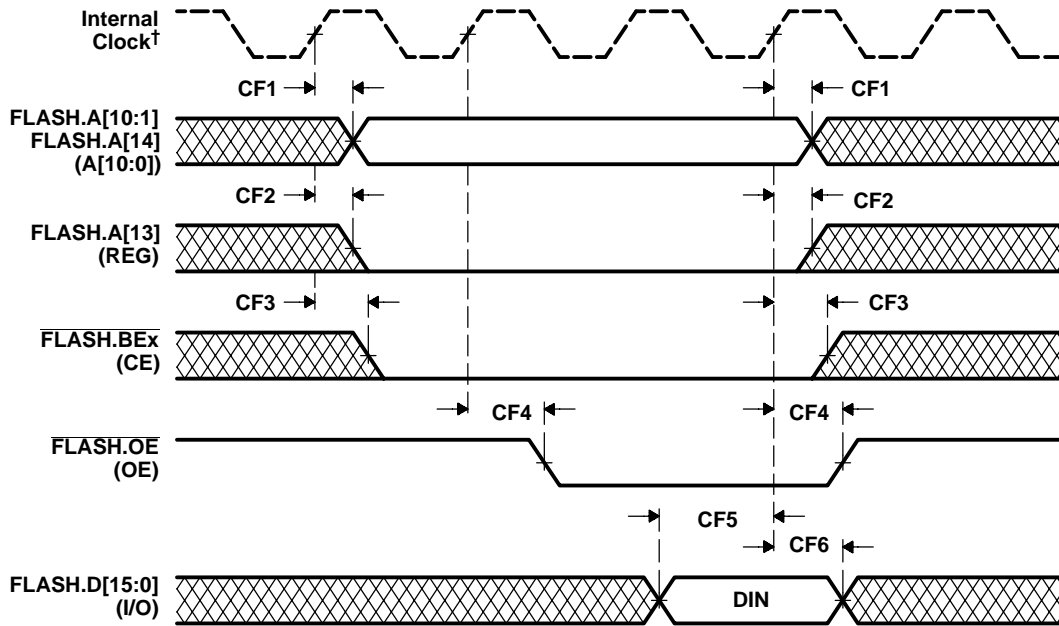
Table 5–15 and Table 5–16 assume testing over operating conditions (see Figure 5–20 through Figure 5–25).

Table 5–15. CompactFlash Interface Timing Requirements

NO.		DV _{DD5} = 1.8 V Nominal		DV _{DD5} = 2.75 V Nominal		DV _{DD5} = 3.3 V Nominal		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
CF5	t _{su} (DV-CLKH) Setup time, FLASH.D[15:0] valid before internal clock high	2		2		2		ns
CF6	t _h (DV-CLKH) Hold time, FLASH.D[15:0] valid after internal clock high	3		3		3		ns
CF9	t _{su} (RDYV-CLKH) Setup time, FLASH.RDY valid before internal clock high	2		2		2		ns
CF10	t _h (CLKH-RDYV) Hold time, FLASH.RDY valid after internal clock high	3		3		3		ns

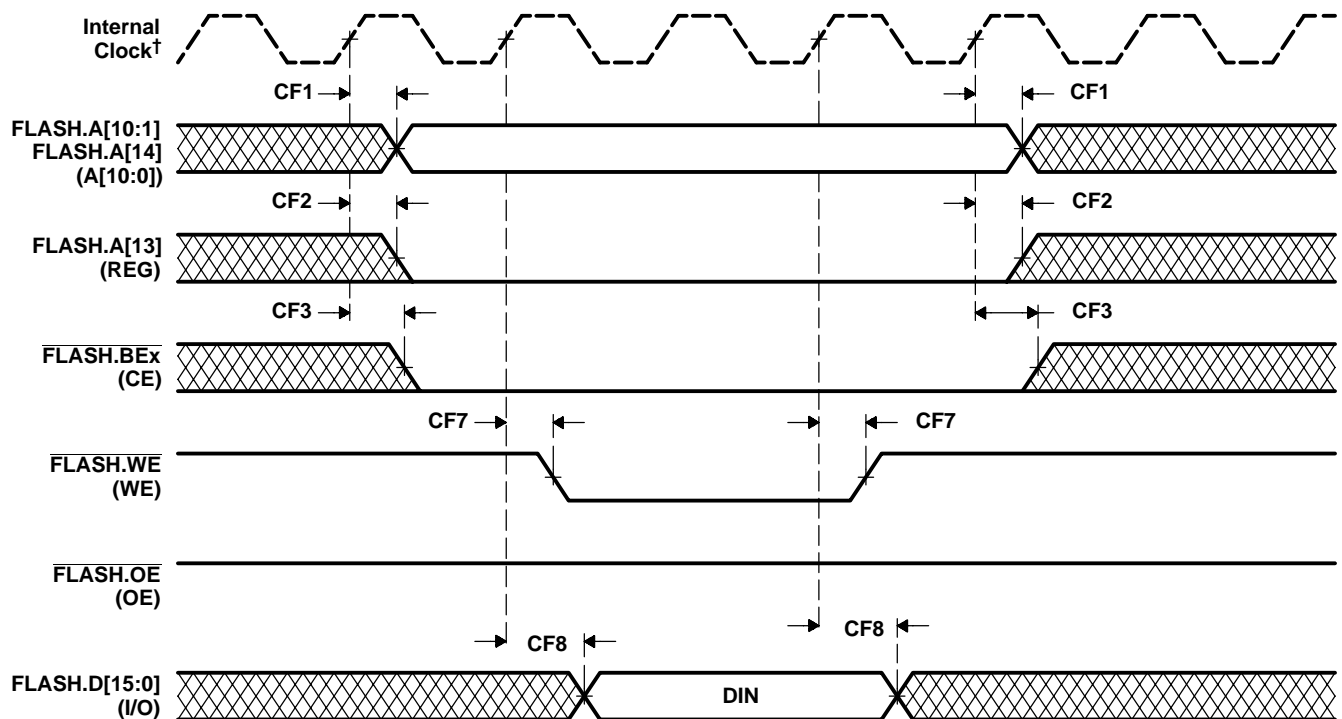
Table 5–16. CompactFlash Interface Switching Characteristics

NO.	PARAMETER	DV _{DD5} = 1.8 V Nominal		DV _{DD5} = 2.75 V Nominal		DV _{DD5} = 3.3 V Nominal		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
CF1	t _d (CLKH-AV) Delay time, internal clock to Address (FLASH.A[10:1] and A[14]) transition	9		8.5		8		ns
CF2	t _d (CLKH-REGV) Delay time, internal clock to REG (FLASH.A[13]) transition	9		8.5		8		ns
CF3	t _d (CLKH-CSV) Delay time, internal clock to \overline{CS} (FLASH.BEX) transition	1.5		1.5		1.5		ns
CF4	t _d (CLKH-OEV) Delay time, internal clock to \overline{OE} (FLASH.OE) transition	1	4.5	1	4	1	3.5	ns
CF7	t _d (CLKH-WEV) Delay time, internal clock to \overline{WE} (FLASH.WE) transition	3	13.5	3.5	12	3	11	ns
CF8	t _d (CLKH-DV) Delay time, internal clock to data (FLASH.D[15:0]) valid	10		9		8		ns
CF11	t _d (CLKH-IORDV) Delay time, internal clock to IORD (FLASH.A[11]) transition	9		8.5		8		ns
CF12	t _d (CLKH-IOIS16V) Delay time, internal clock to IOS16 ($\overline{CFLASH.IOSIS16}$) transition	1.5	4	1.5	4	1.5	4	ns
CF13	t _d (CLKH-IOWRV) Delay time, internal clock to IOWR (FLASH.A[12]) transition	9		8.5		8		ns



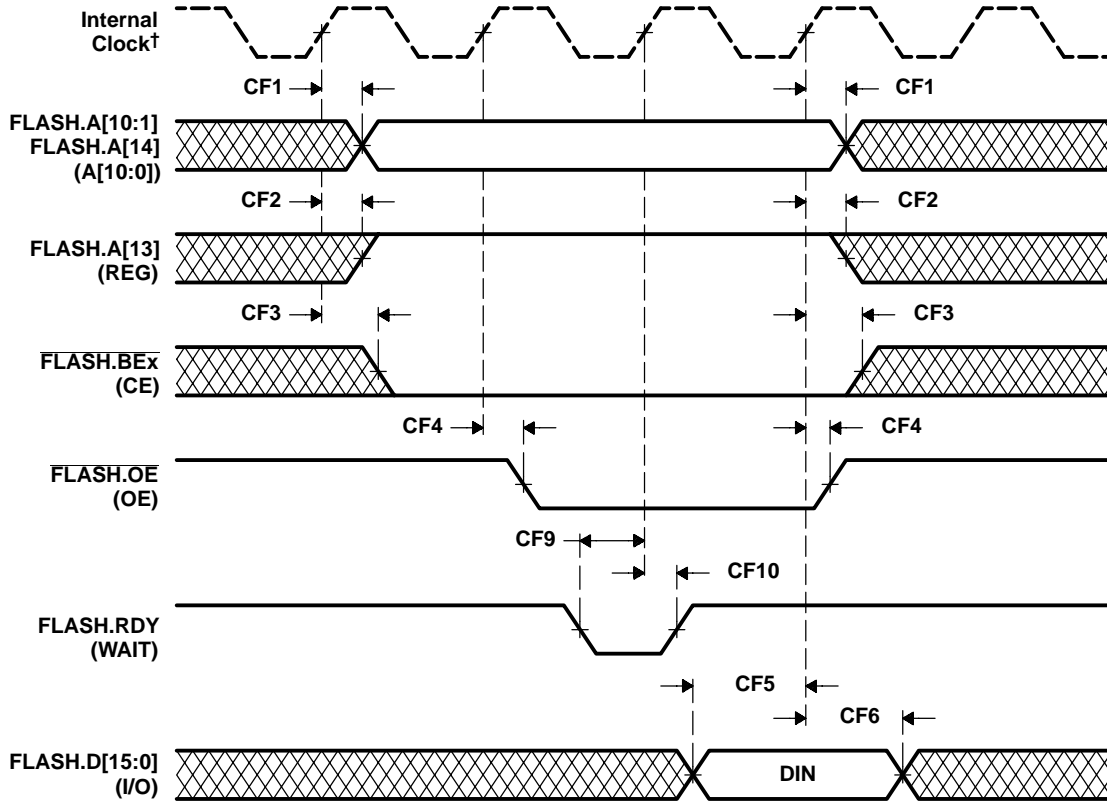
† The signal shown represents the internal clock signal given as a reference to express relative timings.

Figure 5–20. CompactFlash – Attribute Memory Mode Read Timing



† The signal shown represents the internal clock signal given as a reference to express relative timings.

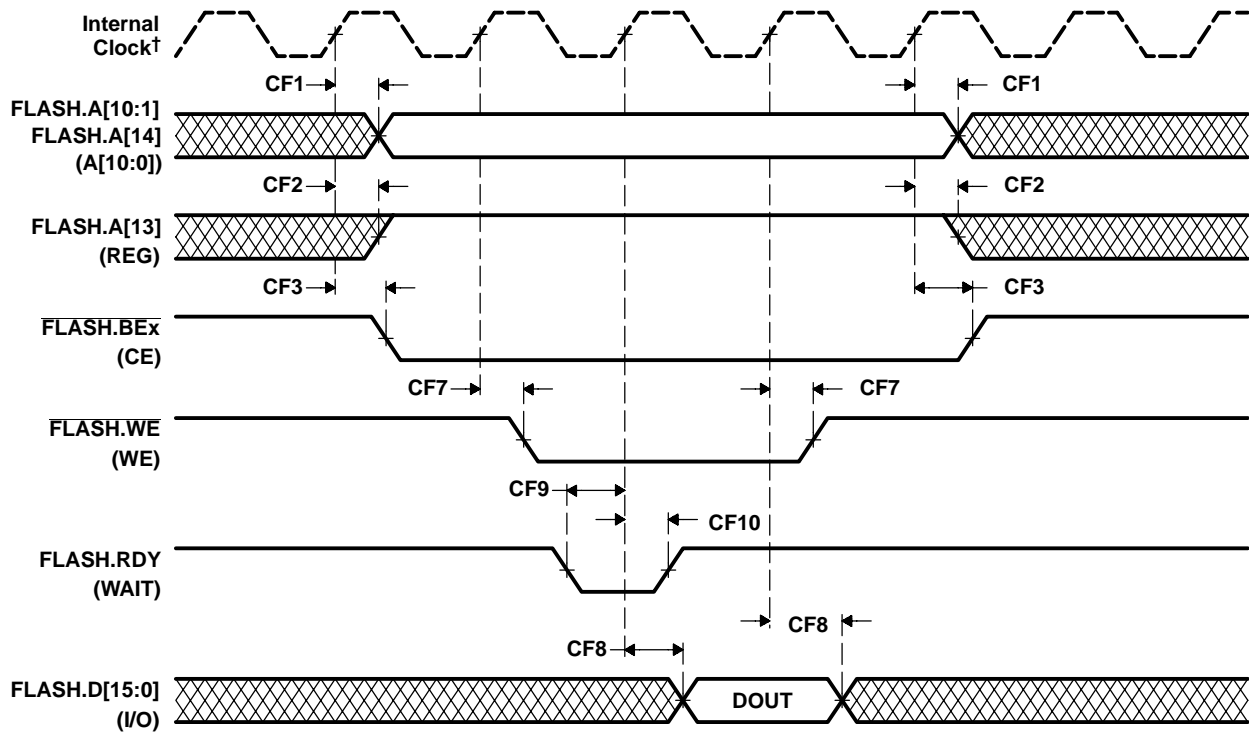
Figure 5–21. CompactFlash – Attribute Memory Mode Write Timing



† The signal shown represents the internal clock signal given as a reference to express relative timings.

Figure 5–22. CompactFlash – Common Memory Mode Read Timing

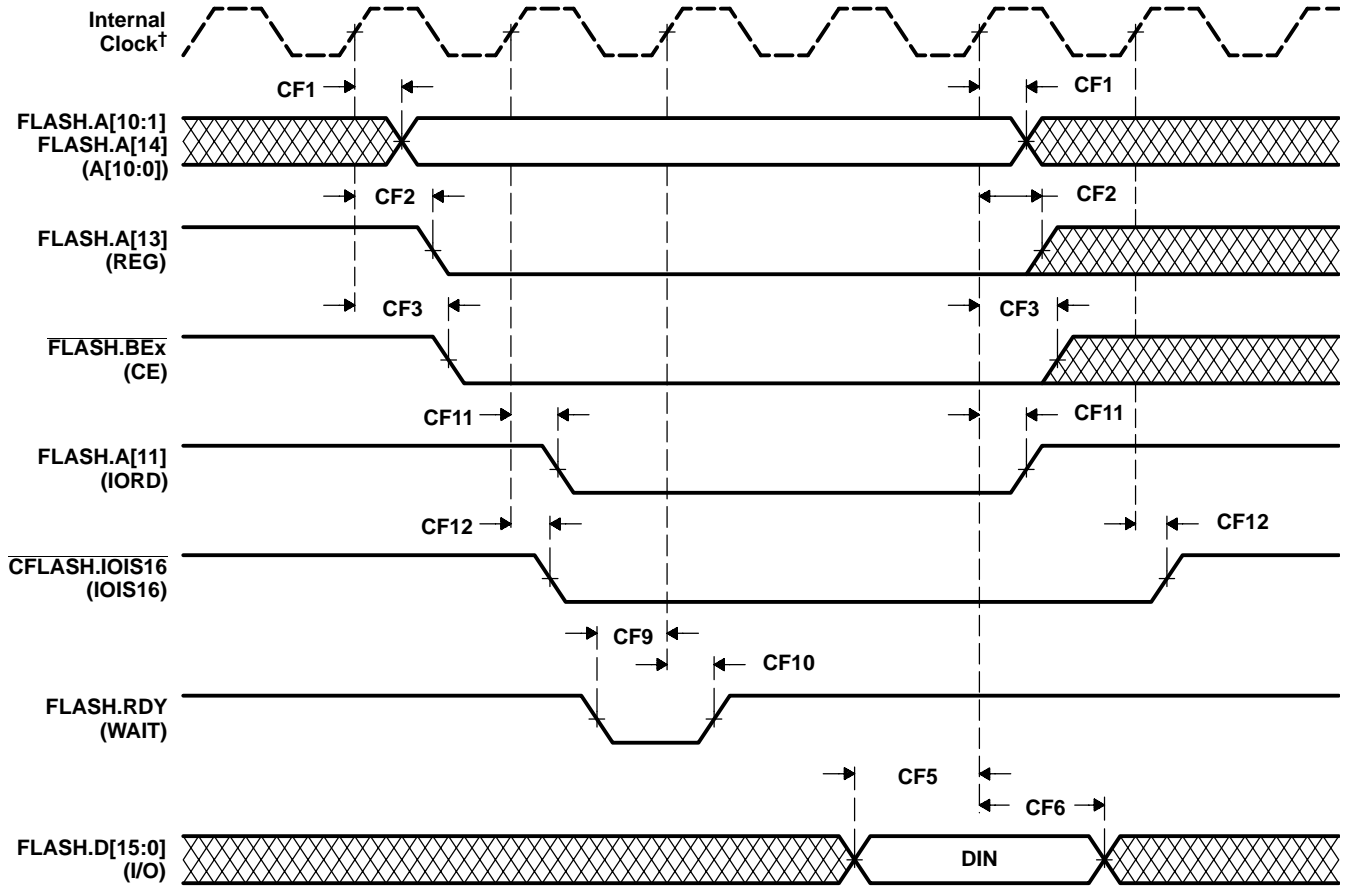
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† The signal shown represents the internal clock signal given as a reference to express relative timings.

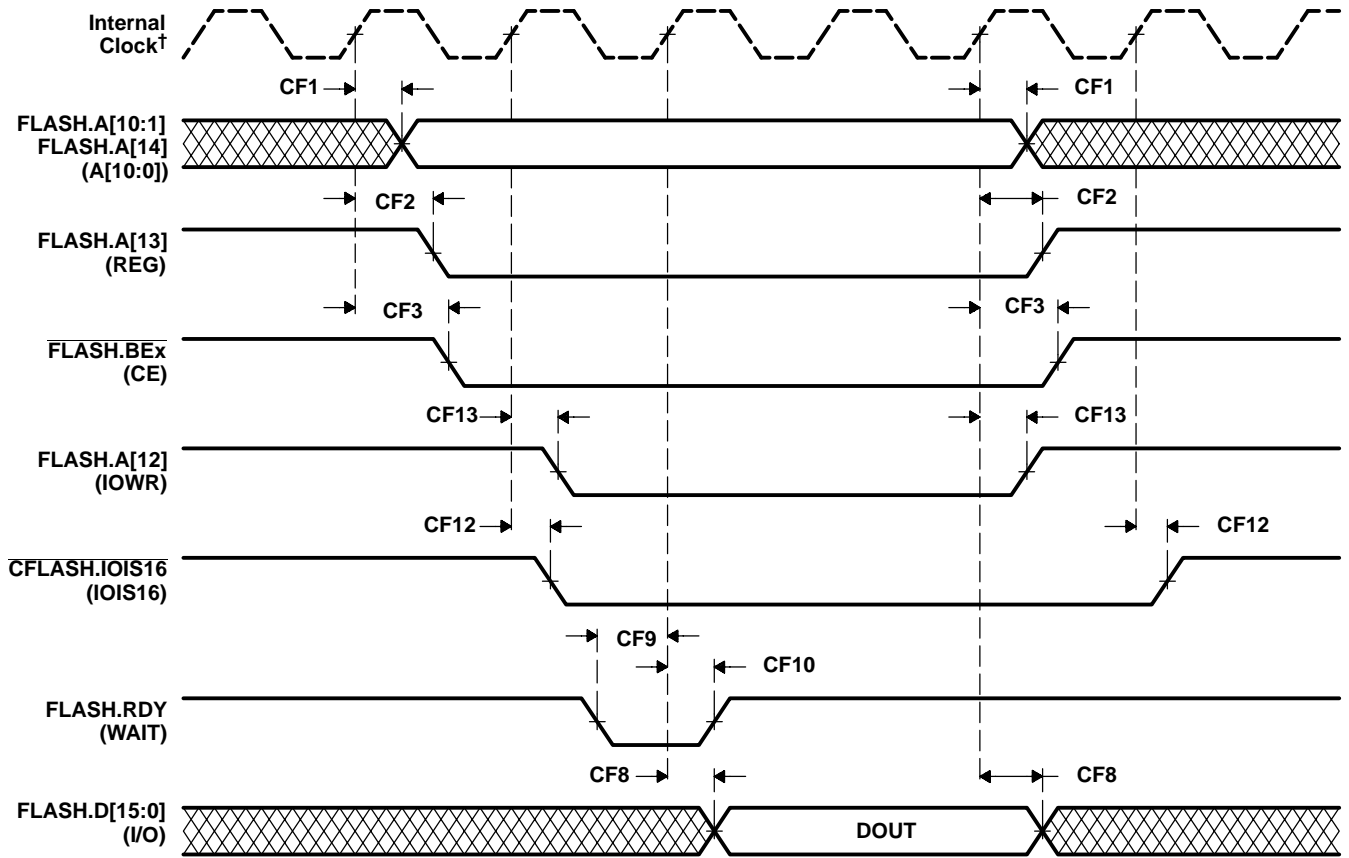
Figure 5–23. CompactFlash – Common Memory Mode Write Timing

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† The signal shown represents the internal clock signal given as a reference to express relative timings.

Figure 5–24. CompactFlash – I/O Mode Read Timing



† The signal shown represents the internal clock signal given as a reference to express relative timings.

Figure 5–25. CompactFlash – I/O Mode Write Timing

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5.10 EMIFF/SDR SDRAM Interface Timing

Table 5–17 and Table 5–18 assume testing over operating conditions (see Figure 5–26 through Figure 5–31).

Table 5–17. EMIFF/SDR SDRAM Interface Timing Requirements†

NO.		DV _{DD4} = 1.8 V Nominal‡		DV _{DD4} = 2.75 V Nominal‡		DV _{DD4} = 3.3 V Nominal‡		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
SD7	t _{su} (DV-CLKH) Setup time, read data valid before SDRAM.CLK high	2		2		2		ns
SD8	t _h (CLKH-DV) Hold time, read data valid after SDRAM.CLK high	1.5		1.5		1.5		ns

† Timing is ensured up to the maximum EMIFF/SDRAM clock rate when the SD_RET field in the EMIFF configuration register is set. Timing is ensured independent of SD_REF for EMIFF/SDRAM clock rates of 50 MHz and lower.

‡ Timing values are given for the CONF_VOLTAGE_SDRAM_R bit of the VOLTAGE_CTRL_0 register programmed as follows: 0 for 1.8 V, 1 for 2.75/3.3 V.

Table 5–18. EMIFF/SDR SDRAM Interface Switching Characteristics†

NO.	PARAMETER	DV _{DD4} = 1.8 V Nominal‡		DV _{DD4} = 2.75 V Nominal‡		DV _{DD4} = 3.3 V Nominal‡		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
SD1	t _c (CLK) Cycle time, SDRAM.CLK	10 [§]		10 [§]		10 [§]		ns
SD2	t _w (CLK) Pulse duration, SDRAM.CLK high/low	4.5		4.5		4.5		ns
SD3	t _d (CLKH-DQMV) Delay time, SDRAM.CLK high to SDRAM.DQMx valid	2	8	2	8	2	8	ns
SD4	t _d (CLKH-DQMIV) Delay time, SDRAM.CLK high to SDRAM.DQMx invalid	2	8	2	8	2	8	ns
SD5	t _d (CLKH-AV) Delay time, SDRAM.CLK high to SDRAM.A[13:0] address valid	3	7	3	7	3	7	ns
SD6	t _d (CLKH-AIV) Delay time, SDRAM.CLK high to SDRAM.A[13:0] address invalid	3	7	3	7	3	7	ns
SD9	t _d (CLKH-SDCASL) Delay time, SDRAM.CLK high to SDRAM.CAS low	3	7	3	7	3	7	ns
SD10	t _d (CLKH-SDCASH) Delay time, SDRAM.CLK high to SDRAM.CAS high	3	7	3	7	3	7	ns
SD11	t _d (CLKH-DV) Delay time, SDRAM.CLK high to SDRAM.D[15:0] data valid	2	8	2	8	2	8	ns
SD12	t _d (CLKH-DIV) Delay time, SDRAM.CLK high to SDRAM.D[15:0] data invalid	2	8	2	8	2	8	ns
SD13	t _d (CLKH-SDWEL) Delay time, SDRAM.CLK high to SDRAM.WE low	3	7	3	7	3	7	ns
SD14	t _d (CLKH-SDWEH) Delay time, SDRAM.CLK high to SDRAM.WE high	3	7	3	7	3	7	ns
SD15	t _d (CLKH-BAV) Delay time, SDRAM.CLK high to SDRAM.BA[1:0] valid	3	7	3	7	3	7	ns
SD16	t _d (CLKH-BAIV) Delay time, SDRAM.CLK high to SDRAM.BA[1:0] invalid	3	7	3	7	3	7	ns
SD17	t _d (CLKH-RASL) Delay time, SDRAM.CLK high to SDRAM.RAS low	3	7	3	7	3	7	ns
SD18	t _d (CLKH-RASH) Delay time, SDRAM.CLK high to SDRAM.RAS high	3	7	3	7	3	7	ns

† Timing is ensured up to the maximum EMIFF/SDRAM clock rate when the SD_RET field in the EMIFF configuration register is set. Timing is ensured independent of SD_REF for EMIFF/SDRAM clock rates of 50 MHz and lower.

‡ Timing values are given for the CONF_VOLTAGE_SDRAM_R bit of the VOLTAGE_CTRL_0 register programmed as follows: 0 for 1.8 V, 1 for 2.75/3.3 V.

§ The maximum EMIFF/SDRAM clock rate is limited to the maximum traffic controller clock rate for the OMAP5912.

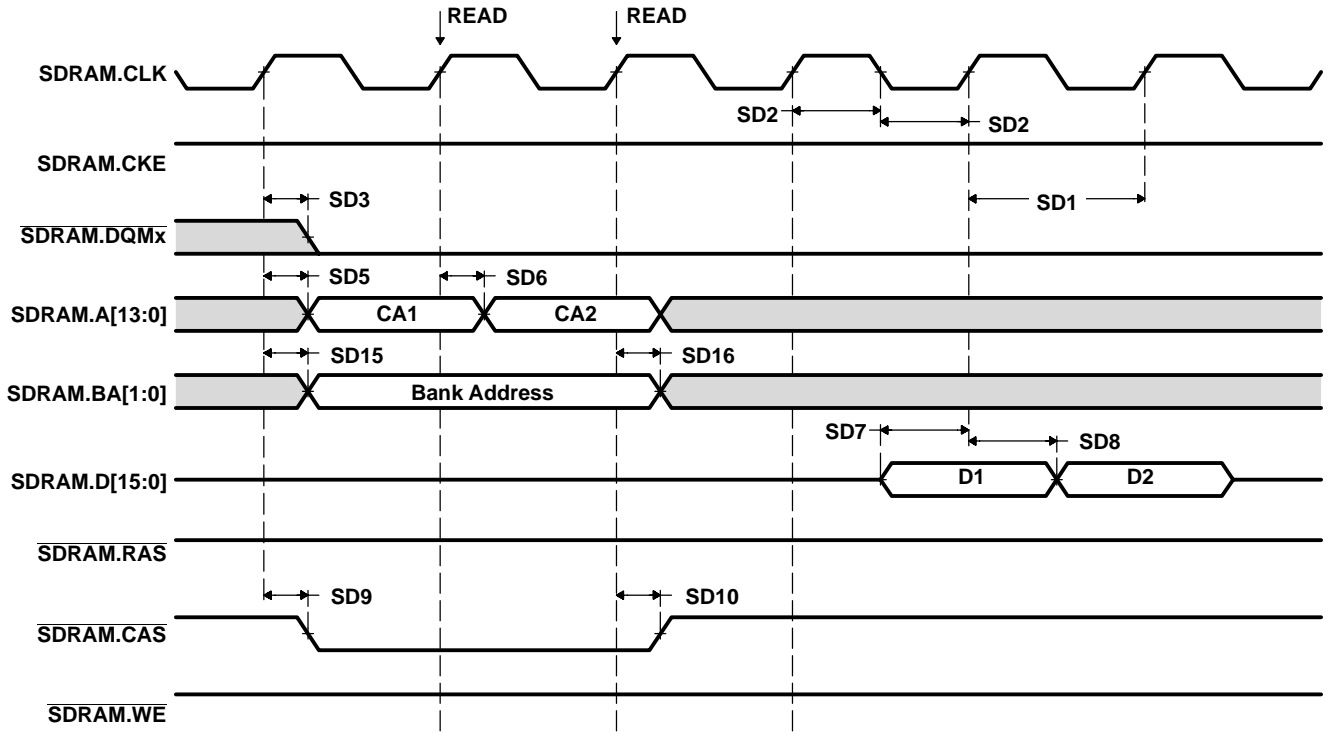


Figure 5-26. EMIFF/SDR Two SDRAM RD (Read) Commands (Active Row)

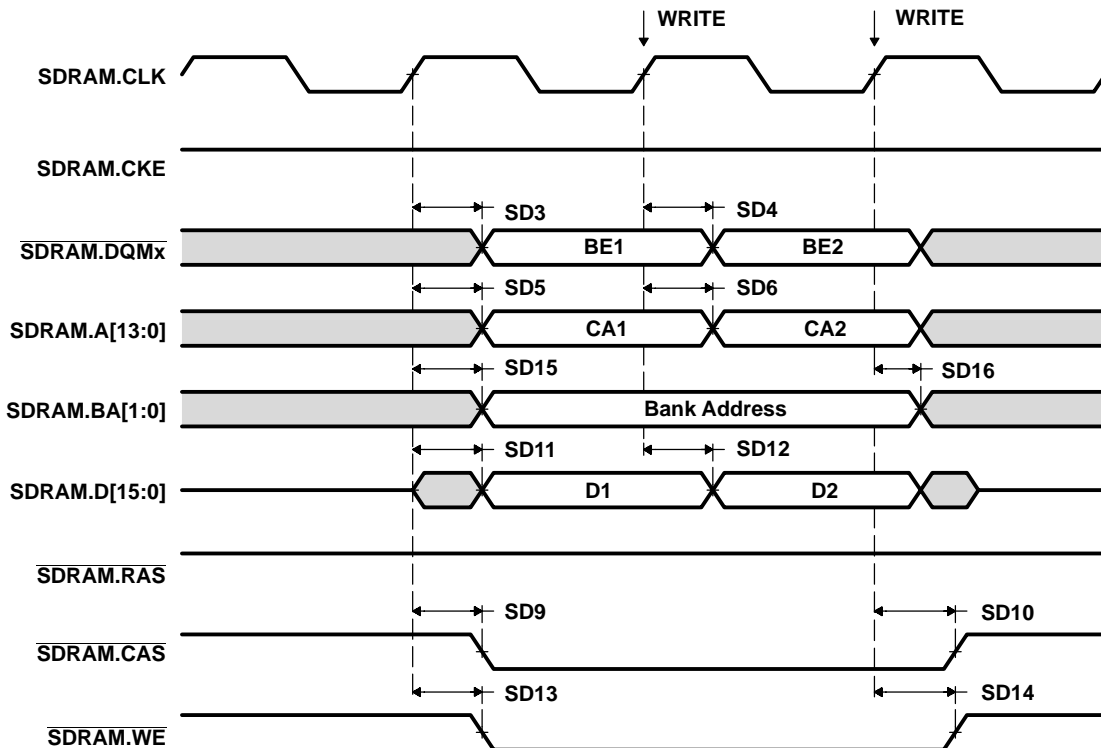


Figure 5-27. EMIFF/SDR Two SDRAM WRT (Write) Commands (Active Row)

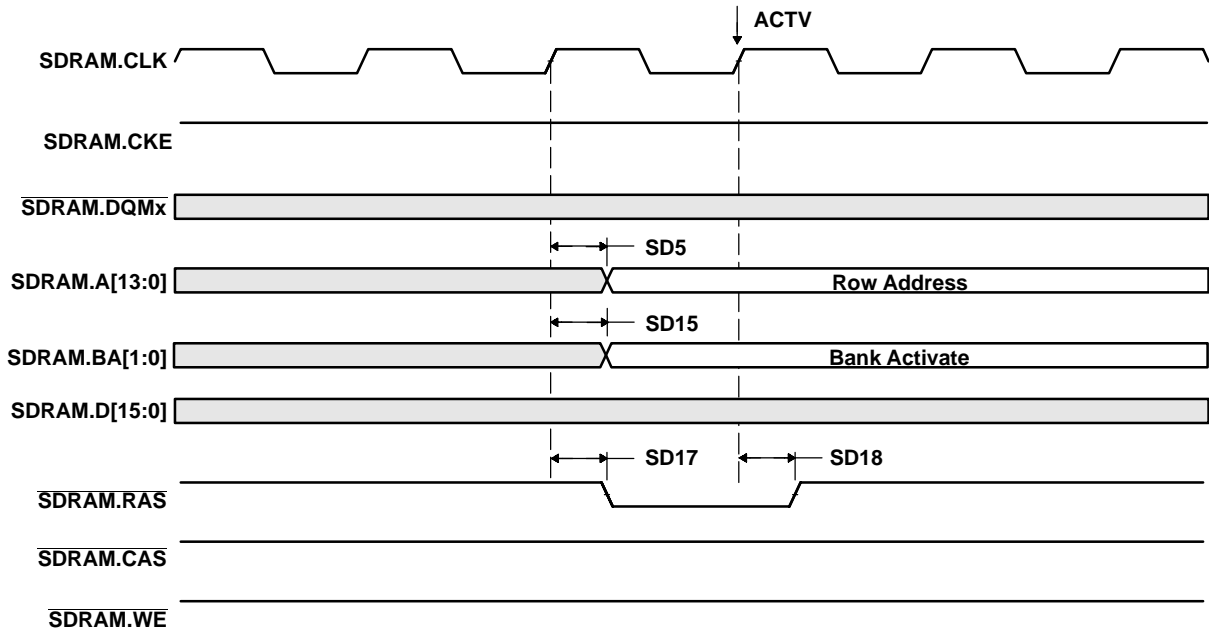


Figure 5–28. EMIFF/SDR SDRAM ACTV (Active Row) Command

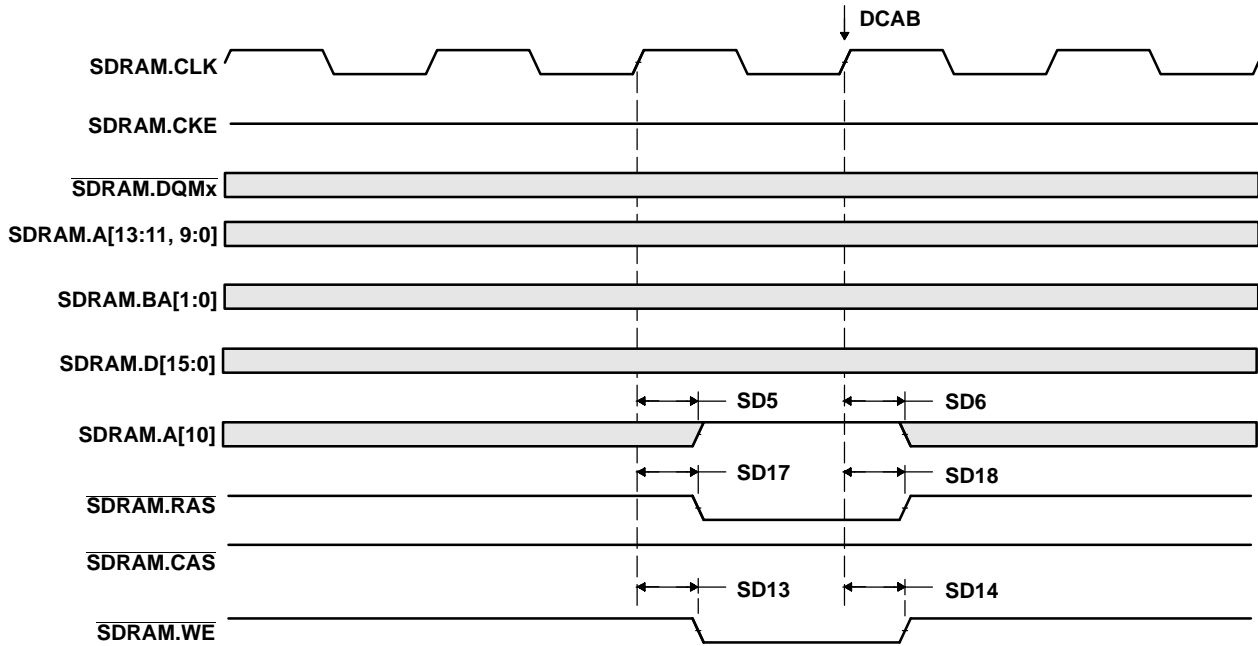


Figure 5–29. EMIFF/SDR SDRAM DCAB (Precharge/Deactivate Row) Command

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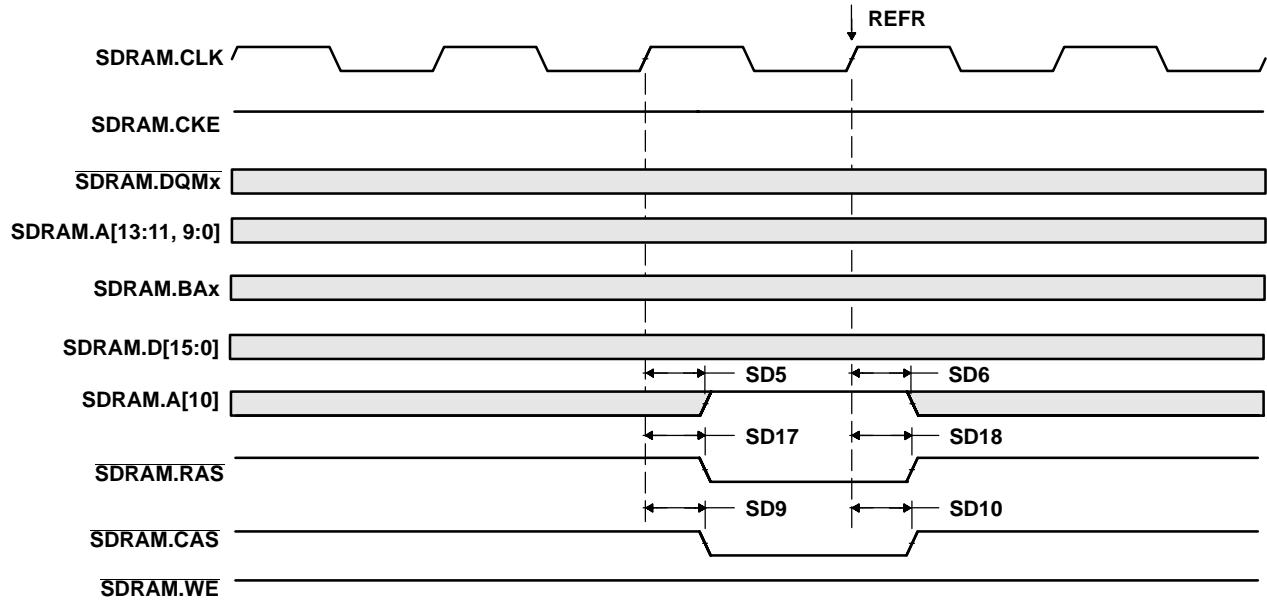


Figure 5–30. EMIFF/SDR SDRAM REFR (Refresh) Command

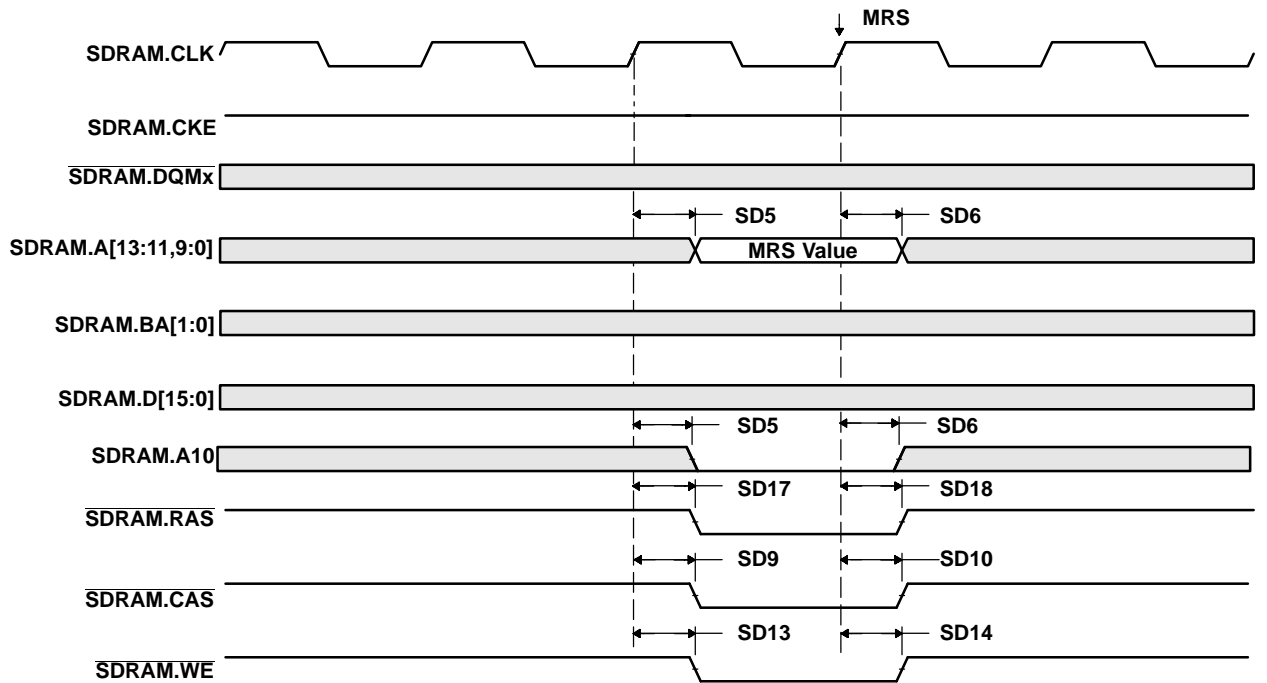


Figure 5–31. EMIFF/SDR SDRAM MRS (Mode Register Set) Command

5.11 EMIFF/DDR SDRAM Interface Timing

Table 5–19 and Table 5–20 assume testing over operating conditions (see Figure 5–32 through Figure 5–34).

Table 5–19. EMIFF/DDR SDRAM Interface Timing Requirements

NO.		DV _{DD4} = 1.8 V Nominal [†]		DV _{DD4} = 2.75 V Nominal [†]		DV _{DD4} = 3.3 V Nominal [†]		UNIT		
		MIN	MAX	MIN	MAX	MIN	MAX			
DD12	t _{d(DQSL/MH-DV)} ^{‡§} Delay time, SDRAM.DQSL/H input high to SDRAM.D[15:0] input data valid ^{‡§}	DLL phase [¶] = 72°		-0.2P	0.2P - 0.8	-0.2P	0.2P - 0.8	-0.2P	0.2P - 0.8	ns
		DLL phase [¶] = 90°		-0.25P	0.25P - 0.8	-0.25P	0.25P - 0.8	-0.25P	0.25P - 0.8	
DD13	t _{d(DQSL/ML-DV)} ^{‡§} Delay time, SDRAM.DQSL/H input low to SDRAM.D[15:0] input data valid ^{‡§}	DLL phase [¶] = 72°		-0.2P	0.2P - 0.8	-0.2P	0.2P - 0.8	-0.2P	0.2P - 0.8	ns
		DLL phase [¶] = 90°		-0.25P	0.25P - 0.8	-0.25P	0.25P - 0.8	-0.25P	0.25P - 0.8	

[†] Timing values are given for the CONF_VOLTAGE_SDRAM_R bit of the VOLTAGE_CTRL_0 register programmed as follows: 0 for 1.8 V, 1 for 2.75/3.3 V.

[‡] Delay time assumes that WRITE_OFFSET bits value = 0 (in the DLL_URD_CONTROL and DLL_LRD_CONTROL registers).

[§] P = SDRAM.CLK (CLKX) period. Delay time assumes that WRITE_OFFSET bits value = 0 (in the DLL_URD_CONTROL and DLL_LRD_CONTROL registers).

[¶] Defined in the EMIFF DLL Read Control Register (DLL_PHASE bit).

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Table 5–20. EMIFF/DDR SDRAM Interface Switching Characteristics

NO.	PARAMETER		DV _{DD4} = 1.8 V Nominal†		DV _{DD4} = 2.75 V Nominal†		DV _{DD4} = 3.3 V Nominal†		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
DD1	t _c (CLK)	Cycle time, SDRAM.CLK (CLKX)	10‡		10‡		10‡		ns
DD2	t _w (CLK)	Pulse duration, SDRAM.CLK (CLKX) high/low	4.5		4.5		4.5		ns
DD3	t _d (CLKH-CSV)	Delay time, SDRAM.CLK high to SDRAM.CS transition	3	7	3	7	3	7	ns
DD4	t _d (CLKH-CAS/RASL)	Delay time, SDRAM.CLK high to SDRAM.CAS/SDRAM.RAS low	3	7	3	7	3	7	ns
DD5	t _d (CLKH-CAS/RASH)	Delay time, SDRAM.CLK high to SDRAM.CAS/SDRAM.RAS high	3	7	3	7	3	7	ns
DD6	t _d (CLKH-BAV)	Delay time, SDRAM.CLK high to SDRAM.BA[1:0] valid	3	7	3	7	3	7	ns
DD7	t _d (CLKH-BAIV)	Delay time, SDRAM.CLK high to SDRAM.BA[1:0] invalid	3	7	3	7	3	7	ns
DD8	t _d (CLKH-AV)	Delay time, SDRAM.CLK high to SDRAM.A[13:0] valid	3	7	3	7	3	7	ns
DD9	t _d (CLKH-AIV)	Delay time, SDRAM.CLK high to SDRAM.A[13:0] invalid	3	7	3	7	3	7	ns
DD10	t _d (CLKH-WEL)	Delay time, SDRAM.CLK high to SDRAM.WE low	3	7	3	7	3	7	ns
DD11	t _d (CLKH-WEH)	Delay time, SDRAM.CLK high to SDRAM.WE high	3	7	3	7	3	7	ns
DD14	t _d (DQSL/HH-DV)	Delay time, SDRAM.DQSL/H high to SDRAM.D[15:0] data valid	DLL phase§ = 72°		0.2P + 1¶		0.2P + 1¶		ns
			DLL phase§ = 90°		0.25P + 1¶		0.25P + 1¶		
DD15	t _d (DQSL/HL-DV)	Delay time, SDRAM.DQSL/H low to SDRAM.D[15:0] data valid	DLL phase§ = 72°		0.2P + 0.8¶		0.2P + 0.8¶		ns
			DLL phase§ = 90°		0.25P + 0.8¶		0.25P + 0.8¶		
DD16	t _d (CLK-DQML/UV)	Delay time, SDRAM.CLK transition to SDRAM.DQML/U valid	1.3	1.3	1.3	1.3	1.3	1.3	ns
DD17	t _d (CLK-DQML/UIV)	Delay time, SDRAM.CLK transition to SDRAM.DQML/U invalid	1.3	1.3	1.3	1.3	1.3	1.3	ns

† Timing values are given for the CONF_VOLTAGE_SDRAM_R bit of the VOLTAGE_CTRL_0 register programmed as follows: 0 for 1.8 V, 1 for 2.75/3.3 V.

‡ The maximum EMIFF/SDRAM clock rate is limited to the maximum traffic controller clock rate for the OMAP5912.

§ Defined in the EMIFF DLL Write Control Register (DLL_PHASE bit).

¶ P = SDRAM.CLK (CLKX) period. Delay time assumes that WRITE_OFFSET bits value = 0 (in the DLL_URD_CONTROL and DLL_LRD_CONTROL registers).

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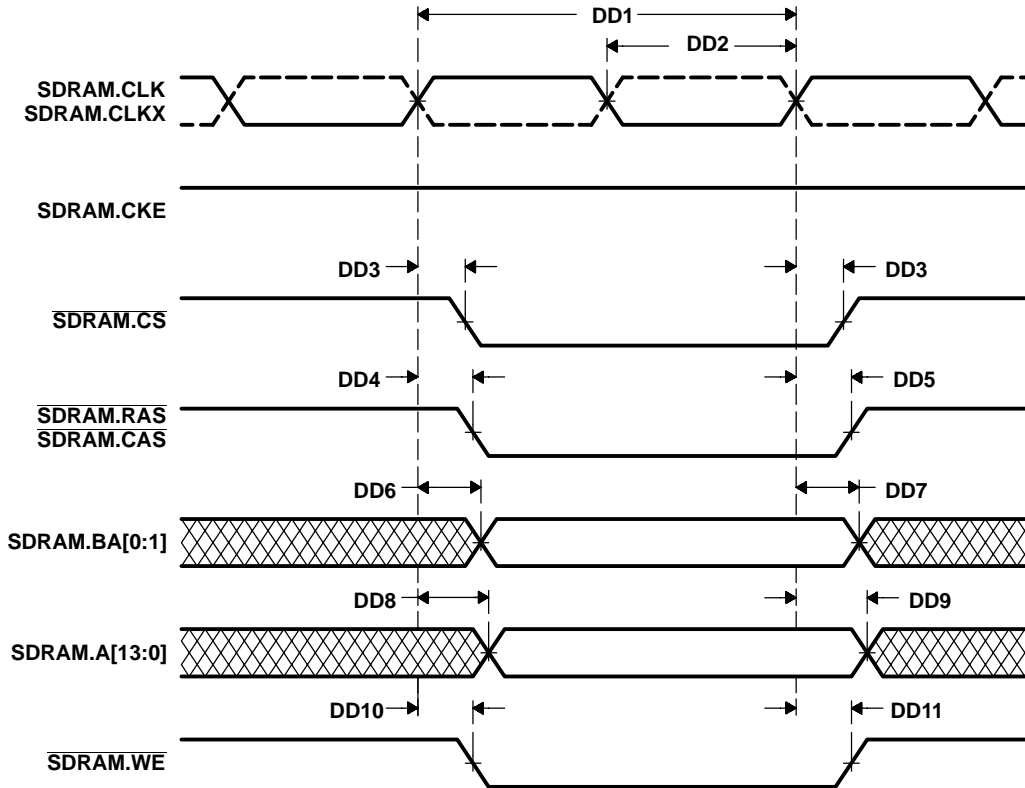
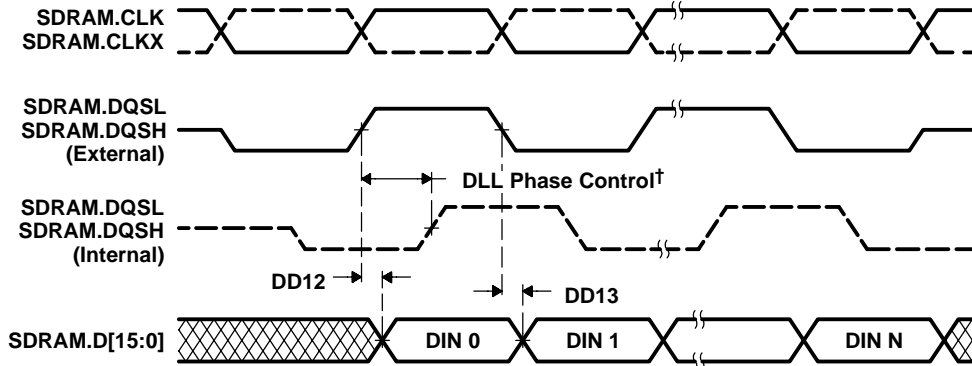
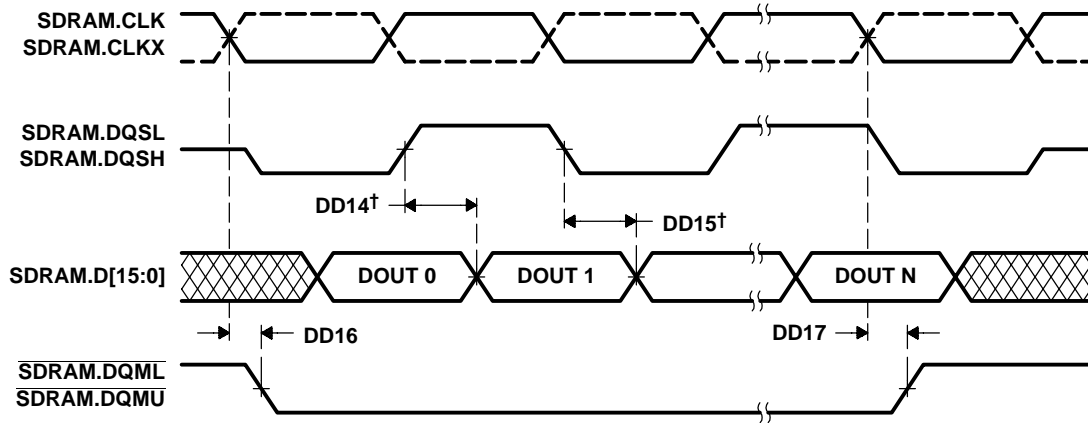


Figure 5–32. EMIFF/DDR SDRAM – Command and Address Output Timing Definition



† DQSL and DQSH internal delays are programmable in the EMIFF DLL_URD/LRD_CONTROL Register (72 to 90 degrees).

Figure 5–33. EMIFF/DDR SDRAM – Memory Read Timing



† This time includes the DLL phase effect on data, programmable in the EMIFF DLL Write Control Register (72 to 90 degrees), plus the device delay time (uncertainty).

Figure 5–34. EMIFF/DDR SDRAM – Memory Write Timing

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5.12 Multichannel Buffered Serial Port (McBSP) Timings

5.12.1 McBSP Transmit and Receive Timings

Table 5–21 and Table 5–22 assume testing over recommended operating conditions (see Figure 5–35 and Figure 5–36). In Table 5–21 and Table 5–22, “ext” indicates that the device pin is configured as an input (slave) driven by an external device and “int” indicates that the pin is configured as an output (master).

Table 5–21. McBSP Timing Requirements†‡

NO.				MIN	MAX	UNIT
M11	$t_c(\text{CKRX})$	Cycle time, CLKR/X	CLKR/X ext	2P		ns
M12	$t_w(\text{CKRX})$	Pulse duration, CLKR/X high or CLKR/X low	CLKR/X ext	0.45P		ns
M13	t_r	Rise time, CLKR/X, MCBSP2.FSR/X	McBSP1	CLKR/X ext	12	ns
			McBSP2	CLKR/X ext, MCBSP2.FSR/X ext	12	
			McBSP3	CLKR/X ext	6	
M14	t_f	Fall time, CLKR/X, MCBSP2.FSR/X	McBSP1	CLKR/X ext	12	ns
			McBSP2	CLKR/X ext, MCBSP2.FSR/X ext	12	
			McBSP3	CLKR/X ext	6	
M15	$t_{su}(\text{FRH-CKRL})$	Setup time, external receiver frame sync (FSR/X) high before CLKR/X low [§]	McBSP1 (FSR)	CLKX int [§]	17	ns
				CLKX ext [§]	20	
			McBSP2 (FSR)	CLKR int	17	
				CLKR ext	5	
			McBSP3 (FSX)	CLKX int [§]	16	
				CLKX ext [§]	10	
M16	$t_h(\text{CKRL-FRH})$	Hold time, external receiver frame sync (FSR/X) high after CLKR/X low [§]	McBSP1 (FSR)	CLKX int [§]	2	ns
				CLKX ext [§]	7	
			McBSP2 (FSR)	CLKR int	2	
				CLKR ext	2	
			McBSP3 (FSX)	CLKX int [§]	9	
				CLKX ext [§]	9	
M17	$t_{su}(\text{DRV-CKRL})$	Setup time, DR valid before CLKR/X low [§]	McBSP1	CLKX int [§]	14	ns
				CLKX ext [§]	2	
			McBSP2	CLKR int	15	
				CLKR ext	2	
			McBSP3	CLKX int [§]	13	
				CLKX ext [§]	7	

† Polarity bits CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.

‡ P = 1/(DSPPER_CK or DSPXOR_CK) for McBSP1 and McBSP3, or 1/(ARMPER_CK clock frequency) in nanoseconds (ns) for McBSP2.

§ For McBSP1 and McBSP3, the receiver clock and frame sync inputs are driven by FSX and CLKX via internal loopback connections enabled via software configuration.

Table 5–21. McBSP Timing Requirements^{†‡} (Continued)

NO.				MIN	MAX	UNIT
M18	$t_{h(CKRL-DRV)}$	Hold time, DR valid after CLKR/X low [§]	McBSP1	CLKX int [§]	2	ns
				CLKX ext [§]	2	
			McBSP2	CLKR int	2	
				CLKR ext	2	
			McBSP3	CLKX int [§]	2	
				CLKX ext [§]	2	
M19	$t_{su(FXH-CKXL)}$	Setup time, external FSX high before CLKX low	McBSP1	CLKX int	20	ns
				CLKX ext	17	
			McBSP2	CLKX int	19	
				CLKX ext	18	
			McBSP3	CLKX int	19	
				CLKX ext	18	
M20	$t_{h(CKXL-FXH)}$	Hold time, external FSX high after CLKX low	McBSP1	CLKX int	2	ns
				CLKX ext	7	
			McBSP2	CLKR int	2	
				CLKR ext	2	
			McBSP3	CLKX int	2	
				CLKX ext	2	

[†] Polarity bits CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.

[‡] $P = 1 / (\text{DSPPER_CK or DSPXOR_CK})$ for McBSP1 and McBSP3, or $1 / (\text{ARMPER_CK clock frequency})$ in nanoseconds (ns) for McBSP2.

[§] For McBSP1 and McBSP3, the receiver clock and frame sync inputs are driven by FSX and CLKX via internal loopback connections enabled via software configuration.

Table 5–22. McBSP Switching Characteristics†‡§

NO.	PARAMETER			MIN	MAX	UNIT	
M0	$t_{d(CKSH-CKRXH)}$	Delay time, CLKS high to CLKR/X high for internal CLKR/X generated from CLKS input	McBSP1	CLKR/X int	4	22	ns
M1	$t_c(CKRX)$	Cycle time, CLKR/X		CLKR/X int	2P		ns
M2	$t_w(CKRXH)$	Pulse duration, CLKR/X high		CLKR/X int	0.90D	1.10D	ns
M3	$t_w(CKRXL)$	Pulse duration, CLKR/X low		CLKR/X int	0.90C	1.10C	ns
M4	$t_{d(CKRH-FRV)}$	Delay time, CLKR high to internal FSR valid	McBSP2	CLKR int	-1	9	ns
				CLKR ext	-4	10	
M5	$t_{d(CKXH-FXV)}$	Delay time, CLKX high to internal FSX valid	McBSP1	CLKX int	-2	9	ns
				CLKX ext	5	26	
			McBSP2	CLKX int	0	3	
				CLKX ext	5	16	
			McBSP3	CLKX int	-1	6	
				CLKX ext	5	25	
M7	$t_{d(CKXH-DXV)}$	Delay time, CLKX high to DX valid. This applies to all bits except the first bit transmitted when in Data Delay 0 (XDATDLY = 00b) mode.	McBSP1	CLKX int	-1	5	ns
				CLKX ext	5	27	
			McBSP2	CLKX int	1	7	
				CLKX ext	6	18	
			McBSP3	CLKX int	-1	7	
				CLKX ext	2	11	
M9	$t_{d(FXH-DXV)}$	Delay time, FSX high to DX valid.¶ Only applies to first bit transmitted when in Data Delay 0 (XDATDLY = 00b) mode.	McBSP1	FSX int		19	ns
				FSX ext		17	
			McBSP2	FSX int		20	
				FSX ext		18	
			McBSP3	FSX int		7	
				FSX ext		18	

† Polarity bits CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.

‡ P = 1/(DSPPER_CK or DSPXOR_CK) for McBSP1 and McBSP3, or 1/(ARMPER_CK clock frequency) in nanoseconds (ns) for McBSP2.

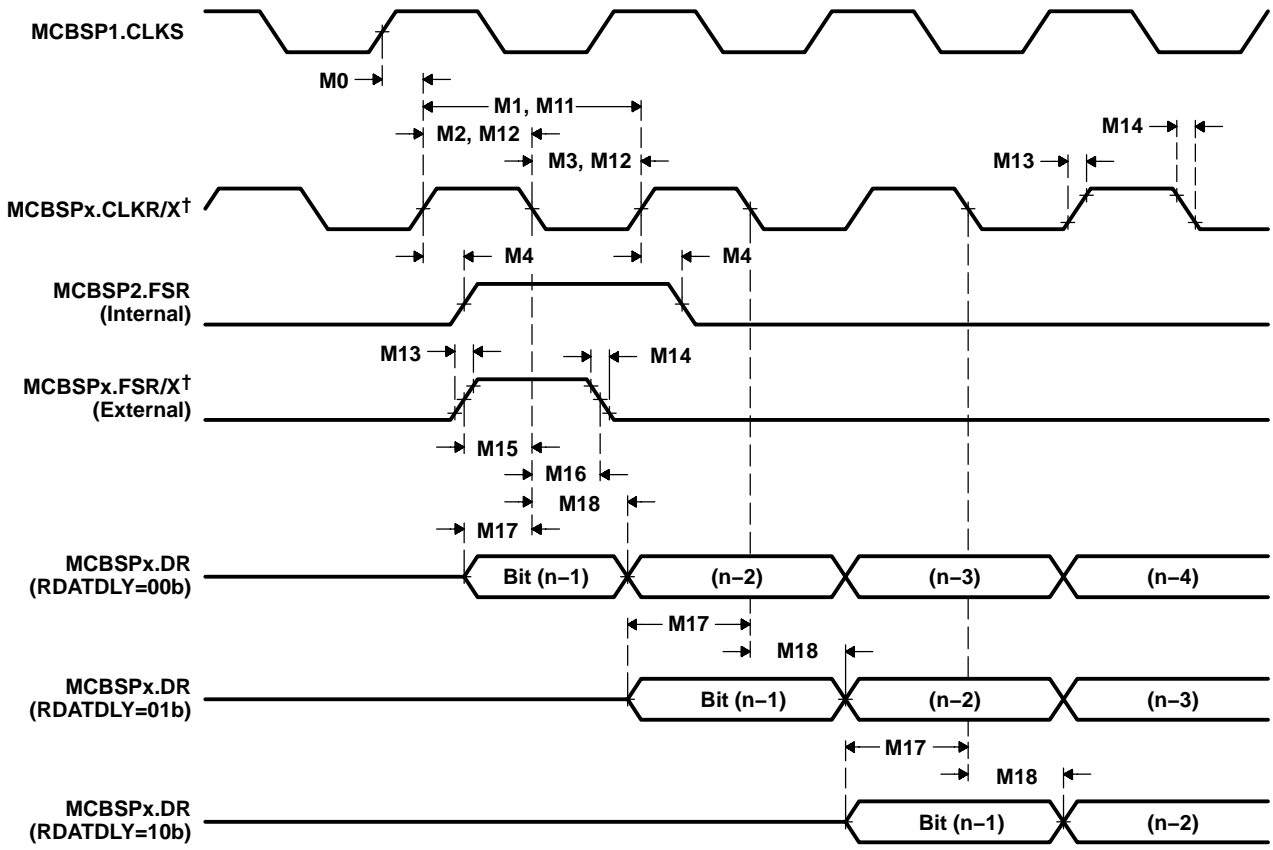
§ T = CLKRX period = (1 + CLKGDV) * P

C = CLKRX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) * P when CLKGDV is even

D = CLKRX high pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2 + 1) * P when CLKGDV is even

¶ Only DXENA = 0 is supported.

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† For McBSP1 and McBSP3, the receiver clock and frame sync inputs are driven by FSX and CLKX via internal loopback connections enabled via software configuration. The M13 and M14 descriptors are applicable only to McBSP2.

Figure 5–35. McBSP Receive Timings

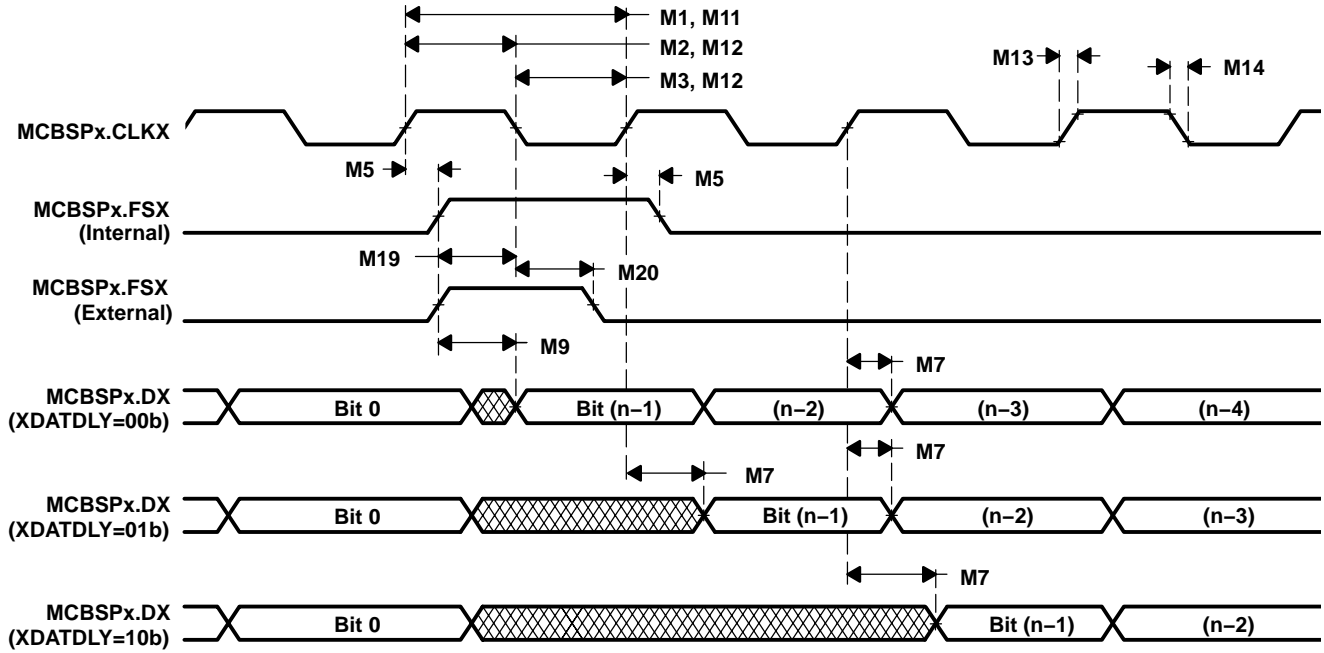


Figure 5-36. McBSP Transmit Timings

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5.12.2 McBSP as SPI Master or Slave Timings

Table 5–23 to Table 5–30 assume testing over recommended operating conditions (see Figure 5–37 to Figure 5–40).

Table 5–23. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 10b, CLKXP = 0)^{†‡}

NO.		MASTER		SLAVE		UNIT
		MIN	MAX	MIN	MAX	
M30	$t_{su}(DRV-CKXL)$ Setup time, MCBSPx.DR valid before MCBSPx.CLKX low	15		2 – 6P		ns
M31	$t_h(CKXL-DRV)$ Hold time, MCBSPx.DR valid after MCBSPx.CLKX low	2		6 + 6P		ns
M32	$t_{su}(BFXL-CKXH)$ Setup time, MCBSPx.FSX low before MCBSPx.CLKX high	McBSP1		20		ns
		McBSP2		5		
		McBSP3		15		
M33	$t_c(CKX)$ Cycle time, MCBSPx.CLKX	2P		16P		ns

[†] For all SPI slave modes, CLKG is programmed as 1/2 of the internal reference clock by setting CLKSM = CLKGDV = 1.

[‡] P = 1/(DSPPER_CK or DSPXOR_CK) for McBSP1 and McBSP3, or 1/(ARMPER_CK clock frequency) in nanoseconds (ns) for McBSP2.

Table 5–24. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 10b, CLKXP = 0)^{†‡§}

NO.	PARAMETER	MASTER		SLAVE		UNIT
		MIN	MAX	MIN	MAX	
M24	$t_h(CKXL-FXL)$ Hold time, MCBSPx.FSX low after MCBSPx.CLKX low [¶]	0.45T	0.55T			ns
M25	$t_d(FXL-CKXH)$ Delay time, MCBSPx.FSX low to MCBSPx.CLKX high [#]	0.45C	0.55C			ns
M26	$t_d(CKXH-DXV)$ Delay time, MCBSPx.CLKX high to MCBSPx.DX valid	-1	7	3P + 2	5P + 18	ns
M29	$t_d(FXL-DXV)$ Delay time, MCBSPx.FSX low to MCBSPx.DX valid				4P + 18	ns

[†] For all SPI slave modes, CLKG is programmed as 1/2 of the internal reference clock by setting CLKSM = CLKGDV = 1.

[‡] P = 1/(DSPPER_CK or DSPXOR_CK) for McBSP1 and McBSP3, or 1/(ARMPER_CK clock frequency) in nanoseconds (ns) for McBSP2.

[§] T = CLKX period = (1 + CLKGDV) * P

C = CLKX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) * P when CLKGDV is even.

[¶] FSRP = FSXP = 1. As a SPI master, MCBSPx.FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on MCBSPx.FSX and MCBSPx.FSR is inverted before being used internally.

CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP

CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP

[#] MCBSPx.FSX must be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (MCBSPx.CLKX).

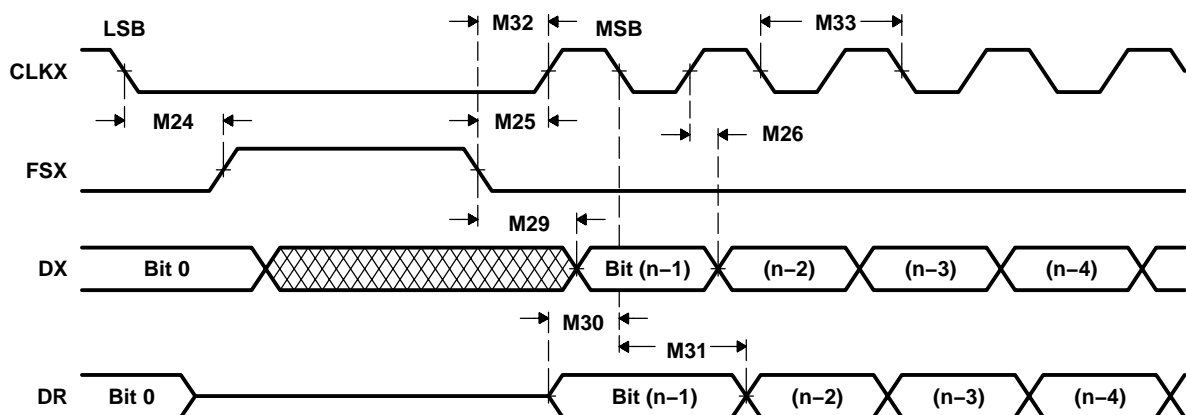


Figure 5–37. McBSP Timings as SPI Master or Slave: CLKSTP = 10b, CLKXP = 0

Table 5–25. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 11b, CLKXP = 0)†‡

NO.		MASTER		SLAVE		UNIT
		MIN	MAX	MIN	MAX	
M39	$t_{su(DRV-CKXH)}$ Setup time, MCBSPx.DR valid before MCBSPx.CLKX high	15		2 – 6P		ns
M40	$t_h(CKXH-DRV)$ Hold time, MCBSPx.DR valid after MCBSPx.CLKX high	2		6 + 6P		ns
M41	$t_{su(FXL-CKXH)}$ Setup time, MCBSPx.FSX low before MCBSPx.CLKX high	McBSP1		20		ns
		McBSP2		5		
		McBSP3		15		
M42	$t_c(CKX)$ Cycle time, MCBSPx.CLKX	2P		16P		ns

† For all SPI slave modes, CLKG is programmed as 1/2 of the internal reference clock by setting CLKSM = CLKGDV = 1.
 ‡ P = 1/(DSPPER_CK or DSPXOR_CK) for McBSP1 and McBSP3, or 1/(ARMPER_CK clock frequency) in nanoseconds (ns) for McBSP2.

Table 5–26. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 11b, CLKXP = 0)†‡§

NO.	PARAMETER	MASTER		SLAVE		UNIT
		MIN	MAX	MIN	MAX	
M34	$t_h(CKXL-FXL)$ Hold time, MCBSPx.FSX low after MCBSPx.CLKX low¶	0.45T	0.55T			ns
M35	$t_d(FXL-CKXH)$ Delay time, MCBSPx.FSX low to MCBSPx.CLKX high#	0.45C	0.55C			ns
M36	$t_d(CKXL-DXV)$ Delay time, MCBSPx.CLKX low to MCBSPx.DX valid	-1	7	3P + 2	5P + 18	ns
M38	$t_d(FXL-DXV)$ Delay time, MCBSPx.FSX low to MCBSPx.DX valid		D + 20		4P + 18	ns

† For all SPI slave modes, CLKG is programmed as 1/2 of the internal reference clock by setting CLKSM = CLKGDV = 1.
 ‡ P = 1/(DSPPER_CK or DSPXOR_CK) for McBSP1 and McBSP3, or 1/(ARMPER_CK clock frequency) in nanoseconds (ns) for McBSP2.
 § T = CLKX period = (1 + CLKGDV) * P
 C = CLKX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) * P when CLKGDV is even.
 D = CLKX high pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2 + 1) * P when CLKGDV is even.
 ¶ FSRP = FSXP = 1. As a SPI master, MCBSPx.FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on MCBSPx.FSX and MCBSPx.FSR is inverted before being used internally.
 CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
 CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
 # MCBSPx.FSX must be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (MCBSPx.CLKX).

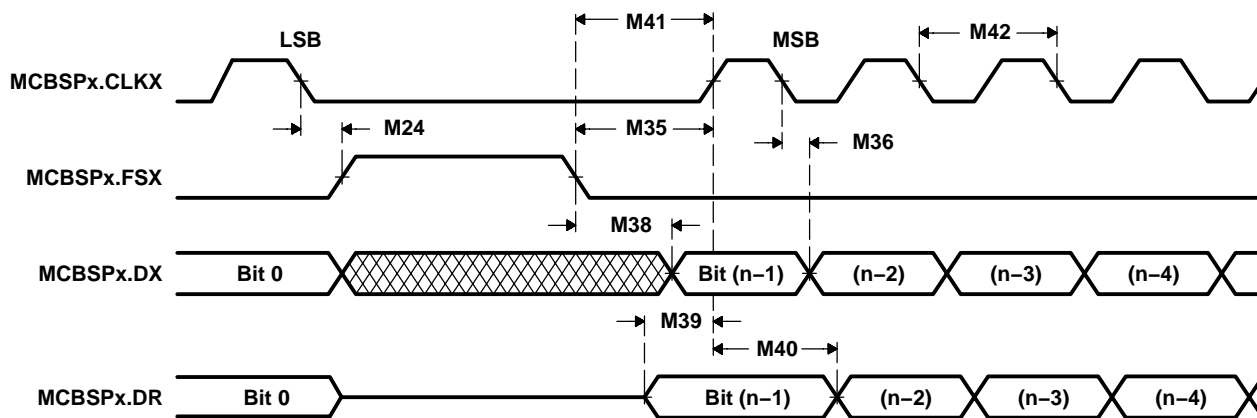


Figure 5–38. McBSP Timings as SPI Master or Slave: CLKSTP = 11b, CLKXP = 0

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Table 5–27. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 10b, CLKXP = 1)†‡

NO.		MASTER		SLAVE		UNIT
		MIN	MAX	MIN	MAX	
M49	$t_{su}(DRV-CKXH)$ Setup time, MCBSPx.DR valid before MCBSPx.CLKX high	15		2 – 6P		ns
M50	$t_h(CKXH-DRV)$ Hold time, MCBSPx.DR valid after MCBSPx.CLKX high	2		6 + 6P		ns
M51	$t_{su}(FXL-CKXL)$ Setup time, MCBSPx.FSX low before MCBSPx.CLKX low	McBSP1		20		ns
		McBSP2		5		
		McBSP3		15		
M52	$t_c(CKX)$ Cycle time, MCBSPx.CLKX	2P		16P		ns

† For all SPI slave modes, CLKG is programmed as 1/2 of the internal reference clock by setting CLKSM = CLKGDV = 1.

‡ P = 1/(DSPPER_CK or DSPXOR_CK) for McBSP1 and McBSP3, or 1/(ARMPER_CK clock frequency) in nanoseconds (ns) for McBSP2.

Table 5–28. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 10b, CLKXP = 1)†‡§

NO.	PARAMETER	MASTER		SLAVE		UNIT
		MIN	MAX	MIN	MAX	
M43	$t_h(CKXH-FXL)$ Hold time, MCBSPx.FSX low after MCBSPx.CLKX high¶	0.45T	0.55T			ns
M44	$t_d(FXL-CKXL)$ Delay time, MCBSPx.FSX low to MCBSPx.CLKX low#	0.45D	0.55D			ns
M45	$t_d(CKXL-DXV)$ Delay time, MCBSPx.CLKX low to MCBSPx.DX valid	-1	7	3P + 2	5P + 18	ns
M48	$t_d(FXL-DXV)$ Delay time, MCBSPx.FSX low to MCBSPx.DX valid				4P + 18	ns

† For all SPI slave modes, CLKG is programmed as 1/2 of the internal reference clock by setting CLKSM = CLKGDV = 1.

‡ P = 1/(DSPPER_CK or DSPXOR_CK) for McBSP1 and McBSP3, or 1/(ARMPER_CK clock frequency) in nanoseconds (ns) for McBSP2.

§ T = CLKX period = (1 + CLKGDV) * P

D = CLKX high pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2 + 1) * P when CLKGDV is even.

¶ FSRP = FSXP = 1. As a SPI master, MCBSPx.FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on MCBSPx.FSX and MCBSPx.FSR is inverted before being used internally.

CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP

CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP

MCBSPx.FSX must be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (MCBSPx.CLKX).

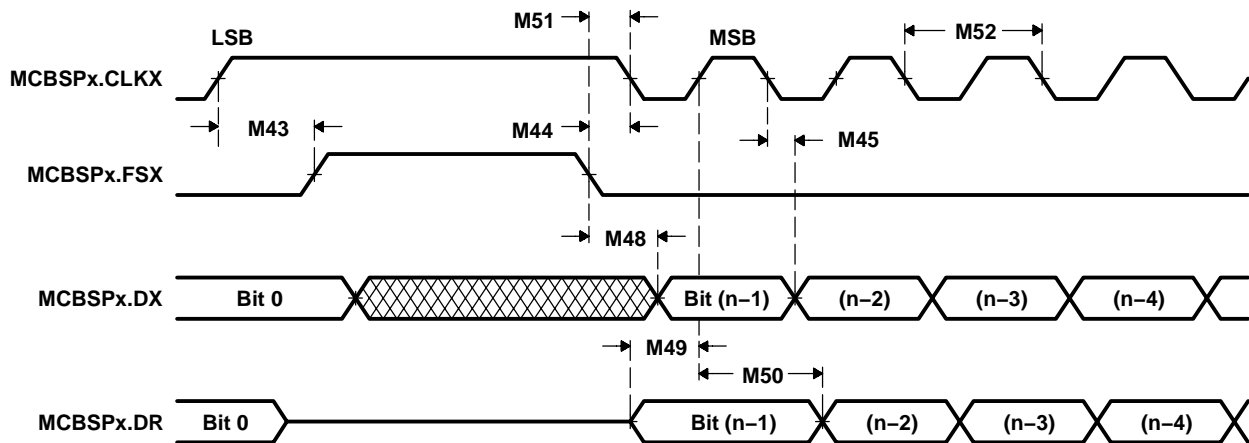


Figure 5–39. McBSP Timings as SPI Master or Slave: CLKSTP = 10b, CLKXP = 1

Table 5–29. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 11b, CLKXP = 1)†‡

NO.		MASTER		SLAVE		UNIT
		MIN	MAX	MIN	MAX	
M58	$t_{su(DRV-CKXL)}$ Setup time, MCBSPx.DR valid before MCBSPx.CLKX low	15		2 – 6P		ns
M59	$t_h(CKXL-DRV)$ Hold time, MCBSPx.DR valid after MCBSPx.CLKX low	2		6 + 6P		ns
M60	$t_{su(FXL-CKXL)}$ Setup time, MCBSPx.FSX low before MCBSPx.CLKX low	McBSP1		20		ns
		McBSP2		5		
		McBSP3		15		
M61	$t_c(CKX)$ Cycle time, MCBSPx.CLKX	2P		16P		ns

† For all SPI slave modes, CLKG is programmed as 1/2 of the internal reference clock by setting CLKSM = CLKGDV = 1.
 ‡ P = 1/(DSPPER_CK or DSPXOR_CK) for McBSP1 and McBSP3, or 1/(ARMPER_CK clock frequency) in nanoseconds (ns) for McBSP2.

Table 5–30. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 11b, CLKXP = 1)†‡§

NO.	PARAMETER	MASTER		SLAVE		UNIT
		MIN	MAX	MIN	MAX	
M53	$t_h(CKXH-FXL)$ Hold time, MCBSPx.FSX low after MCBSPx.CLKX high [¶]	0.45D	0.55D			ns
M54	$t_d(FXL-CKXL)$ Delay time, MCBSPx.FSX low to MCBSPx.CLKX low [#]	0.45T	0.55T			ns
M55	$t_d(CKXH-DXV)$ Delay time, MCBSPx.CLKX high to MCBSPx.DX valid	-1	7	3P + 2	5P + 18	ns
M57	$t_d(FXL-DXV)$ Delay time, MCBSPx.FSX low to MCBSPx.DX valid		C + 20		4P + 18	ns

† For all SPI slave modes, CLKG is programmed as 1/2 of the internal reference clock by setting CLKSM = CLKGDV = 1.
 ‡ P = 1/(DSPPER_CK or DSPXOR_CK) for McBSP1 and McBSP3, or 1/(ARMPER_CK clock frequency) in nanoseconds (ns) for McBSP2.
 § T = CLKX period = (1 + CLKGDV) * P
 C = CLKX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) * P when CLKGDV is even.
 D = CLKX high pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2 + 1) * P when CLKGDV is even.
 ¶ FSRP = FSXP = 1. As a SPI master, MCBSPx.FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on MCBSPx.FSX and MCBSPx.FSR is inverted before being used internally.
 CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
 CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
 # MCBSPx.FSX must be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (MCBSPx.CLKX).

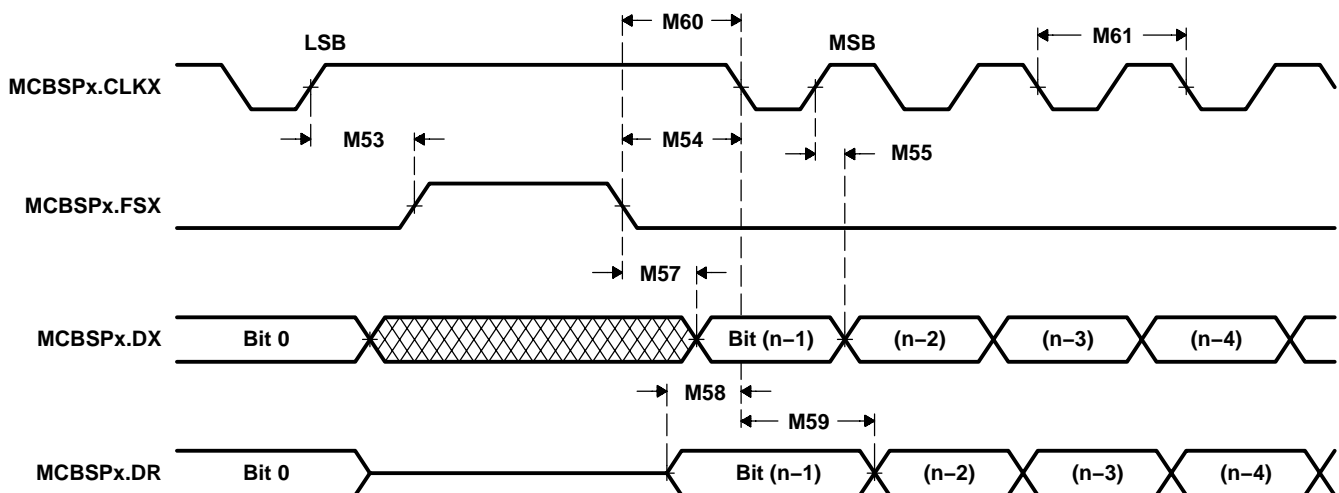


Figure 5–40. McBSP Timings as SPI Master or Slave: CLKSTP = 11b, CLKXP = 1

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5.13 Multichannel Serial Interface (MCSI)

Table 5–31 and Table 5–32 assume testing over recommended operating conditions (see Figure 5–41 and Figure 5–42).

Table 5–31. MCSI Timing Requirements

NO.	PARAMETER		MIN	MAX	UNIT
MC11	$f_{op}(CLK)$	Operating frequency, MCSIx.CLK		B^{\ddagger}	MHz
MC12	$t_w(CLKH)$	Pulse duration, MCSIx.CLK high	$0.45P^{\dagger}$	$0.55P^{\dagger}$	ns
MC13	$t_w(CLKL)$	Pulse duration, MCSIx.CLK low	$0.45P^{\dagger}$	$0.55P^{\dagger}$	ns
MC14	$t_r(CLK)$	Rise time, MCSIx.CLK		12	ns
MC15	$t_f(CLK)$	Fall time, MCSIx.CLK		12	ns
MC16	$t_{su}(FSH-CLKL)$	Setup time, external MCSIx.SYNC high before MCSIx.CLK low	12		ns
MC17	$t_h(CLKL-FSH)$	Hold time, external MCSIx.SYNC high after MCSIx.CLK low	3,5		ns
MC18	$t_{su}(DIV-CLKL)$	Setup time, MCSIx.DIN valid before MCSIx.CLK low	Master	18	ns
			Slave	12	
MC19	$t_h(CLKL-DIV)$	Hold time, MCSIx.DIN valid after MCSIx.CLK low	Master	0	ns
			Slave	0	

\dagger P = MCSIx.CLK period [$t_c(CLK)$] in nanoseconds.

\ddagger B = Base frequency for OMAP5912 (12,13, or 19.2 MHz).

Table 5–32. MCSI Switching Characteristics

NO.	PARAMETER		MIN	MAX	UNIT
MC1	$f_{op}(CLK)$	Operating frequency, MCSIx.CLK		$0.5B^{\ddagger}$	MHz
MC2	$t_w(CLKH)$	Pulse duration, MCSIx.CLK high	$0.45P^{\dagger}$	$0.55P^{\dagger}$	ns
MC3	$t_w(CLKL)$	Pulse duration, MCSIx.CLK low	$0.45P^{\dagger}$	$0.55P^{\dagger}$	ns
MC4	$t_d(CLKH-FS)$	Delay time, MCSIx.CLK high to MCSIx.SYNC transition	0	3	ns
MC7	$t_d(CLKH-DOV)$	Delay time, MCSIx.CLK high to MCSIx.DOUT valid	Master	0,5	ns
			Slave	6	
MC8	$t_{en}(CLKH-DO)$	Enable time, MCSIx.DOUT driven from MCSIx.CLK high	Master	0,5	ns
			Slave	6	

\dagger P = MCSIx.CLK period [$t_c(CLK)$] in nanoseconds.

\ddagger B = Base frequency for OMAP5912 (12,13, or 19.2 MHz).

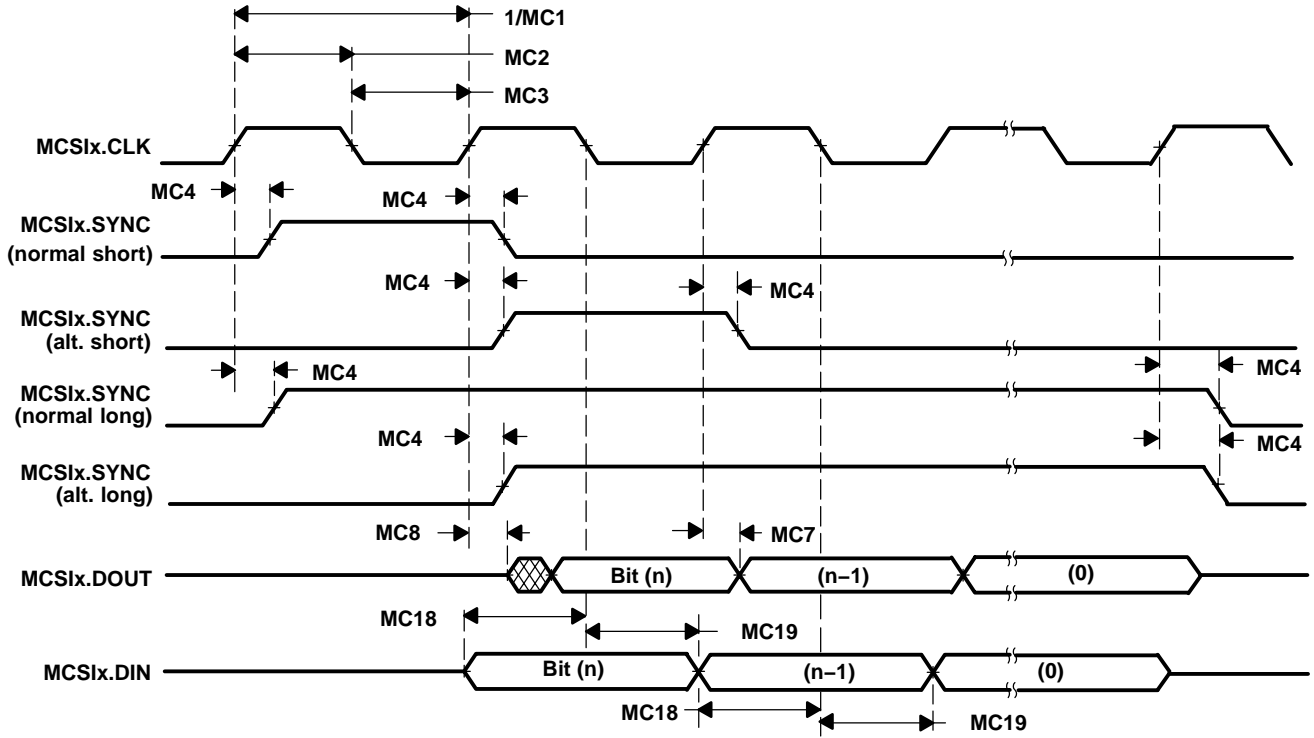


Figure 5-41. MCSI Master Mode Timings

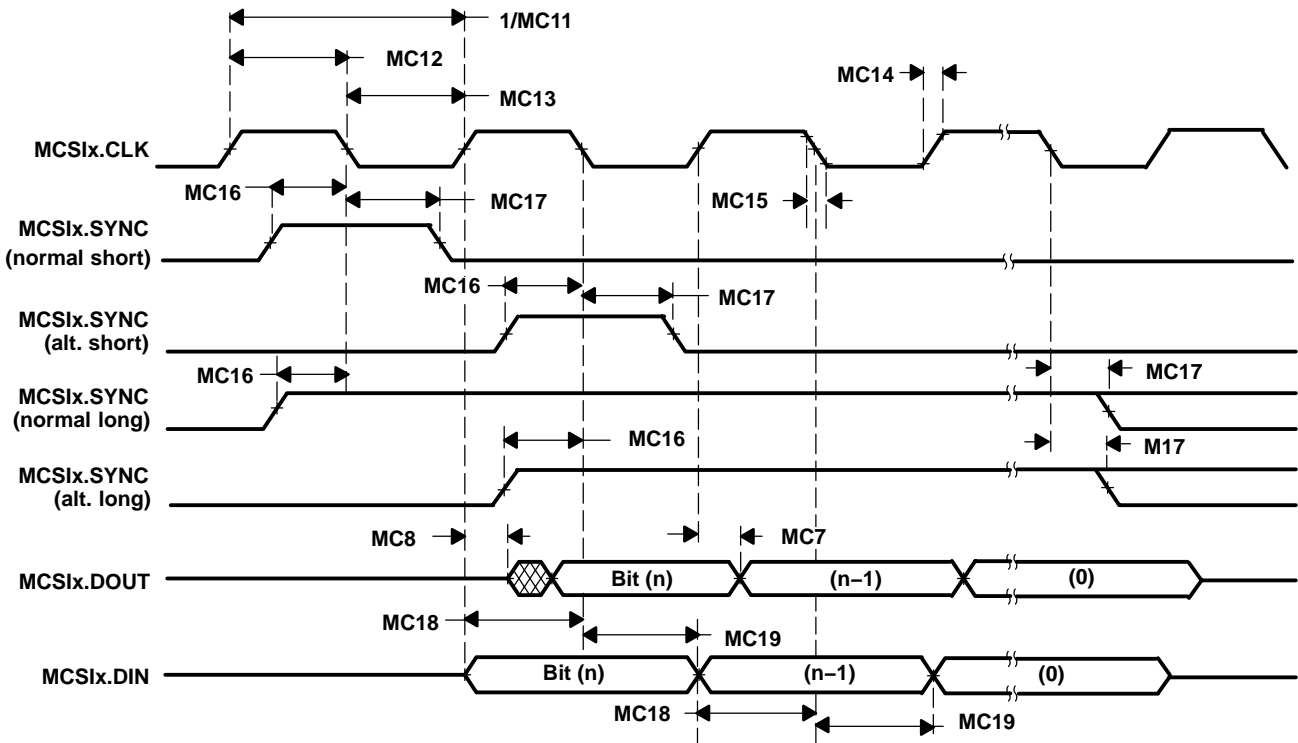


Figure 5-42. MCSI Slave Mode Timings

5.14 Serial Port Interface (SPI) Timings

Table 5–33 and Table 5–34 assume testing over recommended operating conditions (see Figure 5–43).

Table 5–33. SPI Interface Timing Requirements

NO.		MIN	MAX	UNIT
SPI6	$t_{su(DV-CLKH)}$ Setup time, SPIF.DIN valid before SPIF.SCK active edge [†]	0		ns
SPI7	$t_h(CLKH-DV)$ Hold time, SPIF.DIN invalid after SPIF.SCK active edge [†]	15		ns

[†] Polarity of SPIF.SCK and the active clock edge (rising or falling) on which DOUT is driven and DIN data is latched is all software-configurable. These timings apply to all configurations regardless of SPIF.SCK polarity and which clock edges are used to drive output data and capture input data.

Table 5–34. SPI Interface Switching Characteristics

NO.	PARAMETER	MIN	MAX	UNIT
SPI1	$1/t_{op(SCLK)}$ Operating frequency, SPIF.SCK		B [‡]	MHz
SPI2	$t_w(SCLKH)$ Pulse duration, SPIF.SCK high	0.45P [§]	0.55P [§]	ns
SPI3	$t_w(SCLKL)$ Pulse duration, SPIF.SCK low	0.45P [§]	0.55P [§]	ns
SPI4	$t_d(CS-SCLK)$ Delay time, $\overline{SPIF.CSx}$ active to SPIF.SCK active in master mode	2	5	ns
SPI5	$t_d(SCLK-DOUT)$ Delay time, SPIF.SCK active edge to SPIF.DOUT transition [§]	2	5	ns

[‡] B = system clock frequency of OMAP5912 (12, 13, or 19.2 MHz)

[§] P = period of SPIF.SCK in nanoseconds (ns).

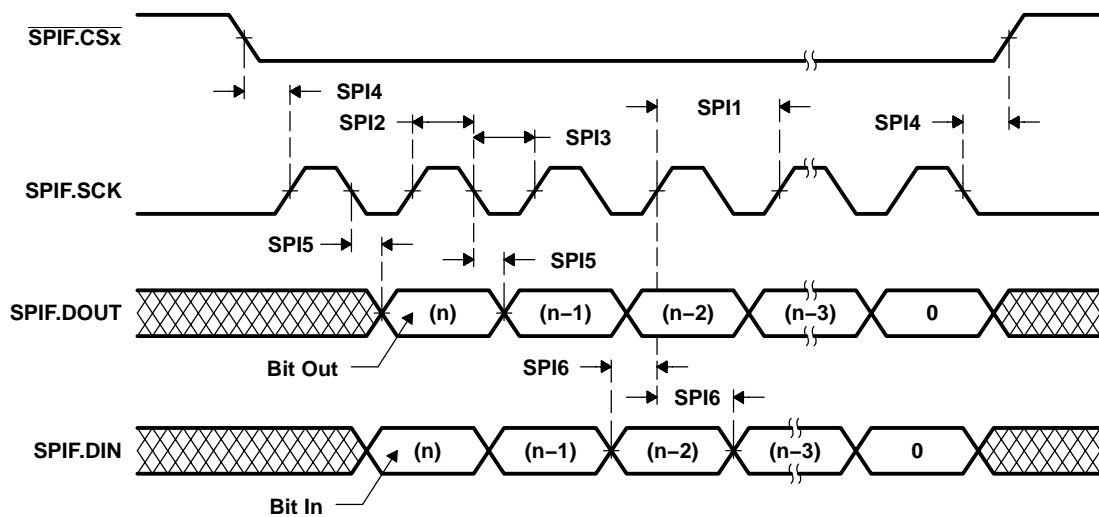


Figure 5–43. SPI Interface – Transmit and Receive in Master or Slave Timings

5.15 VLYNQ Interface Timings

5.15.1 VLYNQ Slave Mode (External Clock Source)

Table 5–35 and Table 5–36 assume testing over recommended operating conditions.

Table 5–35. VLYNQ as Slave Timing Requirements

NO.		MIN	MAX	UNIT
V1	$t_{c}(\text{CLK})$ Clock period, VLYNQ.CLK	12.5		ns
V2	$t_{w}(\text{CLKH})$ Pulse duration, VLYNQ.CLK high	TBD [†]		ns
V3	$t_{w}(\text{CLKL})$ Pulse duration, VLYNQ.CLK low	TBD [†]		ns
V6	$t_{su}(\text{RXV-CLKH})$ Setup time, VLYNQ.RX[1:0] valid before VLYNQ.CLK high	–0.65		ns
V7	$t_{h}(\text{CLKH-DV})$ Hold time, VLYNQ.RX[1:0] valid after VLYNQ.CLK high	2.2		ns
V8	$t_{r}(\text{RXCLKH})$ Rise time, VLYNQ.RX[1:0] and VLYNQ.CLK		TBD	ns
V9	$t_{f}(\text{RXCLKL})$ Fall time, VLYNQ.RX[1:0] and VLYNQ.CLK		TBD	ns

[†] P = period of VLYNQ.CLK in nanoseconds (ns).

Table 5–36. VLYNQ as Slave Switching Characteristics

NO.	PARAMETER	MIN	MAX	UNIT
V4	$t_{d}(\text{CLKH-TXV})$ Delay time, VLYNQ.CLK high to VLYNQ.TX[1:0] valid [‡]		11.3	ns
V5	$t_{d}(\text{CLKH-TXIV})$ Delay time, VLYNQ.CLK high to VLYNQ.TX[1:0] invalid	4		ns
V10	$t_{r}(\text{TXH})$ Rise time, VLYNQ.TX[1:0]		TBD	ns
V11	$t_{f}(\text{TXLL})$ Fall time, VLYNQ.TX[1:0]		TBD	ns

[‡] Maximum pin loading is assumed to be 15 pF (used for maximum VLYNQ_CLK to VLYNQ_TXD valid delay time).

5.15.2 VLYNQ Master Mode (Internal Clock Source)

Table 5–37 and Table 5–38 assume testing over recommended operating conditions (see Figure 5–44).

Table 5–37. VLYNQ as Master Timing Requirements

NO.		MIN	MAX	UNIT
V6	$t_{su(RXV-CLKH)}$ Setup time, VLYNQ.RX[1:0] valid before VLYNQ.CLK high	-0.65		ns
V7	$t_{h(CLKH-DV)}$ Hold time, VLYNQ.RX[1:0] valid after VLYNQ.CLK high	1.75		ns
V8	$t_{r(RXH)}$ Rise time, VLYNQ.RX[1:0] and VLYNQ.CLK		TBD	ns
V9	$t_{f(RXL)}$ Fall time, VLYNQ.RX[1:0] and VLYNQ.CLK		TBD	ns

Table 5–38. VLYNQ as Master Switching Characteristics

NO.	PARAMETER	MIN	MAX	UNIT
V1	$t_{c(CLK)}$ Clock period, VLYNQ.CLK	10		ns
V2	$t_{w(CLKH)}$ Pulse duration, VLYNQ.CLK high	TBD [†]	TBD [†]	ns
V3	$t_{w(CLKL)}$ Pulse duration, VLYNQ.CLK low	TBD [†]	TBD [†]	ns
V4	$t_{d(CLKH-TXV)}$ Delay time, VLYNQ.CLK high to VLYNQ.TX[1:0] valid [‡]		8	ns
V5	$t_{d(CLKH-TXIV)}$ Delay time, VLYNQ.CLK high to VLYNQ.TX[1:0] invalid	2.5		ns
V12	$t_{j(CLK)}$ Cycle-to-cycle jitter, VLYNQ.CLK		TBD	ps

[†] P = period of VLYNQ.CLK in nanoseconds (ns).

[‡] Maximum pin loading is assumed to be 15 pF (used for maximum VLYNQ_CLK to VLYNQ_TXD valid delay time).

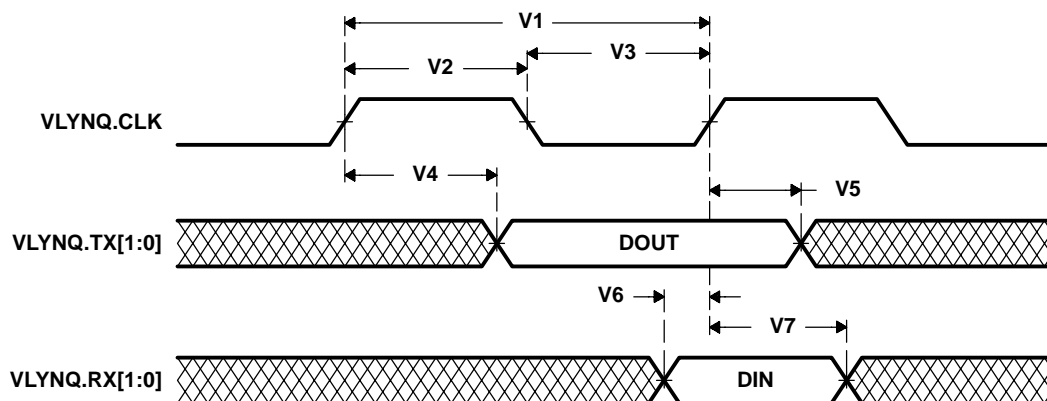


Figure 5–44. VLYNQ Transmit and Receive Timings, in Slave or Master Mode

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5.16 Parallel Camera Interface Timings

Table 5–39 assumes testing over recommended operating conditions (see Figure 5–45).

Table 5–39. Camera Interface Timing Requirements

NO.		MIN	MAX	UNIT
C1	$1/[t_c(LCKH-HSV)]$ Operating frequency, CAM.LCLK		24	MHz
C2	$1/[t_c(XCKH-HSV)]$ Operating frequency, CAM.EXCLK	6	24	MHz
C3	$t_w(LCK)$ Pulse duration, CAM.LCLK high or low	0.45P [†]	0.55P [†]	ns
C5	$t_{su}(LCKH-DV)$ Setup time, CAM.D[7:0] data valid before CAM.LCLK high	1 [‡]		ns
C6	$t_h(DV-LCKH)$ Hold time, CAM.D[7:0] data valid after CAM.LCLK high	6 [‡]		ns
C7	$t_{su}(LCKH-DV)$ Setup time, CAM.VS/CAM.HS active before CAM.LCLK high	1 [‡]		ns
C8	$t_h(DV-CLKH)$ Hold time, CAM.VS/CAM.HS active after CAM.LCLK high	6 [‡]		ns

[†] P = period of CAM.LCLK in nanoseconds (ns).

[‡] Polarity of CAM.LCLK is selectable via the POLCLK bit in the CTRLCLOCK register. Although data is latched on rising CAM.LCLK in the timing diagrams, these timing parameters also apply to falling CAM.LCLK when POLCLK = 1.

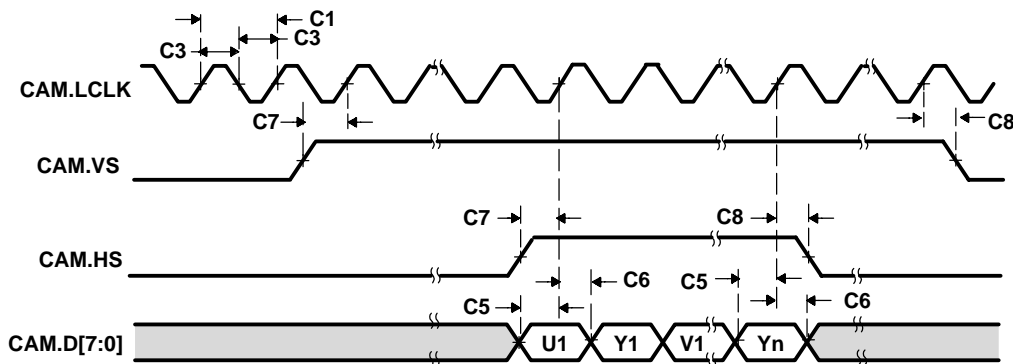


Figure 5–45. Camera Interface Timings

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5.17 Compact Serial Camera Port (CCP) Timings

Table 5–40 assumes testing over recommended operating conditions (see Figure 5–46).

Table 5–40. CCP Interface Timing Requirements

NO.			MIN	MAX	UNIT
C1	$1/[t_{op}(\text{CLK})]$	Operating frequency, CCP.CLK input frequency [†]		208	MHz
C2	$t_w(\text{CLKLH})$	Pulse duration, CCP.CLK low	$0.4P^{\ddagger}$	$0.6P^{\ddagger}$	ns
C3	$t_w(\text{CLKLL})$	Pulse duration, CCP.CLK high	$0.4P^{\ddagger}$	$0.6P^{\ddagger}$	ns
C4	$t_{su}(\text{DV-CLKH})$	Setup time, CCP.DATA valid before CCP.CLK high	1		ns
C5	$t_h(\text{CLKH-DV})$	Hold time, CCP.DATA valid after CCP.CLK high	2		ns
C6	V_{CM}	Input common mode voltage range	0.5	1.3	V

[†] When nothing is being transferred, CLK has to remain high level, except in power shut-down.

[‡] P = period of CAM.LCLK in nanoseconds (ns).

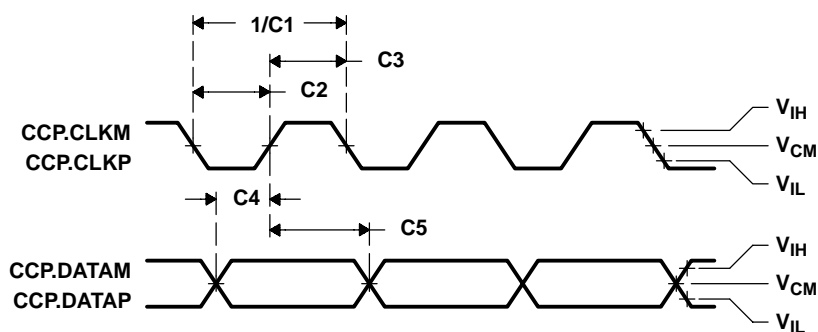


Figure 5–46. CCP Interface Timing

5.18 LCD Controller and LCDCONV Interface Timings

Table 5–41 assumes testing over recommended operating conditions (see Figure 5–47 and Figure 5–48).

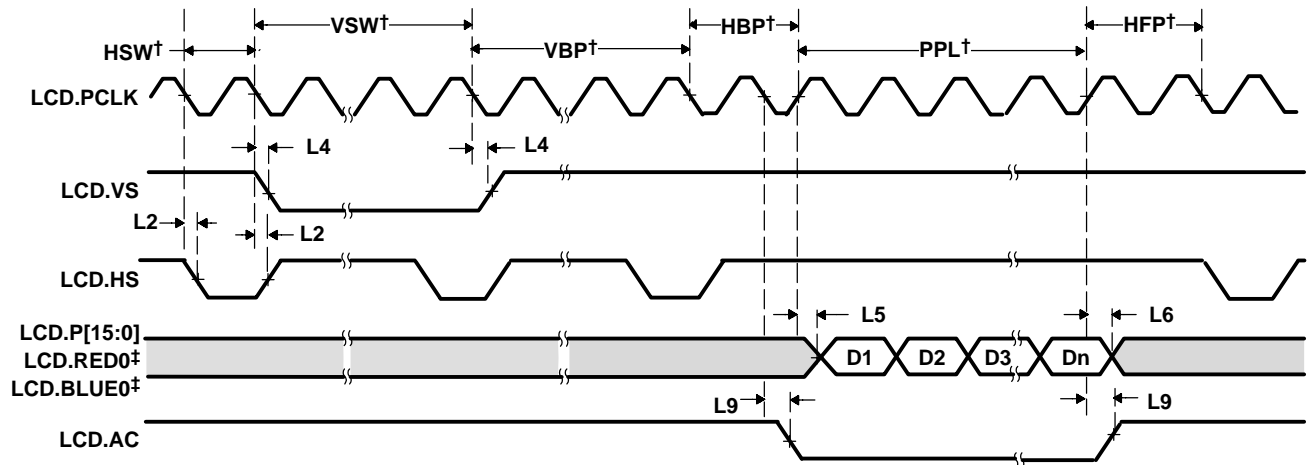
Table 5–41. LCD Controller and LCDCONV Switching Characteristics†

NO.	PARAMETER		MIN	MAX	UNIT
L1	$t_{d(CLKH-HSV)}$	Delay time, LCD.PCLK high to LCD.HS transition	1	7	ns
L2	$t_{d(CLKL-HSV)}$	Delay time, LCD.PCLK low to LCD.HS transition	1	7	ns
L3	$t_{d(CLKH-VSV)}$	Delay time, LCD.PCLK high to LCD.VS transition	1	7	ns
L4	$t_{d(CLKL-VSV)}$	Delay time, LCD.PCLK low to LCD.VS transition	1	7	ns
L5	$t_{d(CLKH-PV)}$	Delay time, LCD.PCLK high to pixel data valid (LCD.P[15:0])	LCD 16-bit mode (LCDCONV bypassed)	-7	ns
			LCD 18-bit mode through LCDCONV (LCD.RED0 and LCD.BLUE0)	7	
L6	$t_{d(CLKH-PIV)}$	Delay time, LCD.PCLK high to pixel data invalid (LCD.P[15:0])	LCD 16-bit mode (LCDCONV bypassed)	-10	ns
			LCD 18-bit mode through LCDCONV (LCD.RED0 and LCD.BLUE0)	-2	
L7	$t_{d(CLKL-PV)}$	Delay time, LCD.PCLK low to pixel data valid (LCD.P[15:0])	LCD 16-bit mode (LCDCONV bypassed)	-7	ns
			LCD 18-bit mode through LCDCONV (LCD.RED0 and LCD.BLUE0)	7	
L8	$t_{d(CLKL-PIV)}$	Delay time, LCD.PCLK low to pixel data invalid (LCD.P[15:0])	LCD 16-bit mode (LCDCONV bypassed)	-10	ns
			LCD 18-bit mode through LCDCONV (LCD.RED0 and LCD.BLUE0)	-2	
L9	$t_{d(CLKH-ACV)}$	Delay time, LCD.PCLK high to LCD.AC transition	1	$5 + P‡$	ns
L10	$t_{d(CLKL-ACV)}$	Delay time, LCD.PCLK low to LCD.AC transition	1	$5 + P‡$	ns

† Although timing diagrams illustrate the logical function of the TFT mode, static timings apply to all supported modes of operation. Likewise, LCD.HS, LCD.VS, and LCD.AC are shown as active-low, but each can optionally be configured as active-high.

‡ P = period of internal undivided pixel clock

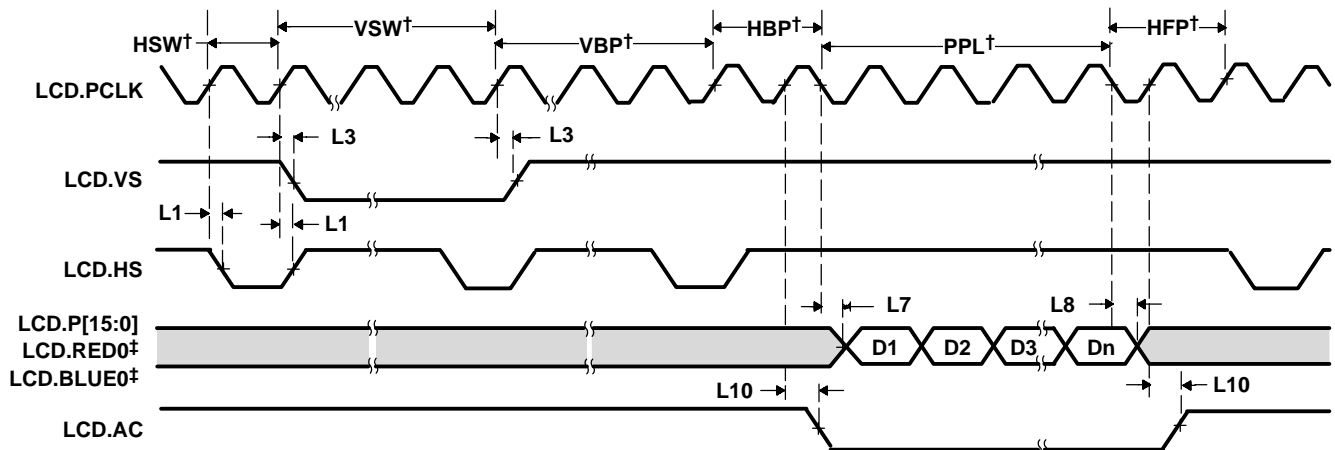
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† Delays for HSW (LCD.HS Width), VSW (LCD.VS Width), VBP (Vertical Back Porch), HFP (Horizontal Front Porch), HBP (Horizontal Back Porch) and PPL (Pixels per Line) are programmable in number of LCD.PCLK cycles via the LCD configuration registers.

‡ The pins LCD.RED0 and LCD.BLUE0 are only available in 18-bit LCD mode (through LCDCONV interface).

Figure 5–47. TFT Mode (LCD.HS/LCD.VS on Falling and LCD.Px on Rising LCD.PCLK)



† Delays for HSW (LCD.HS Width), VSW (LCD.VS Width), VBP (Vertical Back Porch), HFP (Horizontal Front Porch), HBP (Horizontal Back Porch) and PPL (Pixels per Line) are programmable in number of LCD.PCLK cycles via the LCD configuration registers.

‡ The pins LCD.RED0 and LCD.BLUE0 are only available in 18-bit LCD mode (through LCDCONV interface).

Figure 5–48. TFT Mode (LCD.HS/LCD.VS on Rising and LCD.Px on Falling LCD.PCLK)

5.19 SoSSI Display Interface Timings

Table 5–42 and Table 5–43 assume testing over recommended operating conditions (see Figure 5–49 and Figure 5–50).

Table 5–42. SoSSI Display Interface Timing Requirements

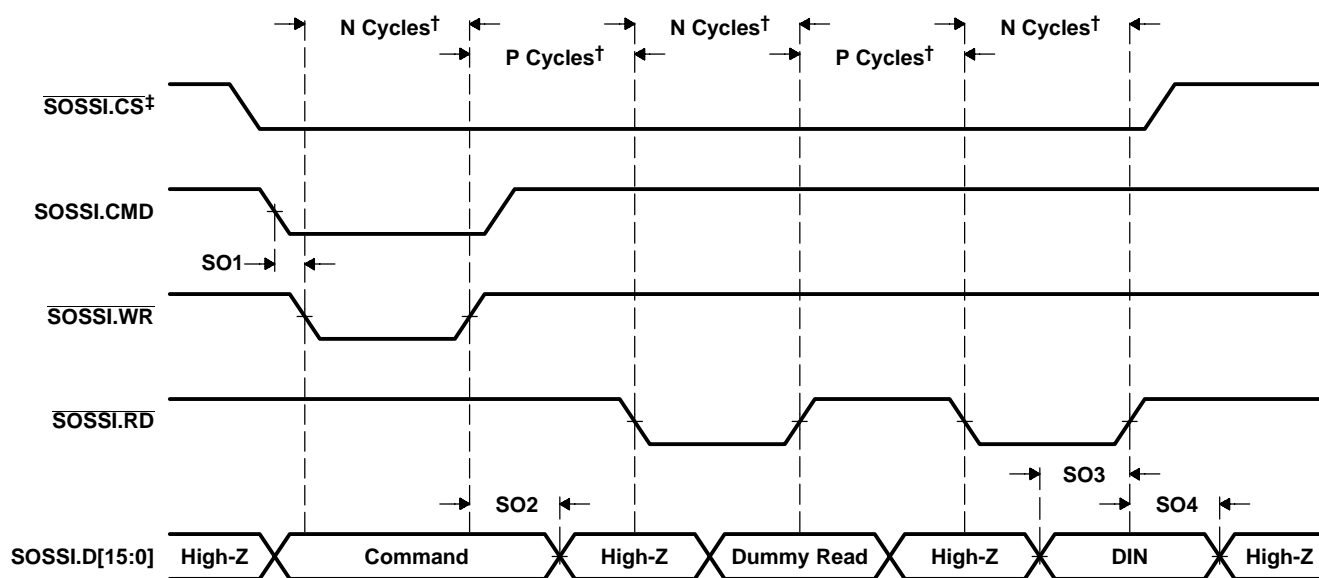
NO.		MIN	MAX	UNIT
SO3	$t_{su}(DV-RDH)$ Setup time, input SOSSI.Dx valid before $\overline{\text{SOSSI.RD}}$ high	25		ns
SO4	$t_{h}(RDH-DV)$ Hold time, input SOSSI.Dx valid after $\overline{\text{SOSSI.RD}}$ high	0		ns

Table 5–43. SoSSI Display Interface Switching Characteristics

NO.	PARAMETER	MIN	MAX	UNIT
SO0	$t_{c}(\text{CLKI})$ Cycle time, SoSSI internal clock	50		ns
SO1	$t_{d}(\text{CMDV-WRV})$ Delay time, SOSSI.CMD to $\overline{\text{SOSSI.WR}}$ active		$P + 1^{\dagger}$	ns
SO2	$t_{d}(\text{WRH-DV})$ Delay time, SOSSI.WR high to SOSSI.Dx transition		$P + 3.5^{\dagger}$	ns

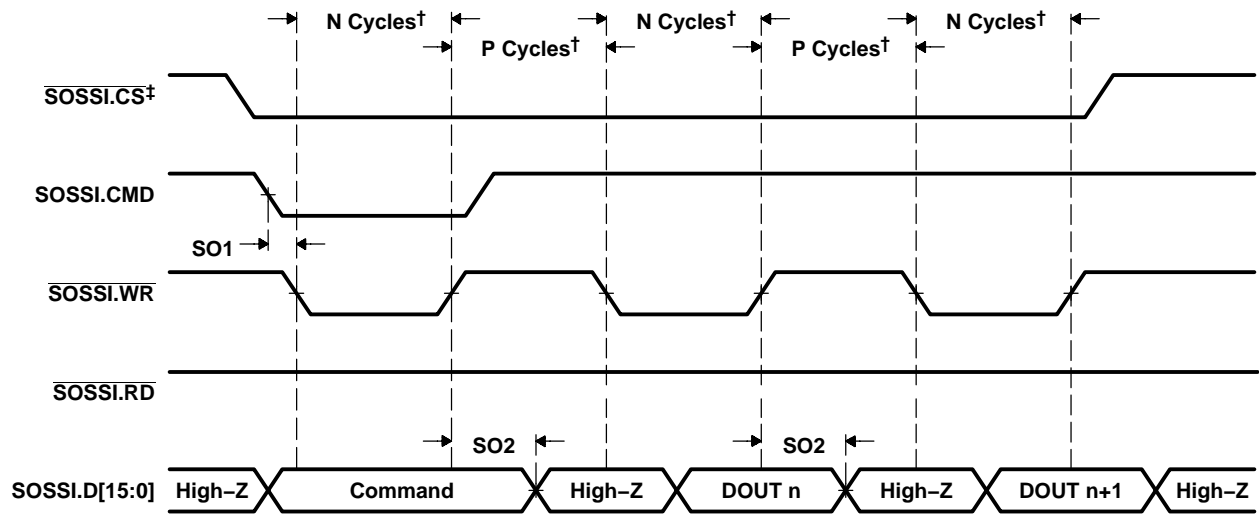
$^{\dagger} P =$ period of internal clock interface in nanoseconds (ns).

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† Numbers of cycles are configurable.
 ‡ Chip Select is controlled by software.

Figure 5–49. SoSSI Display Interface – Read Mode Operation



† Numbers of cycles are configurable.
 ‡ Chip Select is controlled by software.

Figure 5–50. SoSSI Display Interface – Write Mode Operation

5.20 Multimedia Card/Secure Digital (MMC/SD) Timings

Table 5–44 and Table 5–45 assume testing over recommended operating conditions (see Figure 5–51 through Figure 5–54).

Table 5–44. MMC/SD Timing Requirements

NO.		MIN	MAX	UNIT
M1	$t_{su}(CMDV-CLKH)$ Setup time, MMC.CMD valid before MMC.CLK high	3.5		ns
M2	$t_h(CLKH-CMDIV)$ Hold time, MMC.CMD invalid after MMC.CLK high	1		ns
M3	$t_{su}(DATV-CLKH)$ Setup time, MMC.DATx valid before MMC.CLK high	3.5		ns
M4	$t_h(CLKH-DATIV)$ Hold time, MMC.DATx invalid after MMC.CLK high	1		ns

Table 5–45. MMC/SD Switching Characteristics

NO.	PARAMETER		MIN	MAX	UNIT
M7	$t_c(CLK)$	MMC card	50		ns
		SD card	40		
M8	$t_w(CLKL)$	Pulse duration, MMC.CLK low	0.45P [†]	0.55P [†]	ns
M9	$t_w(CLKH)$	Pulse duration, MMC.CLK high	0.45P [†]	0.55P [†]	ns
M10	$t_d(CLKH-CMD)$	Delay time, MMC.CLK high to MMC.CMD transition	8	32	ns
M11	$t_d(CLKH-DAT)$	Delay time, MMC.CLK high to MMC.DATx transition	8	32	ns

[†] MMC.CLK period and pulse duration depend upon software configuration.

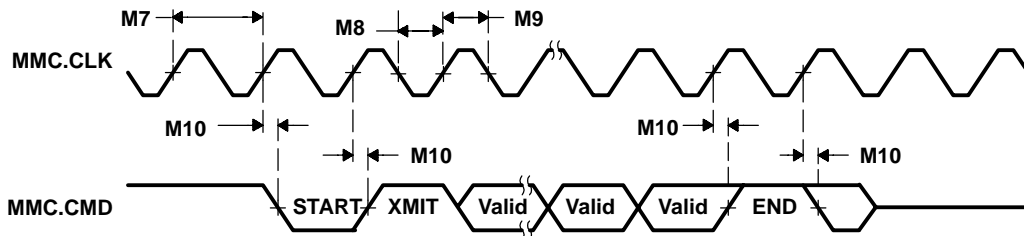


Figure 5–51. MMC/SD Host Command Timings

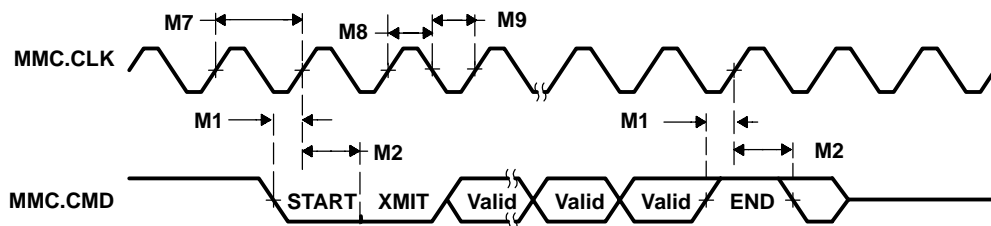


Figure 5–52. MMC/SD Card Response Timings

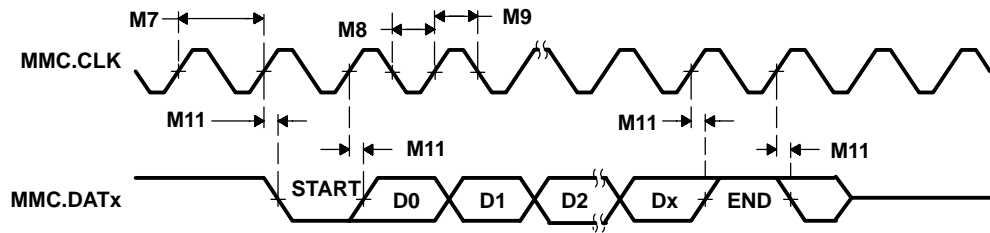


Figure 5-53. MMC/SD Host Write Timings

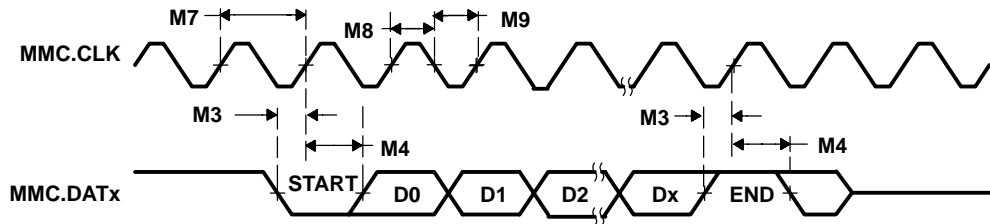


Figure 5-54. MMC/SD Host Read and Card CRC Status Timings

5.21 I²C Timings

Table 5–46 assumes testing over recommended operating conditions (see Figure 5–55).

Table 5–46. I²C Signals (I2C.SDA and I2C.SCL) Switching Characteristics

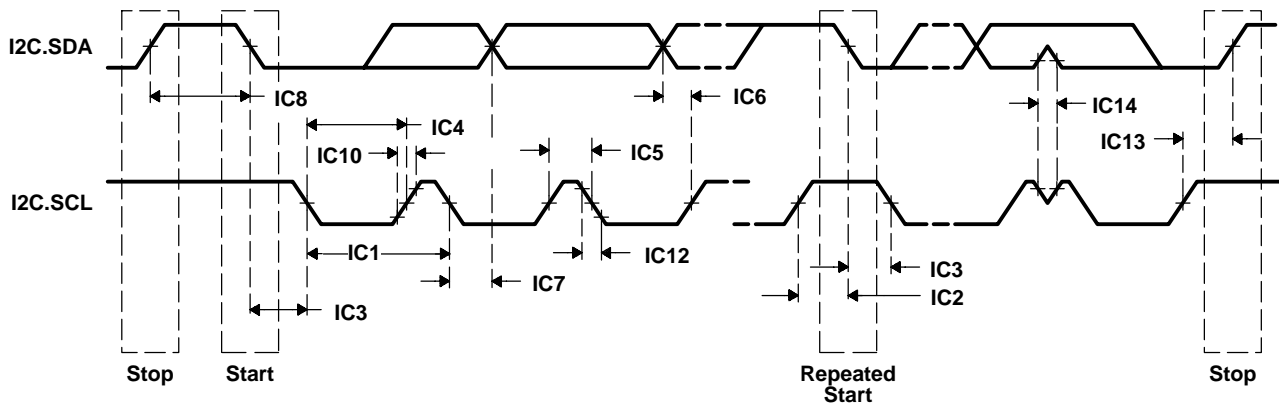
NO.	PARAMETER	STANDARD MODE		FAST MODE		UNIT
		MIN	MAX	MIN	MAX	
IC1	$t_{c(SCL)}$ Cycle time, I2C.SCL	10 [†]		2.5		μs
IC2	$t_{su(SCLH-SDAL)}$ Setup time, I2C.SCL high before I2C.SDA low (for a repeated START condition)	4.7		0.6		μs
IC3	$t_{h(SCLL-SDAL)}$ Hold time, I2C.SCL low after I2C.SDA low (for a repeated START condition)	4		0.6		μs
IC4	$t_{w(SCLL)}$ Pulse duration, I2C.SCL low	4.7		1.3		μs
IC5	$t_{w(SCLH)}$ Pulse duration, I2C.SCL high	4		0.6		μs
IC6	$t_{su(SDA-SDLH)}$ Setup time, I2C.SDA valid before I2C.SCL high	250	‡	100		ns
IC7	$t_{h(SDA-SDLL)}$ Hold time, I2C.SDA valid after I2C.SCL low (for I ² C bus devices)	0		0	0.9	μs
IC8	$t_{w(SDAH)}$ Pulse duration, I2C.SDA high between STOP and START conditions	4.7		1.3		μs
IC9	$t_r(SDA)$ Rise time, I2C.SDA		1000 [§]		300 [§]	ns
IC10	$t_r(SCL)$ Rise time, I2C.SCL		1000 [§]		300 [§]	ns
IC11	$t_f(SDA)$ Fall time, I2C.SDA		300 [§]		300 [§]	ns
IC12	$t_f(SCL)$ Fall time, I2C.SCL		300 [§]		300 [§]	ns
IC13	$t_{su(SCLH-SDAH)}$ Setup time, I2C.SCL high before I2C.SDA high (for STOP condition)	4.0		0.6		μs
IC14	$t_{w(SP)}$ Pulse duration, spike (must be suppressed)			0	50	ns
IC15	C_b [¶] Capacitive load for each bus line		400		400	pF

[†] In the master-only I²C operating mode of OMAP5912, minimum cycle time for I2C.SCL is 12 μs.

[‡] The maximum $t_{h(SCLL-SDAL)}$ has only to be met if the device does not stretch the low period ($t_{w(SCLL)}$) of the I2C.SCL signal.

[§] Max of fall and rise times were measured while considering an internal pullup value of 520 Ω.

[¶] C_b = The total capacitance of one bus line in pF.



- NOTES:
- A. A device must internally provide a hold time of at least 300 ns for the I2C.SDA signal (referred to the V_{IHmin} of the I2C.SCL signal) to bridge the undefined region of the falling edge of I2C.SCL.
 - B. The maximum $t_{h(SCLL-SDAL)}$ has only to be met if the device does not stretch the LOW period ($t_{w(SCLL)}$) of the I2C.SCL signal.
 - C. A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement $t_{su(SDA-SDLH)} \bullet 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the I2C.SCL signal. If such a device does stretch the LOW period of the I2C.SCL signal, it must output the next data bit to the I2C.SDA line $t_r \text{ max} + t_{su(SDA-SDLH)} = 1000 + 250 = 1250$ ns (according to the standard-mode I²C-bus specification) before the I2C.SCL line is released.
 - D. C_b = total capacitance of one bus line in pF. If mixed with fast-mode devices, faster fall times are allowed.

Figure 5–55. I²C Timings

5.22 Universal Serial Bus (USB) Timings

All OMAP5912 USB interfaces are compliant with Universal Serial Bus Specifications, Revision 1.1. Table 5–47 assumes testing over recommended operating conditions (see Figure 5–56).

Table 5–47. USB Integrated Transceiver Interface Switching Characteristics

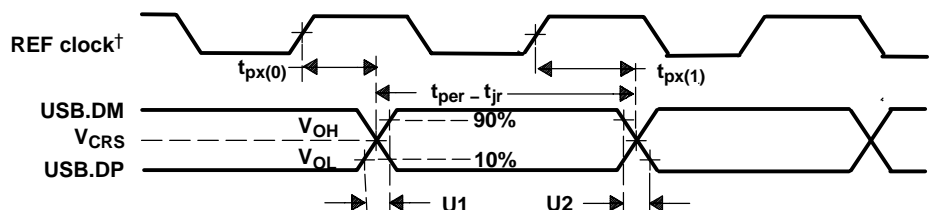
NO.	PARAMETER	LOW SPEED 1.5 Mbps		FULL SPEED 12 Mbps		UNIT
		MIN	MAX	MIN	MAX	
U1	t_r Rise time, USB.DP and USB.DM signals [†]	75 [†]	300 [†]	4 [†]	20 [†]	ns
U2	t_f Fall time, USB.DP and USB.DM signals [†]	75 [†]	300 [†]	4 [†]	20 [†]	ns
U3	t_{RFM} Rise/Fall time matching [‡]	80 [‡]	125 [‡]	90 [‡]	111.11 [‡]	%
U4	V_{CRS} Output signal cross-over voltage [†]	1.3 [†]	2 [†]	1.3 [†]	2 [†]	V
U5	t_{jr} Differential propagation jitter [§]	-25 [§]	25 [§]	-2 [§]	2 [§]	ns
U6	f_{op} Operating frequency [¶]		1.5		12	MHz

[†] Low speed: $C_L = 200$ pF. High speed: $C_L = 50$ pF.

[‡] $t_{RFM} = (t_r/t_f) \times 100$

[§] $t_{jr} = t_{px(1)} - t_{px(0)}$

[¶] $f_{op} = 1/t_{per}$



[†] “REF clock” is not an actual device signal, but an ideal reference clock against which relative timings are specified. REF clock is assumed to be 12 MHz for full-speed mode or 1.5 MHz for low-speed mode.

Figure 5–56. USB Integrated Transceiver Interface Timings

5.23 MICROWIRE Interface Timings

Table 5–48 and Table 5–49 assume testing over recommended operating conditions (see Figure 5–57).

Table 5–48. MICROWIRE Timing Requirements

NO.		MIN	MAX	UNIT
W5	$t_{su}(SDI-SCLK)$ Setup time, UWIRE.SDI valid before UWIRE.SCLK active edge [†]	16		ns
W6	$t_{h}(SCLK-SDI)$ Hold time, UWIRE.SDI invalid after UWIRE.SCLK active edge [†]	1		ns

[†] Polarity of UWIRE.SCLK and the active clock edge (rising or falling) on which SDO data is driven and SDI data is latched is all software-configurable. These timings apply to all configurations regardless of UWIRE.SCLK polarity and which clock edges are used to drive output data and capture input data.

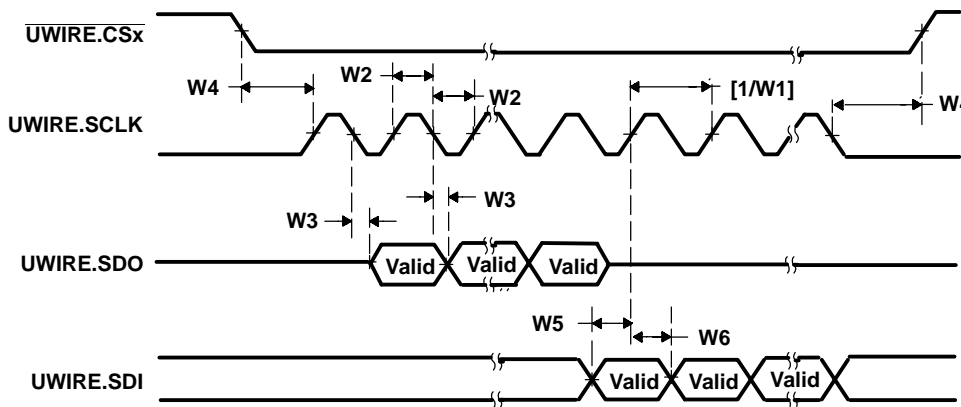
Table 5–49. MICROWIRE Switching Characteristics

NO.	PARAMETER	MIN	MAX	UNIT
W1	$f_{op}(SCLK)$ Operating frequency, UWIRE.SCLK		0.25B [‡]	MHz
W2	$t_w(SCLK)$ Pulse duration, UWIRE.SCLK high/low	0.45P [§]	0.55P [§]	ns
W3	$t_d(SCLK-SDO)$ Delay time, UWIRE.SCLK active edge to UWIRE.SDO transition [†]	-2	4	ns
W4	$t_d(CS-SCLK)$ Delay time, UWIRE.CSx active to UWIRE.SCLK active [†]	1.5P [§]		ns

[†] Polarity of UWIRE.SCLK and the active clock edge (rising or falling) on which SDO data is driven and SDI data is latched is all software-configurable. These timings apply to all configurations regardless of UWIRE.SCLK polarity and which clock edges are used to drive output data and capture input data.

[‡] B = system clock of the OMAP5912 (12, 13, or 19.2 MHz).

[§] P = UWIRE.SCLK cycle time in nanoseconds (ns).



NOTE: The polarities of $\overline{UWIRE.CSx}$ and UWIRE.SCLK and the active UWIRE.SCLK edges on which SDO is driven and SDI is sampled are all software-configurable.

Figure 5–57. MICROWIRE Timings

5.24 HDQ/1-Wire Interface Timings

Table 5–50 and Table 5–51 assume testing over recommended operating conditions (see Figure 5–58 through Figure 5–63).

Table 5–50. HDQ/1-Wire Timing Requirements†

NO.			MIN	MAX	UNIT	
H1	t_c	Cycle time, master read	190	250	μs	
H2	t_v	Read one data valid after HDQ low	32	50	μs	
H3	t_v	Read zero data hold after HDQ low	80	145	μs	
H4	t_v	Response time from HDQ slave device	OMAP5912 base frequency = 12 MHz	190	320	μs
			OMAP5912 base frequency = 13 MHz	190	303	
W1	t_c	Cycle time, master read	190		μs	
W2	t_v	Read data valid after HDQ low (master sample window)	12	13.6	μs	
W3	t_{dis}	Recovery time after slave device inactive	1		μs	

† HDQ timing is OMAP5912 default. 1-Wire timing is selectable through software.

Table 5–51. HDQ/1-Wire Switching Characteristics

NO.		PARAMETER	MIN	MAX	UNIT	
H5	t_c	Cycle time, master write	190		μs	
H6	t_d	Write one data valid after HDQ low	32	50	μs	
H7	t_d	Write zero data hold after HDQ low	OMAP5912 base frequency = 12 MHz	100	145	μs
			OMAP5912 base frequency = 13 MHz	92	145	
H8	t_w	Pulse width, HDQ low for break pulse (reset)	190		μs	
H9	t_w	Pulse width, HDQ high for break pulse recovery	40		μs	
W4	t_c	Cycle time, master write	190		μs	
W5	t_d	Write zero master inactive after HDQ low	15	90	μs	
W6	t_d	Write one master inactive after HDQ low	1.1	1.4	μs	
W7	t_{dis}	Recovery time after master inactive	1		μs	

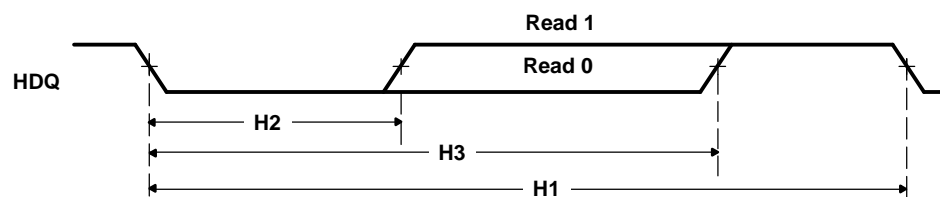


Figure 5–58. HDQ Interface Reading From HDQ Slave Device

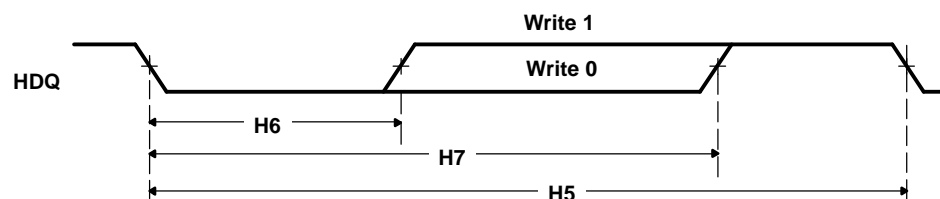


Figure 5–59. HDQ Interface Writing to HDQ Slave Device

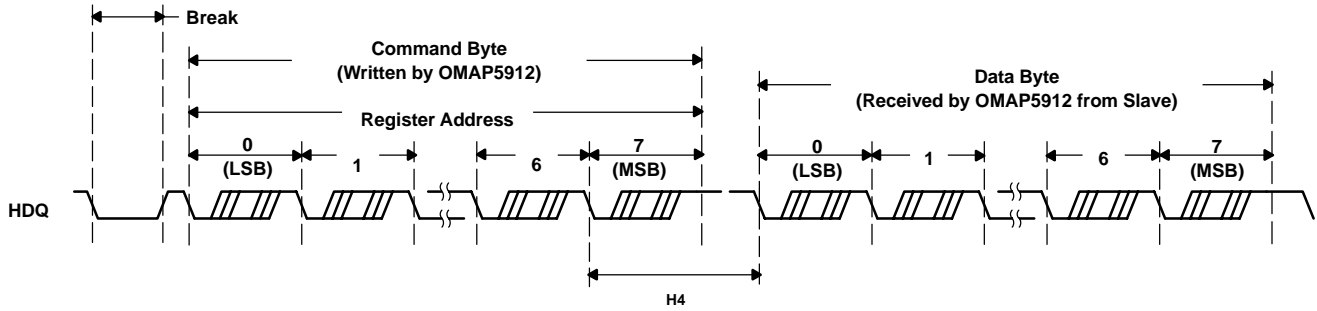


Figure 5–60. Typical Communications Between OMAP5912 HDQ and HDQ Slave

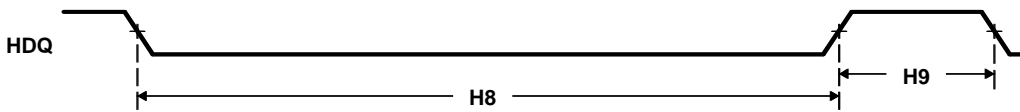


Figure 5–61. HDQ/1-Wire Break (Reset) Timings

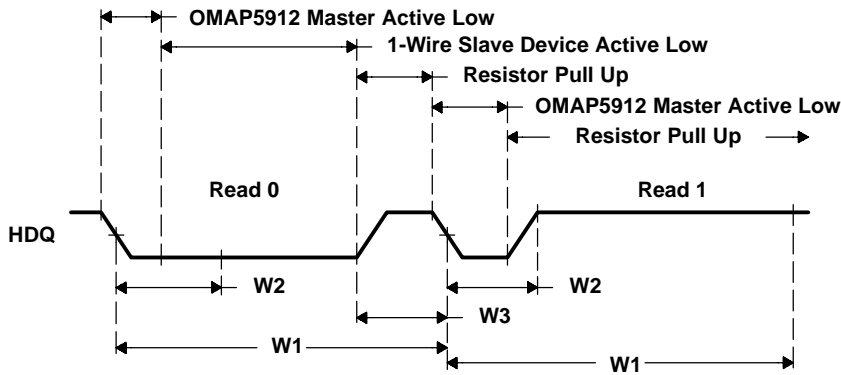


Figure 5–62. 1-Wire Interface Reading From 1-Wire Slave Device

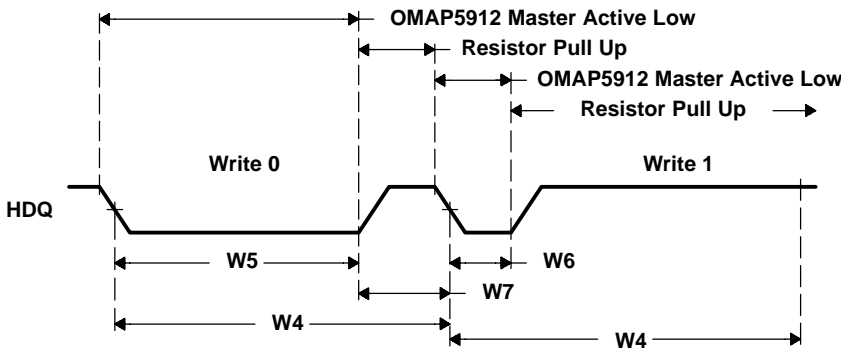


Figure 5–63. 1-Wire Interface Writing to 1-Wire Slave Device

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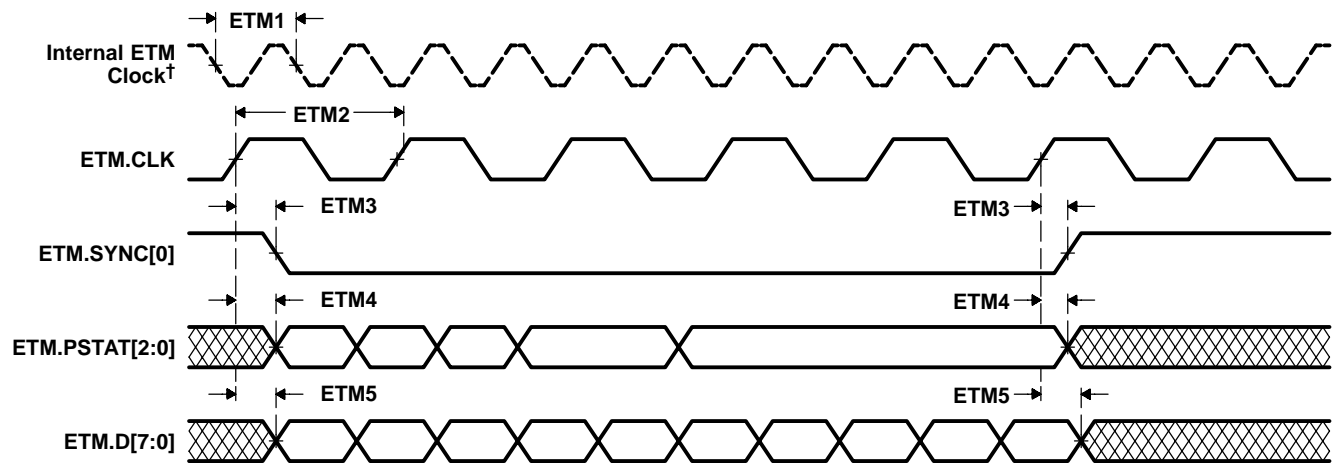
5.25 Embedded Trace Macrocell (ETM) Interface

Table 5–52 assumes testing over recommended operating conditions (see Figure 5–64 and Figure 5–65).

Table 5–52. ETM Interface Switching Characteristics

NO.	PARAMETER		MIN	MAX	UNIT
ETM1	$t_{c(\text{CLKI})}$	Cycle time, ETM internal clock	5		ns
ETM2	$t_{c(\text{CLK})}$	Cycle time, ETM.CLK (external) clock	10		ns
ETM3	$t_{d(\text{CLKIH-SYNCV})}$	Delay time, ETM clock high to ETM.SYNCx transition		$0.5P + 0.39^\dagger$	ns
ETM4	$t_{d(\text{CLKH-PSTATV})}$	Delay time, ETM clock high to ETM.PSTATx transition		$0.5P + 0.45^\dagger$	ns
ETM5	$t_{d(\text{CLKH-DV})}$	Delay time, ETM clock high to ETM.Dx transition		$0.5P + 0.87^\dagger$	ns

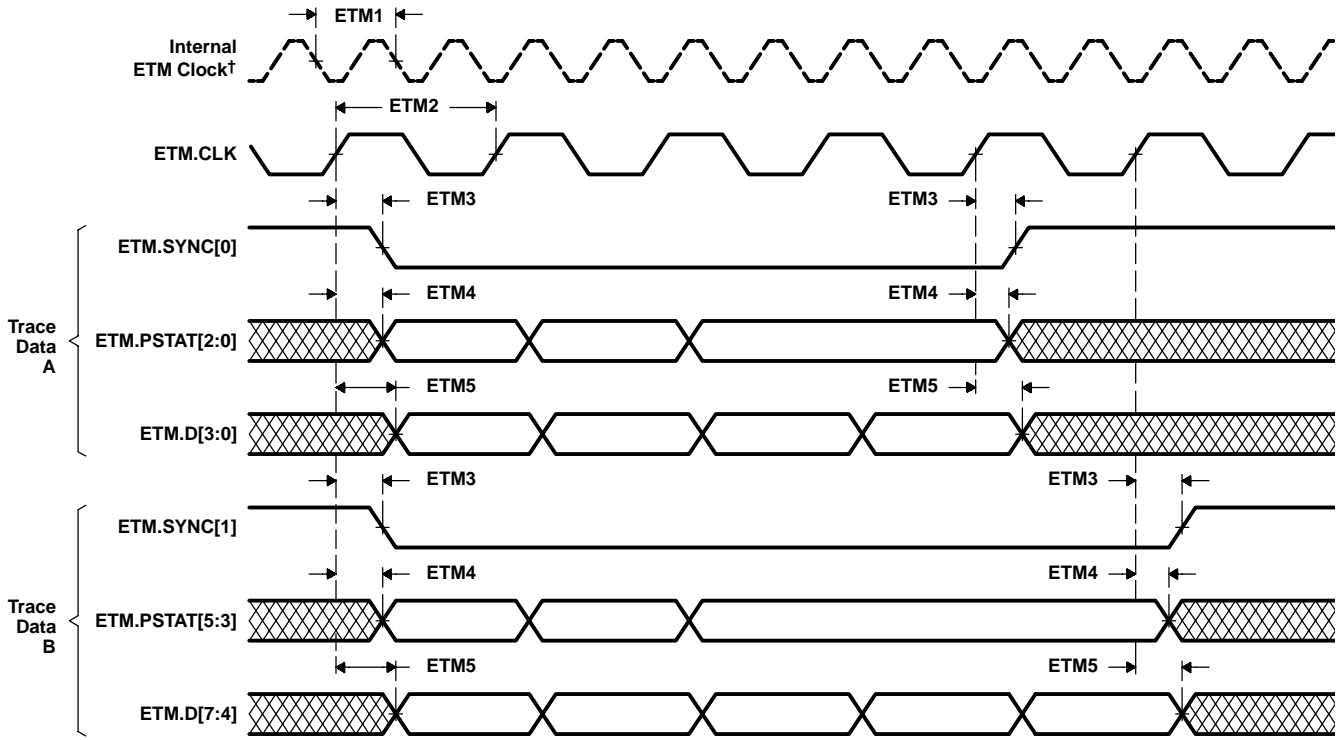
$^\dagger P$ = internal clock period



† The signal shown represents the internal ETM clock signal given as a reference to express delay time.

Figure 5–64. Normal Mode – Half Rate Clock – Rising and Falling Clock Edge

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† The signal shown represents the internal ETM clock signal given as a reference to express delay time.

Figure 5-65. Demultiplexed Mode of Full Rate Clock – Rising Clock Edge

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6 Glossary

ACRONYM	DEFINITION
3DES	triple data encryption security
AAC	Advanced Audio Coding (standard) (ISO/IEC 13818-7)
AC97	Interface Standard for Codecs
ALE	address latch enable
ALU	arithmetic/logic unit
AMR	adaptive multi-rate
APE	application chip
APLL	analog phase-locked loop
ASRAM	asynchronous static random-access memory
AU	address unit
BCD	binary coded decimal
BGA	ball grid array
BIST	built-in self-test
CBC	cipher block chaining
CCP	compact camera port
CE	chip enable
CFB	cipher feedback
CLE	common latch enable
CMOS	complementary metal oxide semiconductor
CMT	cellular mobile telephone
CP15	coprocessor 15
CPU	central processing unit
CRC	cyclic redundancy check
CS	chip select
CSL	Chip Support Library
CTS	clear-to-send
DARAM	dual-access random-access memory
DCDL	digitally controlled delay element
DCT	discrete cosine transform
DDR	dual data rate
DES	data encryption security
DMA	direct memory access
DPLL	digital phase-locked loop
DSP	digital signal processor
DSPLIB	DSP Library
DSR	data-set-ready
DTR	data-terminal-ready
DU	data unit

ACRONYM	DEFINITION
ECB	electronic codebook
EEPROM	electrically erasable programmable read-only memory
EMIFF	external memory interface fast
EMIFS	external memory interface slow
EOF	end of file
EP	endpoint
ESD	electrostatic discharge
ETM	Embedded Trace Macrocell
FAC	frame adjustment counter
FFT	Fast Fourier Transform
FIFO	first-in first out
FIQ	fast interrupt request
FIR	fast infrared
GDD	Generic Distribute DMA
GP	general-purpose
GPIO	general-purpose input/output
GPRS	General Packet Radio Service
GSM	Global System for Mobile Communications
H.26x	an ITU-TSS standard
HBM	Human Body Model
HC	host controller
HCI	host controller interface
HOM	host-only mode
HS	high-speed
I-cache	instruction cache
I ² C	Inter-integrated circuit
I ² S	Inter-IC Sound (specification)
iDCT	Inverse Discrete Cosine Transform
IDE	integrated development environment
I/F	interface
IFR	Interrupt Flag Register
IMGLIB	Image/Video Processing Library
IMR	Interrupt Mask Register
IO	input/output
IOM-2	ISDN Oriented Modular Interface Revision 2
IrDA	infrared data adapter
IRQ	interrupt request
IU	instruction unit
IV	initialization vector

ACRONYM	DEFINITION
JPEG	Joint Photographic Experts Group
JTAG	Joint Test Action Group, IEEE 1149.1 standard
LB	local bus
LCD	liquid-crystal display
LH	local host
LPG	LED pulse generator light pulse generation
LSB	least significant bit
LVC MOS	low-voltage CMOS
MAC	multiply-accumulate
McBSP	multichannel buffered serial port
MCSI	multichannel serial interface
MD5	Message-Digest Algorithm developed by R. Rivest
MeSSI	medium speed screen interface
MIR	medium infrared
MMC	multimedia card
MMC/SD	multimedia card/secure digital multimedia card/secure data
MMU	memory management unit
MPEG	Moving Picture Experts Group
MPU	microprocessor unit
MPUI	microprocessor unit interface
MPUIO	microprocessor unit I/O
MSB	most significant bit
MVIP	multi-vendor integration protocol
OCP	open core protocol
ODM	original design manufacturer
OEM	original equipment manufacturer
OFB	output feedback
OHCI	open host controller interface
OS	operating system
OTG	on-the-go
PCM	pulse code modulation
PI	pixel interpolation
PU	program unit
PWL	pulse-width light pulse width length
PWM	pulse width modulation
PWT	pulse-width tone pulse width time

ACRONYM	DEFINITION
R/B	read/busy
RAM	random-access memory
RE	read enable
RGB	red green blue
RISC	reduced instruction set computer
RNG	random number generator
ROM	read-only memory
RTC	real-time clock
RTS	request-to-send
RX	receive
SAM	shared-access mode
SARAM	single-access random-access memory
SD	secure digital
SDR	single data rate
SDRAM	synchronous dynamic random-access memory
SDW	short distance wireless
SIR	slow infrared
SoSSI	specially optimized screen interface
SPI	serial port interface serial peripheral interface
SRAM	static random-access memory
SRG	Sample Rate Generator
SSI	synchronous serial interconnect
SSR	synchronous serial receiver
SST	synchronous serial transmitter
STN	super twisted nematic
T1/E1	T1 is a digital transmission link with a capacity of 1.544 Mbps. It uses two pairs of normal twisted-wires and can handle 24-voice conversations, each digitized using mu-law coding at 64 kbps. T1 is used in USA, Canada, Hong Kong, and Japan. E1 is a digital transmission link with a capacity of 2.048 Mbps. It is the European equivalent of T1. It can handle 30-voice conversations, each digitized using A-law coding at 64 kbps.
TAP	test access port
TC	traffic controller
TDES	triple data encryption security
TFT	thin-film transistor
TI	Texas Instruments
TIPB	TI peripheral bus
TLB	Translation Look-Aside Buffer
TTB	Translation Table Base
TX	transmit

ACRONYM	DEFINITION
UART	universal asynchronous receiver/transmitter
ULPD	ultra low-power device
URL	uniform resource locator
USB	universal serial bus
VIA	versatile interconnection architecture
VIVT	virtual index virtual tag
WB	write buffer
WDT	watchdog timer
WE	write enable
WMA	Windows Media Audio
WMV	Windows Media Video
WP	write protect

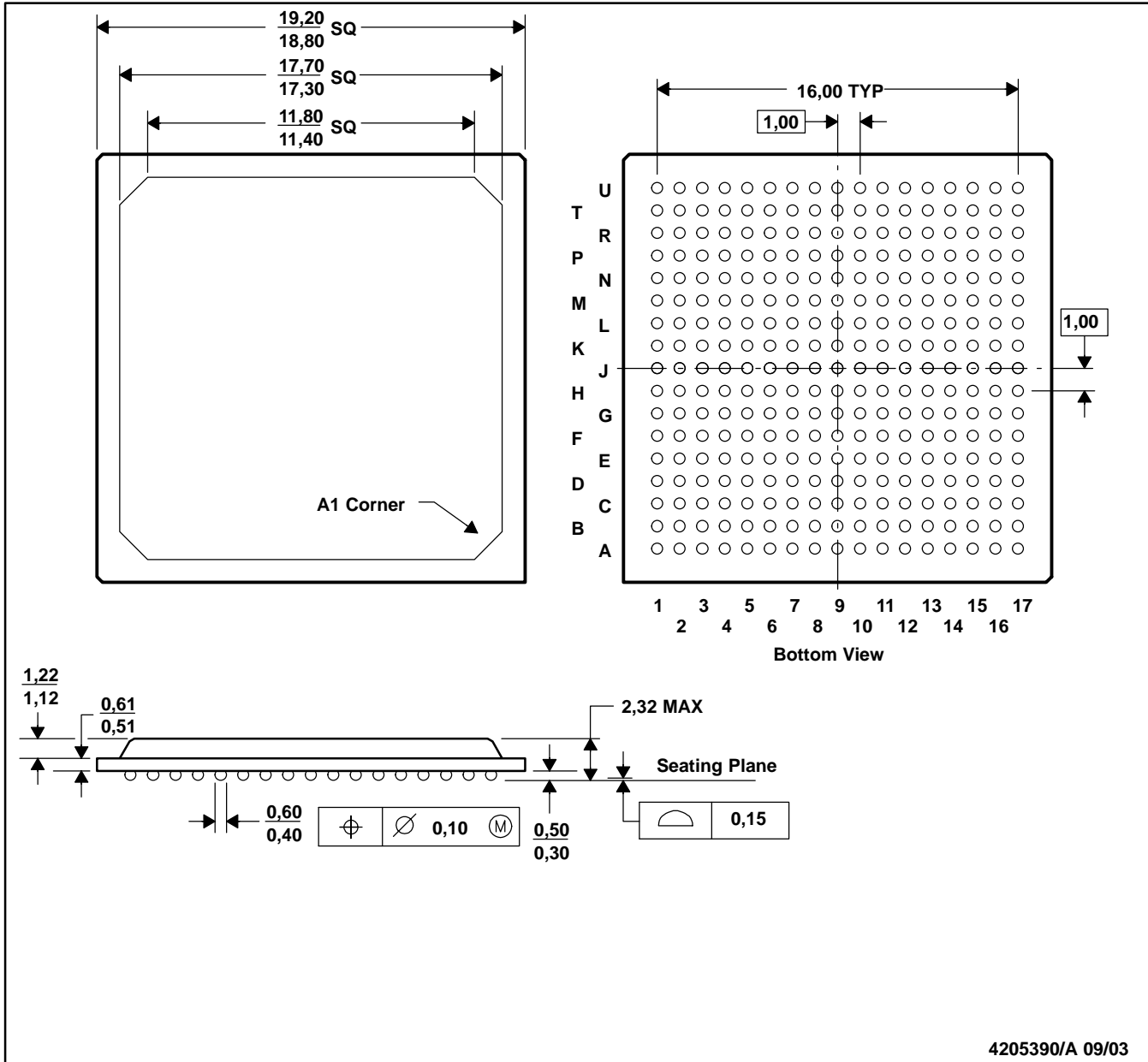
7 Mechanical Data

7.1 Ball Grid Array Mechanical Data

ZDY (S-PBGA-N289)

PLASTIC BALL GRID ARRAY

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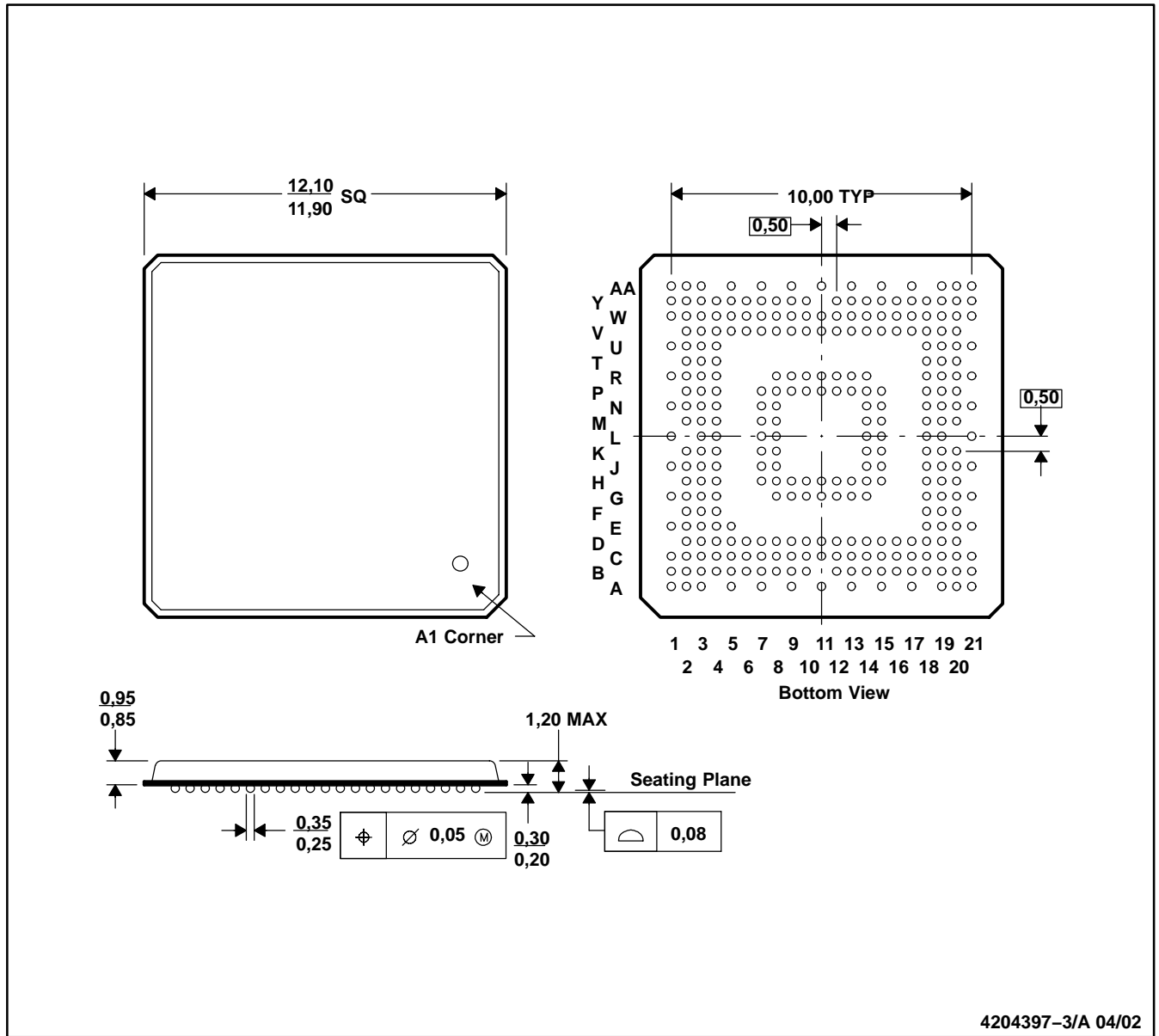


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. This package is lead free.

Figure 7-1. OMAP5912 289-Ball Plastic Ball Grid Array Package (ZDY)

ZZG (S-PBGA-N289)

PLASTIC BALL GRID ARRAY



PRODUCT PREVIEW

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. MicroStar BGA configuration
 D. This package is lead-free.

Figure 7-2. OMAP5912 289-Ball MicroStar BGA™ Plastic Ball Grid Array Package (ZZG)

MicroStar BGA is a trademark of Texas Instruments.