DDP 512Mbit DDR SDRAM

8M x 16bit x 4 Banks

DDR SDRAM Specification

Revision 1.0

July. 2002

Revision History

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Key Features

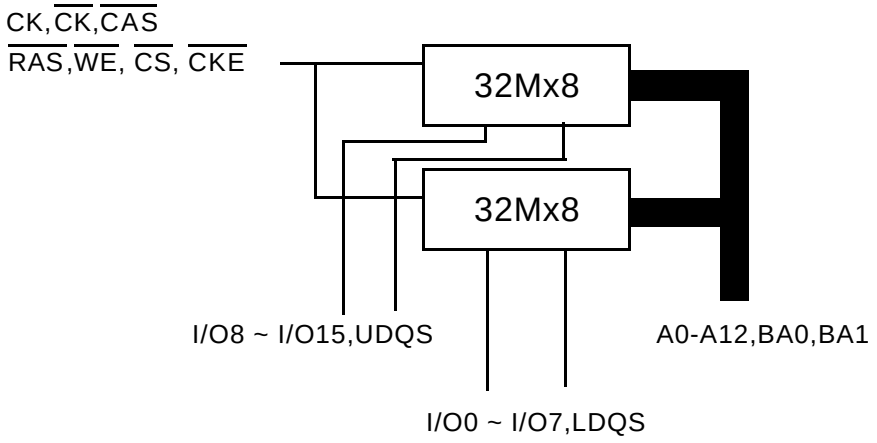
- Double-data-rate architecture; two data transfers per clock cycle
- Bidirectional data strobe(DQS)
- Four banks operation
- Differential clock inputs(CK and $\overline{CK}$)
- DLL aligns DQ and DQS transition with CK transition
- MRS cycle with address key programs
  - -. Read latency 2, 2.5 (clock)
  - -. Burst length (2, 4, 8)
  - -. Burst type (sequential & interleave)
- All inputs except data & DM are sampled at the positive going edge of the system clock(CK)
- Data I/O transactions on both edges of data strobe
- Edge aligned data output, center aligned data input
- LDM,UDM for write masking only
- Auto & Self refresh
- 7.8us refresh interval(8K/64ms refresh)
- Maximum burst refresh cycle : 8
- 66pin TSOP II package

Operating Frequencies

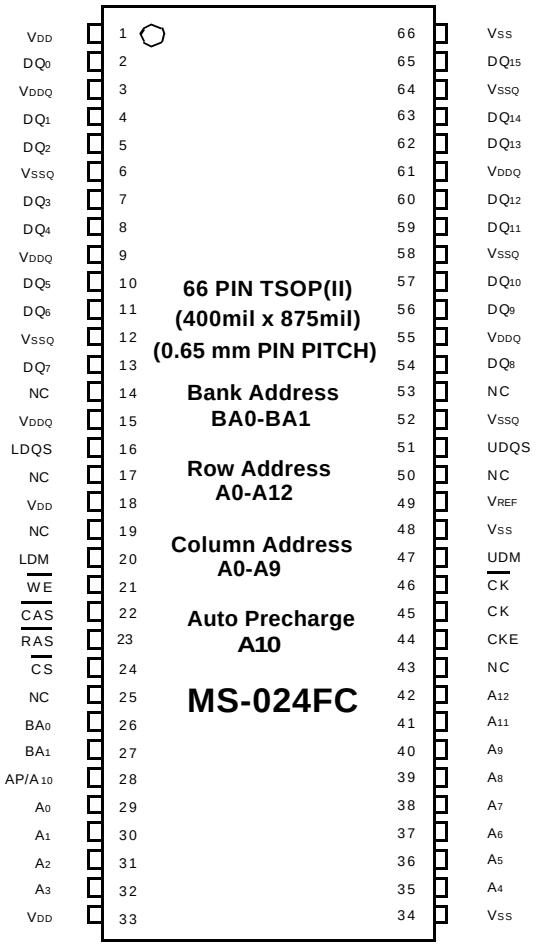
	- B3(DDR333)	- A2(DDR266A)	- B0(DDR266B)	- A0(DDR200)
Speed @CL2	133MHz	133MHz	100MHz	100MHz
Speed @CL2.5	166MHz	133MHz	133MHz	-

*CL : Cas Latency

Functional Block Diagram



Package Pinout



Input/Output Function Description

SYMBOL	TYPE	DESCRIPTION
CK, $\overline{CK}$	Input	Clock : CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to both edges of CK. Internal clock signals are derived from CK/$\overline{CK}$.
CKE	Input	Clock Enable : CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE is synchronous for all functions except for disabling outputs, which is achieved asynchronously. Input buffers, excluding CK, $\overline{CK}$ and CKE are disabled during power-down and self refresh modes, providing low standby power. CKE will recognize an LVCMOS LOW level prior to VREF being stable on power-up.
$\overline{CS}$	Input	Chip Select : $\overline{CS}$ enables(registered LOW) and disables(registered HIGH) the command decoder. All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external bank selection on systems with multiple banks. $\overline{CS}$ is considered part of the command code.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Command Inputs : $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
LDM,(U)DM	Input	Input Data Mask : DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. DM pins include dummy loading internally, to matches the DQ and DQS loading. For the x16, LDM corresponds to the data on DQ0-DQ7 ; UDM correspons to the data on DQ8-DQ15.
BA0, BA1	Input	Bank Addres Inputs : BA0 and BA1 define to which bank ACTIVE, READ, WRITE or PRECHARGE command is being applied.
A [n : 0]	Input	Address Inputs : Provide the row address for ACTIVE commands, the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register is loaded during the MODE REGISTER SET command (MRS or EMRS).
DQ	I/O	Data Input/Output : Data bus
LDQS,(U)DQS	I/O	Data Strobe : Output with read data, input with write data. Edge-aligned with read data, centered in write data. Used to capture write data. For the x16, LDQS corresponds to the data on DQ0-DQ7 ; UDQS corresponds to the data on DQ8-DQ15.
NC	-	No Connect : No internal electrical connection is present.
$V_{DD}Q$	Supply	DQ Power Supply : +2.5V ± 0.2V.
$V_{SS}Q$	Supply	DQ Ground.
V_{DD}	Supply	Power Supply : +2.5V ± 0.2V (device specific).
V_{SS}	Supply	Ground.
V_{REF}	Input	SSTL_2 reference voltage.

Command Truth Table

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$BA_{0,1}$	A_{10}/AP	A_{11}, A_{12} $A_9 \sim A_0$	Note
Register	Extended MRS		H	X	L	L	L	L	OP CODE			1, 2
Register	Mode Register Set		H	X	L	L	L	L	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X			3
	Self Refresh	Entry		L								3
		Exit	L	H	L	H	H	H	X			3
					H	X	X	X				3
Bank Active & Row Addr.			H	X	L	L	H	H	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	V	L	Column Address	4
	Auto Precharge Enable									H		4
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	V	L	Column Address	4
	Auto Precharge Enable									H		4, 6
Burst Stop			H	X	L	H	H	L	X			7
Precharge	Bank Selection		H	X	L	L	H	L	V	L	X	
	All Banks								X	H		5
Active Power Down		Entry	H	L	H	X	X	X	X			
					L	V	V	V				
		Exit	L	H	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X			
					L	H	H	H				
		Exit	L	H	H	X	X	X				
					L	V	V	V				
DM			H	X					X			8
No operation (NOP) : Not defined			H	X	H	X	X	X	X			9
					L	H	H	H				9

1. OP Code : Operand Code. $A_0 \sim A_{12}$ & $BA_0 \sim BA_1$: Program keys. (@EMRS/MRS)
2. EMRS/ MRS can be issued only at all banks precharge state.
   A new command can be issued 2 clock cycles after EMRS or MRS.
3. Auto refresh functions are same as the CBR refresh of DRAM.
   The automatical precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at all banks precharge state.
4. $BA_0 \sim BA_1$: Bank select addresses.
   If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
   If BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank B is selected.
   If BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank C is selected.
   If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
5. If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 are ignored and all banks are selected.
6. During burst write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at t_{RP} after the end of burst.
7. Burst stop command is valid at every burst length.
8. DM sampled at the rising and falling edges of the DQS and Data-in are masked at the both edges (Write DM latency is 0).
9. This combination is not defined for any function, which means "No Operation(NOP)" in DDR SDRAM.

8M x 16Bit x 4 Banks Double Data Rate SDRAM

GENERAL DESCRIPTION

The K4H511638D is 536,870,912 bits of double data rate synchronous DRAM organized as 4 x 8,392,608 words by 16 bits, fabricated with SAMSUNG′s high performance CMOS technology. Synchronous features with Data Strobe allow extremely high performance up to 333Mb/s per pin. I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable burst length and programmable latencies allow the device to be useful for a variety of high performance memory system applications.

Absolute Maximum Rating

Parameter	Symbol	Value	Unit
Voltage on any pin relative to VSS	VIN, VOUT	-0.5 ~ 3.6	V
Voltage on VDD & VDDQ supply relative to VSS	VDD, VDDQ	-1.0 ~ 3.6	V
Storage temperature	TSTG	-55 ~ +150	°C
Power dissipation	PD	3	W
Short circuit current	IOS	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommend operation condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability

DC Operating Conditions

Recommended operating conditions(Voltage referenced to V_{SS}=0V, T_A=0 to 70°C)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage(for device with a nominal V_{DD} of 2.5V)	V_{DD}	2.3	2.7		
I/O Supply voltage	V_{DDQ}	2.3	2.7	V	
I/O Reference voltage	V_{REF}	VDDQ/2-50mV	VDDQ/2+50mV	V	1
I/O Termination voltage(system)	V_{TT}	V_{REF}-0.04	V_{REF}+0.04	V	2
Input logic high voltage	V_{IH}(DC)	V_{REF}+0.15	V_{DDQ}+0.3	V	4
Input logic low voltage	V_{IL}(DC)	-0.3	V_{REF}-0.15	V	4
Input Voltage Level, CK and $\overline{CK}$ inputs	V_{IN}(DC)	-0.3	V_{DDQ}+0.3	V	
Input Differential Voltage, CK and $\overline{CK}$ inputs	V_{ID}(DC)	0.3	V_{DDQ}+0.6	V	3
Input crossing point voltage, CK and $\overline{CK}$ inputs	V_{IX}(DC)	1.15	1.35	V	5
Input leakage current	I_I	-2	2	uA	
Output leakage current	I_{OZ}	-5	5	uA	
Output High Current(Normal strengh driver) ;V_{OUT} = V_{TT} + 0.84V	I_{OH}	-16.8		mA	
Output High Current(Normal strengh driver) ;V_{OUT} = V_{TT} - 0.84V	I_{OL}	16.8		mA	
Output High Current(Half strengh driver) ;V_{OUT} = V_{TT} + 0.45V	I_{OH}	-9		mA	
Output High Current(Half strengh driver) ;V_{OUT} = V_{TT} - 0.45V	I_{OL}	9		mA	

Notes 1. Includes ± 25mV margin for DC offset on V_{REF}, and a combined total of ± 50mV margin for all AC noise and DC offset on V_{REF}, bandwidth limited to 20MHz. The DRAM must accommodate DRAM current spikes on V_{REF} and internal DRAM noise coupled TO V_{REF}, both of which may result in V_{REF} noise. V_{REF} should be de-coupled with an inductance of ≤ 3nH.

2. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}

3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.

4. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a VREF envelop that has been bandwidth limited to 200MHZ.

5. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the dc level of the same.

DDR SDRAM IDD spec table

(V_{DD}=2.7V, T = 10°C)

Symbol		K4H511638D-KC(L)B3 (DDR333)	K4H511638D-KC(L)A2/CB0 (DDR266A/B)	K4H511638D-KC(L)A0 (DDR200)	Unit	Notes
IDD0		180	160	150	mA	
IDD1		240	220	200	mA	
IDD2P		6	6	6	mA	
IDD2F		50	40	36	mA	
IDD2Q		40	36	32	mA	
IDD3P		70	60	50	mA	
IDD3N		110	90	80	mA	
IDD4R		340	280	240	mA	
IDD4W		340	280	230	mA	
IDD5		360	330	300	mA	
IDD6	Normal	6	6	6	mA	
	Low power	3	3	3	mA	Optional
IDD7A		650	560	470	mA	

AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	VIH(AC)	VREF + 0.31		V	3
Input Low (Logic 0) Voltage, DQ, DQS and DM signals.	VIL(AC)		VREF - 0.31	V	3
Input Differential Voltage, CK and $\overline{CK}$ inputs	VID(AC)	0.7	VDDQ+0.6	V	1
Input Crossing Point Voltage, CK and $\overline{CK}$ inputs	VIX(AC)	0.5*VDDQ-0.2	0.5*VDDQ+0.2	V	2

Note 1. VID is the magnitude of the difference between the input level on CK and the input on $\overline{CK}$.

2. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same.

3. These parameters should be tested at the pim on actual components and may be checked at either the pin or the pad in simu lation. the AC and DC input specificatims are refation to a Vref envelope that has been bandwidth limited 20MHz.

Overshoot/Undershoot specification

Parameter	Specification	
	Address & Control pins	Data pins
Maximum peak amplitude allowed for overshoot	1.6 V	1.2V
Maximum peak amplitude allowed for undershoot	1.6 V	1.2V
The area between the overshoot signal and VDD must be less than or equal to	4.5 V-ns	2.5 V-ns
The area between the undershoot signal and GND must be less than or equal to	4.5 V-ns	2.5 V-ns

AC Timming Parameters & Specifications

Parameter		Symbol	KCB3 (DDR333)		-KCA2 (DDR266A)		-KCB0 (DDR266B)		-KCA0 (DDR200)		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max		
Row cycle time		tRC	60		65		65		70		ns	
Refresh row cycle time		tRFC	72		75		75		80		ns	
Row active time		tRAS	42	70K	45	120K	45	120K	48	120K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD	18		20		20		20		ns	
Row precharge time		tRP	18		20		20		20		ns	
Row active to Row active delay		tRRD	12		15		15		15		ns	
Write recovery time		tWR	15		15		15		15		ns	
Last data in to Read command		tWTR	1		1		1		1		tCK	
Col. address to Col. address delay		tCCD	1		1		1		1		tCK	
Clock cycle time	CL=2.0	tCK	7.5	12	7.5	12	10	12	10	12	ns	5
	CL=2.5		6	12	7.5	12	7.5	12			ns	5
Clock high level width		tCH	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
Clock low level width		tCL	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
DQS-out access time from CK/$\overline{CK}$		tDQSCK	-0.6	+0.6	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns	
Output data access time from CK/$\overline{CK}$		tAC	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns	
Data strobe edge to ouput data edge		tDQSQ	-	0.45	-	0.5	-	0.5	-	0.6	ns	5
Read Preamble		tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	tCK	
Read Postamble		tRPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
CK to valid DQS-in		tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	tCK	
DQS-in setup time		tWPRES	0		0		0		0		ns	2
DQS-in hold time		tWPRE	0.25		0.25		0.25		0.25		tCK	
DQS falling edge to CK rising-setup time		tDSS	0.2		0.2		0.2		0.2		tCK	
DQS falling edge from CK rising-hold time		tDSH	0.2		0.2		0.2		0.2		tCK	
DQS-in high level width		tDQSH	0.35		0.35		0.35		0.35		tCK	
DQS-in low level width		tDQSL	0.35		0.35		0.35		0.35		tCK	
DQS-in cycle time		tDSC	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	tCK	
Address and Control Input setup time(fast)		tIS	0.75		0.9		0.9		1.1		ns	6
Address and Control Input hold time(fast)		tIH	0.75		0.9		0.9		1.1		ns	6
Address and Control Input setup time(slow)		tIS	0.8		1.0		1.0		1.1		ns	6
Address and Control Input hold time(slow)		tIH	0.8		1.0		1.0		1.1		ns	6
Data-out high impedence time from CK/$\overline{CK}$		tHZ	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns	
Data-out low impedence time from CK/$\overline{CK}$		tLZ	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns	
Input Slew Rate(for input only pins)		tSL(I)	0.5		0.5		0.5		0.5		V/ns	6
Input Slew Rate(for I/O pins)		tSL(IO)	0.5		0.5		0.5		0.5		V/ns	7
Output Slew Rate(x4,x8)		tSL(O)	1.0	4.5	1.0	4.5	1.0	4.5	1.0	4.5	V/ns	10
Output Slew Rate Matching Ratio(rise to fall)		tSLMR	0.67	1.5	0.67	1.5	0.67	1.5	0.67	1.5		

Parameter	Symbol	-KCB3 (DDR333)		-KCA2 (DDR266A)		-KCB0 (DDR266B)		-KCA0 (DDR200)		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Mode register set cycle time	tMRD	12		15		15		16		ns	
DQ & DM setup time to DQS	tDS	0.45		0.5		0.5		0.6		ns	7,8,9
DQ & DM hold time to DQS	tDH	0.45		0.5		0.5		0.6		ns	7,8,9
Control & Address input pulse width	tIPW	2.2		2.2		2.2		2.5		ns	
DQ & DM input pulse width	tDIPW	1.75		1.75		1.75		2		ns	
Power down exit time	tPDEX	6		7.5		7.5		10		ns	
Exit self refresh to non-Read command	tXSNR	75		75		75		80		ns	4
Exit self refresh to read command	tXSRD	200		200		200		200		tCK	
Refresh interval time	tREFI	7.8		7.8		7.8		7.8		us	1
Output DQS valid window	tQH	tHP -tQHS	-	tHP -tQHS	-	tHP -tQHS	-	tHP -tQHS	-	ns	5
Clock half period	tHP	tCLmin or tCHmin	-	tCLmin or tCHmin	-	tCLmin or tCHmin	-	tCLmin or tCHmin	-	ns	
Data hold skew factor	tQHS		0.55		0.75		0.75		0.8	ns	
DQS write postamble time	tWPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	3
Active to Read with Auto precharge command	tRAP	20		20		20		20			
Autoprecharge write recovery + Precharge time	tDAL	(tWR/tCK) + (tRP/tCK)		(tWR/tCK) + (tRP/tCK)		(tWR/tCK) + (tRP/tCK)		(tWR/tCK) + (tRP/tCK)		tCK	11

1. Maximum burst refresh cycle : 8
2. The specific requirement is that DQS be valid(High or Low) on or before this CK edge. The case shown(DQS going from High_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on tDQSS.
3. The maximum limit for this parameter is not a device limit. The device will operate with a great value for this parameter, but system performance (bus turnaround) will degrade accordingly.
4. A write command can be applied with t_{RCD} satisfied after this command.
5. For registered DIMMs, t_{CL} and t_{CH} are ≥ 45% of the period including both the half period jitter ($t_{JIT(HP)}$) of the PLL and the half period jitter due to crosstalk ($t_{JIT(crosstalk)}$) on the DIMM.
6. Input Setup/Hold Slew Rate Derating

Input Setup/Hold Slew Rate	ΔtIS	ΔtIH
(V/ns)	(ps)	(ps)
0.5	0	0
0.4	+50	+50
0.3	+100	+100

This derating table is used to increase t_{IS}/t_{IH} in the case where the input slew rate is below 0.5V/ns. Input setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

7. I/O Setup/Hold Slew Rate Derating

I/O Setup/Hold Slew Rate	ΔtDS	ΔtDH
(V/ns)	(ps)	(ps)
0.5	0	0
0.4	+75	+75
0.3	+150	+150

This derating table is used to increase t_{DS}/t_{DH} in the case where the I/O slew rate is below 0.5V/ns. I/O setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

8. I/O Setup/Hold Plateau Derating

I/O Input Level	ΔtDS	ΔtDH
(mV)	(ps)	(ps)
± 280	+50	+50

This derating table is used to increase tDS/tDH in the case where the input level is flat below VREF ± 310mV for a duration of up to 2ns.

9. I/O Delta Rise/Fall Rate(1/slew-rate) Derating

Delta Rise/Fall Rate	ΔtDS	ΔtDH
(ns/V)	(ps)	(ps)
0	0	0
±0.25	+50	+50
±0.5	+100	+100

This derating table is used to increase t_{DS}/t_{DH} in the case where the DQ and DQS slew rates differ. The Delta Rise/Fall Rate is calated as 1/SlewRate1-1/SlewRate2. For example, if slew rate 1 = 5V/ns and slew rate 2 =.4V/ns then the Delta Rise/Fall Rate =-0/5ns/V. Input S/H slew rate based on larger of AC-AC delta rise/fall rate and DC-DC delta rise/fall rate.

10. This parameter is fir system simulation purpose. It is guranteed by design.
11. For each of the terms, if not already an integer, round to the next highest integer. tCK is actual to the system clock cycle time.

<Reference>

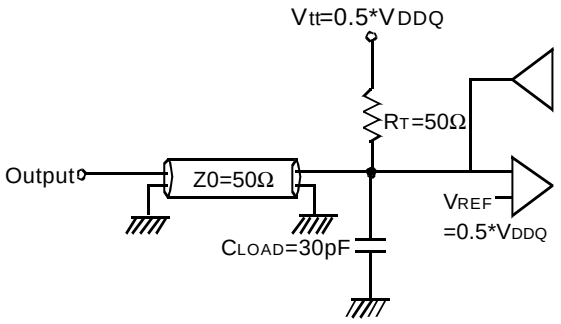
The following table specifies derating values for the specifications listed if the single-ended clock skew rate is less than 1.0V/ns.

CK slew rate (Single ended)	ΔtIH/tIS (ps)	ΔtDSS/tDSH (ps)	ΔtAC/tDQSCK (ps)	ΔtLZ(min) (ps)	ΔtHZ(max) (ps)
1.0V/ns	0	0	0	0	0
0.75V/ns	+50	+50	+50	-50	+50
0.5V/ns	+100	+100	+100	-100	+100

AC Operating Test Conditions

(VDD=2.5V, VDDQ=2.5V, TA= 0 to 70°C)

Parameter	Value	Unit	Note
Input reference voltage for Clock	0.5 * VDDQ	V	
Input signal maximum peak swing	1.5	V	
Input signal minimum slew rate	1.0	V/ns	
Input Levels(VIH/VIL)	VREF+0.31/VREF-0.31	V	
Input timing measurement reference level	VREF	V	
Output timing measurement reference level	Vtt	V	
Output load condition	See Load Circuit		



Output Load Circuit (SSTL_2)

Input/Output Capacitance

(VDD=2.5, VDDQ=2.5V, TA= 25°C, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A12, BA0 ~ BA1, CKE, $\overline{CS}$, $\overline{RAS}$,$\overline{CAS}$, $\overline{WE}$)	CIN1	4.0	6.0	pF
Input capacitance(CK, $\overline{CK}$)	CIN2	4.0	6.0	pF
Data & DQS input/output capacitance	COUT	4.0	6.0	pF
Input capacitance(DM)	CIN3	4.0	6.0	pF