TOSHIBA Bi-CMOS Integrated Circuit Silicon Monolithic

TB62726AN,TB62726AF

16-bit Constant-Current LED Driver with Operating Voltage of 3.3-V and 5-V

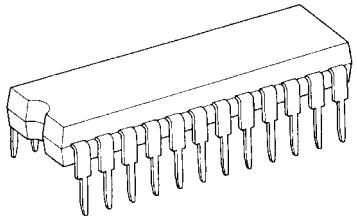
The TB62726A series are comprised of constant-current drivers designed for LEDs and LED displays. The output current value can be set using an external resistor.

As a result, all outputs will have virtually the same current levels.

This driver incorporates 16-bit constant-current outputs, a 16-bit shift register, a 16-bit latch and a 16-bit AND-gate circuit.

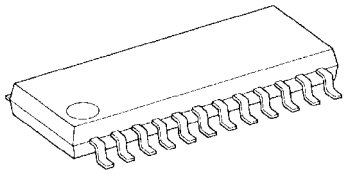
These drivers have been designed using the Bi-CMOS process.

TB62726AN



SDIP24-P-300-1.78

TB62726AF



SSOP24-P-300-1.00B

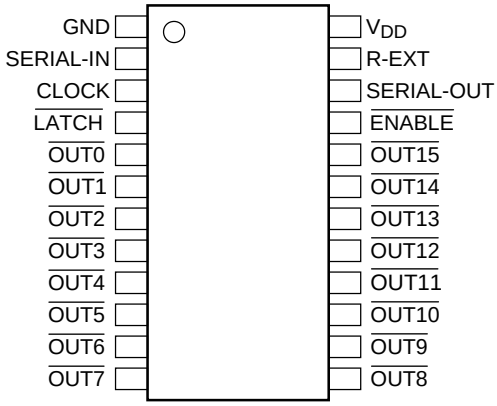
Weight
SDIP24-P-300-1.78: 1.22 g (Typ.)
SSOP24-P-300-1.00B: 0.32 g (Typ.)

Features

- Output current capability and number of outputs: 90 mA × 16 outputs
- Constant current range: 2 to 90 mA
- Application output voltage: 0.7 V (output current 2 to 80 mA)
  0.4 V (output current 2 to 40 mA)
- For anode-common LEDs
- Input signal voltage level: 3.3-V and 5-V CMOS level (Schmitt trigger input)
- Power supply voltage range V_{DD} = 3.0 to 5.5 V
- Maximum output terminal voltage: 17 V
- Serial and parallel data transfer rate: 20 MHz (max, cascade connection)
- Operating temperature range T_{opr} = −40 to 85°C
- Package: Type AN: SDIP24-P-300-1.78
  Type AF: SSOP24-P-300-1.00B
- Current accuracy (All output ON)

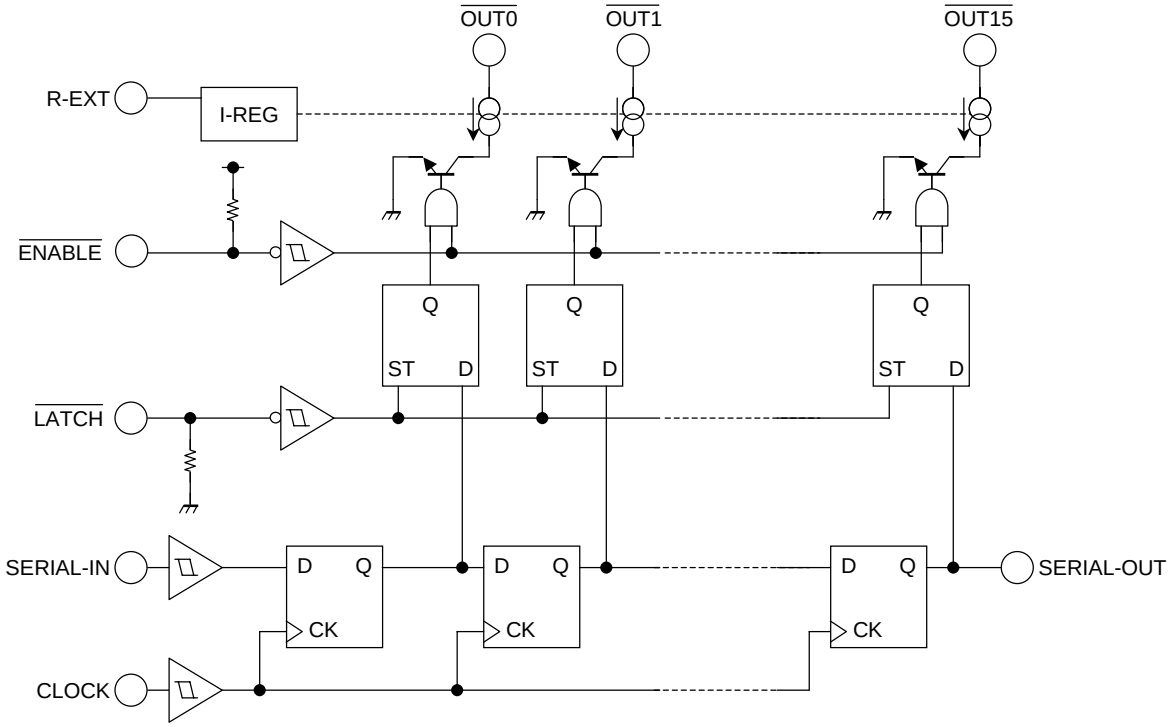
Output Voltage	Current Accuracy		Output Current
	Between Bits	Between ICs	
≧ 0.4 V	±4%	±15%	2 to 5 mA
≧ 0.7 V		±12%	5 to 80 mA

Pin Assignment (top view)



Warnings: Short-circuiting an output terminal toGND or to the power supply terminal may broken the device.
Please take care when wiring the output terminals, the power supply terminal and the GND terminals.

Block Diagram

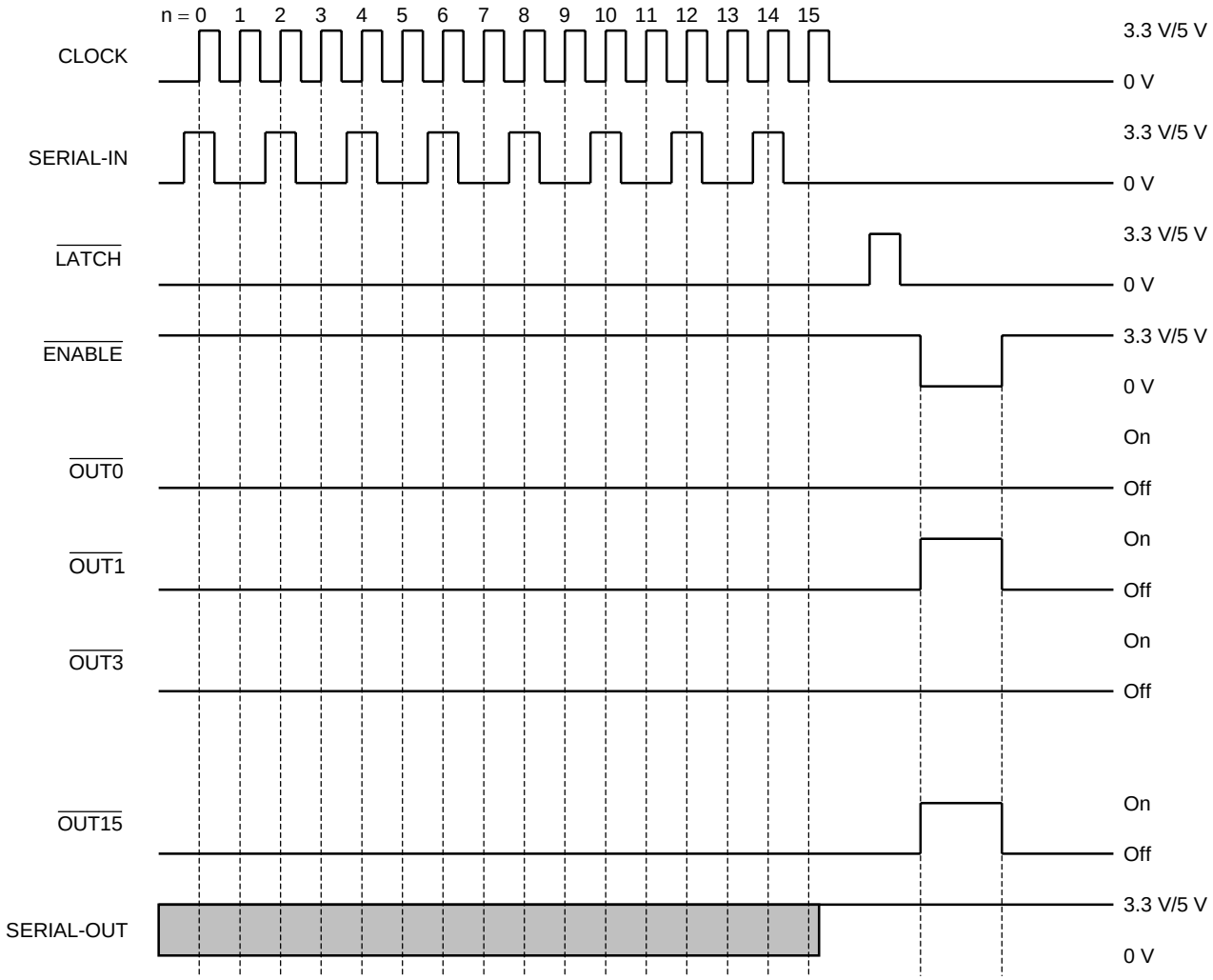


Truth Table

CLOCK	LATCH	ENABLE	SERIAL-IN	OUT0 ⋯ OUT7 ⋯ OUT15	SERIAL-OUT
↑	H	L	Dn	Dn ⋯ Dn – 7 ⋯ Dn – 15	Dn – 15
↑	L	L	Dn + 1	No change	Dn – 14
↑	H	L	Dn + 2	Dn + 2 ⋯ Dn – 5 ⋯ Dn – 13	Dn – 13
↓	X	L	Dn + 3	Dn + 2 ⋯ Dn – 5 ⋯ Dn – 13	Dn – 13
↓	X	H	Dn + 3	OFF	Dn – 13

Note 1: OUT0 to OUT15 = On when Dn = H; OUT0 to OUT15 = Off when Dn = L.
In order to ensure that the level of the power supply voltage is correct, an external resistor must be connected between R-EXT and GND.

Timing Diagram



Warning: Latch circuit is leveled-latch circuit. Be careful because it is not triggered-latch circuit.

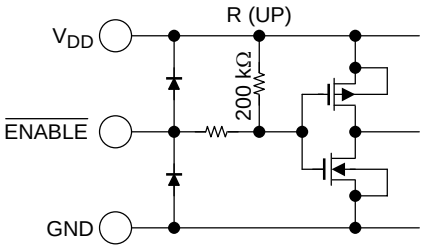
Note 2: The latches circuit holds data by pulling the $\overline{\text{LATCH}}$ terminal Low.
And, when $\overline{\text{LATCH}}$ terminal is a High level, latch circuit doesn't hold data, and it passes from the input to the output.
When $\overline{\text{ENABLE}}$ terminal is a Low level, output terminal $\overline{\text{OUT0}}$ to $\overline{\text{OUT15}}$ respond to the data, and on and off does.
And, when $\overline{\text{ENABLE}}$ terminal is a High level, it offs with the output terminal regardless of the data.

Terminal Description

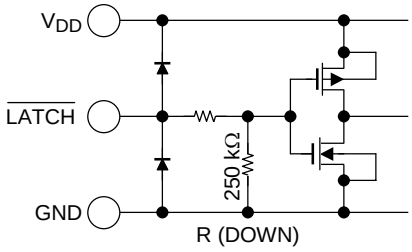
Pin No.	Pin Name	Function
1	GND	GND terminal for control logic
2	SERIAL-IN	Input terminal for serial data for data shift register
3	CLOCK	Input terminal for clock for data shift on rising edge
4	$\overline{\text{LATCH}}$	Input terminal for data strobe When the $\overline{\text{LATCH}}$ input is driven High, data is not latched. When it is pulled Low, data is latched.
5 to 20	$\overline{\text{OUT0}}$ to $\overline{\text{OUT15}}$	Constant-current output terminals
21	$\overline{\text{ENABLE}}$	Input terminal for output enable. All outputs ($\overline{\text{OUT0}}$ to $\overline{\text{OUT15}}$) are turned off, when the $\overline{\text{ENABLE}}$ terminal is driven High. And are turned on, when the terminal is driven Low.
22	SERIAL-OUT	Output terminal for serial data input on SERIAL-IN terminal
23	R-EXT	Input terminal used to connect an external resistor. This regulated the output current.
24	V_{DD}	3.3-V/5-V supply voltage terminal

Equivalent Circuits for Inputs and Outputs

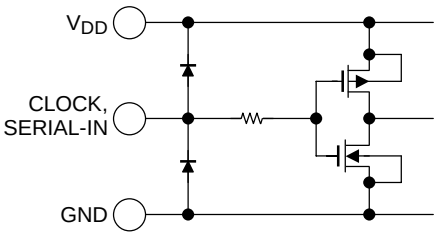
1. $\overline{\text{ENABLE}}$ terminal



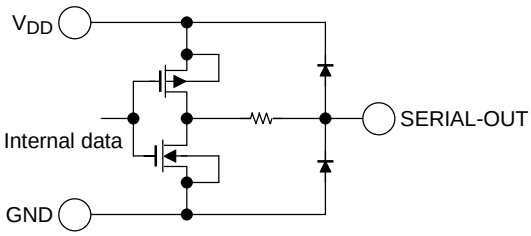
2. $\overline{\text{LATCH}}$ terminal



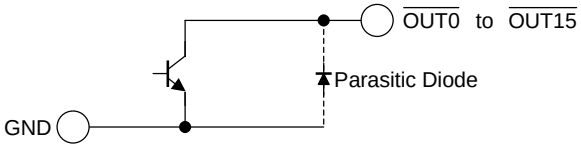
3. CLOCK, SERIAL-IN terminal



4. SERIAL-OUT terminal



5. $\overline{\text{OUT0}}$ to $\overline{\text{OUT15}}$ terminals



Maximum Ratings (T_{opr} = 25°C)

Characteristics		Symbol	Rating	Unit
Supply voltage		V_{DD}	6	V
Input voltage		V_{IN}	−0.2~V_{DD} + 0.2	V
Output current		I_{OUT}	+90	mA/ch
Output voltage		V_{OUT}	−0.2 to 17	V
Power dissipation (Note 3)	AN-type (when not mounted)	P_{d1}	1.25	W
	AN-type (on PCB)		1.78	
	AF-type (when not mounted)	P_{d2}	0.83	
	AF-type (on PCB)		1.00	
Thermal resistance (Note 3)	AN-type (when not mounted)	$R_{th\ (j\text{-}a)\ 1}$	104	°C/W
	AN-type (on PCB)		70	
	AF-type (when not mounted)	$R_{th\ (j\text{-}a)\ 2}$	140	
	AF-type (on PCB)		120	
Operating temperature		T_{opr}	−40 to 85	°C
Storage temperature		T_{stg}	−55 to 150	°C

Note 3: AN-Type: Powers dissipation is derated by 14.28 mW/°C if device is mounted on PCB and ambient temperature is above 25°C.
AF-Type: Powers dissipation is derated by 6.67 mW/°C if device is mounted on PCB and ambient temperature is above 25°C.

With device mounted on glass-epoxy PCB of less than 40% Cu and of dimensions 50 mm × 50 mm × 1.6 mm.

Recommended Operating Conditions (T_{opr} = –40°C to 85°C unless otherwise specified)

Characteristics	Symbol	Conditions	Min	Typ.	Max	Unit
Supply voltage	V_{DD}	—	3	—	5.5	V
Output voltage	V_{OUT}	—	—	0.7	4	V
Output current	I_{OUT}	Each DC 1 circuit	2	—	80	mA/ch
	I_{OH}	SERIAL-OUT	—	—	−1	mA
	I_{OL}	SERIAL-OUT	—	—	1	
Input voltage	V_{IH}	—	0.7 × V_{DD}	—	V_{DD} + 0.15	V
	V_{IL}		−0.15	—	0.3 × V_{DD}	
Clock frequency	f_{CLK}	Cascade connected	—	—	20	MHz
$\overline{\text{LATCH}}$ pulse width	t_{wLAT}		50	—	—	ns
CLOCK pulse width	t_{wCLK}	—	25	—	—	ns
ENABLE pulse width (Note 4)	t_{wENA}	Upper I_{OUT} = 20 mA	2000	—	—	ns
		Lower I_{OUT} = 20 mA	3000	—	—	
Set-up time for CLOCK terminal	t_{SETUP1}	—	10	—	—	ns
Hold time for CLOCK terminal	t_{HOLD}		10	—	—	ns
Set-up time for $\overline{\text{LATCH}}$ terminal	t_{SETUP2}		50	—	—	ns

Note 4: When the pulse of the Low level is inputted to the $\overline{\text{ENABLE}}$ terminal held in the High level.

Electrical Characteristics (T_{opr} = 25°C, V_{DD} = 3.0 V to 5.5 V unless otherwise specified)

Characteristics	Symbol	Conditions		Min	Typ.	Max	Unit
Supply voltage	V_{DD}	Normal operation		3.0	—	5.5	V
Output current	I_{OUT1}	V_{OUT} = 0.4 V, V_{DD} = 3.3 V	R_{EXT} = 490 Ω	31.96	36.20	40.54	mA
	I_{OUT2}	V_{OUT} = 0.4 V, V_{DD} = 5 V		31. 59	35.90	40.20	
	I_{OUT3}	V_{OUT} = 0.7 V, V_{DD} = 3.3 V	R_{EXT} = 250 Ω	63.63	72.30	80.97	
	I_{OUT4}	V_{OUT} = 0.7 V, V_{DD} = 5 V		62.75	71.30	79.95	
Output current error between bits	ΔI_{OUT1}	$V_{OUT} \geqq$ 0.4 V, All outputs ON	R_{EXT} = 490 Ω	—	±1	±4	%
	ΔI_{OUT2}	$V_{OUT} \geqq$ 0.4 V, All outputs ON	R_{EXT} = 250 Ω				
Output leakage current input voltage	I_{OZ}	V_{OUT} = 15.0 V		—	—	1	μA
Input voltage	V_{IN}	—		0.7 V_{DD}	—	V_{DD}	V
		—		GND	—	0.3 V_{DD}	
SOUT terminal voltage	V_{OL}	I_{OL} = 1.0 mA, V_{DD} = 3.3 V		—	—	0.3	V
		I_{OL} = 1.0 mA, V_{DD} = 5 V		—	—	0.3	
	V_{OH}	I_{OH} = − 1.0 mA, V_{DD} = 3.3 V		3	—	—	
		I_{OH} = 1.0 mA, V_{DD} = 5 V		4.7	—	—	
Output current Supply voltage Regulation	%/V_{DD}	When V_{DD} is changed 3 V to 5.5 V		—	−1	−5	%
Pull-up resistor	$R_{(Up)}$	$\overline{ENABLE}$ terminal		115	230	460	kΩ
Pull-down resistor	$R_{(Down)}$	$\overline{LATCH}$ terminal					
Supply current	$I_{DD\ (OFF)\ 1}$	V_{OUT} = 15.0 V	R_{EXT} = OPEN	—	0.1	0.5	mA
	$I_{DD\ (OFF)\ 2}$	V_{OUT} = 15.0 V, All outputs OFF	R_{EXT} = 490 Ω	1	3.5	5	
	$I_{DD\ (OFF)\ 3}$	V_{OUT} = 15.0 V, All outputs OFF	R_{EXT} = 250 Ω	4	6	9	
	$I_{DD\ (ON)\ 1}$	V_{OUT} = 0.7 V, All outputs ON	R_{EXT} = 490 Ω	—	9	15	
		Same as the above, T_{opr} = −40°C		—	—	20	
	$I_{DD\ (ON)\ 2}$	V_{OUT} = 0.7 V, All outputs ON	R_{EXT} = 250 Ω	—	18	25	
		Same as the above, T_{opr} = −40°C		—	—	40	

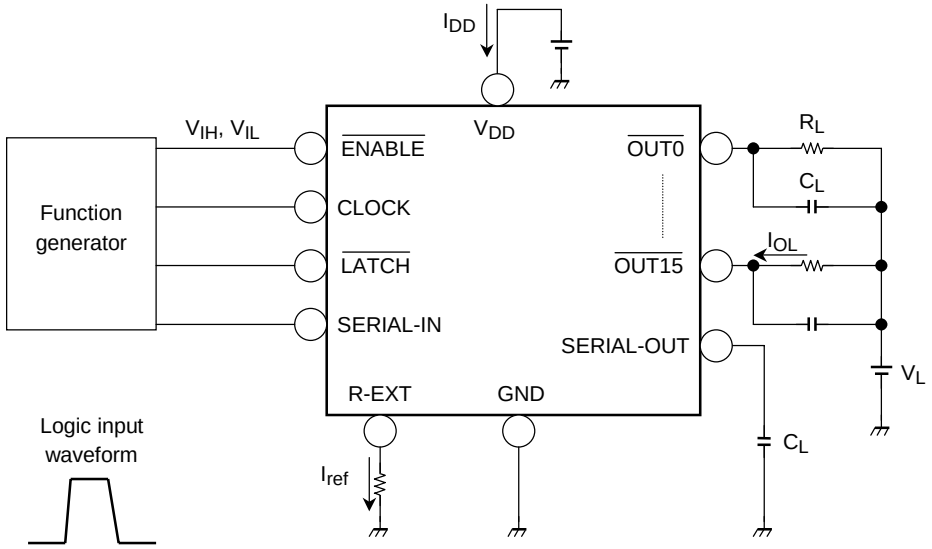
Switching Characteristics (T_{opr} = 25°C unless otherwise specifed)

Characteristics	Symbol	Conditions	Min	Typ.	Max	Unit
Propagation delay	t_{pLH1}	CLK- $\overline{OUTn}$, $\overline{LATCH}$ = "H", $\overline{ENABLE}$ = "L"	—	150	300	ns
	t_{pLH2}	$\overline{LATCH}$ - $\overline{OUTn}$, $\overline{ENABLE}$ = "L"	—	140	300	
	t_{pLH3}	$\overline{ENABLE}$ - $\overline{OUTn}$, $\overline{LATCH}$ = "H"	—	140	300	
	t_{pLH}	CLK-SERIAL OUT	3	6	—	
	t_{pHL1}	CLK- $\overline{OUTn}$, $\overline{LATCH}$ = "H", $\overline{ENABLE}$ = "L"	—	170	340	
	t_{pHL2}	$\overline{LATCH}$ - $\overline{OUTn}$, $\overline{ENABLE}$ = "L"	—	170	340	
	t_{pHL3}	$\overline{ENABLE}$ - $\overline{OUTn}$, $\overline{LATCH}$ = "H"	—	170	340	
	t_{pLH}	CLK-SERIAL OUT	4	7	—	
Output rise time	t_{or}	10~90% of voltage waveform	40	85	150	ns
Output fall time	t_{of}	90~10% of voltage waveform	40	70	150	ns
Maximum CLOCK rise time	t_r	When not on PCB	—	—	5	μs
Maximum CLOCK fall time	t_f	(Note 5)	—	—	5	μs

Conditions: (Refer to test circuit.)
T_{opr} = 25°C, V_{DD} = V_{IH} = 3.3 V and 5 V, V_{OUT} = 0.7 V, V_{IL} = 0 V, R_{EXT} = 490 Ω,
V_L = 3.0 V, R_L = 60 Ω, C_L = 10.5 pF

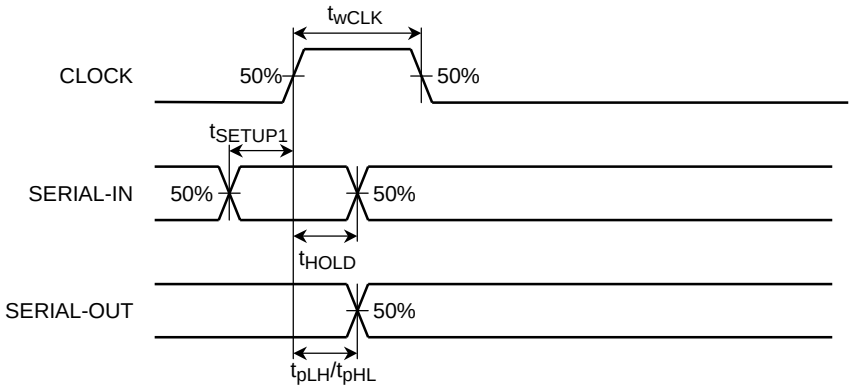
Note 5: If the device is connected in a cascade and t_r/t_f for the waveform is large, it may not be possible to achieve the timing required for data transfer. Please consider the timings carefully.

Test Circuit

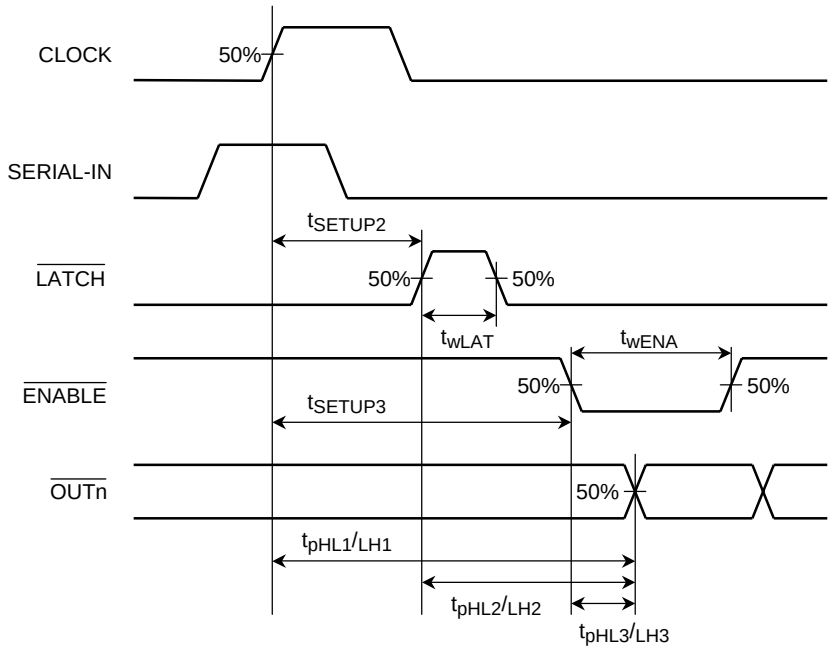


Timing Waveforms

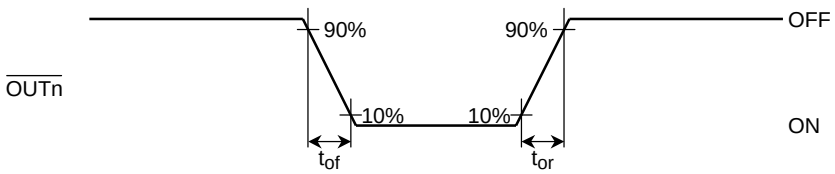
1. CLOCK, SERIAL-IN, SERIAL-OUT



2. CLOCK, SERIAL-IN, $\overline{\text{LATCH}}$, $\overline{\text{ENABLE}}$, $\overline{\text{OUTn}}$

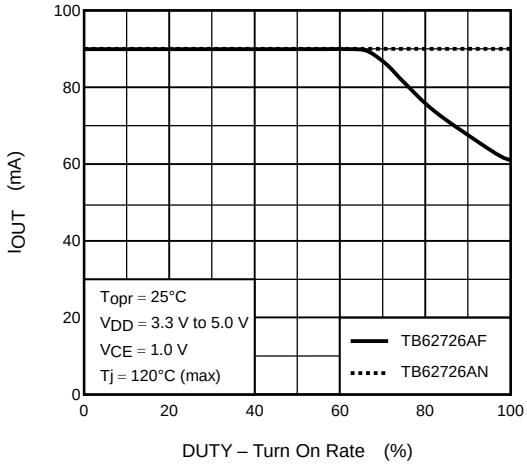


3. $\overline{\text{OUTn}}$

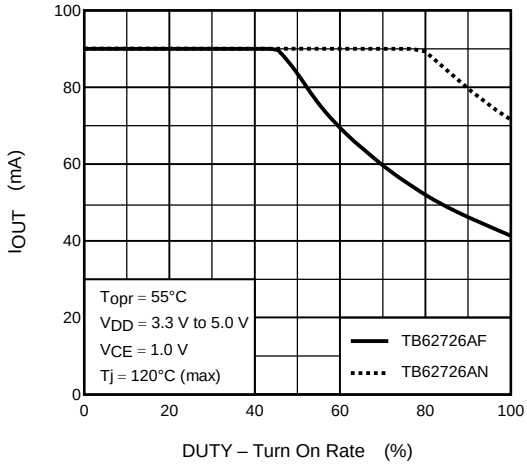


Output Current – Duty (LEDS turn-on rate)

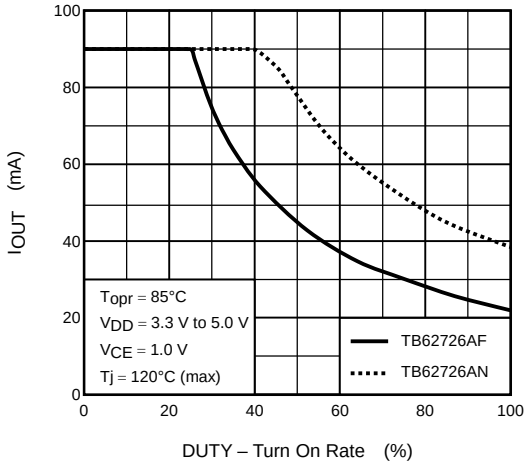
I_{OUT} – DUTY On PCB



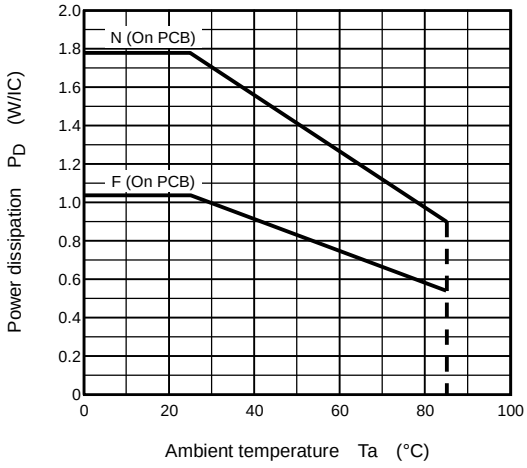
I_{OUT} – DUTY On PCB



I_{OUT} – DUTY On PCB

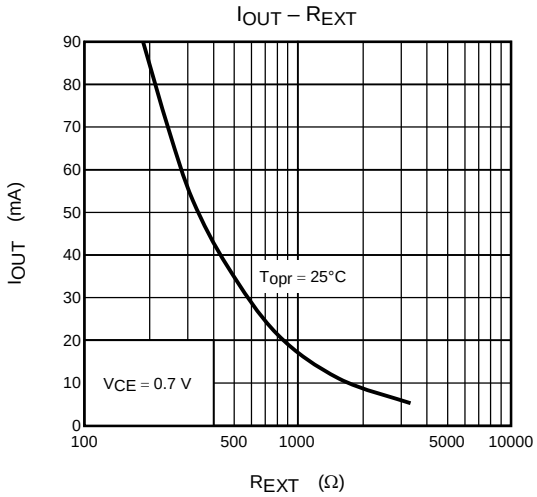


P_d – T_{opr}



Output Current – R_{EXT} Resistor

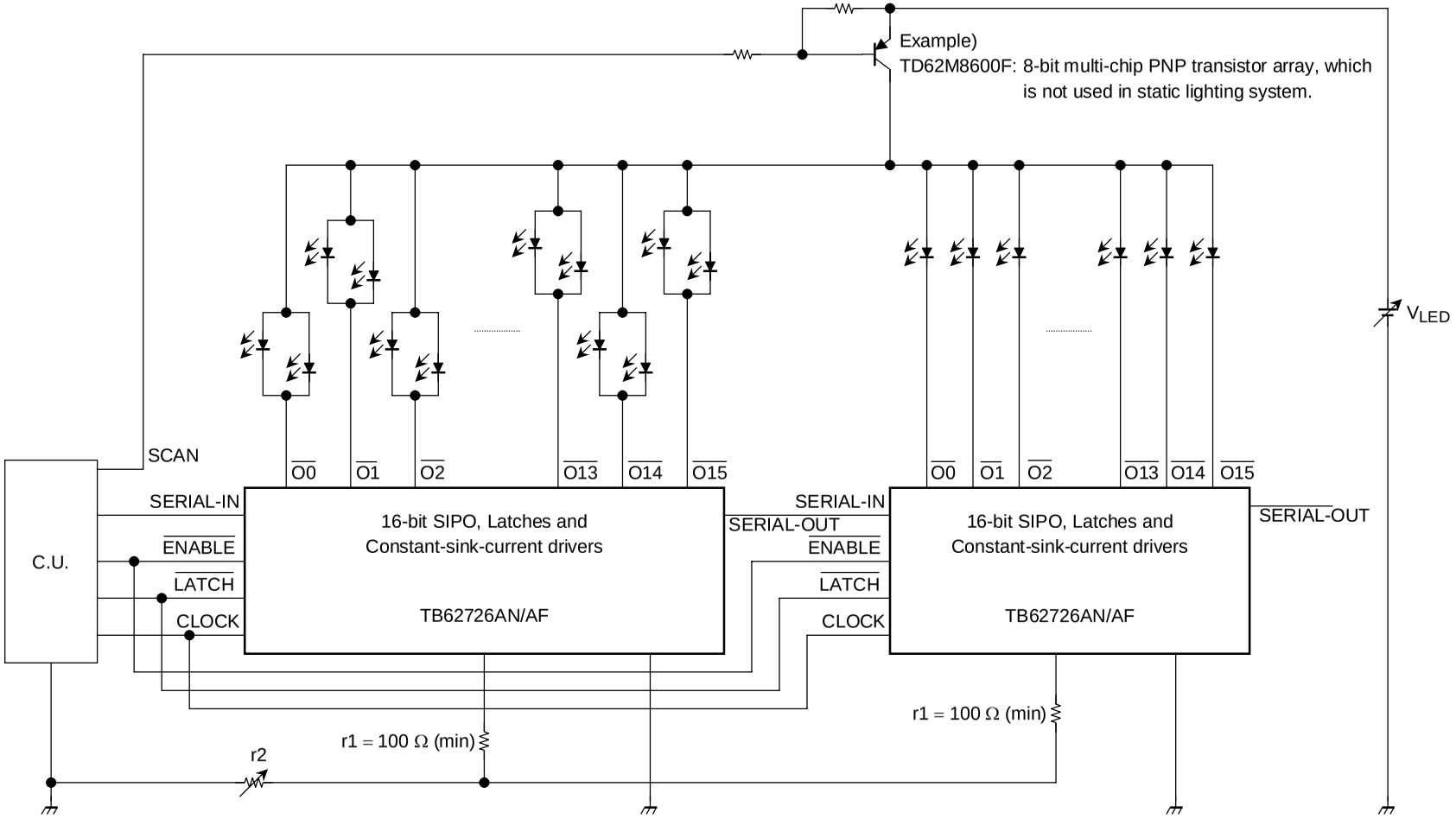
I_{OUT} – R_{EXT}



Application Circuit (example 1): The general composition in static lighting of LED.

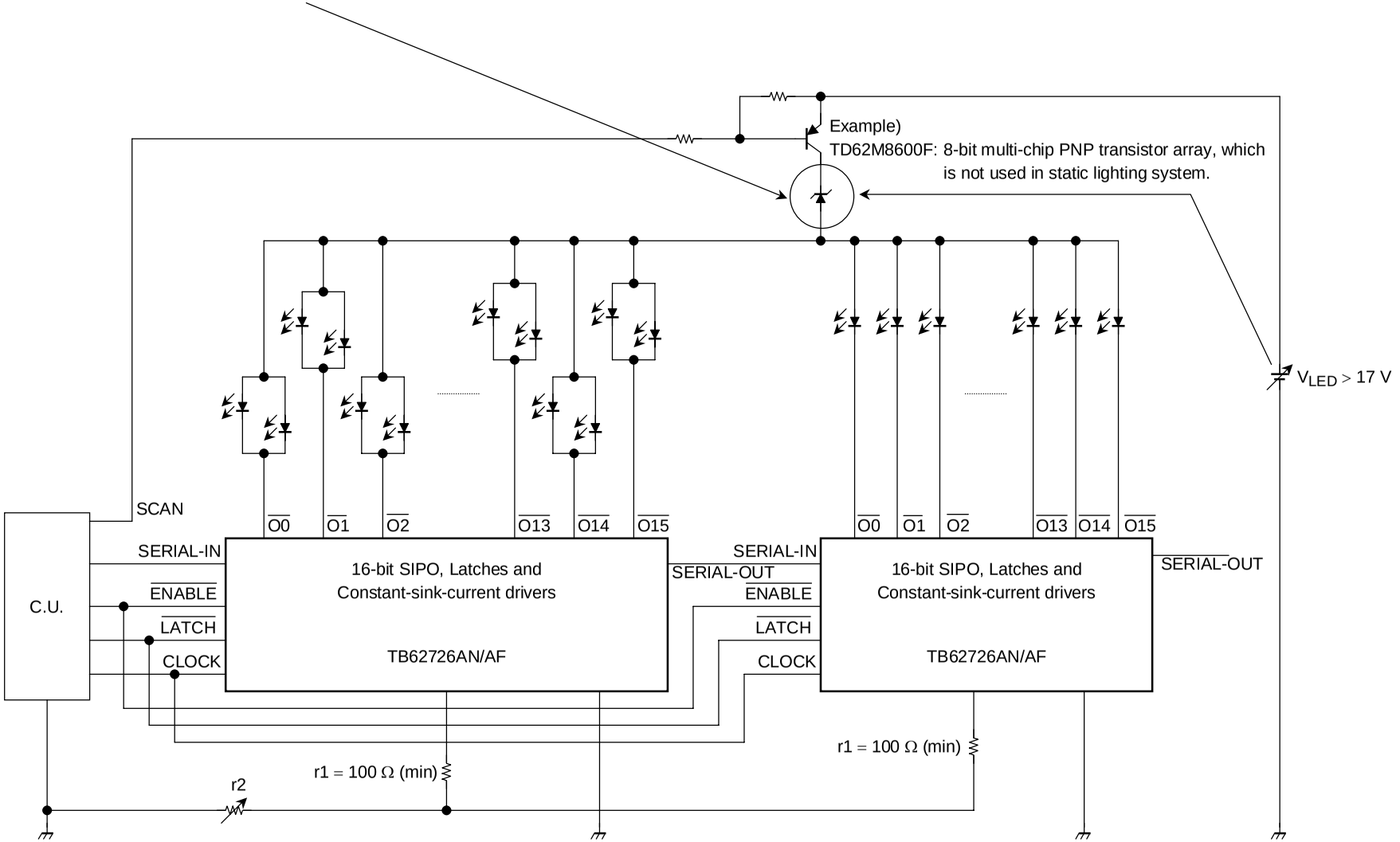
More than VLED (V) ≧ Vf (total max) +0.7 is recommended with the following application circuit with the LED power supply VLED.

r1: The setup resistance for the setup of output current of every IC.
r2: The variable resistance for the brightness control of every LED module.



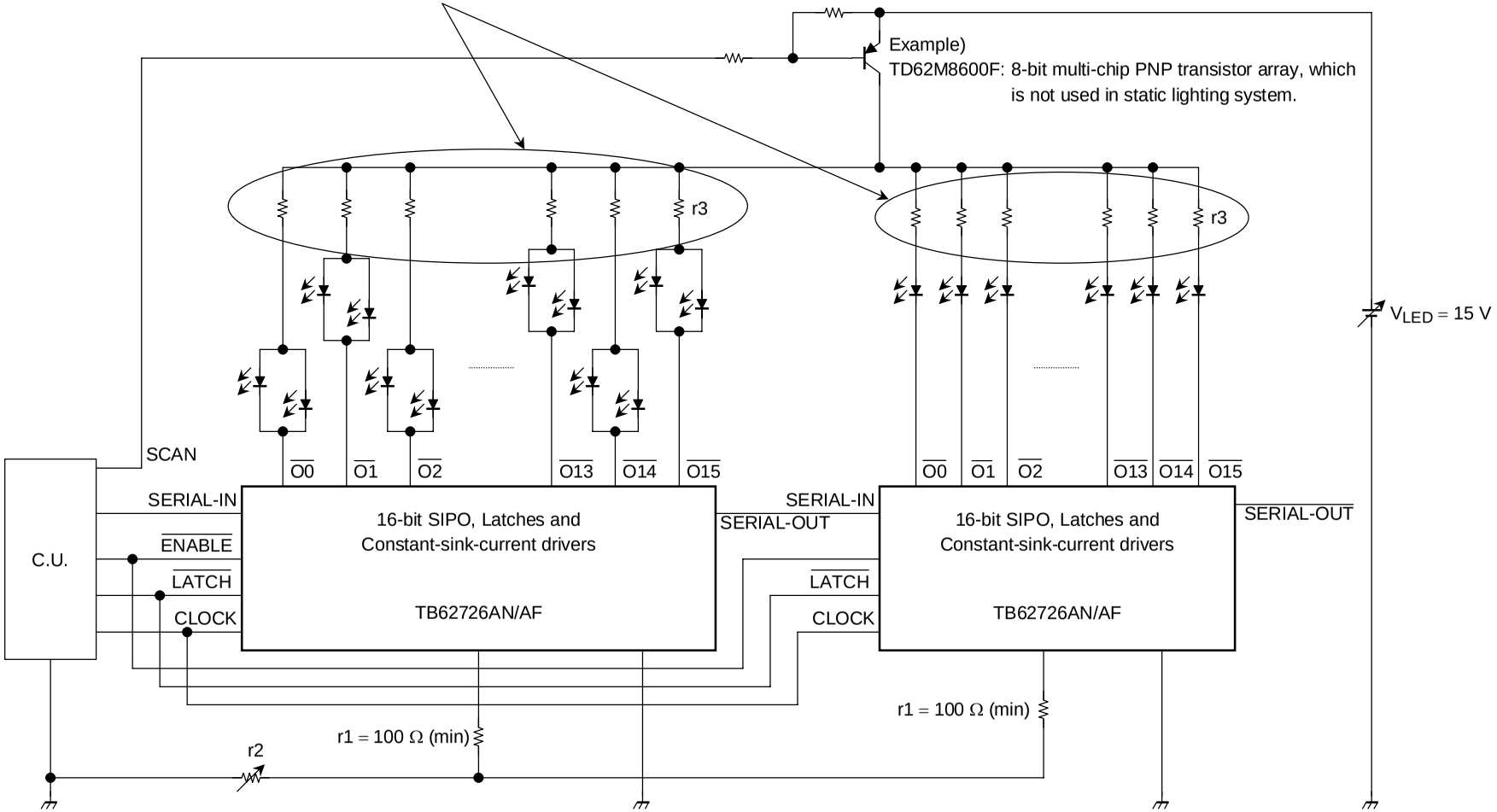
Application Circuit (example 2): When the condition of VLED is VLED > 17 V

The unnecessary voltage is one effective technique as to making the voltage descend with the zenor diode.



Application Circuit (example 3): When the condition of VLED is Vf +0.7 < VLED < 17 V

VOUT = VLED-Vf = 0.7~1.0 V is the most suitable for VOUT.
Surplus VOUT causes an IC fever and the useless consumption electric power.
It is the one way of being effective to build in the r3 in this problem.
r3 can make a calculation to the formula r3 Ω = surplus VOUT/IOUT.
Though the resistance parts increase, the fixed constant current performance is kept



Notes

- Operation may become unstable due to the electromagnetic interference caused by the wiring and other phenomena.
  To counter this, it is recommended that the IC be situated as close as possible to the LED module.
  If overvoltage is caused by inductance between the LED and the output terminals, both the LED and the terminals may suffer damage as a result.

- There is only one GND terminal on this device when the inductance in the GND line and the resistor are large, the device may malfunction due to the GND noise when output switchings by the circuit board pattern and wiring.
  To achieve stable operation, it is necessary to connect a resistor between the REXT terminal and the GND line.
  Fluctuation in the output waveform is likely to occur when the GND line is unstable or when a capacitor (of more than 50 pF) is used.
  Therefore, take care when designing the circuit board pattern layout and the wiring from the controller.

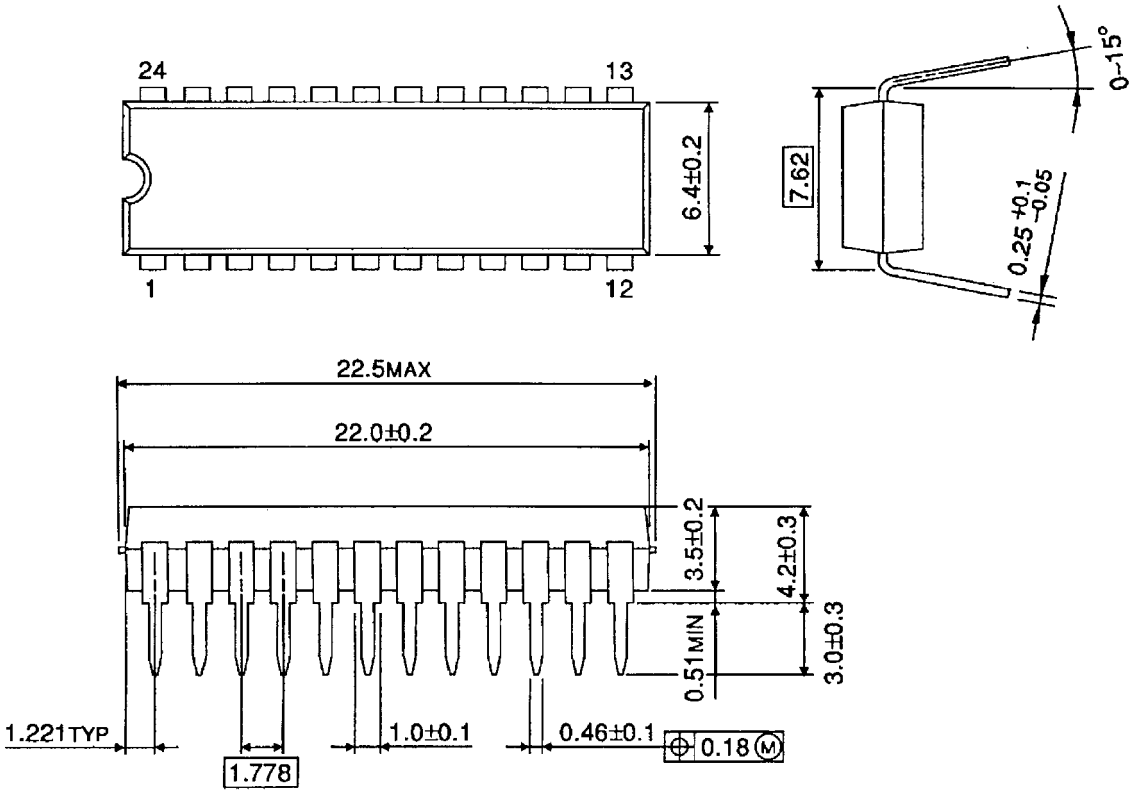
- This application circuit is a reference example and is not guaranteed to work in all conditions.
  Be sure to check the operation of your circuits.

- This device does not include protection circuits for overvoltage, overcurrent or overtemperature.
  If protection is necessary, it must be incorporated into the control circuitry.

- The device is likely to be destroyed if a short-circuit occurs between either of the power supply pins and any of the output terminals when designing circuits, pay special attention to the positions of the output terminals and the power supply terminals (V_{DD} and V_{LED}), and to the design of the GND line.

Package Dimensions

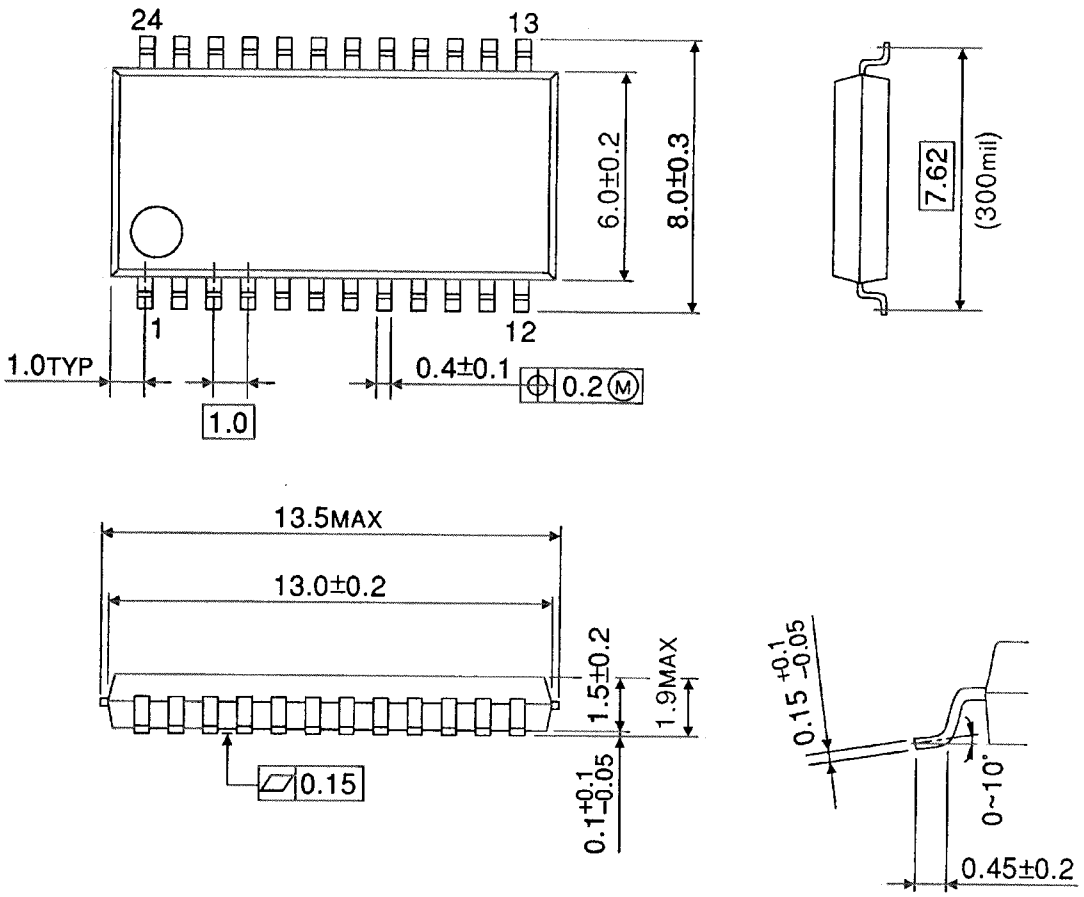
SDIP24-P-300-1.78 Unit : mm



Weight: 1.22 g (typ.)

Package Dimensions

SSOP24-P-300-1.00B Unit : mm



Weight: 0.32 g (typ.)

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000707EBA

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