PS6500 6.5 GHz Fractional-N Frequency Synthesizer

Low-Power Direct Digital Modulation Frequency Synthesizer

Preliminary Datasheet V1.1

Features

- 6.5 GHz operating frequency
- Small step size 400 Hz or less
- High internal reference frequency, up to 25 MHz, enables larger loop bandwidth PLL
- Very fast switching speed (for example, 100 µs with 25 MHz reference frequency)
- Low phase noise floor (for example, -80 dBc/Hz in loop bandwidth)
- Low spurious power (-70 dBc) in loop bandwidth
- Software programmable power-down modes
- Delta-Sigma Fractional-N main and auxiliary synthesizers
- High speed serial interface up to 100 Mbps
- 3 wire programming
- Programmable division ratios on reference frequency
- Phase detectors with programmable gains to provide a programmable loop bandwidth
- Frequency Power Steering™ speeds up acquisition 5x with same loop filter
- On-chip crystal oscillator
- Supports frequency adjust for temperature compensation and automatic frequency control (AFC)
- Direct digital modulation
- 3 volt analog and digital operation
- 5 volt tolerant on digital pins
- Up to 5 volt output to loop filter
- 28-pin EP-TSSOP package

Product Description

The PS6500 Direct Digital Modulation Fractional-N frequency synthesizer provides ultra-fine frequency resolution, fast switching speed, and low phase-noise performance. This synthesizer is a key building block in designing high-performance narrowband and multi-band radio systems that require low power and fine step size.

The ultra-fine step size of less than 400 Hz allows this synthesizer to be used in very narrowband wireless applications. With proper temperature sensing or through control channels, the synthesizer's fine step size can compensate for crystal oscillator or IF filter drift. As a result, crystal oscillators or crystals can replace temperature-compensated or ovenized crystal oscillators, reducing parts count and associated component cost. The PS6500's fine step size can also be used for doppler shift corrections.

The PS6500 has a phase noise floor of -80 dBc/Hz up to 6.5 GHz operation. This is permitted by the on-chip low noise prescalers and low divide ratios provided by the IC's high fractionality.

Reference crystals or oscillators up to 50 MHz can be used with the PS6500. The crystal frequency is divided down by independent programmable dividers (1 to 32) for the main and auxiliary synthesizers. The phase detectors can operate at a maximum speed of 25 MHz, permitting better phase noise due to the lower division value. With a high reference frequency, the loop bandwidths can also be increased. Larger loop bandwidths improve the settling times and reduce in-band phase noise. Typical switching times of less than 100 µs can thus be achieved with a 10 MHz reference. The PS6500's lower in-band phase noise also permits the use of lower cost Voltage Controlled Oscillators (VCOs) in customer applications.

The PS6500 has a Frequency Power Steering™ circuit (patent pending), that assists the loop filter to steer the VCO when the frequency is too fast or too slow. In this configuration, acquisition times of up to five times faster than conventional phase/frequency detectors can be achieved.

The unit operates with a 3-wire, high-speed serial interface. A combination of a large bandwidth, fine resolution, and the 3-wire, high-speed serial interface allows for a direct phase and frequency modulation of the VCO. This supports any constant envelope and continuous phase modulation which means any analog FM or digital FM. This capability can eliminate the need for I & Q DACs, quadrature upconverters, and IF filters from the transmitter portion of the radio system.1

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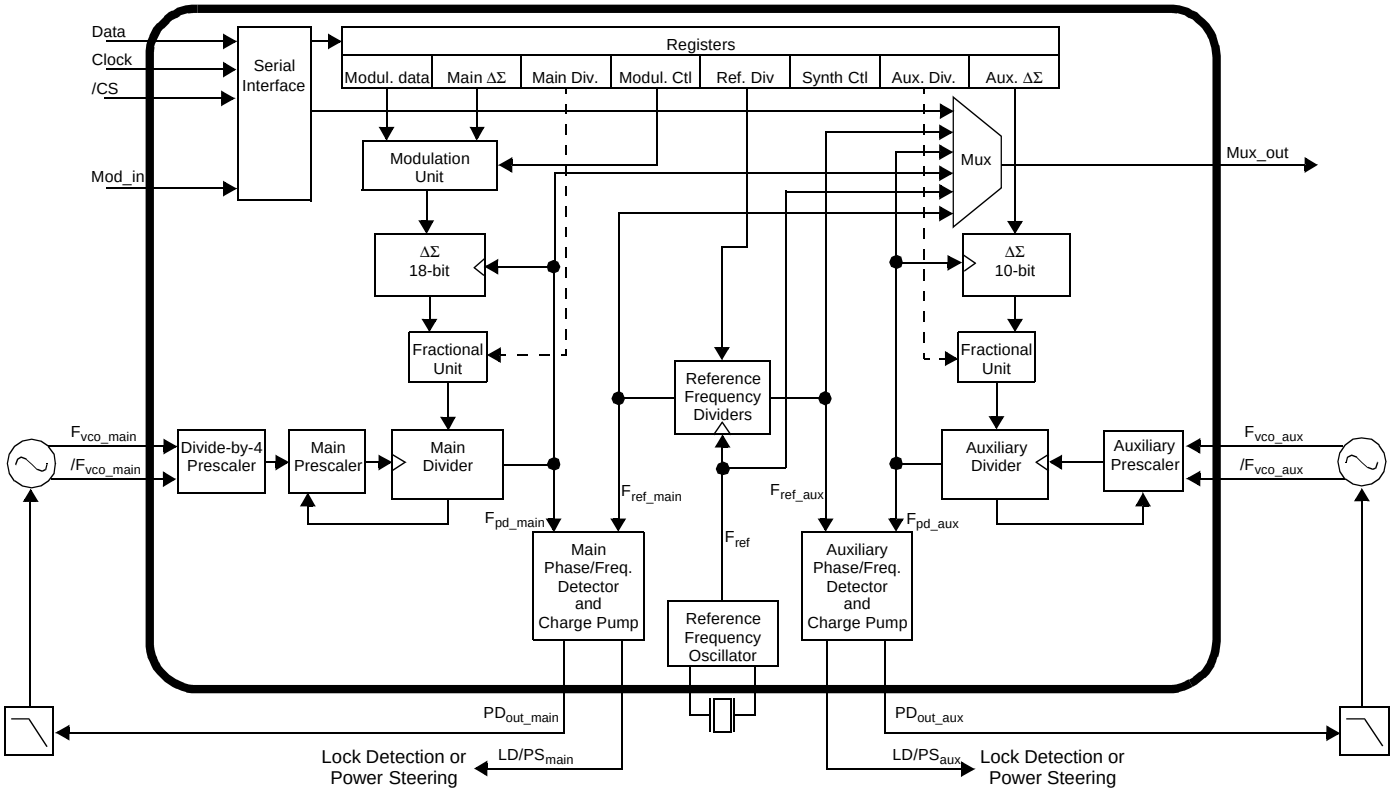
Benefits

The Philsar PS6500 provides has the following benefits:

- Small step size allows for higher internal reference frequency which permits a lower multiplication ratio improving phase noise.
- Lower phase noise permits the use of a wider loop filter bandwidth, which in turn yields a faster frequency switching and acquisition time.
- Small step size allows flexibility in choosing a reference crystal or oscillator frequency, as very narrow channel spacing can be supported.
- The on-chip oscillator permits use of a crystal instead of a crystal oscillator lowering the system cost.
- Programmable phase detector gain allows for variable loop filer bandwidths. Frequency switching and acquisition times can be improved by opening up the bandwidth, and subsequently lower phase noise contribution can be achieved by narrowing down the loop filter bandwidth after phase lock.
- Programmable power-down modes optimize power management.
- Individually configurable main and auxiliary synthesizers as integer-N, allowing a reduction in power consumption.
- Configurable resolution of the main $\Delta\Sigma$ modulator from 18 to 10 bits, allowing further reduction in power consumption. Note that there are 16 to 8 bits of effective resolution as 2 bits are lost to a front-end divide-by-4 before the multi-modulus prescaler.

Figure 1: PS6500 Block Diagram



Product Description

Serial Interface

The serial interface is a versatile 3-wire interface, **Clock** (serial clock), **Data** (serial input) and **/CS** (chip select). It enables the PS6500 to operate in a system where one or multiple masters and slaves are present. To perform a loop-back test at start-up and to check the integrity of the board and processor, the serial data can be fed back to the master device (for example, MCU/MPU) through a programmable multiplexer. This facilitates hardware and software debugging.

For more information, see “Serial Interface” on page 5.

Registers

There are ten 16-bit registers in the PS6500. For more information, see “Registers” on page 19 and “Register Descriptions” on page 19.

Main and Auxiliary ΔΣ Modulators

The PS6500 uses a proprietary (patent pending) configurable 10-bit or 18-bit ΔΣ modulator for the main synthesizer and 10-bit ΔΣ modulator for the auxiliary synthesizer to provide fractionality.

Main and Auxiliary Fractional Units

The PS6500 provides fractionality through the use of main and auxiliary $\Delta\Sigma$ modulators. The output from the main and auxiliary modulators are combined with the main and auxiliary divider ratios through their respective Fractional Units.

VCO Prescalers

The VCO prescalers provide low-noise signal conditioning of the VCO signals. They are used to translate from an off-chip single-ended or differential signal to an on-chip differential ECL/CML signal. The PS6500 has independent main and auxiliary VCO prescalers.

Main and Auxiliary VCO Dividers

The PS6500 provides programmable dividers that control the ECL/CML prescalers and supply the required signals to the charge pump phase detectors. Programmable divide ratios ranging from 152 to 2148 are possible in fractional-N mode, and from 128 to 2172 in integer-N mode. Note that due to the fixed Divide-by-four divider on the main synthesizer, the divide ratios are multiples of four.

Programmable divide ratios ranging from 38 to 537 are possible in fractional-N mode, and from 32 to 543 in integer-N mode for the auxiliary synthesizer.

Reference Frequency Oscillator

The PS6500 has a self-contained low-noise crystal oscillator. This crystal oscillator is followed by the clock generation circuitry that generates the required clock for the programmable reference frequency dividers.

Reference Frequency Dividers

The crystal oscillator signal can be divided by a ratio of 1 to 32 to create the reference frequencies for the phase detectors. The PS6500 has both a Main and an Auxiliary frequency synthesizer and provides independently configurable dividers of the crystal oscillator frequency for both the main and auxiliary phase detectors. The divide ratios can be programmed through the Reference Frequency Dividers Register.

Note: The divided crystal oscillator frequencies (which are the internal reference frequencies) F_{ref_main} and F_{ref_aux} are referred to as the reference frequencies throughout this document.

Phase Detectors and Charge Pumps

The PS6500 uses a separate charge pump phase detector (patent pending), for each synthesizer which provides a programmable gain, Kd, from 8 to 80 µA/radian in steps of 2.25 µA/radian. Phase detector gains are programmable through the control register.

Frequency Steering

When programmed for Power Steering^{TM} (patent pending), the PS6500 has a frequency power steering circuit, which assists the loop filter to steer the VCO, through the **LD/PS** pin. In this configuration, the **LD/PS** pin can provide for more rapid acquisition (approximately five times faster than conventional phase/frequency detectors).

When programmed for lock detection, internal frequency steering is implemented and provides frequency acquisition times comparable to conventional phase/frequency detector.

Lock Detection

When programmed for lock detection, the PS6500 provides on the **LD/PS** pin, an active low pulsing open collector output to indicate the out-of-lock condition. When locked, the **LD/PS** pin is tri-stated (high impedance).

Power Down

The PS6500 supports a number of power-down modes through its serial interface. For more information, see “General Synthesizer Registers” on page 22.

Operation

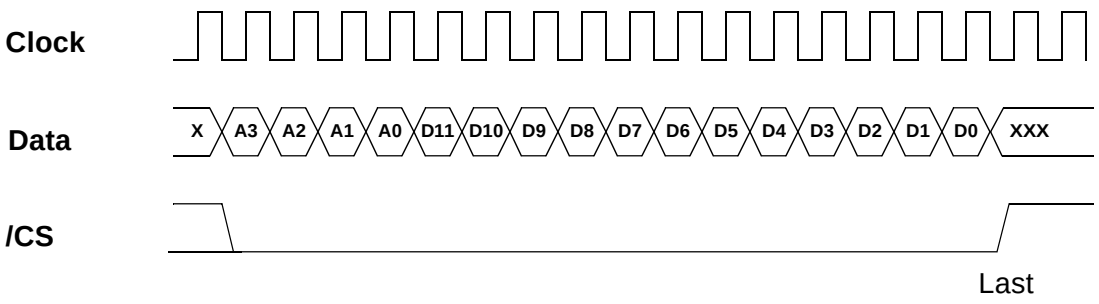
This section describes the operation of the PS6500. The serial interface is described first, followed by information on how to obtain values for the divide ratio registers.

Serial Interface

The serial interface of the PS6500 consists of three pins: **Clock**, **Data** and **/CS**. Data transfers are controlled by the **Clock** signal which synchronizes and samples the information on the two serial data lines (**Data** and **/CS**). The bits on the **Data** pin are shifted into a temporary register on the rising edge of **Clock**. The **/CS** (chip select) line allows individual selection of slave devices on the same bus.

The following diagram functionally depicts how a serial transfer takes place.

Figure 2: Serial Transfer Timing Diagram



A serial transfer is initiated when a microcontroller or microprocessor forces the **/CS** line to a low state. This is immediately followed by an address/data stream being presented to the **Data** pin that coincides with the rising edges of the clock presented on the **Clk** line. Each rising edge of the **Clk** signal shifts in one bit of data on the **Data** line into the shift-register. At the same time, one bit of data is being shifted out for the **Mux_out** pin (if the serial bit stream is selected) at each falling edge of **Clk**. To load any of the synthesizer registers, 16 bits of address/data have to be presented to the **Data** line with the data LSB last while **/CS** is low. If **/CS** is low for more than 16 clock cycles, only the last address/data bits are used for loading the synthesizer registers.

If the **/CS** line is brought to a high state before the thirteenth clock edge on **Clk**, the bit stream is assumed to be modulation data samples. In this case, it is assumed that no address bits are present and that all the bits in the stream should be loaded into the *modulation data register*

Synthesizer Register Programming

In the following equations,

$N_{fractional}$	Desired VCO division ratio in fractional-N applications. This number is a real number and can be interpreted as the reference frequency (F_{ref}) multiplying factor such that the resulting frequency is equal to the desired VCO frequency.
$N_{integer}$	Desired VCO division ratio in integer-N applications. This number is an integer and can be interpreted as the reference frequency (F_{ref}) multiplying factor such that the resulting frequency is equal to the desired VCO frequency.
N_{reg}	9-bit unsigned input value to the divider ranging from 0 to 511(Integer-N mode) and from 6 to 505 (Fractional-N mode)
divider	262144 when the $\Delta\Sigma$ modulator is in 18-bit mode, 1024 when the $\Delta\Sigma$ is in 10-bit mode
dividend	When in 18-bit mode, 18-bit signed input value to the $\Delta\Sigma$ modulator, ranging from -131072 to +131071 providing 262144 steps, each of $\mathbf{F_{div\_ref}} / 2^{18}$ (Hz). or when in 10-bit mode, 10-bit signed input value to the $\Delta\Sigma$ modulator, ranging from -512 to +511 providing 1024 steps, each of $\mathbf{F_{div\_ref}} / 2^{10}$ Hz.
F_{VCO}	Desired VCO frequency (either $\mathbf{F_{vco\_main}}$ or $\mathbf{F_{vco\_aux}}$).
F_{div_ref}	Divided reference frequency presented to the phase detector (either F_{ref_main} or F_{ref_aux}).

Fractional-N Applications

The desired division ratio is for the Main Synthesizer is given by:

$$\mathbf{N_{fractional} = F_{VCO\_main} / (4 \times F_{div\_ref})}$$

The desired division ratio is for the Auxiliary Synthesizer is given by:

$$\mathbf{N_{fractional} = F_{VCO\_aux} / F_{div\_ref}}$$

where $N_{fractional}$ must be between 150 and 2150 for the main synthesizer or between 37.5 and 537.5 for the auxiliary.

The value to be programmed in the *Main or Auxiliary Divider Register* is given by:

$$\mathbf{N_{reg} = Round\ ^{1}\ [N_{fractional}] - 32}$$

When in fractional mode, allowed values for $\mathbf{N_{reg}}$ are from 6 to 505 inclusive.

The value to be programmed in the *Main or Auxiliary Dividend Register(s)* is given by:

$$\mathbf{dividend = Round\ [divider \times (N_{fractional} - N_{reg} - 32)]}$$

1. Where the **Round** function ***rounds*** the number to the nearest integer.

where the **divider** is either 1024 in 10-bit mode or 262144 in 18-bit mode. Therefore, the **dividend** is a signed binary value either 10 or 18 bits long.

Note: Because of the high fractionality of the Direct Digital Modulation Fractional-N Frequency Synthesizer, there is no practical need for any integer relationship between the reference frequency and the channel spacing or desired VCO frequencies.

Fractional-N Example

Case 1: To achieve a desired frequency $\mathbf{F_{VCO\_main}}$ of 5900.4530 MHz using crystal frequency of 40 MHz with operation of the synthesizer in 18-bit mode.

Since the maximum internal reference frequency $\mathbf{F_{div\_ref}}$ is 25 MHz, the crystal frequency is divided by 2 to obtain a $\mathbf{F_{div\_ref}}$ of 20 MHz [1]. Therefore, using:

$$\mathbf{N_{fractional} = F_{VCO} / (4 \times F_{div\_ref})}$$

$$= 5900.4530 / 80$$

$$= 73.7557$$

The value to be programmed in the *Main Divider Register* is:

$$\mathbf{N_{reg} = Round\ [N_{fractional}] - 32}$$

$$= \text{Round}[73.7557] - 32$$

$$= 74 - 32$$

$$= 42$$

$$= 0\ 0010\ 1010 \text{(binary)}$$

With the modulator in 18-bit mode, the value to be programmed in the *Main Dividend Registers* is

$$\mathbf{dividend = Round\ (divider \times (N_{fractional} - N_{reg} - 32))}$$

$$= \text{Round}\ (262144 \times (73.7557 - 42 - 32))$$

$$= \text{Round}\ (262144 \times (-0.2443375))$$

$$= \text{Round}\ (-64051.6096)$$

$$= -64052 \text{ (decimal)}$$

$$= 11\ 0000\ 0101\ 1100\ 1100 \text{ (binary)}$$

Where 11 0000 0101 is loaded in the *Main Dividend MSB Register* and 1100 1100 is loaded in the *Main Dividend LSB Register*.

1. The frequency step size for this case is 4 x 20 MHz divided by 2^{18} giving 305.2 Hz.

Summarizing,

- *Main Divider Register* = 0 0010 1010
- *Main Dividend LSB Register* = 1100 1100
- *Main Dividend MSB Register* = 11 0000 0101
- The resulting main VCO frequency is 5900.4529
- Step size is 305 Hz

Case 2: Assuming a desired frequency $\mathbf{F_{VCO\_main}}$ of 5217.1776 MHz and a crystal frequency of 19.2 MHz with operation of the synthesizer in 10-bit mode.

Since the maximum internal reference frequency $\mathbf{F_{div\_ref}}$ is 25 MHz, the crystal frequency does not require the internal division to be greater than 1, giving us a $\mathbf{F_{div\_ref}}$ of 19.2 MHz [1]. Therefore, using:

$$\mathbf{N_{fractional} = F_{VCO\_main} / (4 \times F_{div\_ref})}$$

$$= 5217.1776 / 4 \times 19.2$$

$$= 67.9320$$

The value to be programmed in the *Main Divider Register* is:

$$\mathbf{N_{reg} = Round\ [N_{fractional}] - 32}$$

$$= \text{Round } [67.9320] - 32$$

$$= 68 - 32$$

$$= 36$$

$$= 0\ 0010\ 0100 \text{ (binary)}$$

With the modulator in 10-bit mode, the value to be programmed in the *Main Dividend Registers* is:

$$\mathbf{dividend = Round\ (divider \times (N_{fractional} - N_{reg} - 32))}$$

$$= \text{Round } (1024 \times (67.9320 - 36 - 32))$$

$$= \text{Round } (1024 \times (-0.068))$$

$$= \text{Round } (-69.632)$$

$$= -70 \text{ (decimal)}$$

$$= 11\ 1011\ 1010 \text{ (binary)}$$

Where 11 1011 1010 is loaded in the *Main Dividend MSB Register*.

1. The frequency step size for this case is 4 x 19.2 MHz divided by 2^{10} giving 75 kHz.

Summarizing,

- *Main Divider Register* = 0 0010 0100
- *Main Dividend MSB Register* =11 1011 1010
- The resulting VCO frequency is 5217.15 MHz
- Step size is 75 kHz

Integer-N Applications

The desired division ratio for the Main or Auxiliary Synthesizer is given by:

$$\mathbf{N_{integer} = F_{VCO\_main} / F_{div\_ref}}$$

where $\mathbf{N_{integer}}$ is an integer number from 32 and 543 for both the main and auxiliary synthesizers.

The value to be programmed in the *Main or Auxiliary Divider Register* is given by:

$$\mathbf{N_{reg} = N_{integer} - 32}$$

When in integer mode, allowed values for $\mathbf{N_{reg}}$ are from 0 and 511 for both the main and auxiliary synthesizers.

Note: As with all integer-N synthesizers, the minimum step size is related to the crystal frequency and reference frequency division ratio.

Integer-N Example

Case 1: To achieve a desired frequency $\mathbf{F_{VCO\_aux}}$ of 400 MHz using a crystal frequency of 16 MHz.

Since the minimum divide ratio is 32, the reference frequency must be a maximum of 12.5 MHz. Choosing a reference frequency divide ratio of 2 provides us with a reference frequency $\mathbf{F_{div\_ref}}$ of 8 MHz. Therefore, using:

$$\mathbf{N_{integer} = F_{VCO\_aux} / F_{div\_ref}}$$

$$= 400 / 8$$

$$= 50$$

The value to be programmed in the *Auxiliary Divider Register* is:

$$\mathbf{N_{reg} = N_{integer} - 32}$$

$$= 50 - 32$$

$$= 18$$

$$= 0\ 0001\ 0010 \text{ (binary)}$$

Summarizing,

- Auxiliary Divider Register = 0 0001 0010

Register Loading Order

In applications where the main synthesizer is in 18-bit mode, the *Main Dividend MSB Register* holds the 10 MSBs of the **dividend** and the *Main Dividend LSB Register* holds the 8 LSBs of the **dividend**. The order in which the registers controlling the main synthesizer's divide ratio are to be loaded is:

- Main Divider Register
- Main Dividend LSB Register
- Main Dividend MSB Register (at which point the new divide ratio takes effect).

In applications where the main synthesizer is in 10-bit mode, the *Main Dividend MSB Register* holds the 10 bits of the **dividend**. The order in which the registers controlling the main synthesizer's divide ratio are to be loaded is:

- Main Divider Register
- Main Dividend MSB Register (at which point the new divide ratio takes effect).

For the auxiliary synthesizer, the *Auxiliary Dividend Register* holds the 10 bits of the **dividend**. The order in which the registers controlling the auxiliary synthesizer's divide ratio is to be loaded is:

- Auxiliary Divider Register
- Auxiliary Dividend Register (at which point the new divide ratio takes effect).

Note: When in integer mode, the new divide ratios take effect as soon as the *Main or Auxiliary Divider Register* is loaded.

Direct Digital Modulation

The PS6500's high fractionality and small step size permit the user to tune to practically any frequency in the VCO's operating range. This frequency tuning permits direct digital modulation by programming the different desired frequencies at precise instants. Typically, the channel frequency is selected through the *main divider and dividend register* and the instantaneous frequency offset from the carrier is entered through the *modulation data register.*

Write access to the *modulation data register* can be performed three ways:

Normal register write

A normal 16-bit serial interface write to the *modulation data register* at address Hex9 where **/CS** is 16 **Clock** cycles wide and modulation data is presented on the **Data** pin. The content of the *modulation data register* is passed to the *modulation unit* at the next falling edge of the divided main VCO frequency (F_{pd_main}).

Short **/CS** through **Data** pin (no address bits required)

A shortened serial interface write where **/CS** is from 2 to 12 **Clock** cycles wide and modulation data (2 to 12 bits) is presented on the **Data** pin. The **Data** is the default pin for entering modulation data directly in *modulation data register* with shortened **/CS** strobes. This method of data entry eliminates the register address overhead on the serial interface. All serial interface bits are re-synchronized internally at the reference oscillator frequency. The content of the *modulation data register* is passed to the *modulation unit* at the next falling edge of the divided main VCO frequency (F_{pd_main}).

Short **/CS** through **Mod_in** pin (no address bits required)

A shortened serial interface write where **/CS** is from 2 to 12 **Clock** cycles wide and modulation data (2 to 12 bits) is presented on the **Mod_in** pin. The **Mod_in** is the alternate pin for entering modulation data directly in *modulation data register* with shortened **/CS** strobes. This mode is selected through the *modulation control register*. This method of data entry also eliminates the register address overhead on the serial interface and permits a different device than the one controlling the channel selection to enter the modulation data (eg. a microcontroller for channel selection and a DSP for modulation data). All serial interface bits are re-synchronized internally at the reference oscillator frequency and the content of the *modulation data register* is passed to the *modulation unit* at the next falling edge of the divided main VCO frequency (F_{pd_main}).

Modulation data samples in the *modulation data register* can be from 2 to 12 bits long, enabling the user to select how many distinct frequency steps will be used for the desired modulation scheme.

The user can also control the frequency deviation through the *Modulation Data Magnitude Offset* in the *modulation control register*. This permits shifting of the modulation data to accomplish a 2^m multiplication of frequency deviation[1].

1. The programmable range of -0.5 to +0.5 of the main $\Delta\Sigma$ modulator can be exceeded up to the condition where the sum of the dividend and the modulation data obey

$$-0.5625 \leq (\mathbf{N_{mod}} + \mathbf{dividend}) \leq +0.5625$$

before requiring changing $\mathbf{N_{integer}}$

Figure 3: PS6500 Pinout

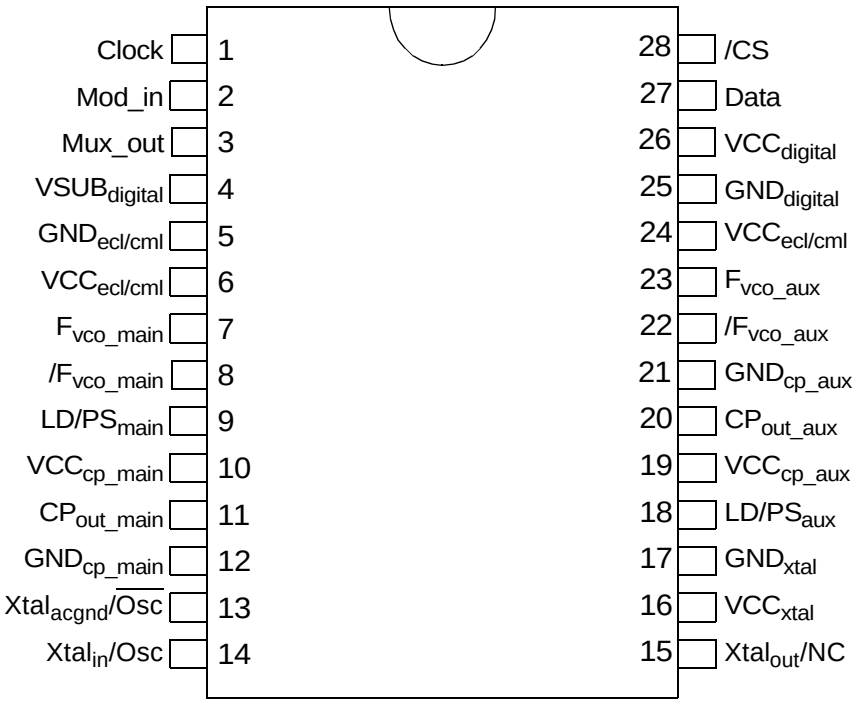


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Table 1: PS1200 Pin Description

Pin Label	Pin #	Type	Description
Clock	Pin 1	Digital input	Clock signal pin. When **/CS** is low, the register address and data is shifted in address bits first on the **Data** pin on the rising edge of **Clock**. For more information, see “Serial Interface” on page 5.
Data	Pin 27	Digital input	Serial address and data input pin. Address bits are followed by data bits. For more information, see “Serial Interface” on page 5.
/CS	Pin 28	Digital input	Active low enable pin. Enables loading of address and data on the **Data** pin on the rising edge of **Clock.** When **/CS** goes high, data is transferred to the register indicated by the address. Subsequent clock edges are ignored. For more information, see “Serial Interface” on page 5.
Mod_in	Pin 2	Digital input	Alternate serial modulation data input pin. Address bits are followed by data bits.
Mux_out	Pin 3	Digital output	Internal multiplexer output. Selects from oscillator frequency, main or auxiliary reference frequency, main or auxiliary divided VCO frequency, serial data out or testability signals. This pin can be tri-stated from the General Synthesizer Registers. For more information, see “General Synthesizer Registers” on page 22.
$Xtal_{acgnd}/\overline{Osc}$	Pin 13	Ground/Input	Reference crystal AC ground, or external oscillator complementary input.
$Xtal_{in}$/Osc	Pin 14	Input	Reference crystal input, or external oscillator differential input.
$Xtal_{out}$/NC	Pin 15	Input	Reference crystal output, or no connect.
F_{vco_main}	Pin 7	Input	Main VCO differential input.
$/F_{vco\_main}$	Pin 8	Input	Main VCO complimentary differential input
F_{vco_aux}	Pin 23	Input	Auxiliary VCO differential input
$/F_{vco\_aux}$	Pin 22	Input	Auxiliary VCO complimentary differential input
CP_{out_main}	Pin 11	Analog Output	Main charge pump output. The gain of the main charge pump phase detector can be controlled from the General Synthesizer Registers.
LD/PS_{main}	Pin 9	Analog Output	Programmable output pin. Indicates main phase detector out-of-lock as an active low pulsing open collector output (high impedance when lock is detected), or assists the loop filter in steering the main VCO. This pin is configured from the General Synthesizer Registers.

Pin Label	Pin #	Type	Description
CP_{out_aux}	Pin 20	Analog Output	Auxiliary charge pump output. The gain of the auxiliary charge pump phase detector can be controlled from the General Synthesizer Registers.
LD/PS_{aux}	Pin 18	Analog Output	Programmable output pin. Indicates auxiliary phase detector out-of-lock as an active low pulsing open collector output (high impedance when lock is detected), or assists the loop filter in steering the auxiliary VCO. This pin is configured from the General Synthesizer Registers.
$VCC_{digital}$	Pin 26	Power and Ground	Digital 3 Volts.
$GND_{digital}$	Pin 25	Power and Ground	Digital Ground.
VCC_{xtal}	Pin 16	Power and Ground	Crystal oscillator ECL/CML 3 Volts.
GND_{xtal}	Pin 17	Power and Ground	Crystal Oscillator Ground.
$VCC_{ecl/cml}$	Pins 6, 24	Power and Ground	ECL/CML 3 Volt. Removing power safely powers down the associated divider chain and charge pump.
$GND_{ecl/cml}$	Pin 5	Power and Ground	ECL/CML Ground.
VCC_{cp_main}, VCC_{cp_aux}	Pins 10, 19	Power and Ground	Main and auxiliary charge pump 3 to 5 Volt. Removing power safely powers down the associated divider chain and charge pump.
GND_{cp_main}, GND_{cp_aux}	Pin 26	Power and Ground	Main and auxiliary charge pump Ground.
$VSUB_{digital}$	Pin 4	-	Substrate isolation, connect to Ground

Note: Associated pairs of power and ground pins need to be decoupled using 0.1 µF capacitors.

Note: The PS1200 is supplied in an exposed pad 28-pin TSSOP package (EP-TSSOP). The exposed pad is located on the bottom side of the package, and must be connected to ground for proper operation. The exposed pad should be soldered directly to the circuit board.

Absolute Maximum Ratings

Maximum Analog Supply Voltage:	3.6 VDC
Maximum Digital Supply Voltage:	3.6 VDC
Maximum Charge Pump Supply Voltage:	5.25 VDC
Storage Temperature:	-65°C to +150°C
Operating Temperature:	-40°C to +85°C

Recommended Operating Conditions

Analog Supplies:	+2.7 to +3.3 VDC
Digital Supply:	+2.7 to +3.3 VDC
Charge Pump Supplies	+2.7 to +5.0 VDC
Operating Temperature (T_A):	-40°C to +85°C

Electrical Characteristics

Test Conditions (unless otherwise stated)	
Analog Supplies:	3.0 VDC
Digital Supply:	3.0 VDC
Charge Pump Supplies	3.0 VDC
Temperature (T_A):	-40°C to +85°C

.

Table 2: Power Consumption

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
P_{total}	Total power consumption	Charge pump currents of 200 µA Both synthesizers fractional F_{ref_main} = 20 MHz F_{ref_aux} = 1 MHz	-	51	-	mW
$I_{CC-PWDN}$	Power down current	-	-	10	-	µA

Table 3: Reference Oscillator

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
F_{osc}	Reference oscillator frequency	-	-	-	50	MHz
V_{osc}	Oscillator sensitivity (as a buffer)	AC Coupled, single-ended	0.05	-	2.0	V_{pp}
F_{shift_ship}	Frequency shift at shipping	T = 25°C, V_{xtal} = 3.0 V With 1% tolerance 20 pF crystal loading capacitors	-	-	± 3	ppm
F_{shift_temp}	Frequency shift vs temperature	-40°C < T < +85°C V_{xtal} = 3.0 V	-	-	± 3	
F_{shift_supply}	Frequency shift vs supply voltage	T = 25°C 2.7 V ≤ V_{xtal} ≤ 3.3 V	-	-	± 0.3	

Table 4: VCOs

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
F_{vco_main}	Main synthesizer operating frequency	Sinusoidal	800	-	6500	MHz
F_{vco_aux}	Auxiliary synthesizer operating frequency		400	-	1200	
V_{vco}	RF input sensitivity	AC Coupled	50	-	250	mV_{peak}
Z_{vco_in}	RF input impedance	-	-	1000	-	Ω
ΔF_{step_main}	Main Fractional-N tuning step size	-	$F_{ref\_main} / 2^{16}$ or $F_{ref\_main} / 2^{8}$			Hz
ΔF_{step_aux}	Aux Fractional-N tuning step size	-	$F_{ref\_aux} / 2^{10}$			

Table 5: Noise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
P_{nf}	Phase noise floor	In PLL loop bandwidth	-	-132 + 20Log(N)	-	dBc/Hz
P_{IB}	Total spurious power		-	-70	-	dBc

Table 6: Phase Detectors and Charge Pumps

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
F_{ref_main}	Main phase detector frequency		-	-	25	MHz
F_{ref_aux}	Auxiliary phase detector frequency					
$I_{cp\text{-}source}$	Charge pump output source current	V_{CP} = 0.5VCC_{cp}	125	-	1000	µA
$I_{cp\text{-}sink}$	Charge pump output sink current		-125	-	-1000	
$I_{cp\text{-}accuracy}$	-	-	-	+/- 20	-	%
I_{cp} vs. V_{cp}	Charge pump output voltage linearity range	0.5V ≤ V_{CP} ≤ (VCC_{cp} - 0.5V) T = 25°C	Gnd + 400	-	VCC_{cp} - 400	mV
I_{cp} vs. T	Charge pump current vs. temperature	VCP = 0.5VCC_{cp} -40°C < T < +85°C	-	-	5	%
I_{cp} vs. V_{cp}	Charge pump current vs. voltage	0.5V ≤ V_{CP} ≤ (VCC_{cp} - 0.5V) T = 25°C	-	-	8	

Table 7: Digital Pins

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VIH	High level input voltage	-	$0.7V_{digital}$	-	-	V
VIL	Low level input voltage	-	-	-	$0.3V_{digital}$	
VOH	High level output voltage	I_{OH} = -2 mA	$V_{digital}$ - 0.2	-	-	
VOL	Low level output voltage	I_{OL} = 2 mA	-	-	Gnd + 0.2	

Timing

Table 8: Timing — Serial Interface

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{clock}	**Clock** frequency	-	-	-	100	MHz
t_{su}	**Data** and **/CS** set up time to **Clock** rising	-	3	-	-	ns
t_{hold}	**Data** and **/CS** hold time after **Clock** rising	-	0	-	-	ns

Registers

This section describes the PS6500's registers. All register writes are programmed address first, followed directly with data. MSBs are entered first. On power up, all register are reset to zero.

Register Map

Table 9: PS6500 Register Map

Address	Register[a]	Length (with address bits)
H0	Main divider register	16 bits
H1	Main dividend MSB register	16 bits
H2	Main dividend LSB register	16 bits
H3	Aux divider register	16 bits
H4	Aux dividend register	16 bits
H5	Reference frequency dividers register	16 bits
H6	Control register - Phase detector/Charge pumps	16 bits
H7	Control register - Power down/Multiplexer Output select	16 bits
H8	Modulation control register	16 bits
H9	Modulation data register	16 bits
	Modulation data register[b] - direct input	2 ≤ length ≤ 12 bits

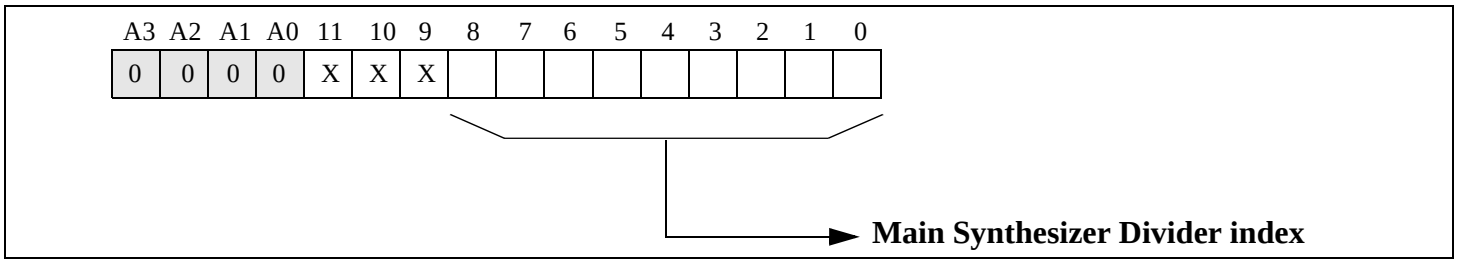
a. All registers are write-only.
b. No address bits are required for modulation data. Any serial data between 2 and 12 bits long is considered modulation data.

Register Descriptions

For more information on register loading order, see "Register Loading Order" on page 10.

Main Synthesizer Registers

Figure 4: Hex0 *Main Divider Register* (Write only)



This register contains the integer portion divided by four closest to the desired fractional-N (or the integer-N) value minus 32 for the main synthesizer. This register, in conjunction with the main dividend registers (which controls the fraction offset from -0.5 to +0.5), permits selection of a precise frequency.

Note: The fixed divide-by-four divider upstream from the programmable main divider must be taken into consideration when determining the value to be programmed in this register. Refer to “Synthesizer Register Programming” on page 6 for more details

Values to be loaded are:

- *Main Synthesizer Divider Index* = 9-bit value for the integer portion of the main synthesizer dividers. Valid values for this register are from 6 to 505 (fractional-N) or from 0 to 511 (integer-N).

Figure 5: Hex1 *Main Dividend MSB Register* (Write only)

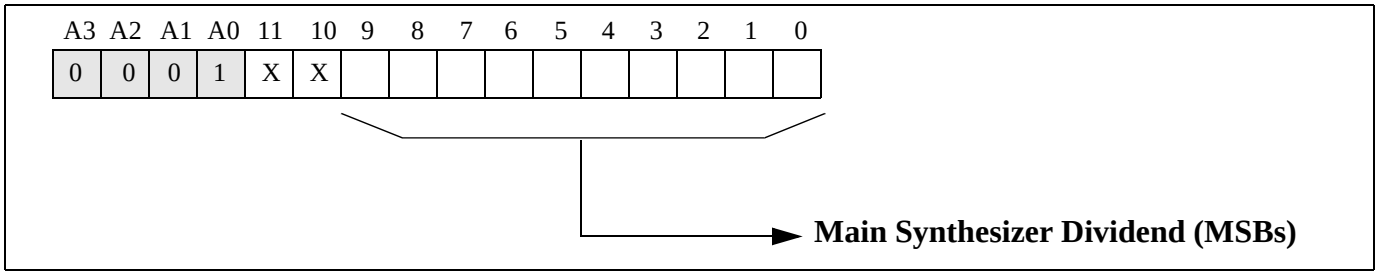
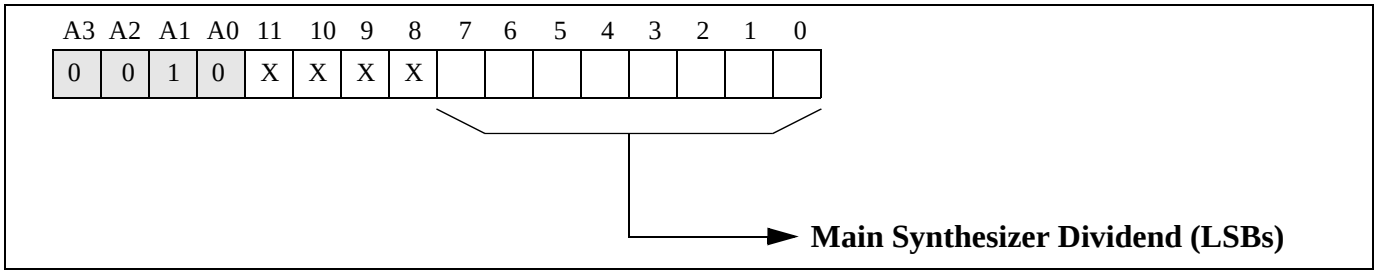


Figure 6: Hex2 *Main Dividend LSB Register* (Write only)



These registers control the fraction part of the desired fractional-N value and permit an offset of - 0.5 to + 0.5 to the main integer selected through the Main Divider Register.

Values to be loaded are:

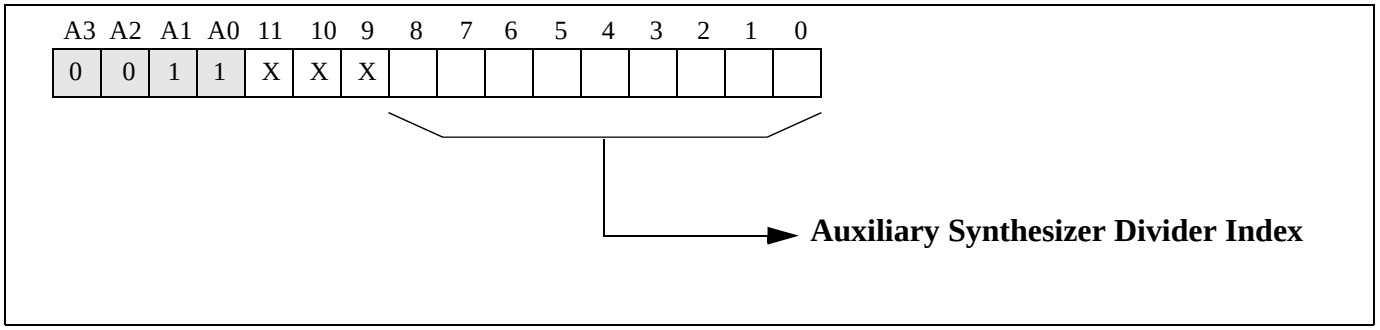
- *Main Synthesizer Dividend (MSBs)* = 10-bit value for the MSBs of the 18-bit dividend for the main synthesizer.
- *Main Synthesizer Dividend (LSBs)* = 8-bit value for the LSBs of the 18-bit dividend for the main synthesizer.

Note: When in 10-bit mode, the *Main Synthesizer Dividend (LSBs)* is not required.

For information on programming these registers, see “Synthesizer Register Programming” on page 6. For information on loading order for these registers, see “Register Loading Order” on page 10.

Auxiliary Synthesizer Registers

Figure 7: Hex3 *Auxiliary Divider Register* (Write only)

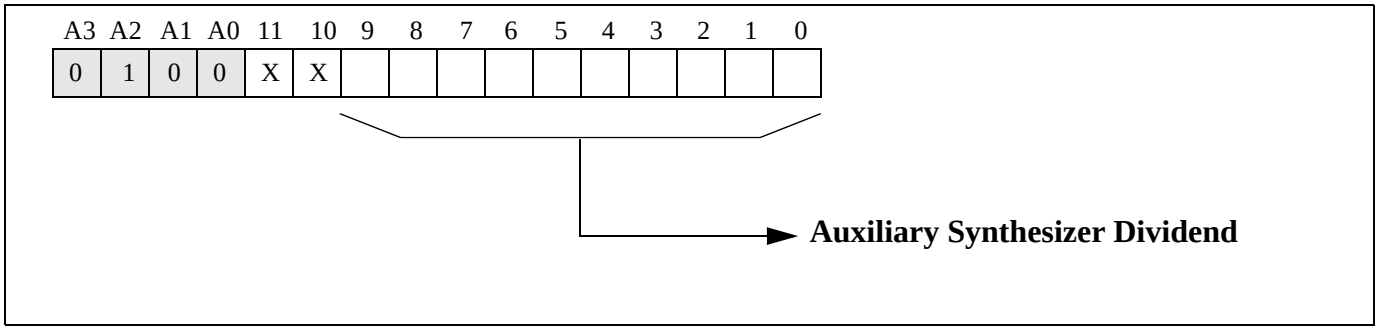


This register contains the integer portion closest to the desired fractional-N (or integer-N) value minus 32 for the auxiliary synthesizer. This register, in conjunction with the auxiliary dividend register, which controls the fraction offset (from - 0.5 to + 0.5) permits selection of a precise frequency.

Values to be loaded are:

- *Auxiliary Synthesizer Divider Index* = 9-bit value for the integer portion of the auxiliary synthesizer dividers. Valid values for this register are from 6 to 505 (fractional-N) or from 0 to 511 (integer-N).

Figure 8: Hex4 *Auxiliary Dividend Register* (Write only)



This register controls the fraction part of the desired fractional-N value and permits an offset of - 0.5 to + 0.5 to the auxiliary integer selected through the Auxiliary Divider Register.

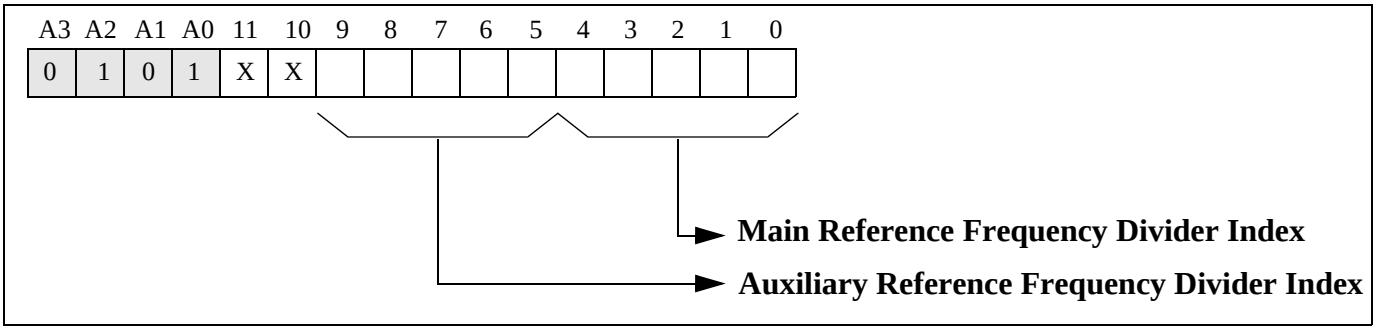
Values to be loaded are:

- *Auxiliary Synthesizer Dividend* = 10-bit value for the dividend for the auxiliary synthesizer.

For information on programming these registers, see “Synthesizer Register Programming” on page 6. For information on loading order for these registers, see “Register Loading Order” on page 10.

General Synthesizer Registers

Figure 9: Hex5 *Reference Frequency Dividers Register* (Write only)



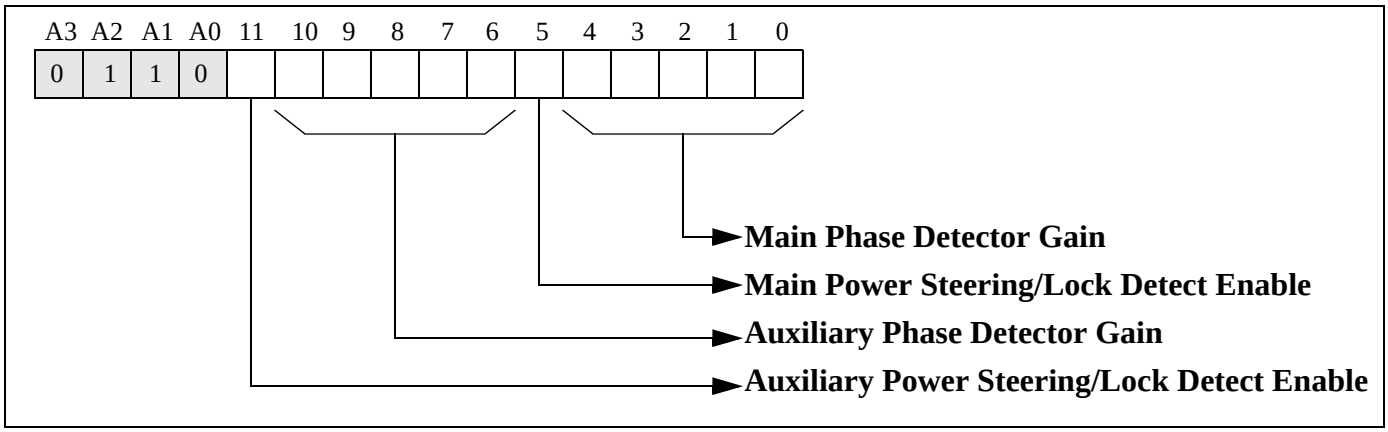
This register configures the dual-programmable reference frequency dividers for the main and auxiliary synthesizers.

The dual-programmable reference frequency dividers provide the reference frequencies to the phase detectors by dividing the crystal oscillator frequency. The lower five bits hold the reference frequency divide index for the main phase detector. The next five bits hold the reference frequency divide index for the auxiliary phase detector. Divide ratios from 1 to 32 are possible for each reference frequency divider.

Values to be loaded are:

- *Main Reference Frequency Divider Index* = Desired main oscillator frequency division ratio - 1. Default value on power up is 0, signifying that the reference frequency is not divided for the main phase detector.
- *Auxiliary Reference Frequency Divider Index* = Desired Auxiliary oscillator frequency division ratio - 1. Default value on power up is 0, signifying that the reference frequency is not divided for the auxiliary phase detector.

Figure 10: Hex6 *Phase Detectors Register* (Write only)

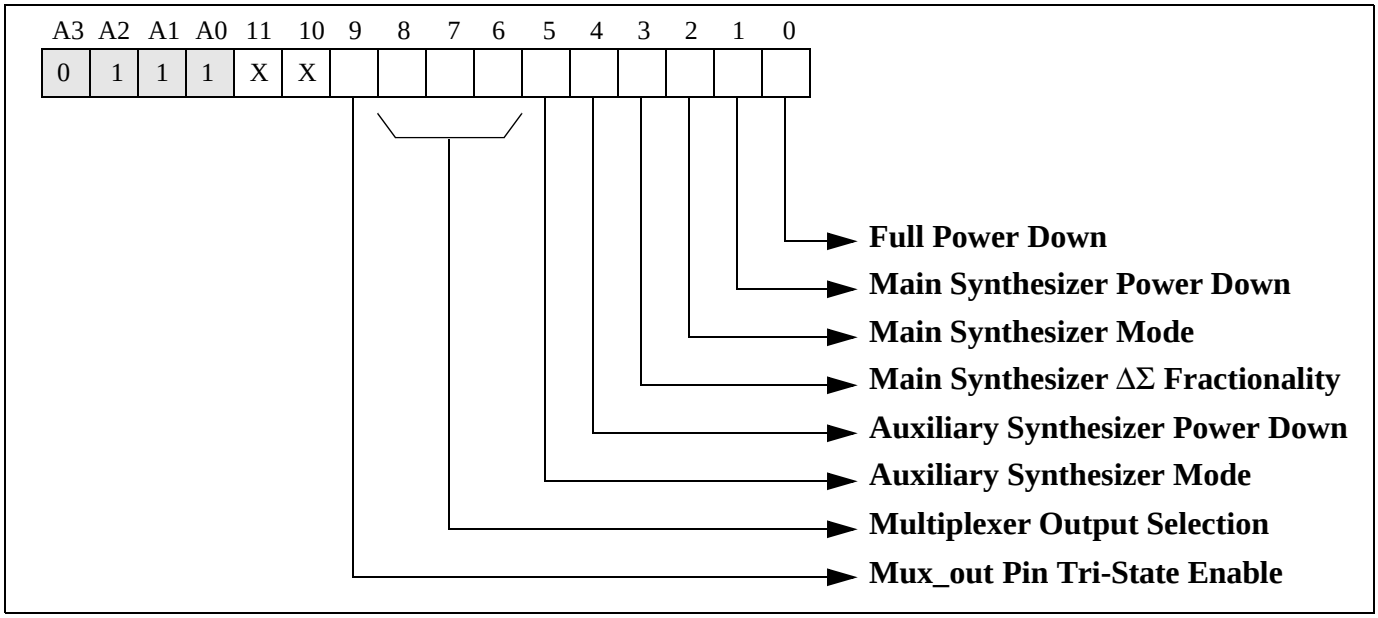


This register permits control of the gain for both phase detectors, and configuration of the **LD/PS** pins for frequency power steering or lock detection.

Values to be loaded are:

- *Main Phase Detector Gain* = 5-bit value for programmable main phase detector gain, Kd, of 20 to 160 µA/radian in steps of approximately 5 µA/radian. Valid range is from 4 to 31 decimal for 20 to 160 µA/radian respectively.
- *Main Power Steering Enable* = 1-bit value to enable the frequency power steering circuitry of the main phase detector. When this bit is a 0, the **LD/PS$_{main}$** is configured to be a lock detect active low open collector pin. When this bit is a 1, the **LD/PS$_{main}$** is configured to be a frequency power steering pin and can be used to bypass the external main loop filter to provide faster frequency acquisition.
- *Aux Phase Detector Gain* = 5-bit value for programmable auxiliary phase detector gain, Kd, of 20 to 160 µA/radian in steps of approximately 5 µA/radian. Valid range is from 4 to 31 decimal for 20 to 160 µA/radian respectively.
- *Aux Power Steering Enable* = 1-bit value to enable the frequency power steering circuitry of the auxiliary phase detector. When this bit is a 0, the **LD/PS$_{aux}$** is configured to be a lock detect active low open collector pin. When this bit is a 1, the **LD/PS$_{aux}$** is configured to be a frequency power steering pin and may be used to bypass the external auxiliary loop filter to provide faster frequency acquisition.

Figure 11: Hex7 *Power Down and Multiplexer Output Register* (Write only)



This register permits control of the power-down modes, internal multiplexer output and Main ΔΣ synthesizer fractionality.

Values to be loaded are:

- *Full Power Down* = 1-bit value for powering down the whole chip except for the reference oscillator and the serial interface. When this bit is 0, the PS6500 is powered up. When this bit is 1, the PS6500 is in full power-down mode excluding the Mux_out pin.

- *Main Synthesizer Power Down* = 1-bit value for powering down the main synthesizer. When this bit is 0, the main synthesizer is powered up. When this bit is 1, the main synthesizer is in power down mode.
- *Main Synthesizer Mode* = 1-bit value for powering down the main synthesizer's ΔΣ modulator and fractional unit to operate as a integer-N synthesizer. When this bit is 0, the main synthesizer is in fractional-N mode. When this bit is 1, the main synthesizer is in integer-N mode.
- *Main Synthesizer ΔΣ Fractionality* = 1-bit value to configure the size of the main ΔΣ modulator. This has a direct effect on power consumption and on the level of fractionality and step size. When this bit is 0, the main ΔΣ modulator is 18-bit with fractionality of 2^{18} and step size of $F_{ref\_main}/262144$. When this bit is 1, the main ΔΣ modulator is 10-bit with fractionality of 2^{10} and step size of $F_{ref\_main}/1024$.
- *Auxiliary Synthesizer Power Down* = 1-bit value for powering down the auxiliary synthesizer. When this bit is 0, the auxiliary synthesizer is powered up. When this bit is 1, the auxiliary synthesizer is in power-down mode.
- *Auxiliary Synthesizer Mode* = 1-bit value for powering down the auxiliary synthesizer's ΔΣ modulator and fractional unit to operate as a integer-N synthesizer. When this bit is 0, the auxiliary synthesizer is in fractional-N mode. When this bit is 1, the auxiliary synthesizer is in integer-N mode.

Note: There are no special power up sequences required for the PS6500.

- *Multiplexer Output Selection* = 3-bit value for selecting which internal signal is output to the **Mux_out** pin. Internal signals available on this pin are:
  - — Reference Oscillator: F_{ref}
  - — Main or auxiliary divided reference (post reference frequency main or auxiliary dividers): F_{ref_main} or F_{ref_aux}
  - — Main or auxiliary phase detector frequency (post main and auxiliary frequency dividers): F_{pd_main} or F_{pd_aux}
  - — Serial data out, for loop-back and test purposes

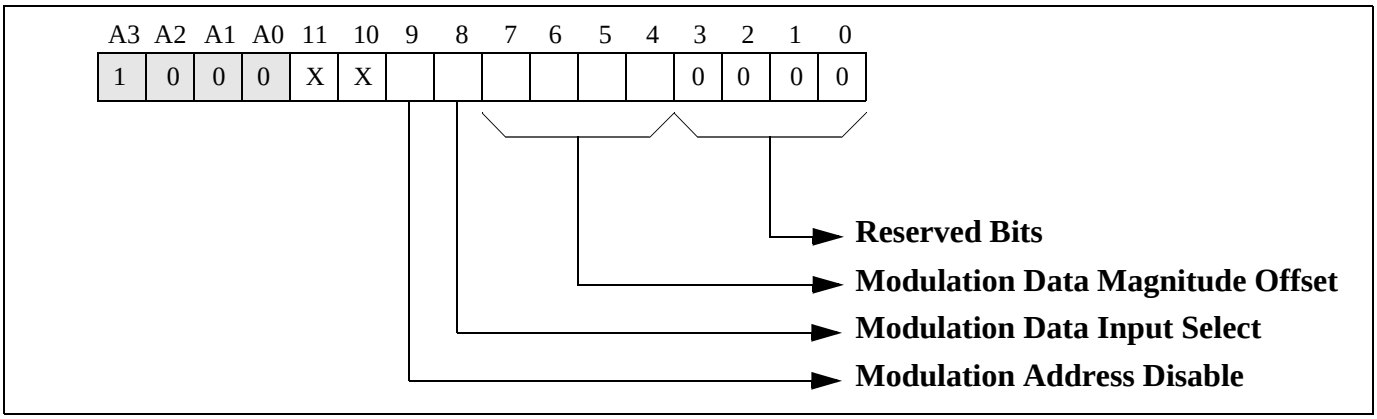
Refer to the following table for more information.

Table 10: Multiplexer Output

Multiplexer Output Select bit 2	Multiplexer Output Select bit 1	Multiplexer Output Select bit 0	Multiplexer Output (Mux_out)
0	0	0	Reference Oscillator
0	0	1	Auxiliary Reference Frequency (F_{ref_aux})
0	1	0	Main Reference Frequency (F_{ref_main})
0	1	1	Auxiliary Phase Detector Frequency (F_{pd_aux})
1	0	0	Main Phase Detector Frequency (F_{pd_main})
1	0	1	Serial Data Out
1	1	0	Serial Interface Register Test Output

- *Mux_out Pin Tri-State Enable* = 1-bit value for tri-stating the **Mux_out** pin. When this bit is 0, the **Mux_out** pin is enabled. When this bit is 1, the **Mux_out** pin is tri-stated.

Figure 12: Hex8 *Modulation Control Register* (Write only)



This register is used to configure the modulation unit of the main synthesizer.

The modulation unit provides for adding or subtracting a frequency offset to the selected center frequency at which the main synthesizer is operating. The size of the modulation data sample, controlled by the duration of **/CS**, can be from 2 to 12 bits wide, to provide from 4 to 4096 selectable frequency offsets steps.

The modulation data magnitude offset selects the magnitude multiplier for the modulation data and can be from 0 to 8.

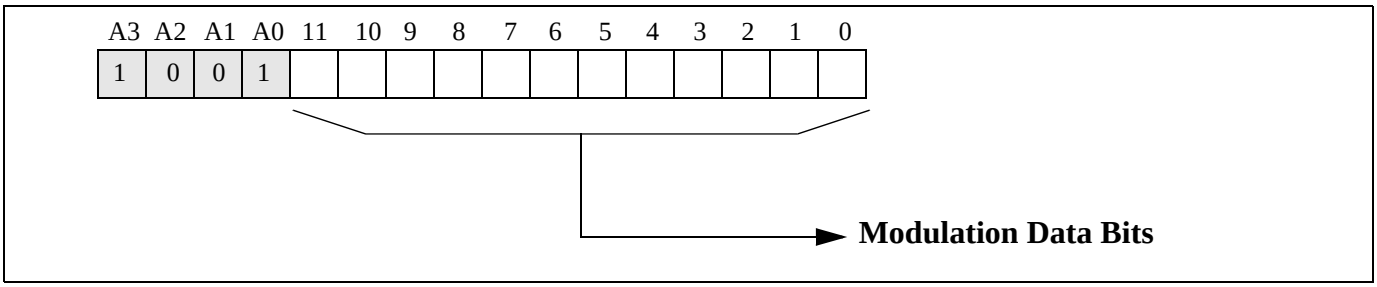
Values to be loaded are:

Modulation Data Magnitude Offset = 4-bit value indicating magnitude multiplier (m) for the modulation data samples. Valid values range from 0 to 13, effectively providing a 2^m multiplication of the modulation data sample.

Modulation Data Input Select = 1-bit value indicating the pin on which modulation data samples are serially input when **/CS** is between 2 and 12 bits long. When this bit is 0, modulation data samples are to be presented on the **Data** pin. When this bit is 1, modulation data samples are to be presented on the **Mod_in** pin. For more details, please refer to section “Direct Digital Modulation” on page 10.

Modulation Address Disable = 1-bit value indicating the presence of the address as modulation data samples are presented on either the **Mod_in** or **Data** pins. When this bit is 0, address is presented with the modulation data samples (i.e. all transfers are 16 bits long). When this bit is 1, no address is presented with the modulation data samples (i.e. all transfers are 2 to 12 bits long). For more details, please refer to section “Direct Digital Modulation” on page 10.

Figure 13: Hex9 *Modulation Data Register* (Write only)



This register is used to load the modulation data samples to the modulation unit. This value is transferred to the modulation unit on the falling edge of F_{pd_main} where it will be passed to the main ΔΣ modulator at the selected magnitude offset on the next falling edge of F_{pd_main}.

Values to be loaded are:

Modulation Data Bits = Modulation data samples representing desired instantaneous frequency offset to the selected main synthesizer frequency (selected channel) before being affected by the *Modulation Data Magnitude Offset*.

Packaging Information

Figure 14: 28-Pin EP-TSSOP

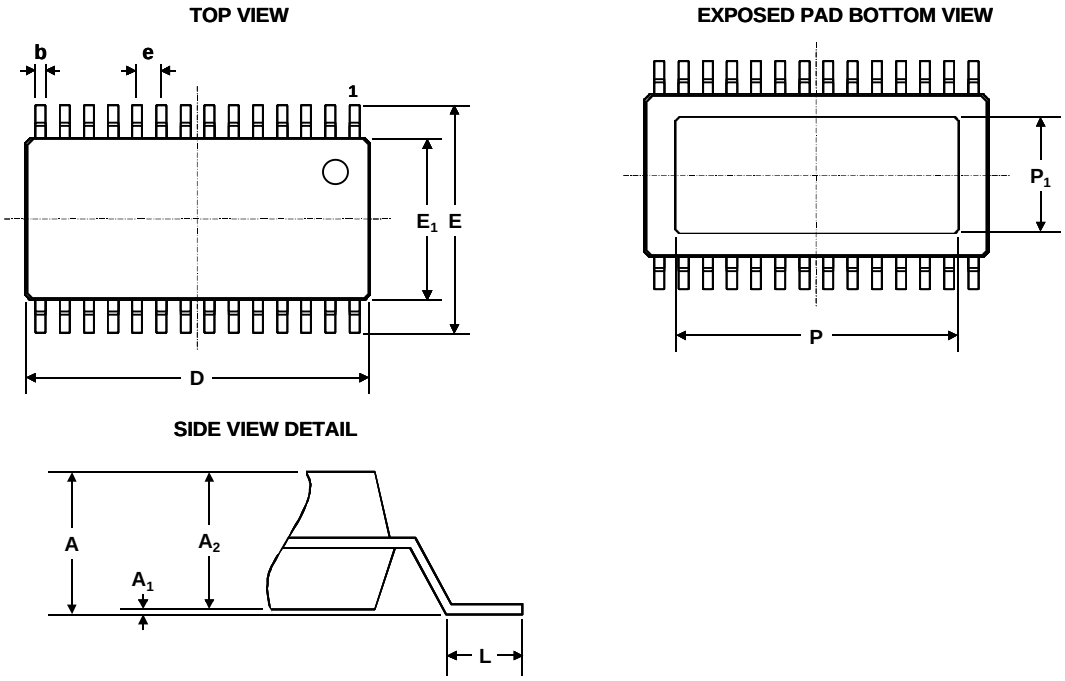


Table 11: 28-Pin EP-TSSOP Dimensions

	Min	Max
A		1.10
A_1	0.05	0.15
A_2	0.85	0.95
D	9.70 BSC	
E	6.40 BSC	
E_1	4.30	4.50
L	0.50	0.70
P		3.5
P_1		3.0
e	0.65 BSC	
b	0.19	0.30

All dimensions in millimeters (mm)

Ordering Information

Table 12: Ordering Information

Part Number	Temperature Range	Package	Minimum Order Quantity	Notes
PS6500AIT-ES2/2	-	28-Pin TSSOP	2	Engineering prototype units that are not necessarily representative of the final device's electrical specifications. Verified for functionality only, quality and reliability verification not completed.
PS6500AIT	-40 to 85°C	28-Pin TSSOP	50	

Electrostatic Discharge Information

The PS6500 device is an electrostatic sensitive device. Observe precautions when handling.