HFA1130/883

Output Clamping, 850MHz Current Feedback Amplifier

July 1994

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **User Programmable Output Voltage Clamps**
- **Low Distortion (HD3, 30MHz) . . . . -84dBc (Typ)**
- **Wide -3dB Bandwidth . . . . 850MHz (Typ)**
- **Very High Slew Rate . . . . 2300V/μs (Typ)**
- **Fast Settling (0.1%) . . . . 11ns (Typ)**
- **Excellent Gain Flatness (to 50MHz) . . . . . 0.05dB (Typ)**
- **High Output Current . . . . 65mA (Typ)**
- **Fast Overdrive Recovery. . . . . <1ns (Typ)**

Applications

- **Residue Amplifier**
- **Video Switching and Routing**
- **Pulse and Video Amplifiers**
- **Wideband Amplifiers**
- **RF/IF Signal Processing**
- **Flash A/D Driver**
- **Medical Imaging Systems**

Description

The HFA1130/883 is a high speed, wideband current feedback amplifier featuring programmable output clamps. Built with Intersil' proprietary complementary bipolar UHF-1 process, it is the fastest monolithic amplifier available from any semiconductor manufacturer.

This amplifier is the ideal choice for high frequency applications requiring output limiting, especially those needing ultra fast overdrive recovery times. The output clamp function allows the designer to set the maximum positive and negative output levels, thereby protecting later stages from damage or input saturation. The sub-nanosecond overdrive recovery time quickly returns the amplifier to linear operation following an overdrive condition.

The HFA1130/883's wide bandwidth, fast settling characteristic, and low output impedance, coupled with the output clamping ability, make this amplifier ideal for driving fast A/D converters.

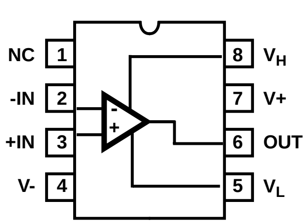
Component and composite video systems will also benefit from this amplifier's performance, as indicated by the excellent gain flatness, and 0.03%/0.05 Degree Differential Gain/Phase specifications (R_L = 75Ω).

Ordering Information

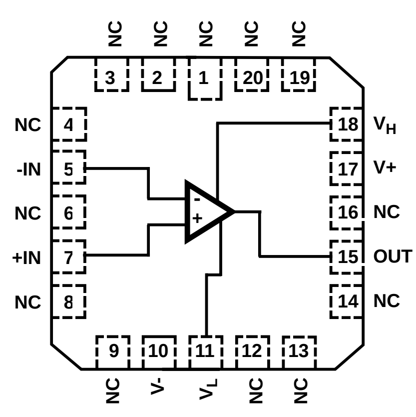
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HFA1130MJ/883	-55°C to +125°C	8 Lead CerDIP
HFA1130ML/883	-55°C to +125°C	20 Lead Ceramic LCC

Pinouts

HFA1130/883
(CERDIP)
TOP VIEW



HFA1130/883
(CLCC)
TOP VIEW



Spec Number 511082-883
File Number 3625.1

Absolute Maximum Ratings

Voltage Between V+ and V- 12V
Differential Input Voltage 5V
Voltage at Either Input Terminal . . . . V+ to V-
Voltage at V_H or V_L Terminal . . . .(V+) + 2V to (V-) - 2V
Output Current (50% Duty Cycle) . . . . ±55mA
Junction Temperature. . . . . +175°C
ESD Rating. . . . . < 2000V
Storage Temperature Range . . . . -65°C ≤ T_A ≤ +150°C
Lead Temperature (Soldering 10s). +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
CerDIP Package	115°C/W	30°C/W
Ceramic LCC Package	75°C/W	23°C/W

Maximum Package Power Dissipation at +75°C
CerDIP Package 0.87W
Ceramic LCC Package 1.33W
Package Power Dissipation Derating Factor above +75°C
CerDIP Package . . . . 8.7mW/°C
Ceramic LCC Package . . . . 13.3mW/°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Supply Voltage (±V_S) . . . . ±5V
Operating Temperature Range. . . . . -55°C ≤ T_A ≤ +125°C
R_L ≥ 50Ω

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: V_{SUPPLY} = ±5V, A_V = +1, R_F = 510Ω, R_{SOURCE} = 0Ω, R_L = 100Ω, V_{OUT} = 0V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	V_{CM} = 0V	1	+25°C	-6	6	mV
			2, 3	+125°C, -55°C	-10	10	mV
Common Mode Rejection Ratio	CMRR	ΔV_{CM} = ±2V V+ = 3V, V- = -7V V+ = 7V, V- = -3V	1	+25°C	40	-	dB
			2, 3	+125°C, -55°C	38	-	dB
Power Supply Rejection Ratio	PSRRP	ΔV_{SUP} = ±1.25V V+ = 6.25V, V- = -5V V+ = 3.75V, V- = -5V	1	+25°C	45	-	dB
			2, 3	+125°C, -55°C	42	-	dB
	PSRRN	ΔV_{SUP} = ±1.25V V+ = 5V, V- = -6.25V V+ = 5V, V- = -3.75V	1	+25°C	45	-	dB
			2, 3	+125°C, -55°C	42	-	dB
Non-Inverting Input (+IN) Current	I_{BSP}	V_{CM} = 0V	1	+25°C	-40	40	μA
			2, 3	+125°C, -55°C	-65	65	μA
+IN Current Common Mode Sensitivity	CMS_{IBP}	ΔV_{CM} = ±2V V+ = 3V, V- = -7V V+ = 7V, V- = -3V	1	+25°C	-	40	μA/V
			2, 3	+125°C, -55°C	-	50	μA/V
+IN Resistance	$+R_{IN}$	Note 1	1	+25°C	25	-	kΩ
			2, 3	+125°C, -55°C	20	-	kΩ
Inverting Input (-IN) Current	I_{BSN}	V_{CM} = 0V	1	+25°C	-50	50	μA
			2, 3	+125°C, -55°C	-75	75	μA
-IN Current Common Mode Sensitivity	CMS_{IBN}	ΔV_{CM} = ±2V V+ = 3V, V- = -7V V+ = 7V, V- = -3V	1	+25°C	-	7	μA/V
			2, 3	+125°C, -55°C	-	10	μA/V
-IN Current Power Supply Sensitivity	$PPSS_{IBN}$	ΔV_{SUP} = ±1.25V V+ = 6.25V, V- = -5V V+ = 3.75V, V- = -5V	1	+25°C	-	15	μA/V
			2, 3	+125°C, -55°C	-	27	μA/V
	$NPSS_{IBN}$	ΔV_{SUP} = ±1.25V V+ = 5V, V- = -6.25V V+ = 5V, V- = -3.75V	1	+25°C	-	15	μA/V
			2, 3	+125°C, -55°C	-	27	μA/V
Output Voltage Swing	V_{OP100}	A_V = -1, R_L =100Ω, V_{IN} = 3.5V	1	+25°C	3	-	V
		A_V = -1, R_L =100Ω, V_{IN} = -3V	2, 3	+125°C, -55°C	2.5	-	V
	V_{ON100}	A_V = -1, R_L =100Ω, V_{IN} =+3.5V	1	+25°C	-	-3	V
		A_V = -1, R_L =100Ω, V_{IN} = +3V	2, 3	+125°C, -55°C	-	-2.5	V

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: V_{SUPPLY} = ±5V, A_V = +1, R_F = 510Ω, R_{SOURCE} = 0Ω, R_L = 100Ω, V_{OUT} = 0V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS		GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
						MIN	MAX	
Output Voltage Swing	V_{OP50}	A_V = -1, R_L = 50Ω	V_{IN} = -3V	1, 2	+25°C, +125°C	2.5	-	V
			V_{IN} = -2V	3	-55°C	1.5	-	V
	V_{ON50}	A_V = -1, R_L = 50Ω	V_{IN} = +3V	1, 2	+25°C, +125°C	-	-2.5	V
			V_{IN} = +2V	3	-55°C	-	-1.5	V
Output Current	$+I_{OUT}$	Note 2		1, 2	+25°C, +125°C	50	-	mA
				3	-55°C	30	-	mA
	$-I_{OUT}$	Note 2		1, 2	+25°C, +125°C	-	-50	mA
				3	-55°C	-	-30	mA
Quiescent Power Supply Current	I_{CC}	R_L = 100Ω		1	+25°C	14	26	mA
				2, 3	+125°C, -55°C	-	33	mA
	I_{EE}	R_L = 100Ω		1	+25°C	-26	-14	mA
				2, 3	+125°C, -55°C	-33	-	mA
Clamp Accuracy	V_HCLMP	A_V = -1, V_{IN} = -2V, V_H = 1V		1	+25°C	-125	125	mV
				2, 3	+125°C, -55°C	-200	200	mV
	V_LCLMP	A_V = -1, V_{IN} = +2V, V_L = -1V		1	+25°C	-125	125	mV
				2, 3	+125°C, -55°C	-200	200	mV
Clamp Input Current	V_HBIAS	V_H = 1V		1	+25°C	-	200	μA
				2, 3	+125°C, -55°C	-	300	μA
	V_LBIAS	V_L = -1V		1	+25°C	-200	-	μA
				2, 3	+125°C, -55°C	-300	-	μA

NOTES:

1. Guaranteed from +IN Common Mode Rejection Test, by: $+R_{IN} = 1/CMS_{IBP}$.
2. Guaranteed from V_{OUT} Test with R_L = 50Ω, by: $I_{OUT} = V_{OUT}/50Ω$.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Table 2 Intentionally Left Blank.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: V_{SUPPLY} = ±5V, A_V = +2, R_F = 360Ω, R_L = 100Ω, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
-3dB Bandwidth	BW(-1)	A_V = -1, R_F = 430Ω, V_{OUT} = 200mV_{P-P}	1	+25°C	300	-	MHz
	BW(+1)	A_V = +1, R_F = 510Ω, V_{OUT} = 200mV_{P-P}	1	+25°C	550	-	MHz
	BW(+2)	A_V = +2, V_{OUT} = 200mV_{P-P}	1	+25°C	350	-	MHz
Gain Flatness	GF30	A_V = +2, R_F = 510Ω, f ≤ 30MHz, V_{OUT} = 200mV_{P-P}	1	+25°C	-	±0.04	dB
	GF50	A_V = +2, R_F = 510Ω, f ≤ 50MHz, V_{OUT} = 200mV_{P-P}	1	+25°C	-	±0.10	dB
	GF100	A_V = +2, R_F = 510Ω, f ≤ 100MHz, V_{OUT} = 200mV_{P-P}	1	+25°C	-	±0.30	dB

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Characterized at: V_{SUPPLY} = ±5V, A_V = +2, R_F = 360Ω, R_L = 100Ω, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Slew Rate	+SR(+1)	A_V = +1, R_F = 510Ω V_{OUT} = $5V_{P-P}$	1, 2	+25°C	1200	-	V/µs
	-SR(+1)	A_V = +1, R_F = 510Ω V_{OUT} = $5V_{P-P}$	1, 2	+25°C	1100	-	V/µs
	+SR(+2)	A_V = +2, V_{OUT} = $5V_{P-P}$	1, 2	+25°C	1650	-	V/µs
	-SR(+2)	A_V = +2, V_{OUT} = $5V_{P-P}$	1, 2	+25°C	1500	-	V/µs
Rise and Fall Time	T_R	A_V = +2, V_{OUT} = $0.5V_{P-P}$	1, 2	+25°C	-	1	ns
	T_F	A_V = +2, V_{OUT} = $0.5V_{P-P}$	1, 2	+25°C	-	1	ns
Overshoot	+OS	A_V = +2, V_{OUT} = $0.5V_{P-P}$	1, 3	+25°C	-	25	%
	-OS	A_V = +2, V_{OUT} = $0.5V_{P-P}$	1, 3	+25°C	-	20	%
Settling Time	TS(0.1)	A_V = +2, R_F = 510Ω V_{OUT} = 2V to 0V, to 0.1%	1	+25°C	-	20	ns
	TS(0.05)	A_V = +2, R_F = 510Ω V_{OUT} = 2V to 0V, to 0.05%	1	+25°C	-	33	ns
2nd Harmonic Distortion	HD2(30)	A_V = +2, f = 30MHz V_{OUT} = $2V_{P-P}$	1	+25°C	-	-48	dBc
	HD2(50)	A_V = +2, f = 50MHz V_{OUT} = $2V_{P-P}$	1	+25°C	-	-45	dBc
	HD2(100)	A_V = +2, f = 100MHz V_{OUT} = $2V_{P-P}$	1	+25°C	-	-35	dBc
3rd Harmonic Distortion	HD3(30)	A_V = +2, f = 30MHz V_{OUT} = $2V_{P-P}$	1	+25°C	-	-65	dBc
	HD3(50)	A_V = +2, f = 50MHz V_{OUT} = $2V_{P-P}$	1	+25°C	-	-60	dBc
	HD3(100)	A_V = +2, f = 100MHz V_{OUT} = $2V_{P-P}$	1	+25°C	-	-40	dBc

NOTES:

1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot-to-lot and within lot variation.
2. Measured between 10% and 90% points.
3. For 200ps input transition times. Overshoot decreases as input transition times increase, especially for A_V = +1. Please refer to Performance Curves.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLE 1)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1 (Note 1), 2, 3
Group A Test Requirements	1, 2, 3
Groups C and D Endpoints	1

NOTE:

1. PDA applies to Subgroup 1 only.

Die Characteristics

DIE DIMENSIONS:
63 x 44 x 19 mils ± 1 mils
1600 x 1130 x 483μm ± 25.4μm

METALLIZATION:
Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ± 0.4kÅ
Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ ± 0.8kÅ

GLASSIVATION:
Type: Nitride
Thickness: 4kÅ ± 0.5kÅ

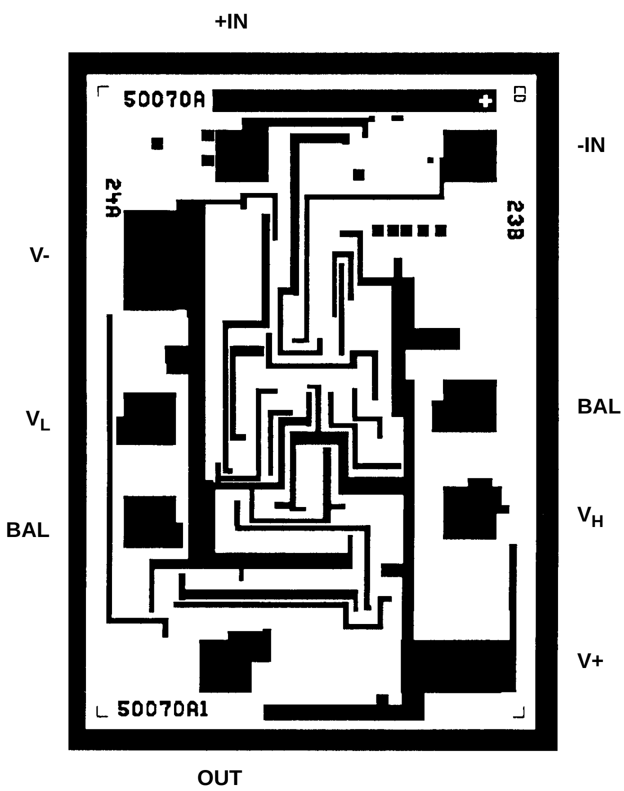
WORST CASE CURRENT DENSITY:
2.0×10^5 A/cm^2 at 47.5mA

TRANSISTOR COUNT: 52

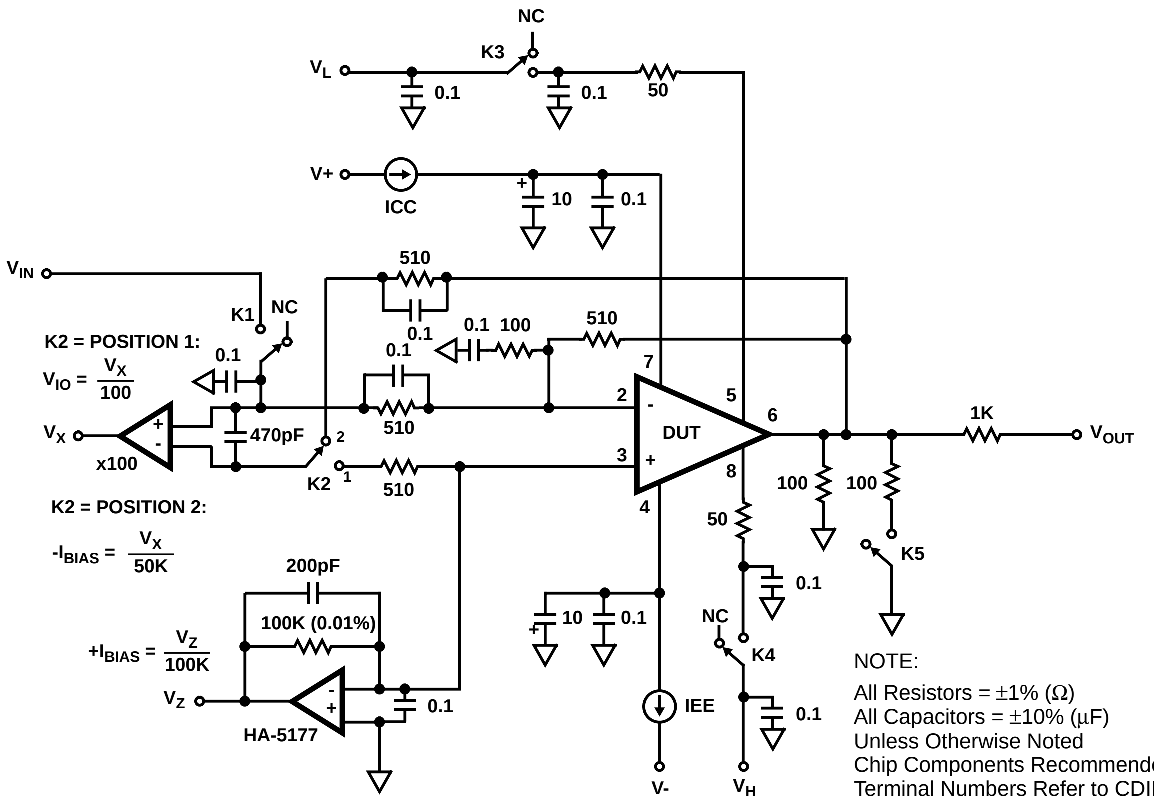
SUBSTRATE POTENTIAL (Powered Up): Floating (Recommend Connection to V-)

Metallization Mask Layout

HFA1130/883



Test Circuit (Applies to Table 1)

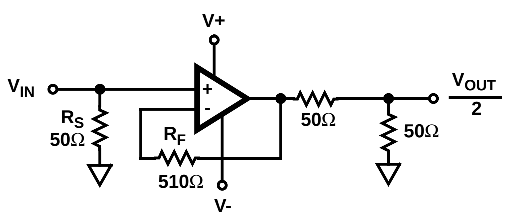


NOTE:
All Resistors = ±1% (Ω)
All Capacitors = ±10% (µF)
Unless Otherwise Noted
Chip Components Recommended
Terminal Numbers Refer to CDIP Package

Test Waveforms

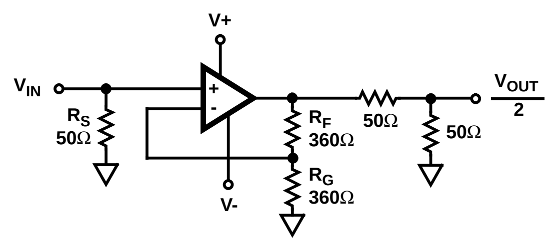
SIMPLIFIED TEST CIRCUIT FOR LARGE AND SMALL SIGNAL PULSE RESPONSE (Applies to Table 3)

A_V = +1 TEST CIRCUIT



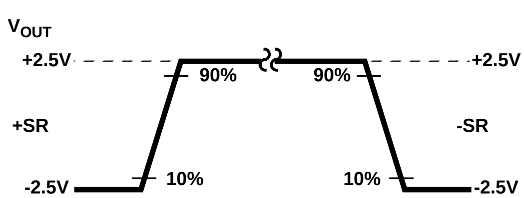
NOTE: V_S = ±5V, A_V = +1
R_S = 50Ω
R_L = 100Ω For Small and Large Signals

A_V = +2 TEST CIRCUIT

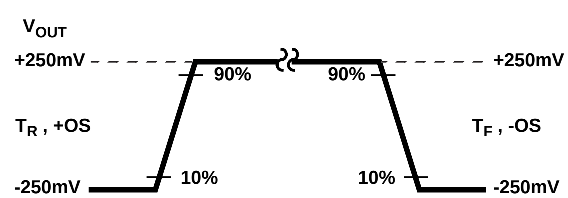


NOTE: V_S = ±5V, A_V = +2
R_S = 50Ω
R_L=100Ω For Small and Large Signals

LARGE SIGNAL WAVEFORM

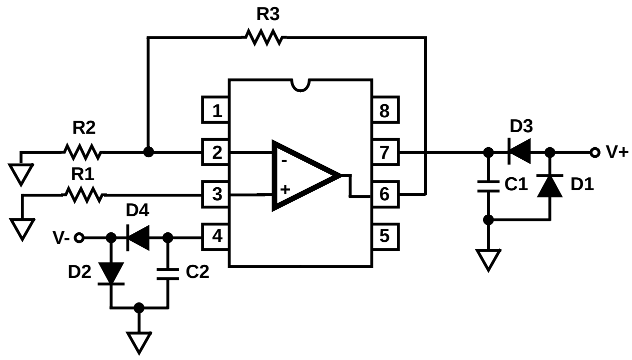


SMALL SIGNAL WAVEFORM



Burn-In Circuits

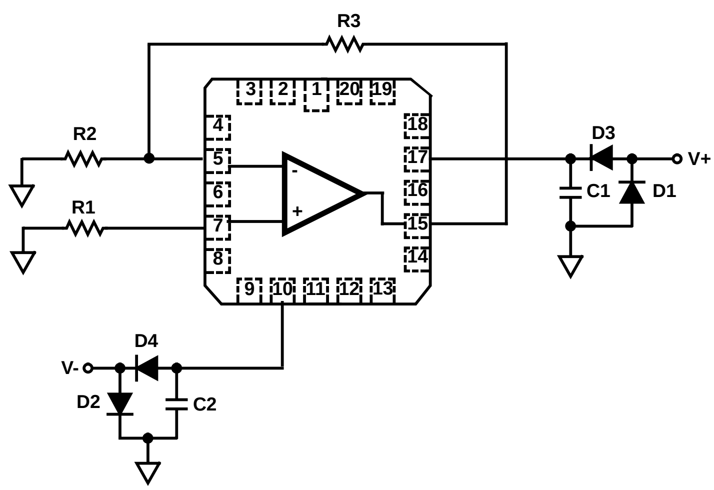
HFA1130MJ/883 CERAMIC DIP



NOTES:

R1 = R2 = 1kΩ, ±5% (Per Socket)
R3 = 10kΩ, ±5% (Per Socket)
C1 = C2 = 0.01µF (Per Socket) or 0.1µF (Per Row) Minimum
D1 = D2 = 1N4002 or Equivalent (Per Board)
D3 = D4 = 1N4002 or Equivalent (Per Socket)
V+ = +5.5V ± 0.5V
V- = -5.5V ± 0.5V

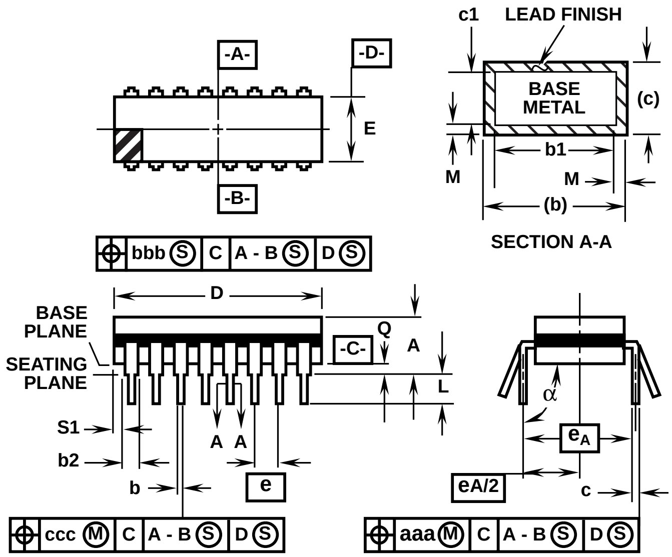
HFA1130ML/883 CERAMIC LCC



NOTES:

R1 = R2 = 1kΩ, ±5% (Per Socket)
R3 = 10kΩ, ±5% (Per Socket)
C1 = C2 = 0.01µF (Per Socket) or 0.1µF (Per Row) Minimum
D1 = D2 = 1N4002 or Equivalent (Per Board)
D3 = D4 = 1N4002 or Equivalent (Per Socket)
V+ = +5.5V ± 0.5V
V- = -5.5V ± 0.5V

Packaging



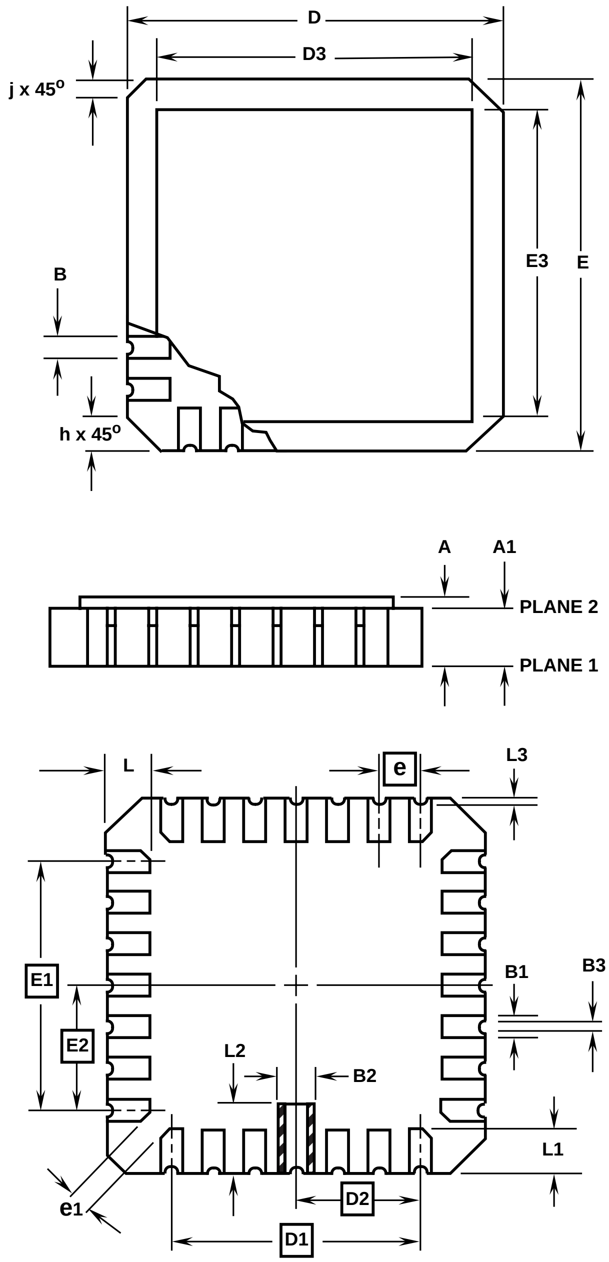
F8.3A MIL-STD-1835 GDIP1-T8 (D-4, CONFIGURATION A)
8 LEAD DUAL-IN-LINE FRIT-SEAL CERAMIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.405	-	10.29	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
S2	0.005	-	0.13	-	-
α	90^{o}	105^{o}	90^{o}	105^{o}	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	8		8		8

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b1.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling Dimension: Inch
11. Lead Finish: Type A.
12. Materials: Compliant to MIL-I-38535.

Packaging (Continued)



J20.A MIL-STD-1835 CQCC1-N20 (C-2)
20 PAD METAL SEAL LEADLESS CERAMIC CHIP CARRIER

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.060	0.100	1.52	2.54	6, 7
A1	0.050	0.088	1.27	2.23	7
B	-	-	-	-	4
B1	0.022	0.028	0.56	0.71	2, 4
B2	0.072 REF		1.83 REF		-
B3	0.006	0.022	0.15	0.56	-
D	0.342	0.358	8.69	9.09	-
D1	0.200 BSC		5.08 BSC		-
D2	0.100 BSC		2.54 BSC		-
D3	-	0.358	-	9.09	2
E	0.342	0.358	8.69	9.09	-
E1	0.200 BSC		5.08 BSC		-
E2	0.100 BSC		2.54 BSC		-
E3	-	0.358	-	9.09	2
e	0.050 BSC		1.27 BSC		-
e1	0.015	-	0.38	-	2
h	0.040 REF		1.02 REF		5
j	0.020 REF		0.51 REF		5
L	0.045	0.055	1.14	1.40	-
L1	0.045	0.055	1.14	1.40	-
L2	0.075	0.095	1.90	2.41	-
L3	0.003	0.015	0.08	0.38	-
ND	5		5		3
NE	5		5		3
N	20		20		3

NOTES:

1. Metallized castellations shall be connected to plane 1 terminals and extend toward plane 2 across at least two layers of ceramic or completely across all of the ceramic layers to make electrical connection with the optional plane 2 terminals.
2. Unless otherwise specified, a minimum clearance of 0.015 inch (0.381mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.)
3. Symbol "N" is the maximum number of terminals. Symbols "ND" and "NE" are the number of terminals along the sides of length "D" and "E", respectively.
4. The required plane 1 terminals and optional plane 2 terminals shall be ellectrically connected.
5. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.
7. Maximum limits allows for 0.007 inch solder thickness on pads.
8. Lead Finish: Type A.
9. Materials: Compliant to MIL-I-38535.

DESIGN INFORMATION

August 1999

Output Clamping, Ultra High Speed Current Feedback Amplifier

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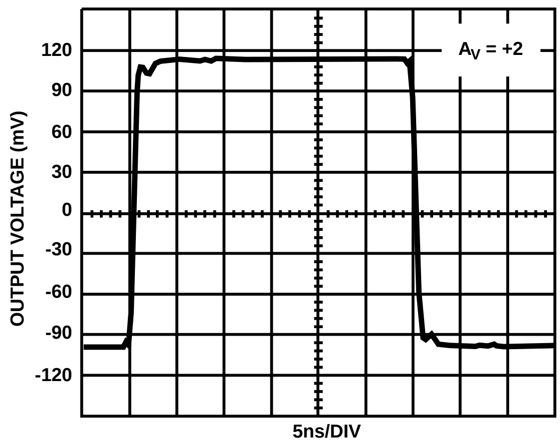
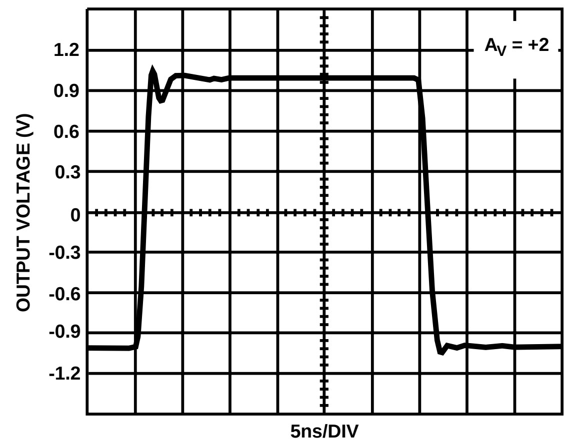
Typical Performance Curves V_{SUPPLY} = ±5V, R_F = 510Ω, T_A = +25^{o}C, R_L = 100Ω, Unless Otherwise Specified.

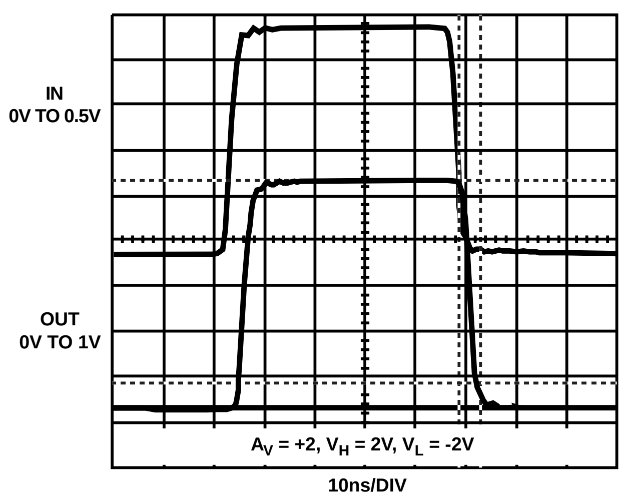
SMALL SIGNAL PULSE RESPONSE



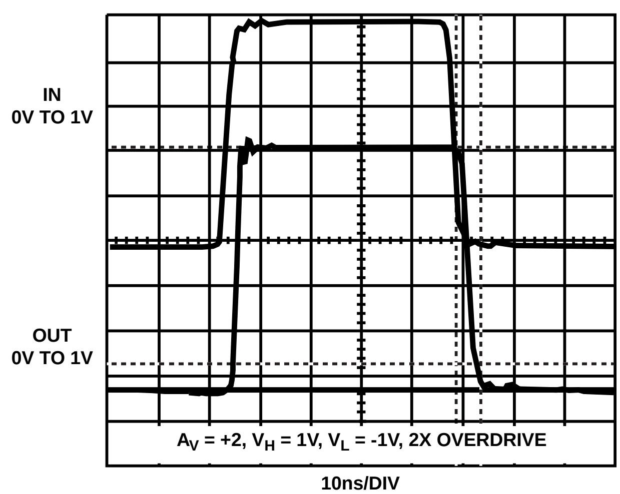
LARGE SIGNAL PULSE RESPONSE



UNCLAMPED PERFORMANCE



CLAMPED PERFORMANCE



DESIGN INFORMATION (Continued)

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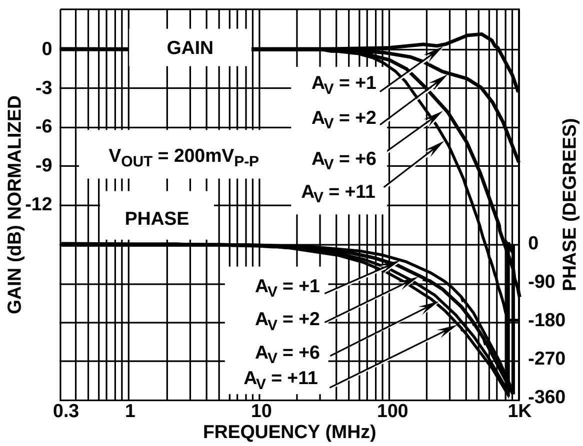
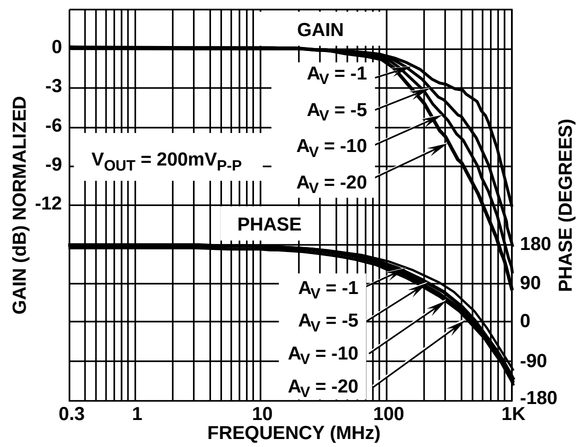
Typical Performance Curves V_{SUPPLY} = ±5V, R_F = 510Ω, T_A = +25°C, R_L = 100Ω, Unless Otherwise Specified. (Continued)

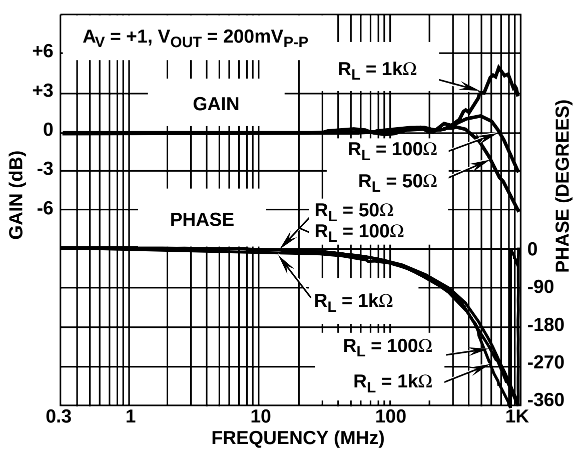
NON-INVERTING FREQUENCY RESPONSE



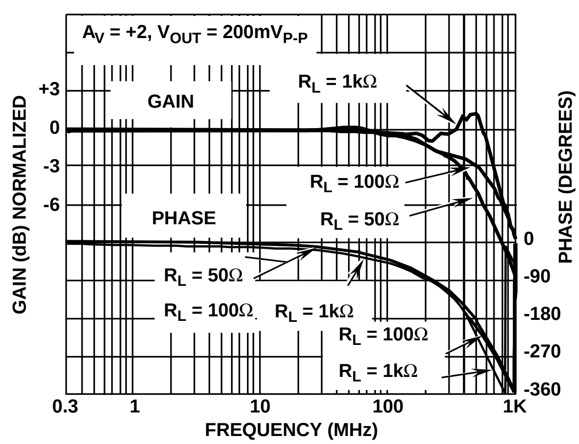
INVERTING FREQUENCY RESPONSE



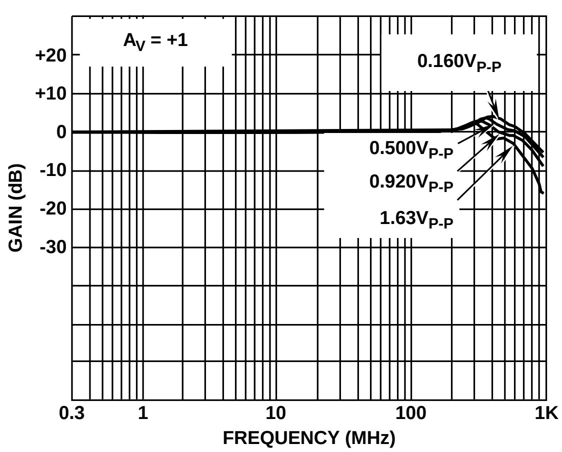
FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS



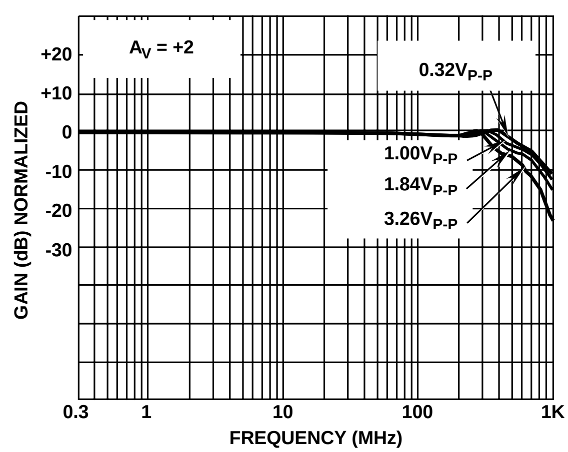
FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS



FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES



FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES



DESIGN INFORMATION (Continued)

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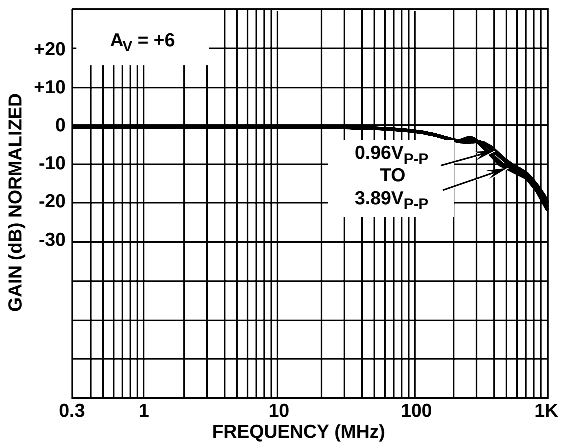
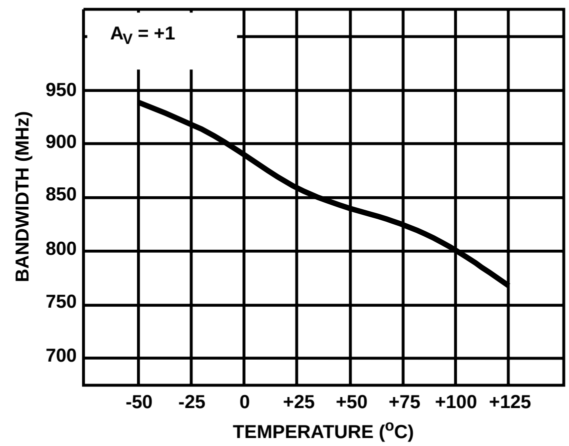
Typical Performance Curves V_{SUPPLY} = ±5V, R_F = 510Ω, T_A = +25°C, R_L = 100Ω, Unless Otherwise Specified. (Continued)

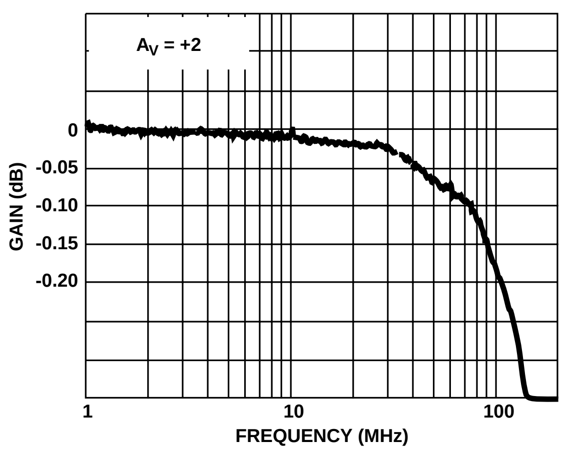
FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES



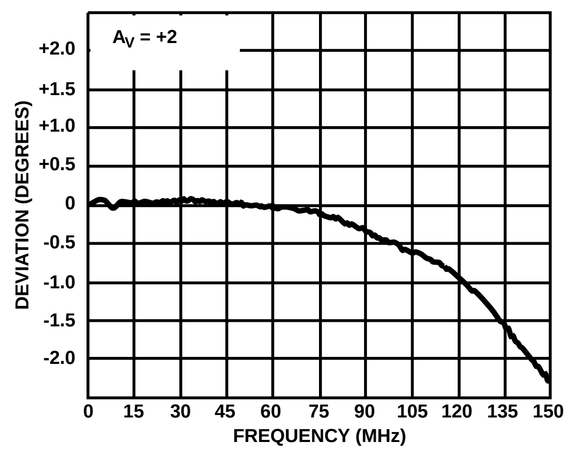
-3dB BANDWIDTH vs TEMPERATURE



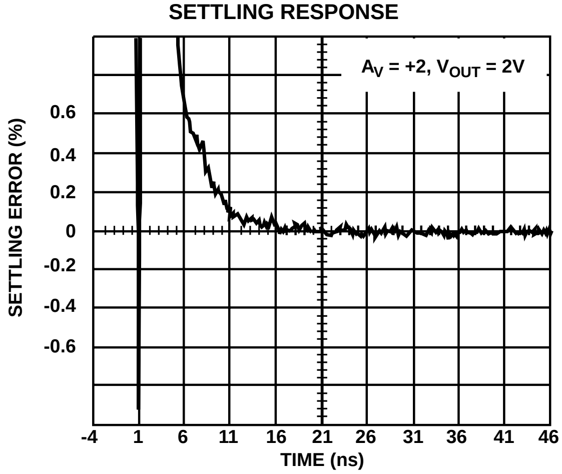
GAIN FLATNESS



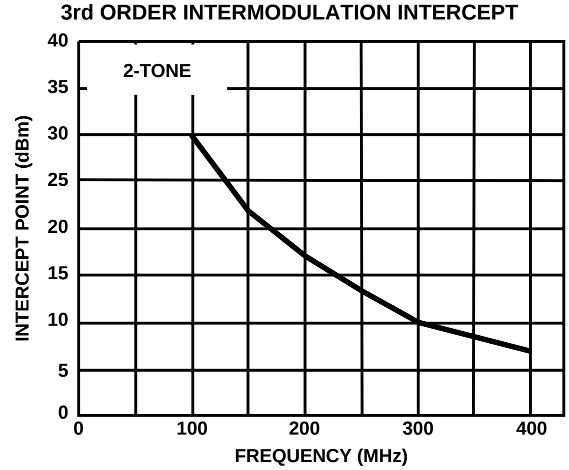
DEVIATION FROM LINEAR PHASE



SETTLING RESPONSE



3rd ORDER INTERMODULATION INTERCEPT



DESIGN INFORMATION (Continued)

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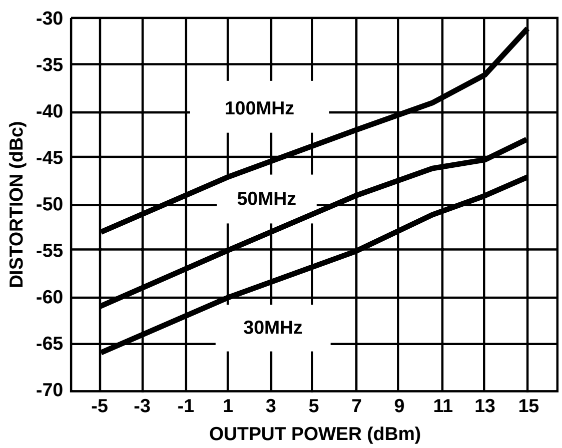
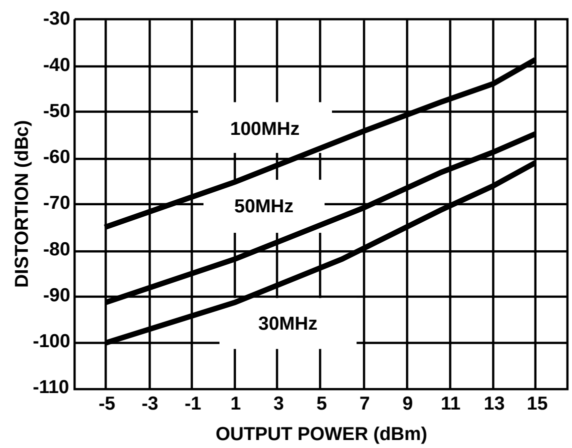
Typical Performance Curves V_{SUPPLY} = ±5V, R_F = 510Ω, T_A = +25°C, R_L = 100Ω, Unless Otherwise Specified. (Continued)

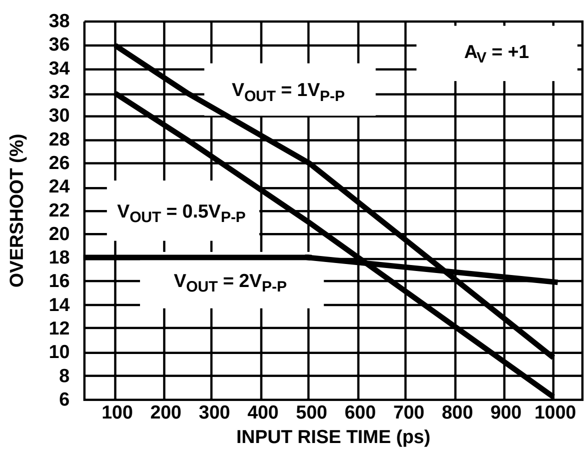
2nd HARMONIC DISTORTION vs P_{OUT}



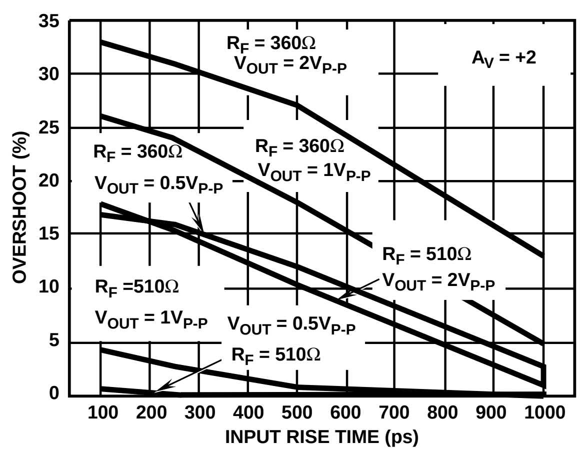
3rd HARMONIC DISTORTION vs P_{OUT}



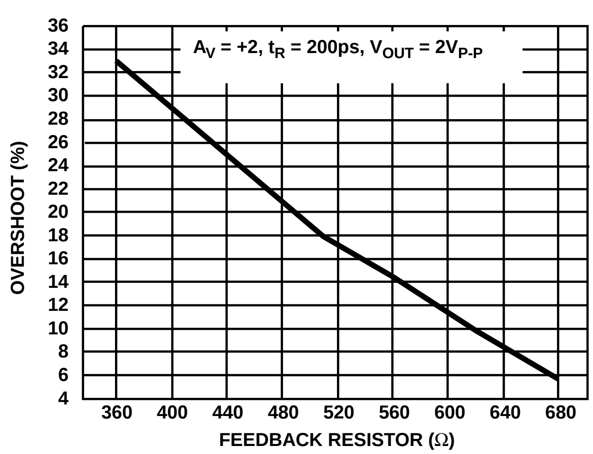
OVERSHOOT vs INPUT RISE TIME



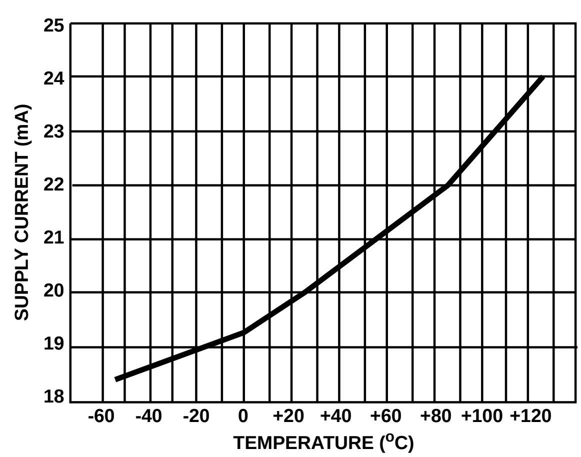
OVERSHOOT vs INPUT RISE TIME



OVERSHOOT vs FEEDBACK RESISTOR



SUPPLY CURRENT vs TEMPERATURE



DESIGN INFORMATION (Continued)

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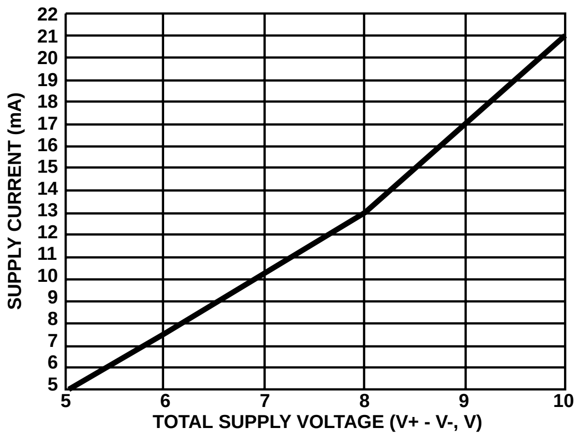
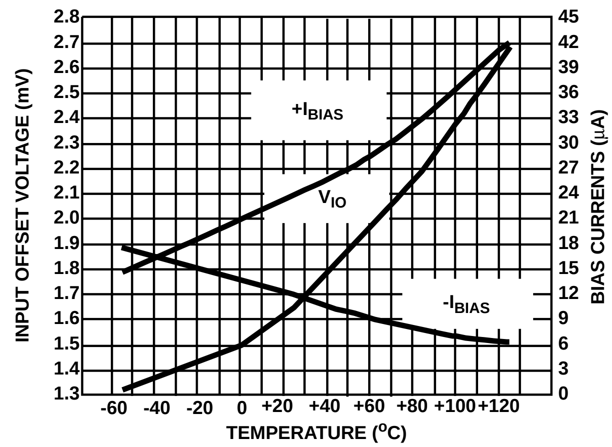
Typical Performance Curves

V_{SUPPLY} = ±5V, R_F = 510Ω, T_A = +25°C, R_L = 100Ω, Unless Otherwise Specified. **(Continued)**

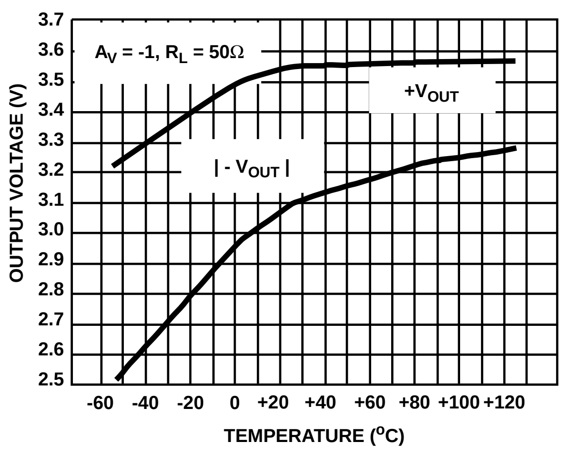
SUPPLY CURRENT vs SUPPLY VOLTAGE



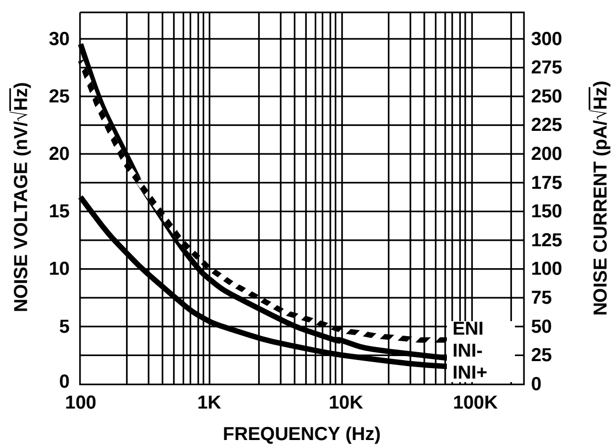
V_{IO} AND BIAS CURRENTS vs TEMPERATURE



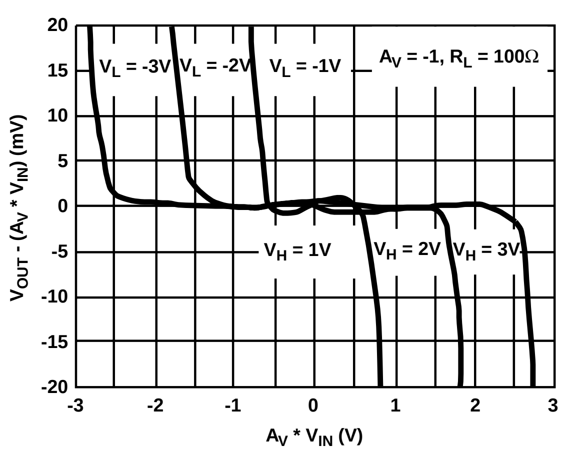
OUTPUT VOLTAGE vs TEMPERATURE



INPUT NOISE vs FREQUENCY



NON-LINEARITY NEAR CLAMP VOLTAGE



DESIGN INFORMATION (Continued)

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Application Information

Optimum Feedback Resistor

The enclosed plots of inverting and non-inverting frequency response illustrate the performance of the HFA1130 in various gains. Although the bandwidth dependency on closed loop gain isn't as severe as that of a voltage feedback amplifier, there can be an appreciable decrease in bandwidth at higher gains. This decrease may be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and R_F. All current feedback amplifiers require a feedback resistor, even for unity gain applications, and R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HFA1130 design is optimized for a 510Ω R_F at a gain of +1. Decreasing R_F in a unity gain application decreases stability, resulting in excessive peaking and overshoot. At higher gains the amplifier is more stable, so R_F can be decreased in a trade-off of stability for bandwidth.

The table below lists recommended R_F values for various gains, and the expected bandwidth.

GAIN (A_{CL})	R_F (Ω)	BANDWIDTH (MHz)
-1	430	580
+1	510	850
+2	360	670
+5	150	520
+10	180	240
+19	270	125

PC Board Layout

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10µF) tantalum in parallel with a small value (0.1µF) chip capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Capacitance directly on the output must be minimized, or isolated as discussed in the next section.

Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input (-IN). The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. To this end, it is recommended that the ground plane be removed under traces connected to -IN, and connections to -IN should be kept as short as possible.

An example of a good high frequency layout is the Evaluation Board shown in Figure 2.

Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor (R_S) in series with the output prior to the capacitance.

Figure 1 details starting points for the selection of this resistor. The points on the curve indicate the R_S and C_L combinations for the optimum bandwidth, stability, and settling time, but experimental fine tuning is recommended. Picking a point above or to the right of the curve yields an overdamped response, while points below or left of the curve indicate areas of underdamped performance.

R_S and C_L form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth of 850MHz. By decreasing R_S as C_L increases (as illustrated in the curves), the maximum bandwidth is obtained without sacrificing stability. Even so, bandwidth does decrease as you move to the right along the curve. For example, at $A_V = +1$, $R_S = 50\Omega$, $C_L = 30pF$, the overall bandwidth is limited to 300MHz, and bandwidth drops to 100MHz at $A_V = +1$, $R_S = 5\Omega$, $C_L = 340pF$.

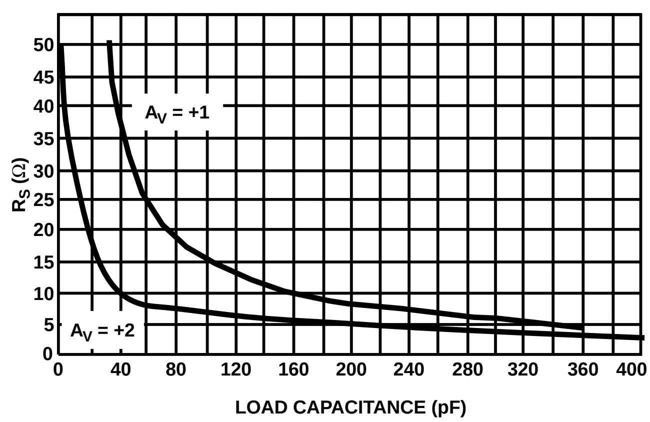

FIGURE 1. RECOMMENDED SERIES OUTPUT RESISTOR vs LOAD CAPACITANCE

Evaluation Board

The performance of the HFA1130 may be evaluated using the HFA11XX Evaluation Board.

The layout and schematic of the board are shown in Figure 2. To order evaluation boards, please contact your local sales office.

DESIGN INFORMATION (Continued)

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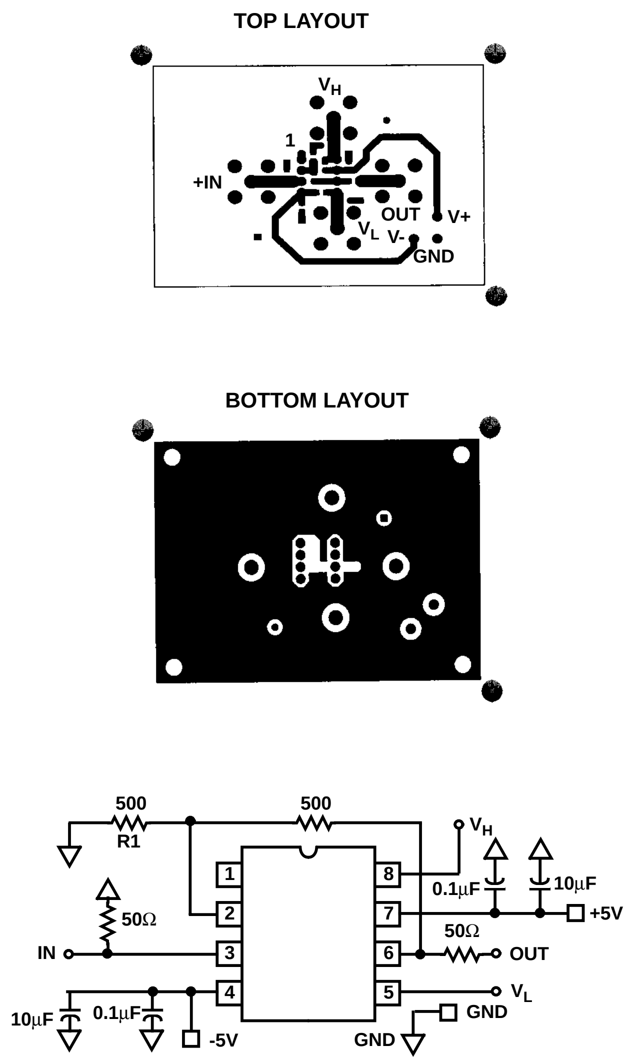

FIGURE 2. EVALUATION BOARD SCHEMATIC AND LAYOUT

Clamp Operation

General

The HFA1130 features user programmable output clamps to limit output voltage excursions. Clamping action is obtained by applying voltages to the V_H and V_L terminals (DIP pins 8 and 5) of the amplifier. V_H sets the upper output limit, while V_L sets the lower clamp level. If the amplifier tries to drive the output above V_H, or below V_L, the clamp circuitry limits the output voltage at V_H or V_L (± the clamp accuracy), respectively. The low input bias currents of the clamp pins allow them to be driven by simple resistive divider circuits, or active elements such as amplifiers or DACs.

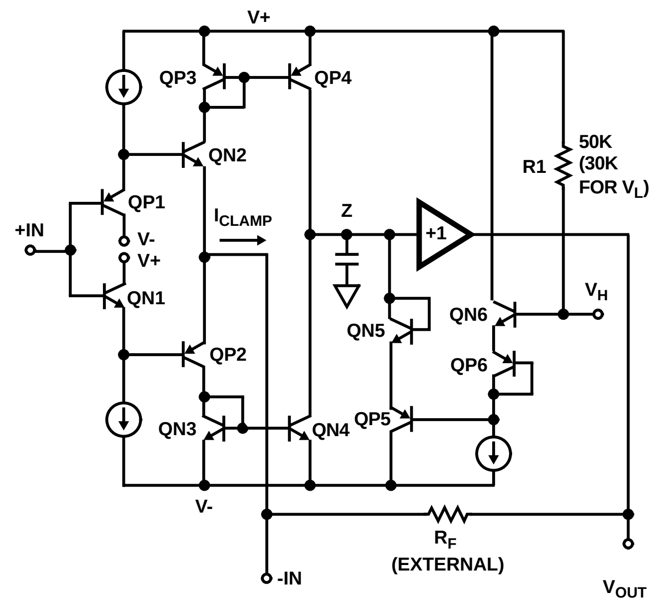

FIGURE 3. HFA1130 SIMPLIFIED VH CLAMP CIRCUITRY

Clamp Circuitry

Figure 3 shows a simplified schematic of the HFA1130 input stage, and the high clamp (V_H) circuitry. As with all current feedback amplifiers, there is a unity gain buffer (QX1 - QX2) between the positive and negative inputs. This buffer forces -IN to track +IN, and sets up a slewing current of:

$$(V_{-IN} - V_{OUT})/R_F + V_{-IN} / R_G$$

where R_G is the gain setting resistor from -IN to GND. This current is mirrored onto the high impedance node (Z) by QX3 - QX4, where it is converted to a voltage and fed to the output via another unity gain buffer. If no clamping is utilized, the high impedance node may swing within the limits defined by QP4 and QN4. Note that when the output reaches it's quiescent value, the current flowing through -IN is reduced to only that small current ($-I_{BIAS}$) required to keep the output at the final voltage.

Tracing the path from V_H to Z illustrates the effect of the clamp voltage on the high impedance node. V_H decreases by $2V_{BE}$ (QN6 and QP6) to set up the base voltage on QP5.

QP5 begins to conduct whenever the high impedance node reaches a voltage equal to QP5's base voltage + $2V_{BE}$ (QP5 and QN5). Thus, QP5 clamps node Z whenever Z reaches V_H. R1 provides a pull-up network to ensure functionality with the clamp inputs floating. A similar description applies to the symmetrical low clamp circuitry controlled by V_L.

DESIGN INFORMATION (Continued)

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When the output is clamped, the negative input continues to source a slewing current (I_{CLAMP}) in an attempt to force the output to the quiescent voltage defined by the input. QP5 must sink this current while clamping, because the -IN current is always mirrored onto the high impedance node. The clamping current is calculated as:

$I_{CLAMP} = (V_{-IN} - V_{OUT\ CLAMPED}) / R_F + V_{-IN} / R_G$.

As an example, a unity gain circuit with V_{IN} = 2V, V_H = 1V, and R_F = 510Ω would have I_{CLAMP} = (2V - 1V) / 510Ω + 2V / ∞ = 1.96mA. Note that Icc will increase by I_{CLAMP} when the output is clamp limited.

Clamp Accuracy

The clamped output voltage will not be exactly equal to the voltage applied to V_H or V_L Offset errors, mostly due to V_{BE} mismatches, necessitate a clamp accuracy parameter which is found in the device specifications. Clamp accuracy is a function of the clamping conditions. Referring again to Figure 3, it can be seen that one component of clamp accuracy is the V_{BE} mismatch between the QX6 transistors, and the QX5 transistors. If the transistors always ran at the same current level there would be no V_{BE} mismatch, and no contribution to the inaccuracy. The QX6 transistors are biased at a constant current, but as described earlier, the current through QX5 is equivalent to I_{CLAMP}. V_{BE} increases as I_{CLAMP} increases, causing the clamped output voltage to increase as well. I_{CLAMP} is a function of the overdrive level (A_{VCL} x V_{IN} - $V_{OUT\ CLAMPED}$) and R_F, so clamp accuracy degrades as the overdrive increases, and as R_F decreases. As an example, the specified accuracy of ±60mV for a 2X overdrive with R_F = 510Ω degrades to ±220mV for R_F = 240Ω at the same overdrive, or to ±250mV for a 3X overdrive with R_F = 510Ω.

Consideration must also be given to the fact that the clamp voltages have an effect on amplifier linearity. The “Nonlinearity Near Clamp Voltage” curve in the data sheet illustrates the impact of several clamp levels on linearity.

Clamp Range

Unlike some competitor devices, both V_H and V_L have usable ranges that cross 0V. While V_H must be more positive than V_L, both may be positive or negative, within the range restrictions indicated in the specifications. For example, the HFA1130 could be limited to ECL output levels by setting V_H = -0.8V and V_L = -1.8V. V_H and V_L may be connected to the same voltage (GND for instance) but the result won’t be in a DC output voltage from an AC input signal. A 150mV - 200mV AC signal will still be present at the output.

Recovery from Overdrive

The output voltage remains at the clamp level as long as the overdrive condition remains. When the input voltage drops below the overdrive level (V_{CLAMP} / A_{VCL}) the amplifier will return to linear operation. A time delay, known as the Overdrive Recovery Time, is required for this resumption of linear operation. The plots of “Unclamped Performance” and “Clamped Performance” highlight the HFA1130’s subnanosecond recovery time. The difference between the unclamped and clamped propagation delays is the overdrive recovery time. The appropriate propagation delays are 4.0ns for the unclamped pulse, and 4.8ns for the clamped (2X overdrive) pulse yielding an overdrive recovery time of 800ps. The measurement uses the 90% point of the output transition to ensure that linear operation has resumed. Note: The propagation delay illustrated is dominated by the fixturing. The delta shown is accurate, but the true HFA1130 propagation delay is 500ps.

DESIGN INFORMATION (Continued)

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TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: V_{SUPPLY} = ±5V, R_F = 360Ω, A_V = +2V/V, R_L = 100Ω, Unless Otherwise Specified

PARAMETERS	CONDITIONS	TEMPERATURE	TYPICAL	UNITS
Input Offset Voltage *	V_{CM} = 0V	+25°C	2	mV
Average Offset Voltage Drift	Versus Temperature	Full	10	µV/°C
V_{IO} CMRR	ΔV_{CM} = ±2V	+25°C	46	dB
V_{IO} PSRR	ΔV_S = ±1.25V	+25°C	50	dB
+Input Current *	V_{CM} = 0V	+25°C	25	µA
Average +Input Current Drift	Versus Temperature	Full	40	nA/°C
-Input Current *	V_{CM} = 0V	+25°C	12	µA
Average -Input Current Drift	Versus Temperature	Full	40	nA/°C
+Input Resistance	ΔV_{CM} = ±2V	+25°C	50	kΩ
-Input Resistance		+25°C	16	Ω
Input Capacitance		+25°C	2.2	pF
Input Noise Voltage *	f = 100kHz	+25°C	4	nV/√Hz
+Input Noise Current *	f = 100kHz	+25°C	18	pA/√Hz
-Input Noise Current *	f = 100kHz	+25°C	21	pA/√Hz
Input Common Mode Range		Full	±3.0	V
Open Loop Transimpedance	A_V = -1	+25°C	500	kΩ
Output Voltage	A_V = -1, R_L = 100Ω	+25°C	±3.3	V
	A_V = -1, R_L = 100Ω	Full	±3.0	V
Output Current *	A_V = -1, R_L = 50Ω	+25°C to +125°C	±65	mA
	A_V = -1, R_L = 50Ω	-55°C to 0°C	±50	mA
DC Closed Loop Output Resistance		+25°C	0.1	Ω
Quiescent Supply Current *	R_L = Open	Full	24	mA
-3dB Bandwidth *	A_V = -1, R_F = 430Ω, V_{OUT} = 200mV_{P-P}	+25°C	580	MHz
	A_V = +1, R_F = 510Ω, V_{OUT} = 200mV_{P-P}	+25°C	850	MHz
	A_V = +2, R_F = 360Ω, V_{OUT} = 200mV_{P-P}	+25°C	670	MHz
Slew Rate	A_V = +1, R_F = 510Ω, V_{OUT} = 5V_{P-P}	+25°C	1500	V/µs
	A_V = +2, V_{OUT} = 5V_{P-P}	+25°C	2300	V/µs
Full Power Bandwidth	V_{OUT} = 5V_{P-P}	+25°C	220	MHz
Gain Flatness *	To 30MHz, R_F = 510Ω	+25°C	±0.014	dB
	To 50MHz, R_F = 510Ω	+25°C	±0.05	dB
	To 100MHz, R_F = 510Ω	+25°C	±0.14	dB
Linear Phase Deviation *	To 100MHz, R_F = 510Ω	+25°C	±0.6	Degrees
2nd Harmonic Distortion *	30MHz, V_{OUT} = 2V_{P-P}	+25°C	-55	dBc
	50MHz, V_{OUT} = 2V_{P-P}	+25°C	-49	dBc
	100MHz, V_{OUT} = 2V_{P-P}	+25°C	-44	dBc
3rd Harmonic Distortion *	30MHz, V_{OUT} = 2V_{P-P}	+25°C	-84	dBc
	50MHz, V_{OUT} = 2V_{P-P}	+25°C	-70	dBc
	100MHz, V_{OUT} = 2V_{P-P}	+25°C	-57	dBc

DESIGN INFORMATION (Continued)

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TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Characterized at: V_{SUPPLY} = ±5V, R_F = 360Ω, A_V = +2V/V, R_L = 100Ω, Unless Otherwise Specified

PARAMETERS	CONDITIONS	TEMPERATURE	TYPICAL	UNITS
3rd Order Intercept *	100MHz, R_F = 510Ω	+25°C	30	dBm
1dB Compression	100MHz, R_F = 510Ω	+25°C	20	dBm
Reverse Isolation (S_{12})	40MHz, R_F = 510Ω	+25°C	-70	dB
	100MHz, R_F = 510Ω	+25°C	-60	dB
	600MHz, R_F = 510Ω	+25°C	-32	dB
Rise & Fall Time	V_{OUT} = 0.5V_{P-P}	+25°C	500	ps
	V_{OUT} = 2V_{P-P}	+25°C	800	ps
Overshoot *	V_{OUT} = 0.5V_{P-P}, Input t_R/t_F = 550ps	+25°C	11	%
Settling Time *	To 0.1%, V_{OUT} = 2V to 0V, R_F = 510Ω	+25°C	11	ns
	To 0.05%, V_{OUT} = 2V to 0V, R_F = 510Ω	+25°C	19	ns
	To 0.02%, V_{OUT} = 2V to 0V, R_F = 510Ω	+25°C	34	ns
Differential Gain	A_V = +2, R_L = 75Ω, NTSC	+25°C	0.03	%
Differential Phase	A_V = +2, R_L = 75Ω, NTSC	+25°C	0.05	Degrees
Overdrive Recovery Time (2X Overdrive)	R_F = 510Ω, V_{IN} = ±1V, V_H = +1V, V_L = -1V	+25°C	750	ps
Clamp Accuracy	A_V = -1, R_F = 510Ω, V_{IN} = ±2V, V_H = +1V, V_L = -1V	+25°C	±60	mV
Clamped Overshoot	R_F = 510Ω, V_{IN} = ±1V, V_H = +1V, V_L = -1V, Input t_R / t_F = 2ns	+25°C	4	%
Negative Clamp Range (V_L)	R_F = 510Ω	+25°C	-5.0 to +2.0	V
Positive Clamp Range (V_H)	R_F = 510Ω	+25°C	-2.0 to +5.0	V
Clamp Input Bias Current	V_H = +1V, V_L = -1V	+25°C	50	µA
Clamp Input Bandwidth	V_{IN} = ±100mV, V_H or V_L = 100mV_{P-P}	+25°C	500	MHz

*See Typical Performance Curves For More Information