PM8315

TEMUX

ANSWERS TO FREQUENTLY ASKED QUESTIONS REGARDING THE TEMUX

APPLICATION NOTE

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1 REFERENCES

[1] PMC-Sierra, PMC-1990495, “High-Density T1/E1 Framer with Integrated VT/TU Mapper and M13 Multiplexer – Register Descriptions”, Issue 3, 1999.

[2] PMC-Sierra, PMC-1981125, “High-Density T1/E1 Framer with Integrated VT/TU Mapper and M13 Multiplexer Telecom Standard Product Datasheet”, Issue 5, 2000.

[3] PMC-Sierra, PMC-1991268, “TEMUX Programmer’s Guide”, Issue 1, 2000.

2 ACRONYMS

CAS	Channel Associated Signaling
CCS	Common Channel Signaling
CES	Circuit Emulation Service
LIU	Line Interface Unit
SBI	Scalable Bandwidth Interconnect
SDH	Synchronous Digital Hierarchy
SONET	Synchronous Optical Network
SPE	Synchronous Payload Envelope
TU	Tributary Unit
VT	Virtual Tributary

3 BACKGROUND AND OVERVIEW

The PMC-Sierra PM8315 TEMUX is a High Density T1/E1 Framer with Integrated VT/TU Mapper and M13 Multiplexer. It is suitable for high density T1/E1 interfaces for multiplexers, multi-service switches, routers and digital modems.

The data sheets for the TEMUX are extensive documents with detailed description of device's operation and registers.

This document gives the customer a set of the most frequently asked questions with answers and reference literature for additional study.

If further clarification is required, please contact PMC-Sierra's technical support team at apps@pmc-sierra.com.

4 ANSWERS TO FREQUENTLY ASKED QUESTIONS

4.1 General Questions

Q1) Are there any reference designs, evaluation kits or development kits available for the TEMUX?

A1) Yes, there is the Frame Relay Port Card reference design (PMC-1990533) available. In addition, there is an AAL1gator-32 CES paper reference design (PMC-1990887). Both reference designs implement two possible applications of TEMUX in the Telecom Bus Line Side – SBI System Side mode of operation.

There is a FREEDM-32P672 with DS3 LIU paper reference design (PMC-1991724). This design shows the TEMUX in a DS3 clock and data mode of operation. And an AAL1gator-32/TEMUX development kit (PMC-1991144) is available as well.

Q2) What is the difference between the TEMUX and the TEMAP?

A2) The TEMAP (PM5365) is a monolithic device which integrates a SONET/SDH VT1.5/VT2/TU-11/TU12 bit asynchronous mapper with ingress or egress performance monitoring, a full featured M13 multiplexer with DS3 framer, and a SONET/SDH DS3 mapper in a single device.

The key differences between the TEMUX and TEMAP are as follows:

- The TEMUX has 28 T1 or 21 E1 framers capable of full processing of CAS and FDL. The TEMAP only supports performance monitoring in the ingress direction.
- The TEMUX is capable of generating T1/E1 framing and inserting alarms and signaling in the egress direction. The TEMAP does not modify the T1/E1 egress data stream in any way.
- The TEMAP does not support an H-MVIP backplane interface.

Both the TEMUX and the TEMAP support receive and transmit jitter attenuation for all T1/E1 links.

The TEMAP is suitable for data-communication applications when the processing of voice is not required. Two typical examples are High Density Frame Relay and Unstructured CES applications.

Q3) What is the packaging option available for the TEMUX?

A3) The TEMUX (PM8315) is packaged in 324 pin Plastic Ball Grid Array (PBGA). This package option has a –PI suffix.

Q4) Does the TEMUX support industrial temperature range?

A4) Yes, the TEMUX supports an industrial temperature range (-40C to 85C).

Q5) Are IBIS models available for the TEMUX?

A5) Yes, PMC-Sierra does provide IBIS models for the TEMUX. The IBIS model can be downloaded after registering at PMC-Sierra's website http://www.pmc-sierra.com

4.2 Software Questions

Q6) Is there a Programmer's Guide available for the TEMUX?

A6) Yes, the TEMUX Programmer's Guide (PMC-1991268) is available at PMC-Sierra's website http://www.pmc-sierra.com.

Q7) Is there a software driver available for the TEMUX?

A7) Yes, the software driver is available and can be downloaded after registering at PMC-Sierra's website http://www.pmc-sierra.com.

Q8) Is it possible to reset the TEMUX via software?

A8) Yes. It is possible to reset the TEMUX via software by writing 01h into register 0000h. This command will implement software reset for the entire TEMUX. The reset bit is not self-clearing, therefore, a logic 0 must be written to bring the TEMUX out of reset. Note that the Telecom bus output signals are driven, not tri-stated when held in software or hardware reset.

Full recommendations for device initialization are given in the TEMUX Programmer's Guide (PMC-1991268).

Q9) What kind of loopbacks does the TEMUX support at the T1/E1 interface?

A9) The TEMUX provides three loopback modes for T1/E1 links. These loopbacks are:

- T1/E1 Line Loopback: when in this loopback mode, the selected T1/E1 framer in the TEMUX is configured to internally connect the jitter-attenuated

clock and data from the receive jitter-attenuator to the transmit clock and data going to the M13 multiplexer or SONET/SDH mapper.

- T1/E1 Diagnostic Digital Loopback: when this loopback is configured, the selected T1/E1 framer in the TEMUX is configured to internally connect its transmit clock and data to its T1/E1 receive clock and data.

- Per-Channel Loopback: when the loopback is configured, the data passes through the receive clock and data, receive jitter-attenuator unit, T1/E1 framer, elastic store and back through T1/E1 basic transmitter, transmit digital attenuator to the transmit clock and data. The TEMUX also supports a full payload loopback, where all channels are looped back.

Q10) What kind of loopbacks does the TEMUX support at the SONET/SDH interface?

A10) The TEMUX provides two loopback modes at the SONET/SDH interface:

- Telecom Diagnostic Loopback. This loopback allows the transmitted Telecom Bus data stream to be looped back into the receive SONET/SDH receive path, overriding the data stream received on the Telecom Drop bus inputs. While the Telecom diagnostic loopback is active, valid SONET/SDH data continues to be transmitted on the Telecom Add bus outputs.

- Telecom Line Loopback. The Telecom Bus Line loopback allows the received Telecom Drop bus data stream to be looped back to the Telecom Add bus after the data stream is being processed by both the ingress and egress VTPPs. Both VTPPs must be setup for the same STS-1 SPE, STM-1/VC4 TUG3 or STM-1/VC3 otherwise no loopback data will get through.

Q11) What kind of loopbacks does the TEMUX support at the DS3 interface?

A11) The TEMUX provides five DS3 M13 multiplexer loopbacks at the DS3 interface:

- DS3 Diagnostic Loopback. This loopback allows the transmitted DS3 stream to be looped back into the receive DS3 path, overriding the DS3 stream received on the RDAT/RPOS and RNEG/RLCV inputs.

- DS3 Line Loopback. This loopback allows the received DS3 stream to be looped back into the transmit DS3 path, overriding the DS3 stream created internally by the multiplexing of the lower speed tributaries or the unchannelized DS3 payload.

- DS3 Payload Loopback. There is a second form of line loopback which only loops back the DS3 payload. In this mode the DS3 framing overhead is regenerated for the receive DS3 stream and then retransmitted.

- DS2 Demultiplex Loopback. This loopback allows each of the seven demultiplexed DS2 streams to be looped back into the M23 and multiplexed up into the transmit DS3 stream.

- DS1 Demultiplex Loopback. This loopback allows each of the four demultiplexed DS1 streams to be looped back into the M12 and multiplexed up into the transmit DS2 stream. There are seven DS2 streams.

4.3 Microprocessor Interface Questions

Q12) Is a microcontroller required to control and monitor the TEMUX?

A12) Yes, the TEMUX must be controlled and monitored via an 8-bit parallel microprocessor bus. This bus is compatible with both Motorola and Intel microprocessors.

Q13) How should the RSTB and TRSTB signals be connected for designs using JTAG? How should these signals be connected for designs not using JTAG?

A13) If JTAG is not used, the TRSTB signal should be connected to the RSTB signal.

If JTAG is used, the TRSTB signal should be connected to the appropriate JTAG circuitry. For an example of this, please refer to the Frame Relay Port Card reference design.

Q14) Is there a register bit we can use to assert/deassert the interrupt pin, INTB on the TEMUX device?

A14) The TEMUX does not support a software assert/deassert of the interrupt INTB signal. Note that interrupt INTB can occur only on reaction to an interrupt signal that is enabled

Q15) Is the INTB signal independent of the microprocessor read cycles, i.e., is it like a normal asynchronous interrupt pin out of a device, or it is only active during a microprocessor read transaction, which is what the timing diagram in the TEMUX datasheet implies?

A15) The assertion of the INTB signal is independent of the microprocessor cycles, but it is deactivated when the interrupt register is read. Full information on software processing of TEMUX interrupts is given in the Programmer's Guide.

4.4 Line Side Interface Questions

Q16) Which DS3 LIU is recommended for use with the TEMUX?

A16) Quite a number of DS3 LIUs can be connected to the PMC-Sierra's DS3 framers. We have used TDK 78P7200 in our reference designs: Interfacing the D3MX to the 78P7200 DS3 LIU (PMC-1950946), FREEDM-32P672 with DS3 LIU reference design (PMC-1991724) and the AAL1gator32 development kit (PMC-1991144).

Q17) Can the customer use the TEMUX with the PM7362 TUPP+ when the TEMUX has enabled the VTPP function of the receive side?

A17) Yes, but note that the TUPP+ can only reside in the Telecom bus drop side between the SPECTRA and the TEMUX. The TEMUX will have to receive RDI, RFI and REI indications from TUPP+. It can get these signals from the Receive Alarm Port (RAD) which is an output of TUPP+.

Q18) The TEMUX supports LREFCLK 19.44 MHz for a Byte Telecom bus. How does this work with the SPECTRA-622? Does LREFCLK need to run at 77 MHz?

A18) TEMUX always runs at 19.44 MHz, and each TEMUX processes one STS-1 payload within an STS-3.

SPECTRA-622 has two different operating modes for the Telecom bus. It can be configured as a single 77.76 MHz bus, or as four 19.44 MHz buses. The later configuration is required when interfacing to the TEMUX.

Q19) Does the Telecom bus need buffers between the backplane and the TEMUX output if we want to use three TEMUXes?

A19) Buffers are needed if the three TEMUXes and the SPECTRA-155/622 are located on two separate boards connected to a backplane. If the four devices are on the same board, then only pull-up resistors are required on the Telecom signals.

Q20) When TUPP+ receives TU-LOP alarm, it sends AIS downstream. How will the TEMUX respond to the AIS signal?

A20) When TUPP+ or TEMUX's VTPP receives TU-LOP, it sends AIS downstream. The TEMUX is capable of generating RDI upon detection of AIS. Register 1207h controls the insertion of tributary path RDI to the egress Tributary Alarm Processor (TRAP) and optionally the Ingress V5 byte, as a result of tributary pointer alarms, tributary path signal label alarms and tributary multiframe alarms.

The Egress AIS registers in the TRAP module must be set correctly, in addition to setting this register, for RDI insertion.

Q21) Will TUPP+ or TEMUX's VTPP detect the TU-LOP alarm when it receives 5 consecutive invalid pointers and 3 consecutive valid pointers?

A21) TU-LOP will occur only after 8 consecutive invalid pointers or eight consecutive NDF enabled indications. When the same valid pointer with the normal NDF is detected for three consecutive frames, TU-LOP will be removed.

4.5 Frame Format Questions

Q22) What are the differences between the TEMUX T1/E1 framers and the PM4351 COMET?

A22) Some important differences are:

1) The COMET has a fully programmable 32 bit Pseudo Random Sequence generator while the TEMUX has only 3 PRBS sequences that can be selected at the T1/E1 framer level. Note, however, that the TEMUX has a fully programmable 32-bit PRBS pattern generator at the DS3 level.

2) V5.2 support - The COMET has 3 HDLC controllers while the TEMUX framers have only one HDLC controller per channel. In the TEMUX, V5.1/V5.2 may be supported by processing CCS data extracted to the HMVIP backplane interface.

3) The TEMUX T1 framers do not have T1 Inband loopback code insertion or detection. The COMET does have inband loopback code functionality.

Q23) The TEMUX can support DS3 framing and SONET/SDH DS3 mapping. Does the same apply to E3, since it supports E1 mapping?

A23) No, the TEMUX does not support E3 framing. The E1 frames are mapped into DS3 format and then through TUG-3,VC-3 into Administrative Pointer 3 (AU-3). Please refer to Question 25 for details.

Q24) Is it possible to multiplex/demultiplex 21 E1s into a DS3 using the M13 multiplex function in the TEMUX?

A24) Yes, this is possible. The TEMUX supports the ITU-T G.747 standard to multiplex/demultiplex 21 E1s into a DS3 using the M13 multiplex function in the TEMUX. This function is an M23 based method.

The M12 multiplexer integrates circuitry required to asynchronously multiplex and demultiplex three 2048 kbit/s into and out of a G.747 formatted 6312 kbit/s high speed signal.

Note that multiplexing/demultiplexing of 21 E1s to the SBI interface through the DS3 M13 multiplexer is not supported. System side interfaces for E1 multiplexing can be MVIP or Serial Clock and Data.

Q25) Are there any TEMUX indications for SF and ESF boundaries (i.e. 6th , 12th, 18th , 24th frame)?

A25) The T1-FRMR block searches for the framing bit position in the egress or ingress stream. It works in conjunction with the FRAM block to search for the framing bit pattern in the standard superframe (SF), or extended superframe (ESF) framing formats. When searching for frame, the framer simultaneously examines each of the 193 (SF) or each of the 772 (ESF) framing bit candidates. The TEMUX has no SF or ESF boundary indications. Since the signaling is extracted for the entire multiframe, the multiframe indications are not needed.

Q26) If we choose VT/TU Mapper mode on the TEMUX, can we turn on/off the T1/ E1 framers?

A26) Yes, the T1 / E1 framers can be turned off using the OPMODE[1:0] bits in Master configuration register 0001H. When set to 00, the framers are enabled. This mode is called the High Density Framer Mode. When set to 10, the framers are disabled. This mode is called Mapper/Multiplexer mode

Q27) Do DS3 framers need a TICLK clock?

A27) The DS3 framers will always require TICLK clock when the DS3 mappers are used. If the DS3 mappers are not used, the TICLK clock should be connected to ground.

4.6 System Side Interface Questions

Q28) On our SBI bus we have 3 TEMUX devices. Should we configure only one of them as a BUSMASTER?

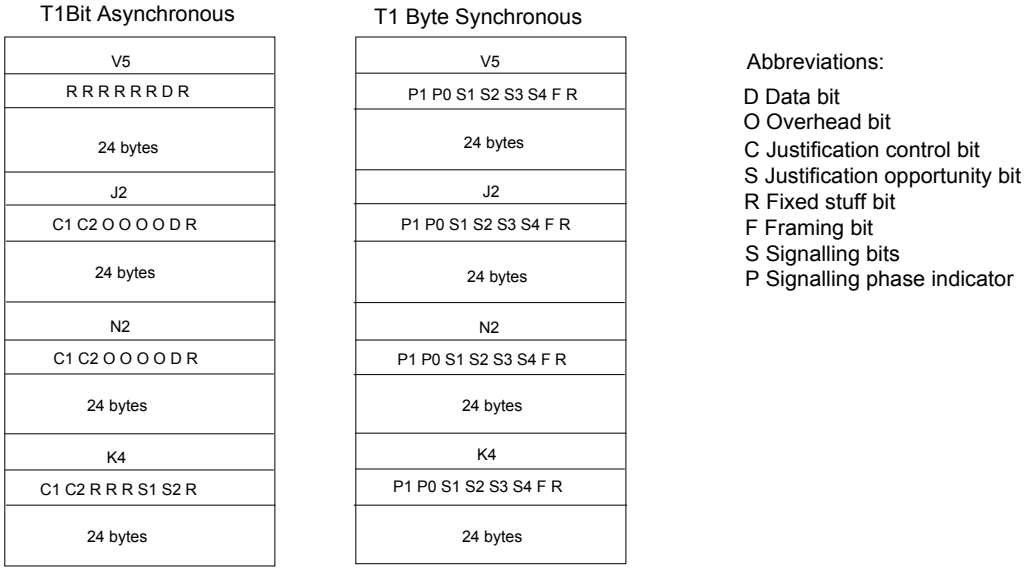
A28) Yes, only one TEMUX should be configured as a BUSMASTER. Bit 0 in the register 1702H should be set to 1.

Q29) Is Byte Synchronous Mode Supported in the TEMUX?

A29) No, Byte Synchronous Mode is not supported in the TEMUX. The TEMUX supports only Bit Asynchronous Mapping.

The Receive Tributary Demapper (RTDM) demaps up to 28 T1 or 21 E1 bit asynchronous mapped signals from an STS-1 SPE, TUG3 within a STM-1/VC4 or STM-1 VC3 payload. The bit asynchronous T1 mapping consists of 104 octets every 500 microseconds (2kHz) while the bit asynchronous E1 mapping consists of 140 octets every 500 micro seconds. Figure 1 shows the tributary data structure for the bit asynchronous T1 mapping and byte synchronous T1 mapping.

Figure 1 Tributary Data Structure



Q30) How does the TEMUX configure an SBI tributary for synchronous or asynchronous mode?

A30) In the Ingress direction, the SYNCH_TRIB bit in indirect Tributary data register 1726H should be enabled for each tributary to be configured for synchronous mode.

In the Egress direction there is no such bit since the timing comes from one source: the TEMUX or the Link Layer Device. Hence there is the CLK_MSTR bit in register 1716h indicates whether the TEMUX or the Link Layer Device is responsible for the timing.

Q31) Can we use the HDLC controller in an ISDN 30B+D application?

A31) Yes, the TEMUX's E1 framers can be configured to process an ISDN D-channel. The Data Links can be specified using the Egress and Ingress Data Link Control registers (0020H+80H*N, 0028H+80H*N).

Note that this application can be microprocessor intensive. A fully configured TEMUX may need to process 21 ingress and 21 egress 64 kbit/s D-channels. Given that the FIFOs are 128 bytes deep for each of the 42 HDLC controllers, timely servicing of the data links may be an issue.

Note also that 640 ns waits are required between consecutive read or write accesses to any individual FIFO. It is suggested that each E1 link be serviced in some interleaved manner to maximize data throughput while respecting this 640 ns requirement. Software written to service the HDLC controllers should consider these requirements.

Another option is to extract the D-channel using an external HDLC controller. The TEMUX, in this case, uses the MVIP CCS port to provide the D-channel.

The TEMUX Programmer's Guide gives more information on the software necessary to operate the HDLC controllers.

4.7 Board Design Related Questions

Q32) What is the accuracy needed for TICLK, XCLK, CTCLK, etc. signals in ppm?

A32) The Table 1 shows the TEMUX timing characteristics of various signals. Details can be found in the TEMUX datasheet in chapter 17.

Table 1 Timing Characteristics

Signal	Frequency	Accuracy	Duty Cycle
TICLK	44.736 MHz	20 ppm	40-60%
XCLK	37.056 MHz for T1 49.152 MHz for E1	32 ppm	50%
CTCLK	1.544 MHz for T1 2.048 MHz for E1	130 ppm 50 ppm	40-60%
CICLK	1.544 MHz for T1 2.048 MHz for E1	130 ppm 50 ppm	40-60%
CLK52M	51.84 MHz or 44.928 MHz	50 ppm	40-60%
LREFCLK	19.44 MHz	50 ppm	40-60%
SREFCLK	19.44 MHz	50 ppm	40-60%
CMV8MCLK	16.384 MHz	130 ppm for T1 50 ppm for E1	40-60%
CMVFPC	4.096 MHz	130 ppm for T1 50 ppm for E1	40-60%
CECLK	1.544 MHz for T1 2.048 MHz for E1	130 ppm for T1 50 ppm for E1	40-60%

Q33) We want to connect the SPECTRA-155 to three TEMUX devices. We think that the Byte Wide Telecom bus is the best way to do this. Is this correct? Are there any reference design schematics available to show us the correct connections for this bus?

A33) Yes, the Byte Wide Telecom Bus is the only way to do this. Consult the Frame Relay Port Card reference design (PMC-1990533) for more details on this application.

Q34) When is the clock CLK52M required?

A34) The clock CLK52M is required as a high speed reference for both demapping a DS3 from the STS-1 on the Telecom bus as well as for transferring a DS3 across the SBI bus. It is not required that this clock be network timed since it is only a reference.

4.8 Power Supply Related Questions

Q35) How is the power sequencing implemented for the TEMUX?

A35) The TEMUX datasheet states that the VDD3.3 and VDDQ should power up before VDD2.5. In addition, VDD3.3 and VDDQ should not be allowed to drop below the VDD2.5 voltage by more than 0.5 V level except when VDD2.5 is not powered.

In the Frame Relay Port Card reference design, power sequencing is implemented by Hot Swap Controller LTC 1422. With two external FET pass transistors, the LTC 1422 can switch 3.3V and 2.5V power supplies. The 3.3V power supply is generated from 5V power supply by using voltage regulator LT1585 and the 2.5V power supply is generated from 3.3V power supply by using voltage regulator LP3966ES-2.5.

The circuit in the Frame Relay Port Card Schematics powers the 3.3V supply first. Corresponding resistors and capacitors are used to set the rise and fall delays on the 3.3V power supply. Next, the 2.5V supply ramps up with a 20 msec delay. On the falling edge, the 2.5V ramps down first.

Q36) What is the maximum power dissipation for the TEMUX?

A36) The typical power dissipation for the TEMUX is 1.2W while the maximum power dissipation for the fully functional device is 1.3W. Table 2 shows operating currents of the TEMUX for different modes of operation with unloaded outputs. Board power estimates should include factors of signal loading.

Table 2 Operating Currents of the TEMUX

Conditions and Mode of Operation	Symbol	Parameter	Typical Value (mA)
Telecom to SBI mode VDD2.5V = 2.7V VDD3.3 = 3.63 V	IDDOP1	Operating Current	368 (2.5V) 4 (3.3V)
DS3 to MVIP mode VDD2.5 = 2.7 V VDD3.3 = 3.63 V	IDDOP2	Operating Current	202 (2.5V) 3 (3.3V)
DS3 to serial clock and data mode VDD2.5 = 2.7 V VDD3.3 = 3.63 V	IDDOP3	Operating Current	225 (2.5V) 5 (3.3V)
Transmux mode VDD2.5 = 2.7 V	IDDOP4	Operating Current	340 (2.5V) 5 (3.3V)

Q37) What is the maximum case temperature Tc for the TEMUX?

A37) The maximum case temperature Tc for the TEMUX is +85^{o}C.

The maximum rating is the worst case limit that the device can withstand without sustaining permanent damage. It is not indicative of normal mode operation conditions.

Q38) What is the maximum junction temperature Tj for the TEMUX?

A38) The maximum junction temperature Tj for the TEMUX is +150^{o}C.

The maximum rating is the worst case limit that the device can withstand without sustaining permanent damage. It is not indicative of normal mode operation conditions.

Q39) Can we assume that the 2.5V supply of the TEMUX is used by the core and the 3.3V supply is used by I/O pads?

A39) Yes, this assumption is correct. The 3.3V power supply is used by I/O pads. Beside this, all the outputs are TTL compatible and the minimum guaranteed output high voltage is 2.4V.

Q40) Does the TEMUX support power down modes to reduce power consumption of unused features?

A40) Yes, the TEMUX supports power down modes. Most functional blocks can be held in a reset state that only draws a small fraction of the power. This is selected by setting the enable/reset register bits appropriately for each block.

Q41) Are the TEMUX inputs 5V tolerant? What is the maximum input voltage?

A41) Yes, the TEMUX inputs except SBI inputs are 5V tolerant. The maximum input voltage is 5.5V for 5V tolerant inputs.

5 NOTES

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