

# MOS FIELD EFFECT POWER TRANSISTOR $\mu$ PA1700

# SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

#### **DESCRIPTION**

This product is N-Channel MOS Field Effect Transistor designed for DC/DC converter and power management applications of note book computers.

#### **FEATURES**

· Low On-Resistance

 $R_{DS(on)1} = 27~m\Omega~Typ.~(V_{GS} = 10~V,~I_{D} = 3.5~A)$   $R_{DS(on)2} = 50~m\Omega~Typ.~(V_{GS} = 4~V,~I_{D} = 3.5~A)$ 

- Low Ciss Ciss = 850 pF Typ.
- · Built-in G-S Protection Diode
- Small and Surface Mount Package (Power SOP8)

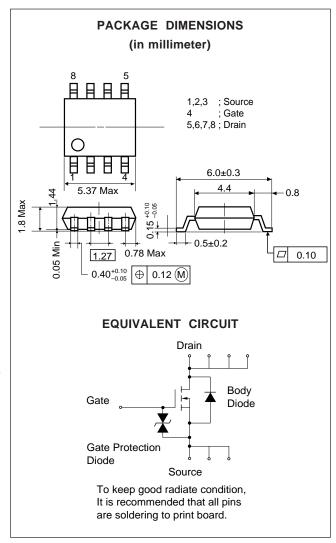
#### ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA1700G	Power SOP8

#### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C)

Drain to Source Voltage	VDSS	30	V
Gate to Source Voltage	Vgds	±20	V
Drain Current (DC)	$I_{D(DC)}$	±7.0	Α
Drain Current (pulse)*	ID(pulse)	±28	Α
Total Power Dissipation	PT	2.0	W
(T <sub>A</sub> = 25 °C)**			
Channel Temperature	Тсн	150	°C
Storage Temperature	T <sub>stg</sub> -55	to +150	°C

- \* PW  $\leq$  10  $\mu$ s, Duty Cycle  $\leq$  1 %
- \*\* Mounted on ceramic substate of 1200 mm $^2 \times 0.7$  mm



The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.



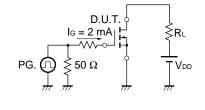
#### ELECTRICAL CHARACTERISTICS (TA = 25 °C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state	RDS(on)1	Vgs = 10 V, ID = 3.5 A		20	27	mΩ
Resistance	RDS(on)2	Vgs = 4 V, ID = 3.5 A		33	50	mΩ
Gate to Source Cutoff Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	1.0	1.6	2.0	V
Forward Transfer Admittance	yfs	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 3.5 A	5.0			S
Drain Leakage Current	IDSS	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0			10	μΑ
Gate to Source Leakage Current	Igss	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0			±10	μΑ
Input Capacitance	Ciss	V <sub>DS</sub> = 10 V		850		pF
Output Capacitance	Coss	V <sub>GS</sub> = 0		550		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		270		pF
Turn-On Delay Time	td(on)	ID = 3.5 A		20		ns
Rise Time	tr	V <sub>GS(on)</sub> = 10 V		105		ns
Turn-Off Delay Time	td(off)	V <sub>DD</sub> = 15 V		90		ns
Fall Time	tr	R <sub>G</sub> = 10 Ω		60		ns
Total Gate Charge	QG	ID = 7.0 A		33		nC
Gate to Source Charge	Qgs	VDD = 24 V		2.4		nC
Gate to Drain Charge	Q <sub>GD</sub>	V <sub>GS</sub> = 10 V		13		nC
Body Diode Forward Voltage	V <sub>F(S-D)</sub>	IF = 7.0 A, VGS = 0		0.84		V
Reverse Recovery Time	trr	IF = 7.0 A, VGS = 0		60		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/μs		90		nC

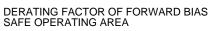
#### **Test Circuit 1 Switching Time**

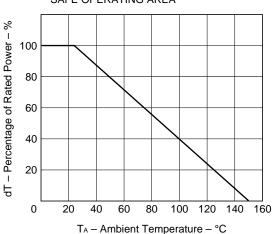
# PG. $\bigcap_{RG} RG = 10 \ \Omega$ $V_{GS} \bigvee_{Wave \ Form} V_{GS} \bigvee_{Wave \ F$

#### **Test Circuit 2 Gate Charge**

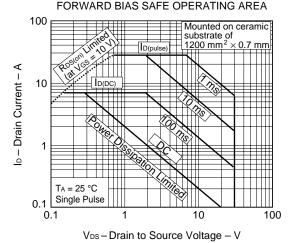


#### TYPICAL CHARACTERISTICS (TA = 25 °C)

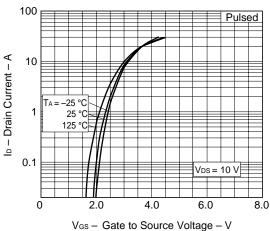




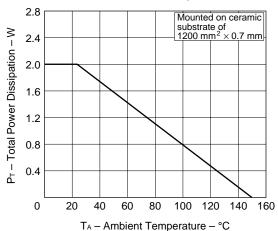
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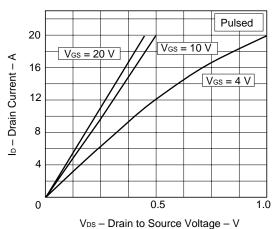
#### FORWARD TRANSFER CHARACTERISTICS



# TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE

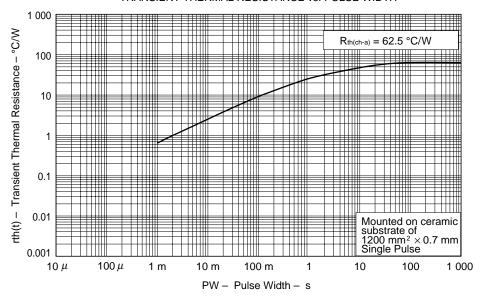


#### DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

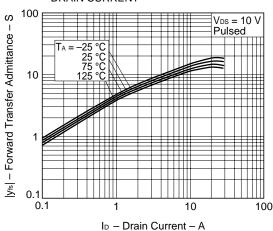




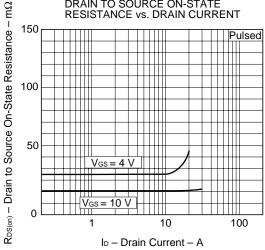
#### TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



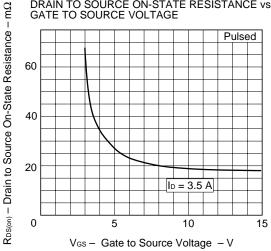




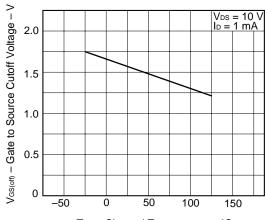
# DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



### DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

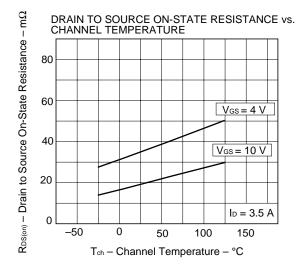


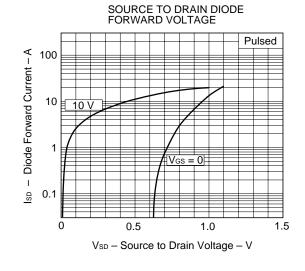
# GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE

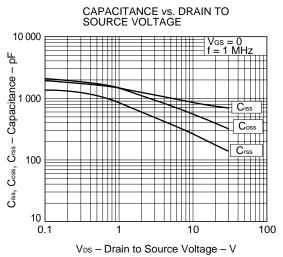


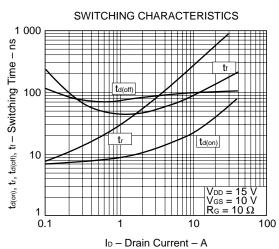
Tch - Channel Temperature - °C

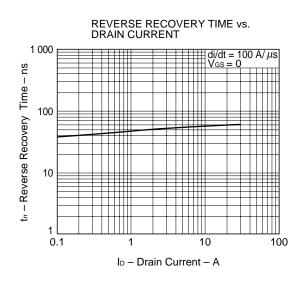


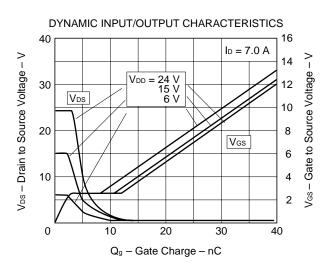














#### REFERENCE

Document Name	Document No.		
NEC semiconductor device reliability/quality control system	TEI-1202		
Quality grade on NEC semiconductor devices	IEI-1209		
Semiconductor device mounting technology manual	IEI-1207		
Semiconductor device package manual	IEI-1213		
Guide to quality assurance for semiconductor devices	MEI-1202		
Semiconductor selection guide	MF-1134		
Power MOS FET features and application switching power supply	TEA-1034		
Application circuits using Power MOS FET	TEA-1035		
Safe operating area of Power MOS FET	TEA-1037		

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Anti-radioactive design is not implemented in this product.

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